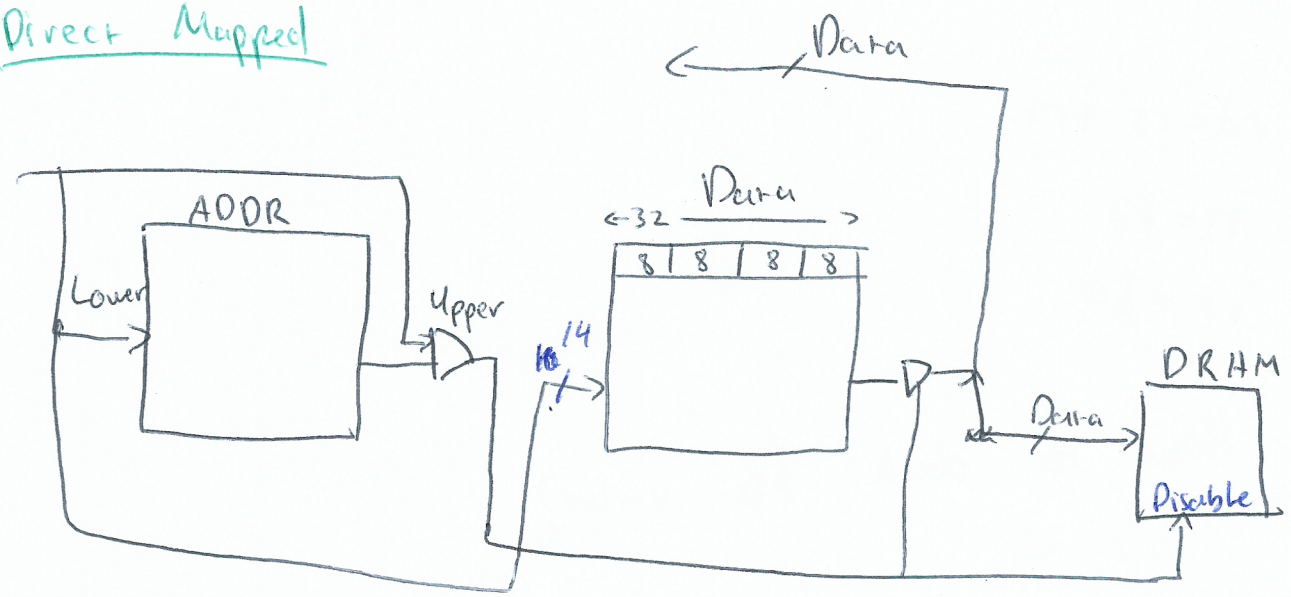
Comp Arch 3 - Formal Element

04-10-18

Direct Mapped



-> 32 bit CPU ADDR

-> 8 bit data bus

-> Cache Lin - 4 Bytes

-> CPU sends 32-bit ADDR & gets back a Byte either from cache or DRAM

-> 64KB Data Cache - 16k lines x 4B per line

Code

```
struct cacheEntry {
    unsigned short upperAddr; // 16 bit e.g 32/2
    bool validFlag;
    bool LRUFlag;
    char data[4]; // ~~data~~ 32-bit bus
};
struct cacheEntry way0[16384]; // 2^14, 2 left for data
unsigned int CPUAddr; // 32-bit CPU address
unsigned short CPULower, CPUUpper; //
CPULower = ~~& 0x0000ffff~~; ~~CPU~~ CPUAddr & 0x0000 ffff;
CPUUpper = (CPUAddr & 0xffff0000) >> 16;
```

~~rd = rs + rt~~

~~rs = $8~~

~~rt = $9~~

~~How to check $8 value)~~

~~if (cPUUpper == way0[cPULower].upperAddr) { // check upper Addr~~

~~"Hit"~~

byteNo = cPULower & 3;

SetNo = cPULower & 0xfffc) >> 2;

if ((cPUUpper == way0[~~cPULower~~ SetNo].upperAddr) {

way0 [setNo].data [byteNo];