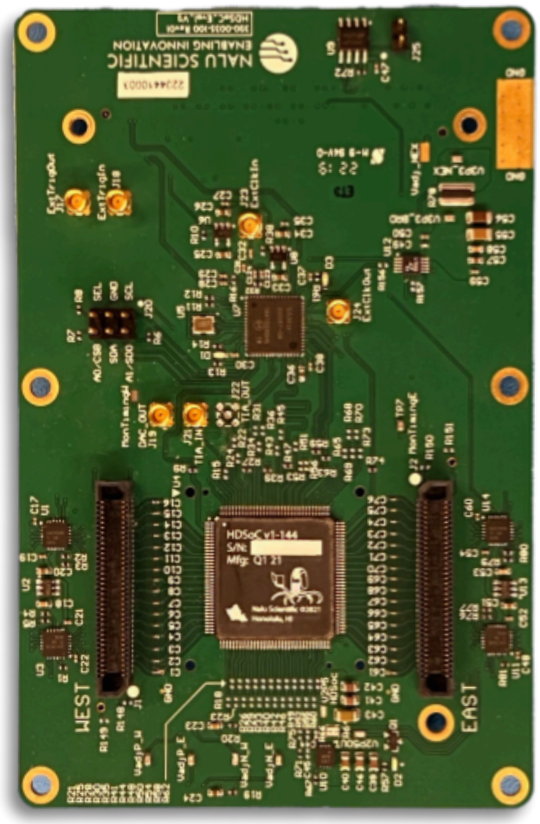
# HDSoCv1 Evaluation card rev2

## High-Density Digitizer System on Chip Evaluation Board System
## Product Sheet




### Features:

- 32 analog input channels
- 1.0 - 1.8 GSPS sampling rate
- 0.5-1.0 GSPS possible on request
- Input bandwidth > 500MHz
- Self and external triggering
- Individual channel configuration
- Trigger edge selectable (level and edge)
- 2.5V analog voltage input range
- 1.2V linear range with calibration
- Record length: 1,984 samples per channel

## 1. Description:

A variety of applications in modern particle imaging-based physics experiments utilize multiple imagers and high sampling rate data converters to digitize events lasting hundreds of nanoseconds in duration. The HDSoCv1 Eval Board System has 32 analog input channels and can digitize 410 nanoseconds at a sample rate of 1-1.8Gsa/sec. The eval board is paired with a Nexys Artix-7 FPGA FMC Board for control and communication to the ASIC.



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## 2. Applications:

- SiPM array
- Photodiode array
- 3D imaging
- Streak camera
- LIDAR
- Medical Imaging
- Photosensor arrays
    - PMT
    - MA-PMT
    - MCP-PMT
    - SiPM array

| Order Code | Description | Cost (USD) |
|---|---|---|
| HDSoCv1 FMC Eval Card | HDSoCv1 EVB r2 | Quote |



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## 3. Connection Diagram:

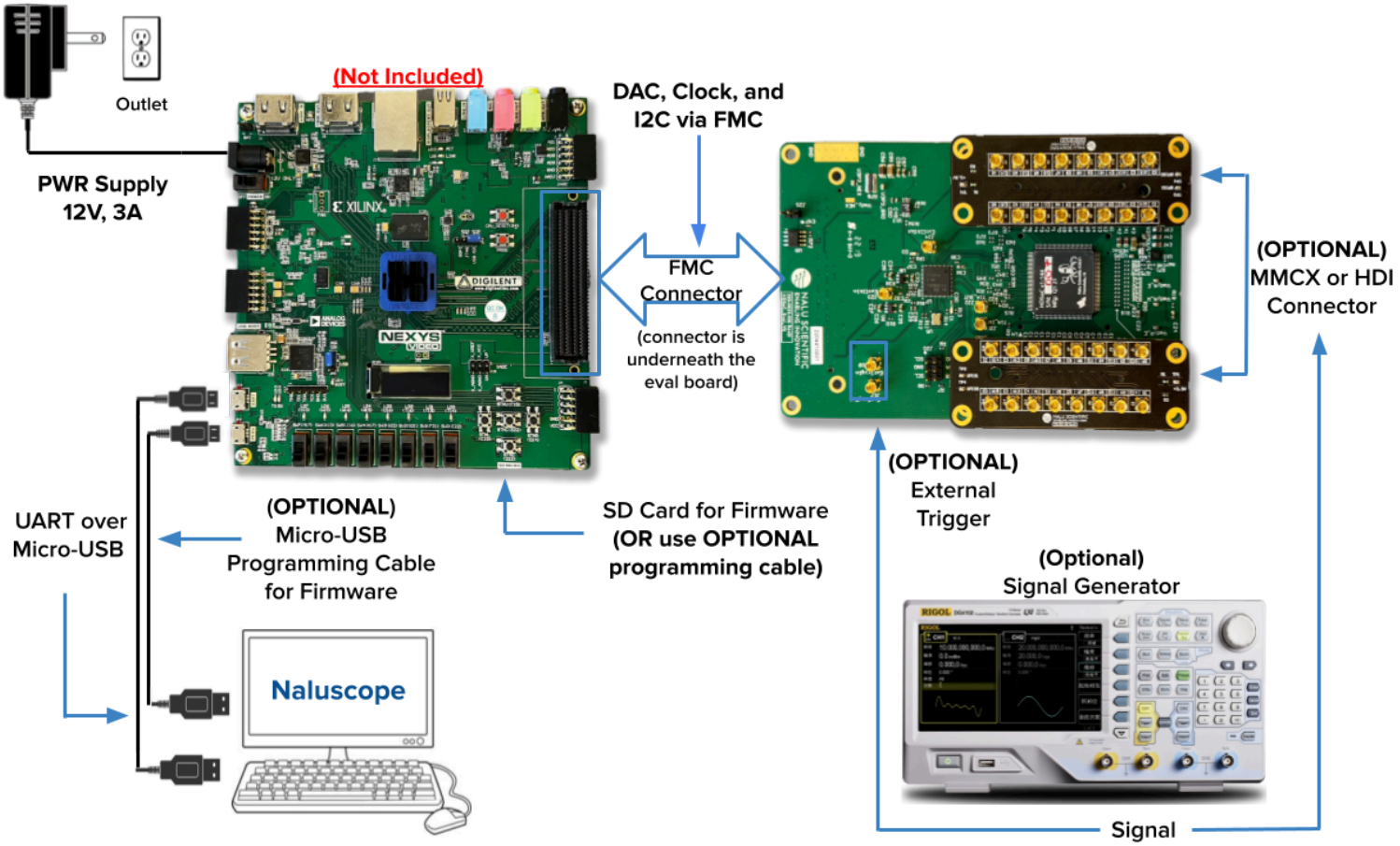


***Figure 1:*** *Connection Diagram for the HDSoCv1 EVBr2.*

The Nexys Artix 7 Video Card is **required** to enable all functionality on the EVBr2. This includes using the board with NaluScope and optional functions such as external trigger setup and programming firmware. The Nexys board can receive power two ways. The power jack requires a coax center positive 2.1mm internal-diameter plug, and delivers 12VDC ±5%. The minimum current rating of the supply depends on the actual design implemented in the FPGA, but at least 3A of current (i.e. at least 36W of power) is recommended. If there is no wall supply available, the Nexys can also be powered by connecting the positive pin of J22 and the negative terminal to the negative pin. Incorrect polarity may cause permanent damage to the board. The voltage of this battery must be 12V ± 5% where 15V is the absolute maximum. Please refer to the **Nexys Video FPGA Board Reference Manual** for more information.



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## 3.1 Optional Adapter Cards

Included with the HDSoCv1 EVBr2 are two optional adapter cards which allow 32 analog inputs to be connected via MMCX cables.

| West HDI | | East HDI | | West HDI | | East HDI | |
|---|---|---|---|---|---|---|---|
| **Pin#** | **Description** | **Pin#** | **Description** | **Pin#** | **Description** | **Pin#** | **Description** |
| 1 | 3.3V | 1 | 3.3V | 46-48 | Ground | 46-48 | Ground |
| 2-4 | Ground | 2-4 | Ground | 49 | W04 | 49 | E04 |
| 5 | W15 | 5 | E15 | 50-52 | Ground | 50-52 | Ground |
| 6-8 | Ground | 6-8 | Ground | 53 | W03 | 53 | E03 |
| 9 | W14 | 9 | E14 | 54-56 | Ground | 54-56 | Ground |
| 10-12 | Ground | 10-12 | Ground | 57 | W02 | 57 | E02 |
| 13 | W13 | 13 | E13 | 58-60 | Ground | 58-60 | Ground |
| 14-16 | Ground | 14-16 | Ground | 61 | W01 | 61 | E01 |
| 17 | W12 | 17 | E12 | 62-64 | Ground | 62-64 | Ground |
| 18-20 | Ground | 18-20 | Ground | 65 | W00 | 65 | E00 |
| 21 | W11 | 21 | E11 | 66-68 | Ground | 66-68 | Ground |
| 22-24 | Ground | 22-24 | Ground | 69 | GPIO | 69 | GPIO |
| 25 | W10 | 25 | E10 | 70 | GPIO | 70 | GPIO |
| 26-28 | Ground | 26-28 | Ground | | | | |
| 29 | W09 | 29 | E09 | | | | |
| 30-32 | Ground | 30-32 | Ground | | | | |
| 33 | W08 | 33 | E08 | | | | |
| 34-36 | Ground | 34-36 | Ground | | | | |
| 37 | W07 | 37 | E07 | | | | |
| 38-40 | Ground | 38-40 | Ground | | | | |
| 41 | W06 | 41 | E06 | | | | |
| 42-44 | Ground | 42-44 | Ground | | | | |
| 45 | W05 | 45 | E05 | | | | |



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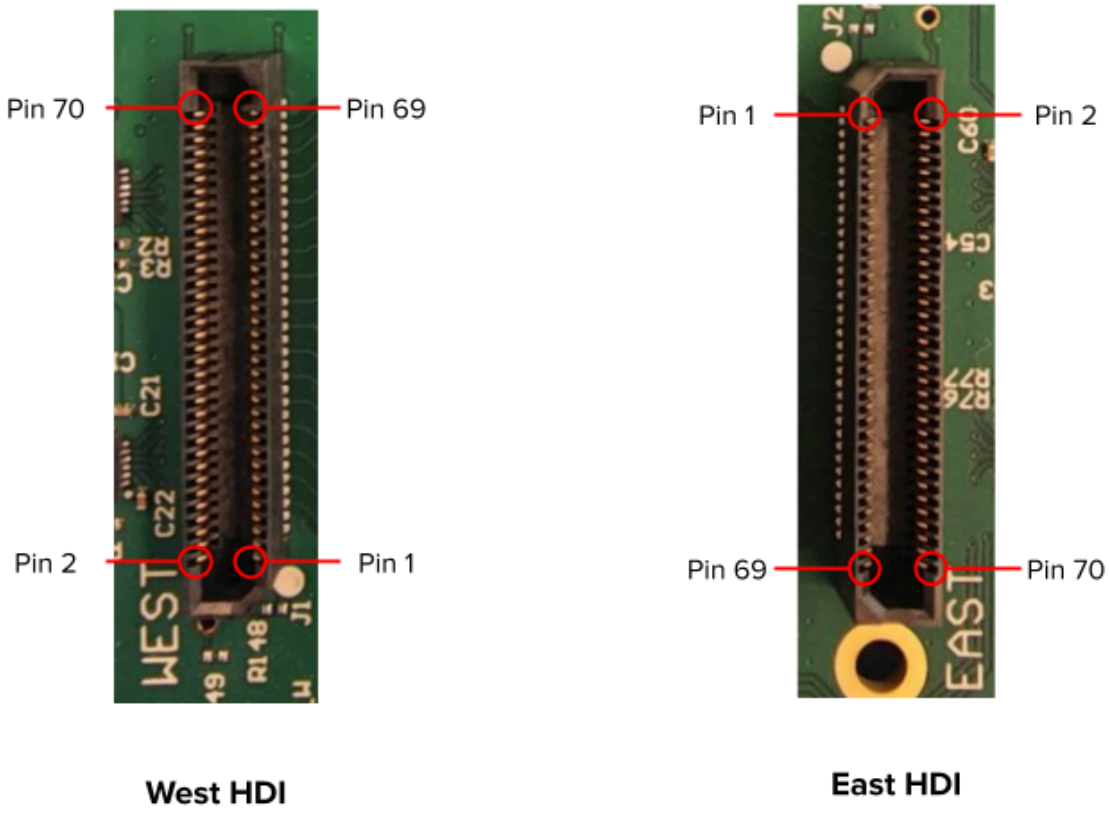
***Table 1:*** *Pinout for HDI adapters.*




**West HDI** **East HDI**

***Figure 2:*** *The East and West HDI adapters* ***have different orientations.*** *It is important to note that while the West and East HDI connectors have the same pinout, they are* ***oriented differently****. The image above shows the difference in pin placements for the West and East respectively. The component used for the HDI adapter is the ERM8-035-05.0-L-DV-TR. Please visit the Samtec website for more information on this component.*



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## 4. Communication Interfaces:

The system requires the use of a Micro USB cable to the Nexys Artix 7 Video Card for connecting and communicating with the ASIC.

- UART over USB, using virtual comport, up to 2M baud
- JTAG over USB for firmware updates
- Gigabit Ethernet (GbE)

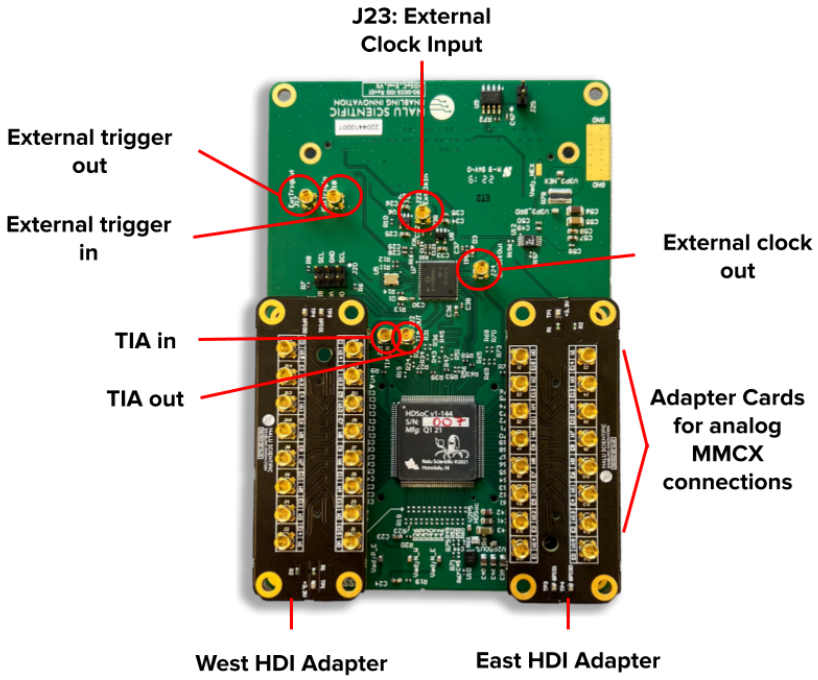


***Figure 3:*** *Top view of the HDSoCv1 with the optional adapter cards.*


***Figure 4:*** *The back of the HDSoCv1 EVB where the FMC connector is attached. This connector mates with the Nexys Artix 7 Video Card.*



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# 5. System Diagram and Internal Functions:

## 5.1 System Level Block Diagram

Below is a functional block diagram of the entire system. The Nexys Artix 7 Video Card is connected to a PC via micro USB to program, control, and monitor using the NaluScope application. The FPGA is connected to the HDSoCv1 Eval Board via FMC connector.

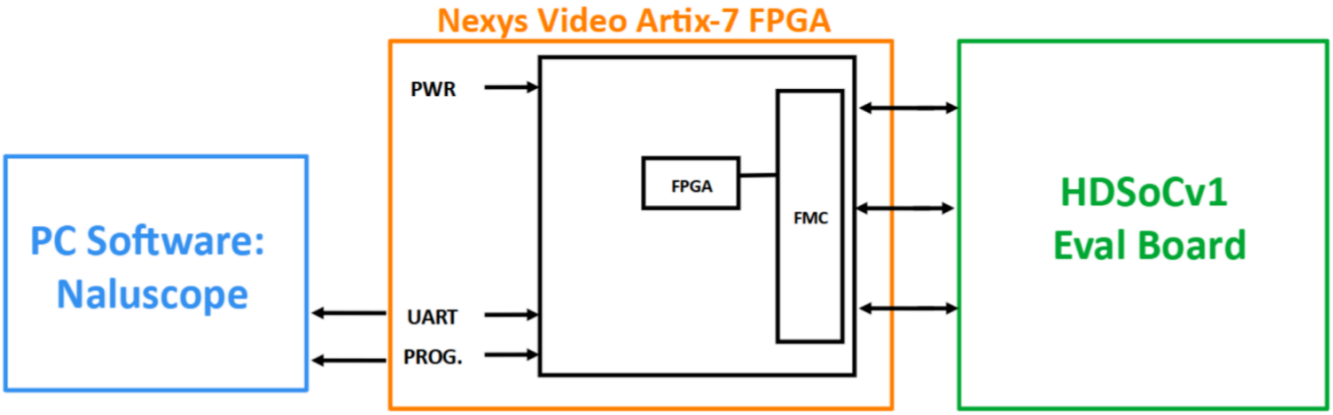


***Figure 5:*** *System level block diagram of what is included in the entire system.*

## 5.2 HDSoCv1 Eval Board Block Diagram

The following functional diagram highlights the important components on the HDSoCv1 Eval Board. An additional feature on the eval board is that it has 32 analog inputs.

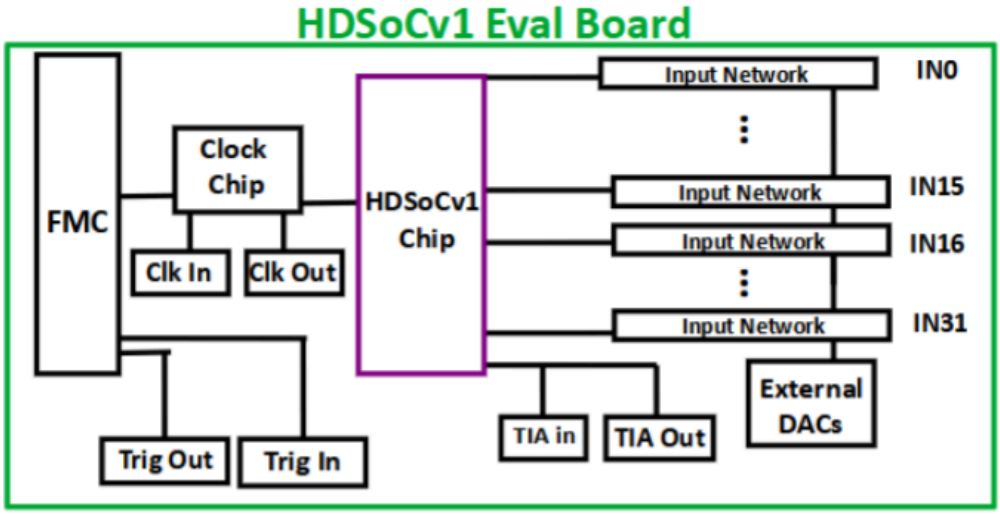


***Figure 6:*** *Block diagram for the HDSoCv1 EVBr2. Highlighted in purple is the HDSoCv1.*



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## 5.3 HDSoCv1 ASIC Internal Functions

The functional block diagram below focuses on important internal functions of the ASIC on the eval board.

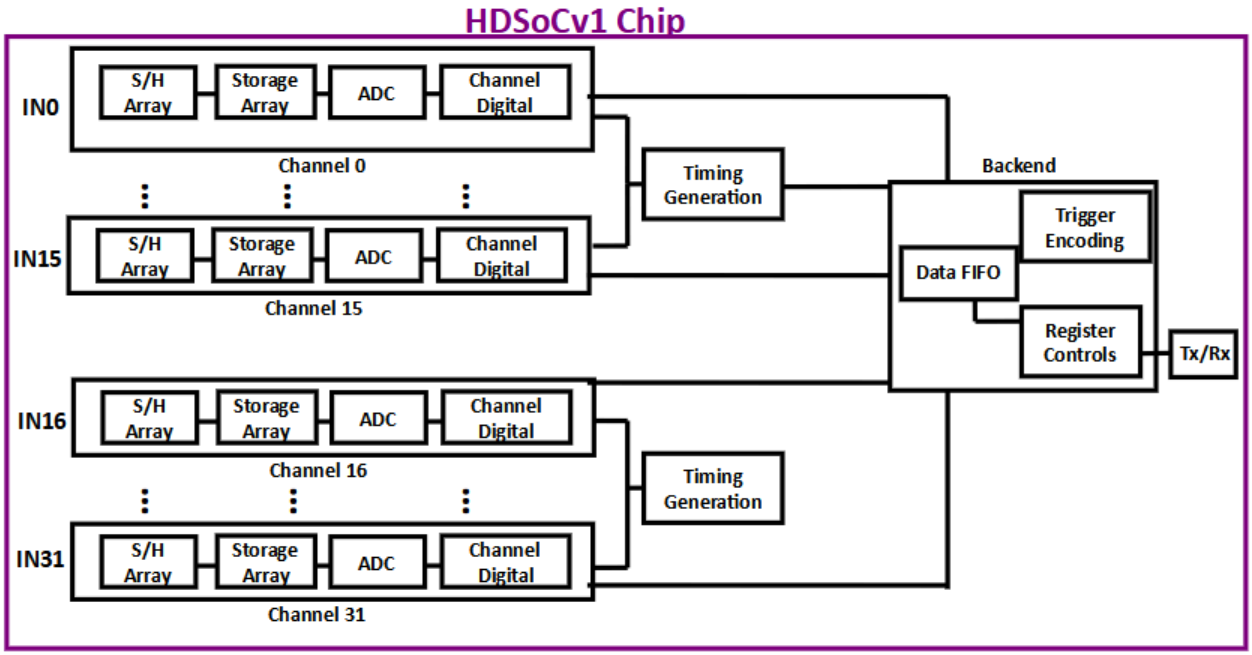


**Figure 7:** The diagram above exhibits an in-depth view of the important internal functions of the ASIC.

**If you have any questions or would like to request more information please contact us.**



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# 6. General Specifications

| | |
|---|---|
| **PC Connectivity** | UART over USB using virtual comport up to 2 Mbaud<br>10/100/ 1000BASE-T |
| **PC Connector Type** | microUSB to USB-A |
| **Power Requirement** | 12V DC 3A |
| **Dimensions (EVB)** | Length: 128mm, Width: 85mm, Height: ZZ mm |
| **Weight (EVB)** | 49g |
| **Dimensions (System)** | |
| **Weight (System)** | 200g (49g + 151g) |
| **Temperature Range** | tbd |
| **Humidity Range** | Operating: 5% to 80% RH non-condensing<br>Storage: 5% to 95% RH non-condensing |
| **Software** | NaluScope (Naludaq: Python package available upon request) |
| **PC Requirement** | Processor, memory and disk space: as required by the operating system |

***Table 2:*** *This table presents the general specifications for the software and HDSoCv1 EVBr2*

## 6.1 Digitization Rate

| | |
|---|---|
| **Simple readout mechanism: (externally trigger and get data from 32 channels)** | All channels digitize in parallel in at most ~4 us per set of 32 samples |
| | Parallel Interface: (can be 2X, 4X, 8X clock<br>• By default it is set at 2X (32ns per period) |
| **Serial Interface** | Maximum rate supported ~ 40kHz/channel (for all channels) at a 4X clock rate |
| **Trigger Mode** | Limit of about 25 kHz/channel with current clocking |

***Table 3:*** *The digitization rate of the HDSoCv1 EVBr2 system*



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## 7. Device Outline and Dimensions

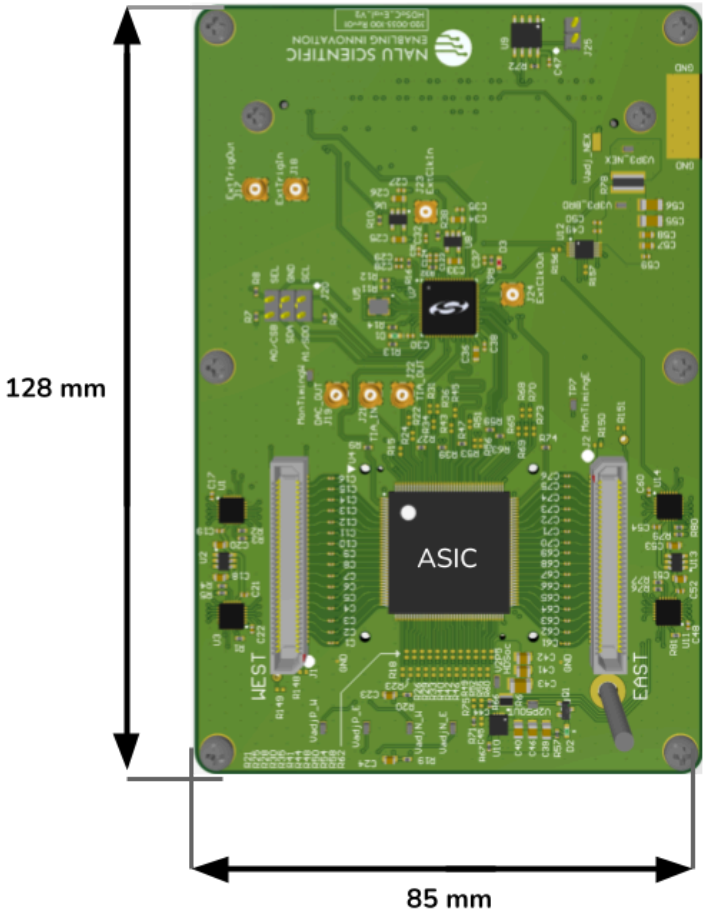


***Figure 5:*** *HDSoCV1 EVBr2 Dimensions. Step model available upon request.*

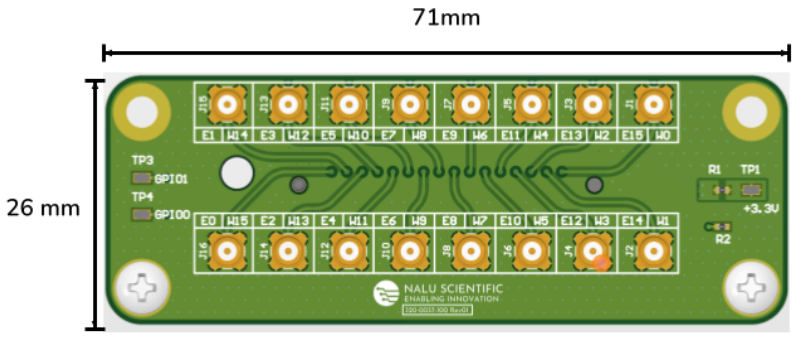


***Figure 6:*** *HDSoCv1 EVBr2 HDI Adapter Card Dimensions. Step model available upon request.*



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