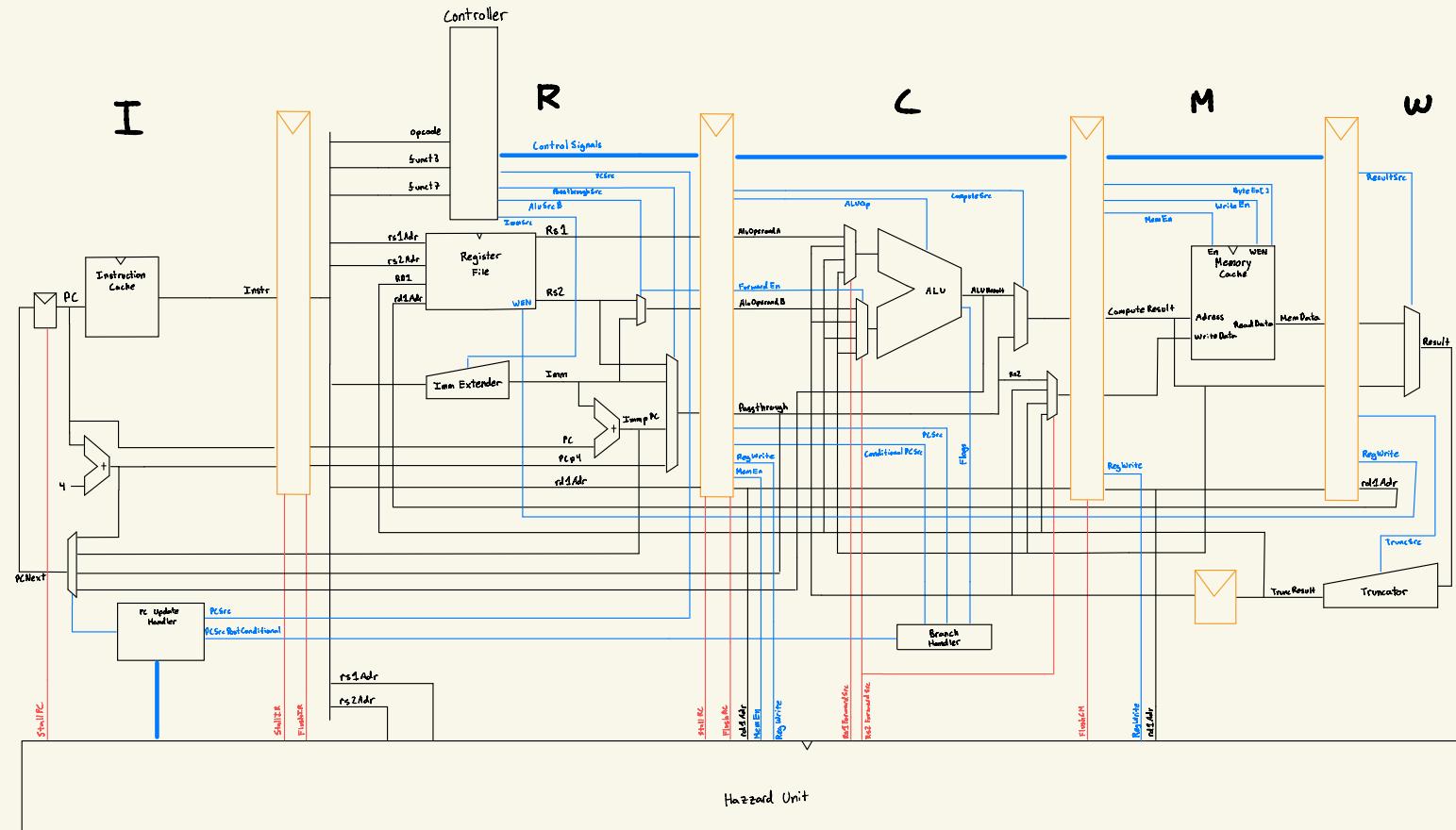
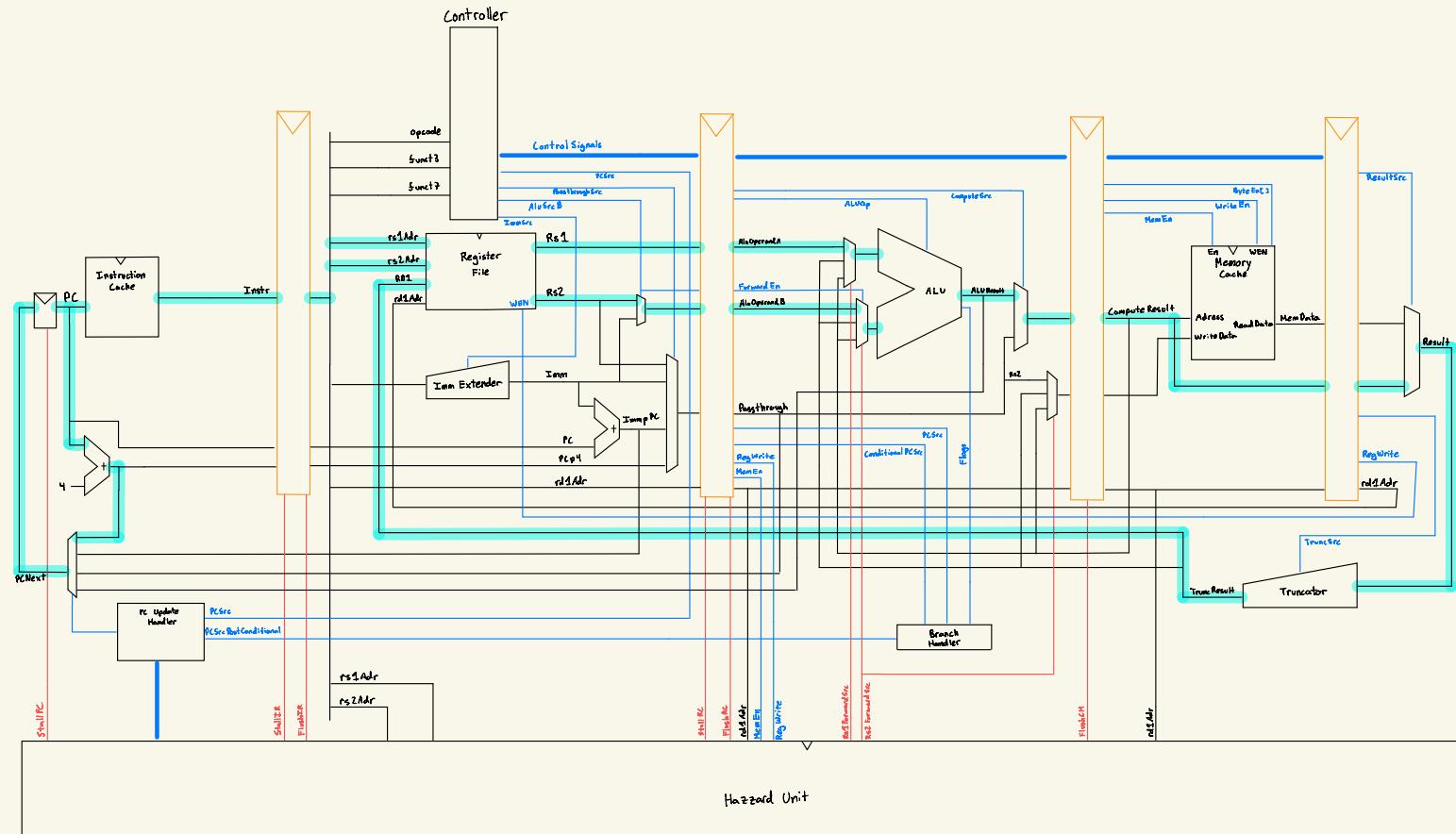


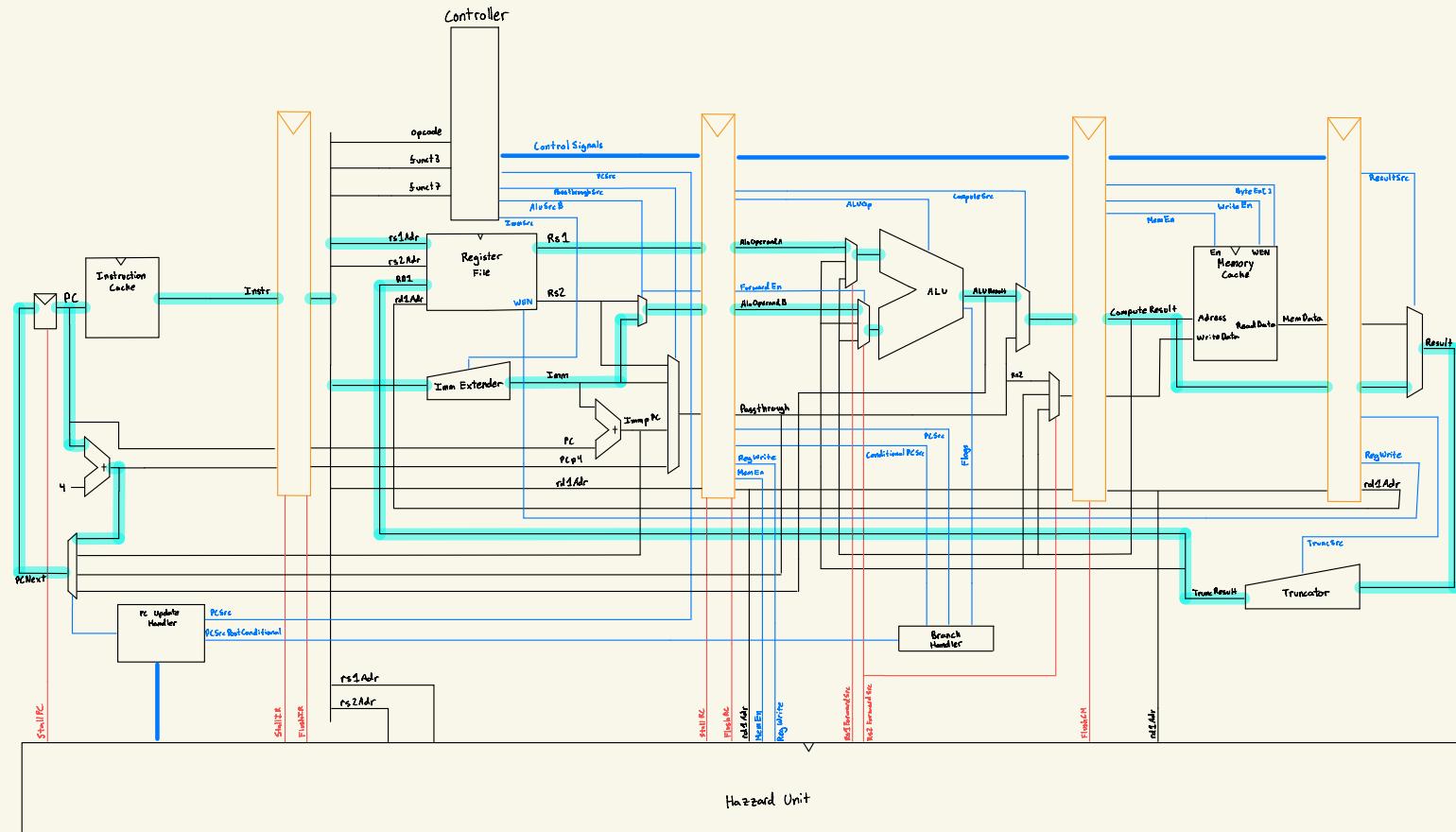
RV32/64I 5-Stage Pipelined Processor



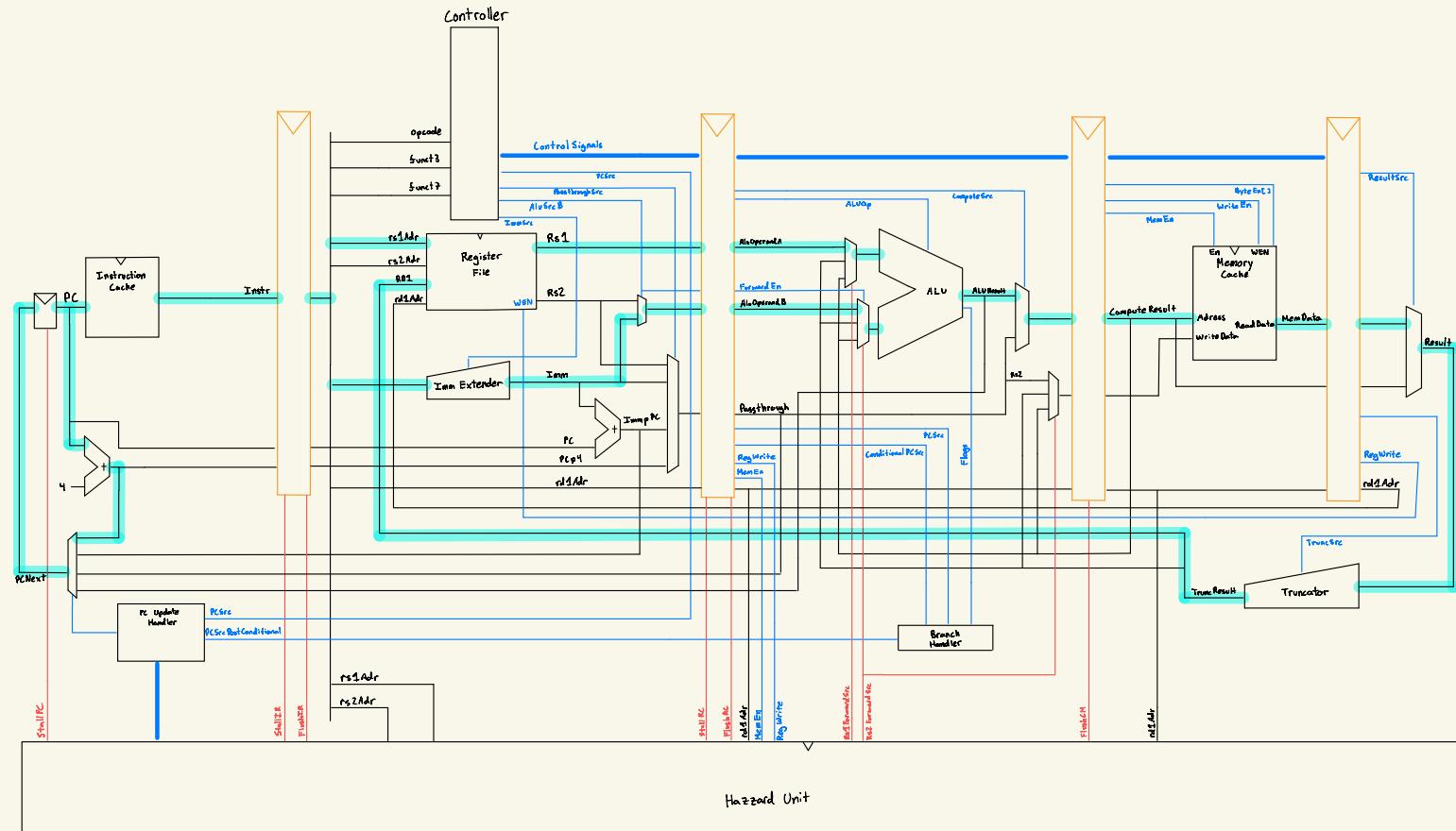
R-Type



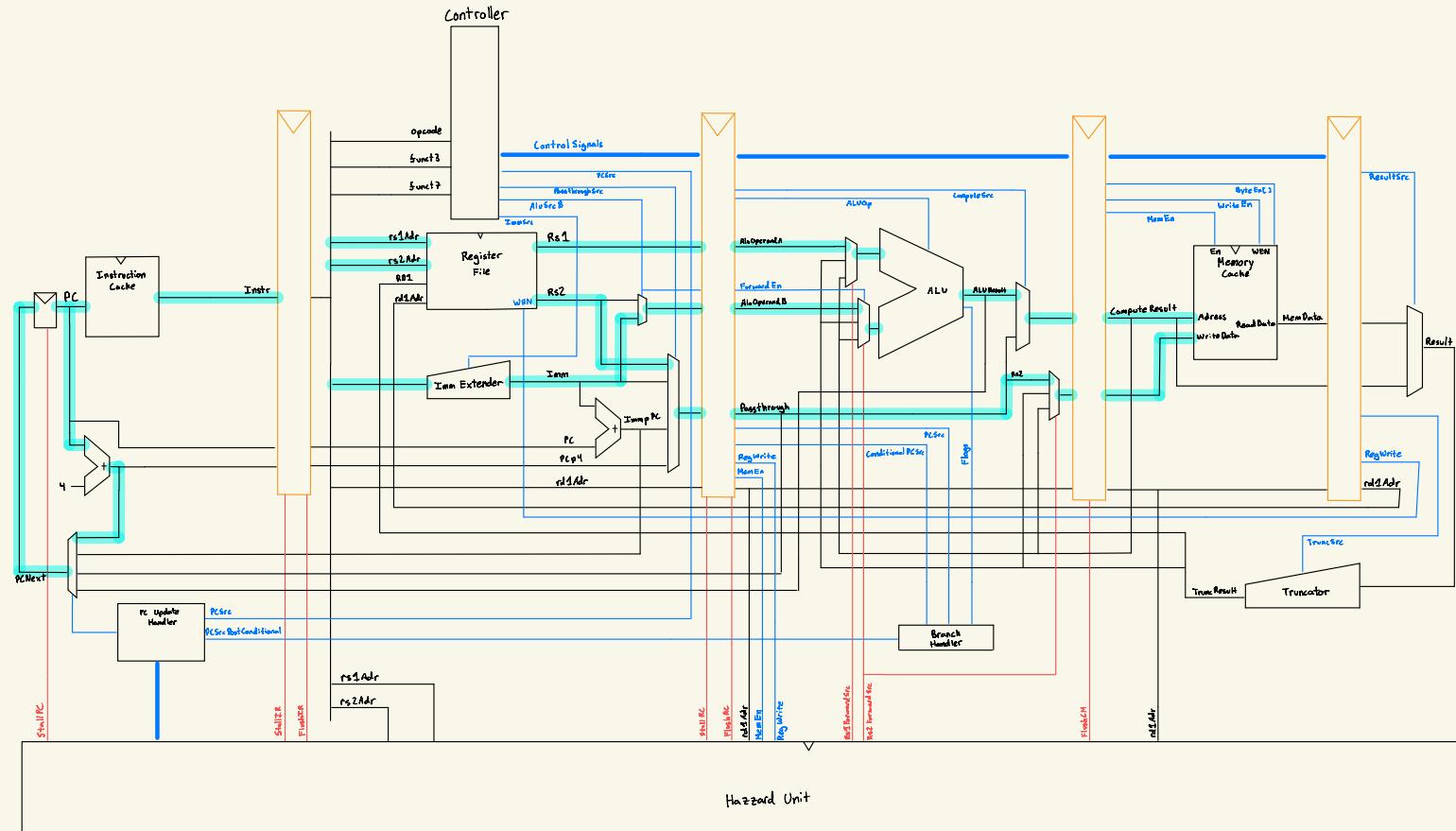
I-Type



L-Type

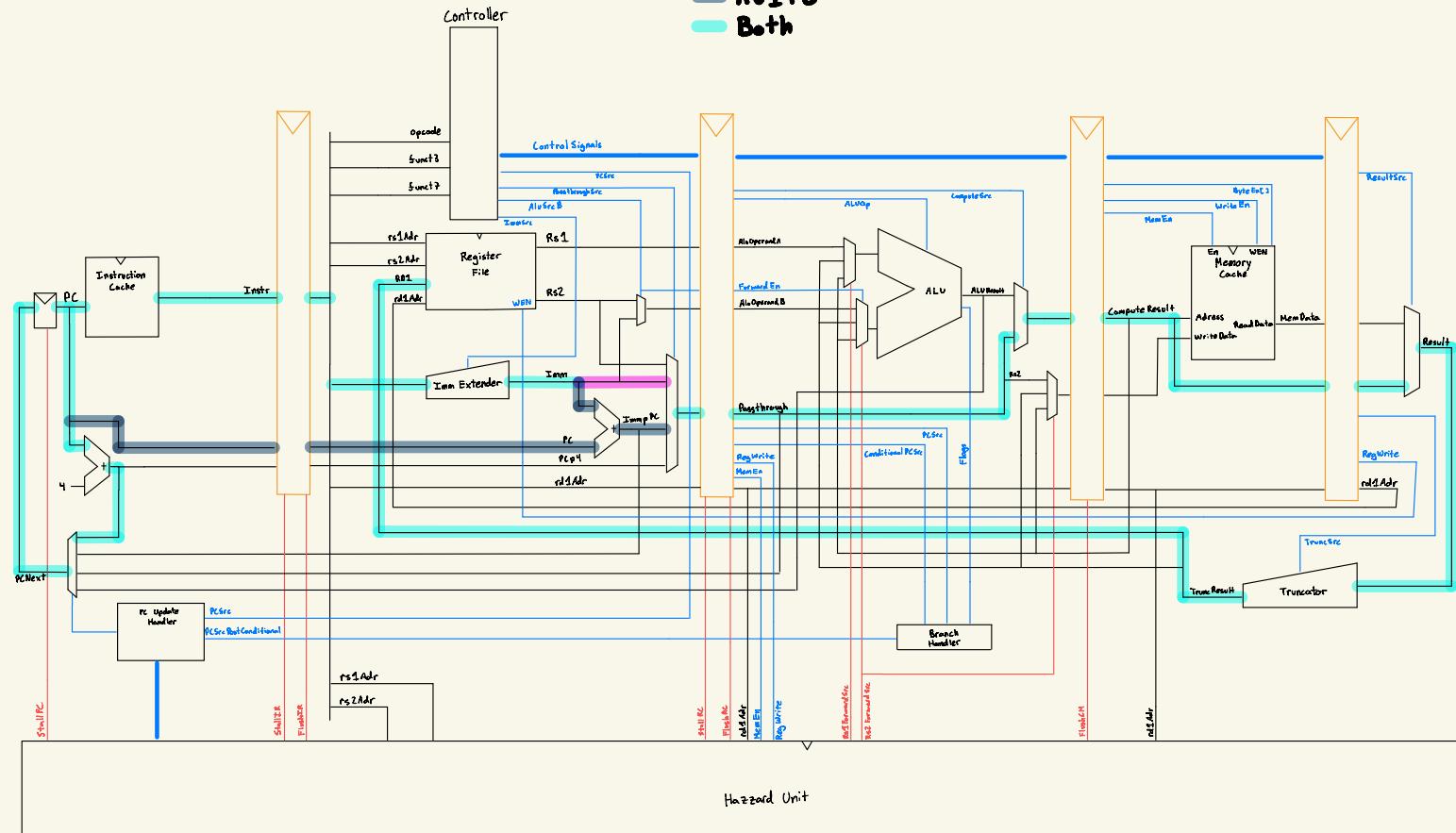


S-Type



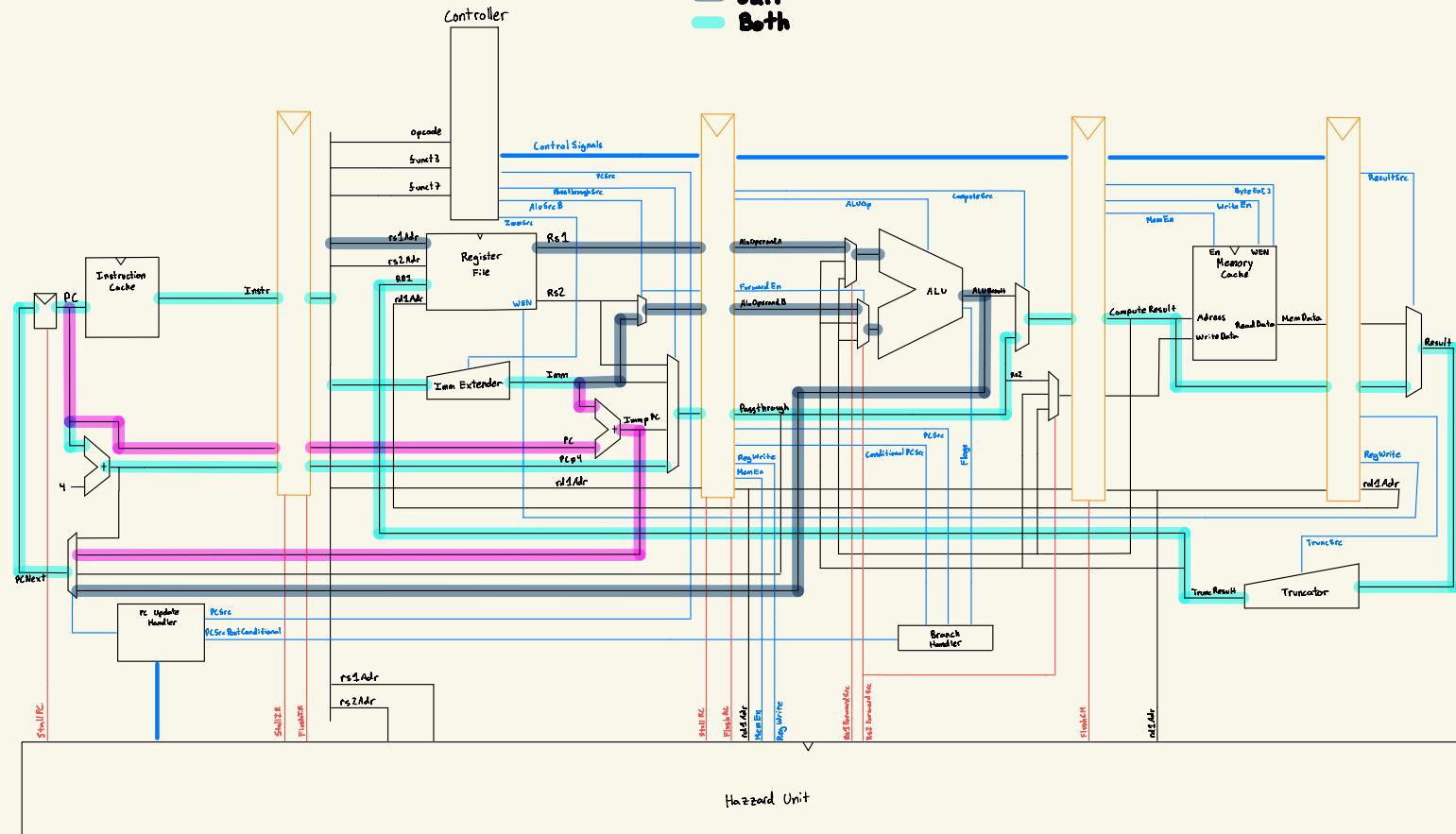
U-Type

- LUI
- AUIPC
- Both

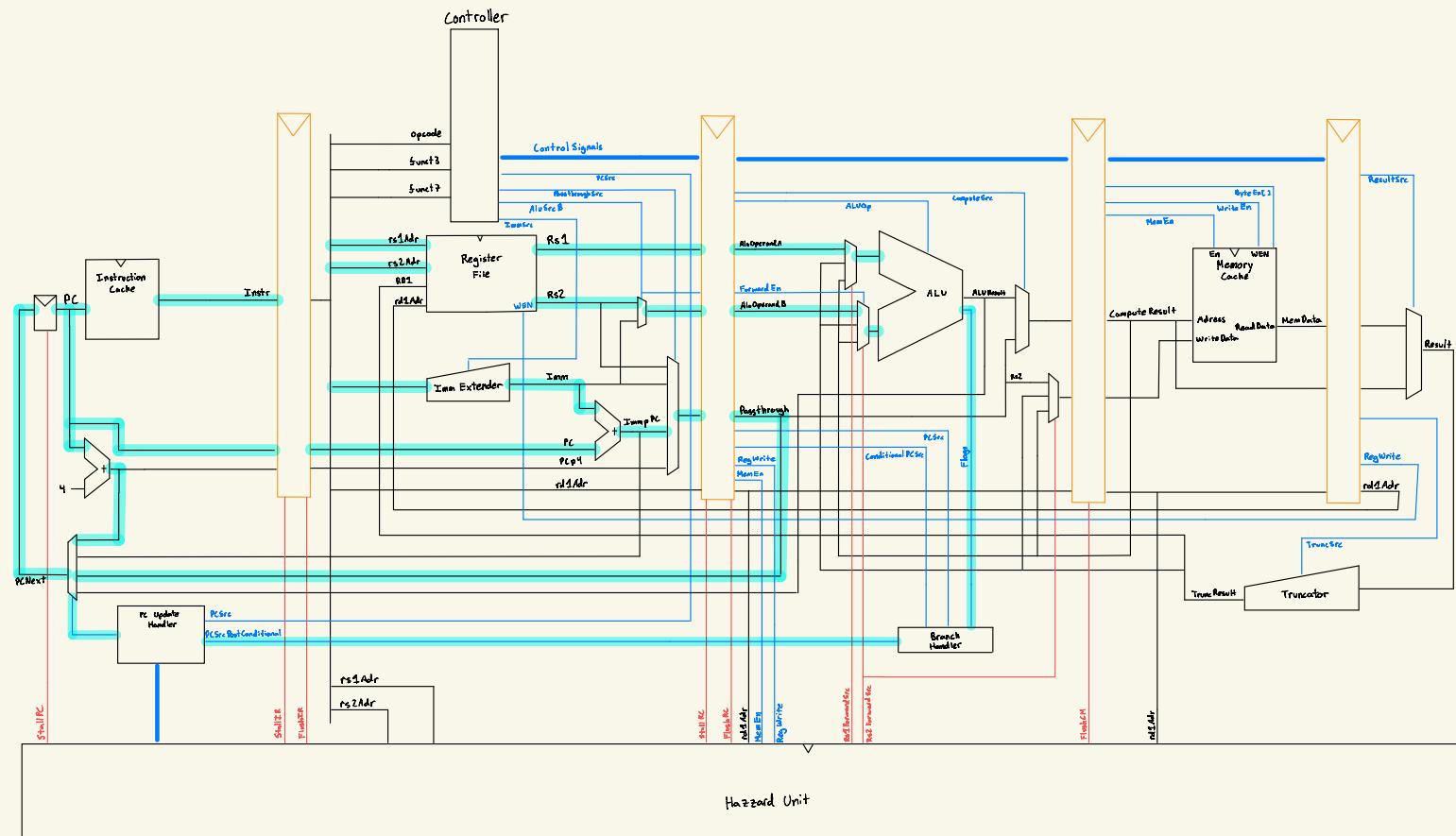


J-Type

- Jal
- Jalr
- Both

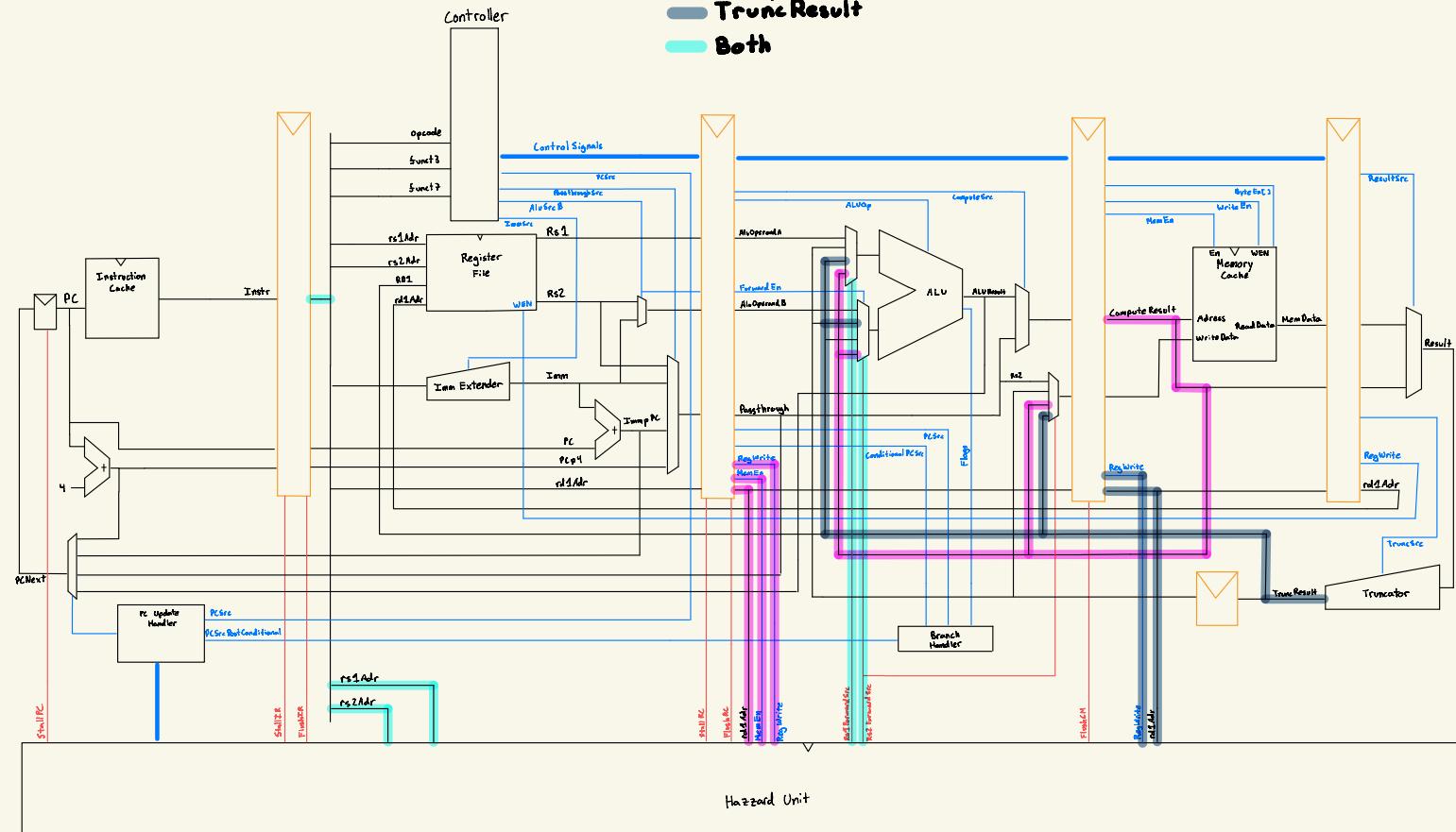


B-Type



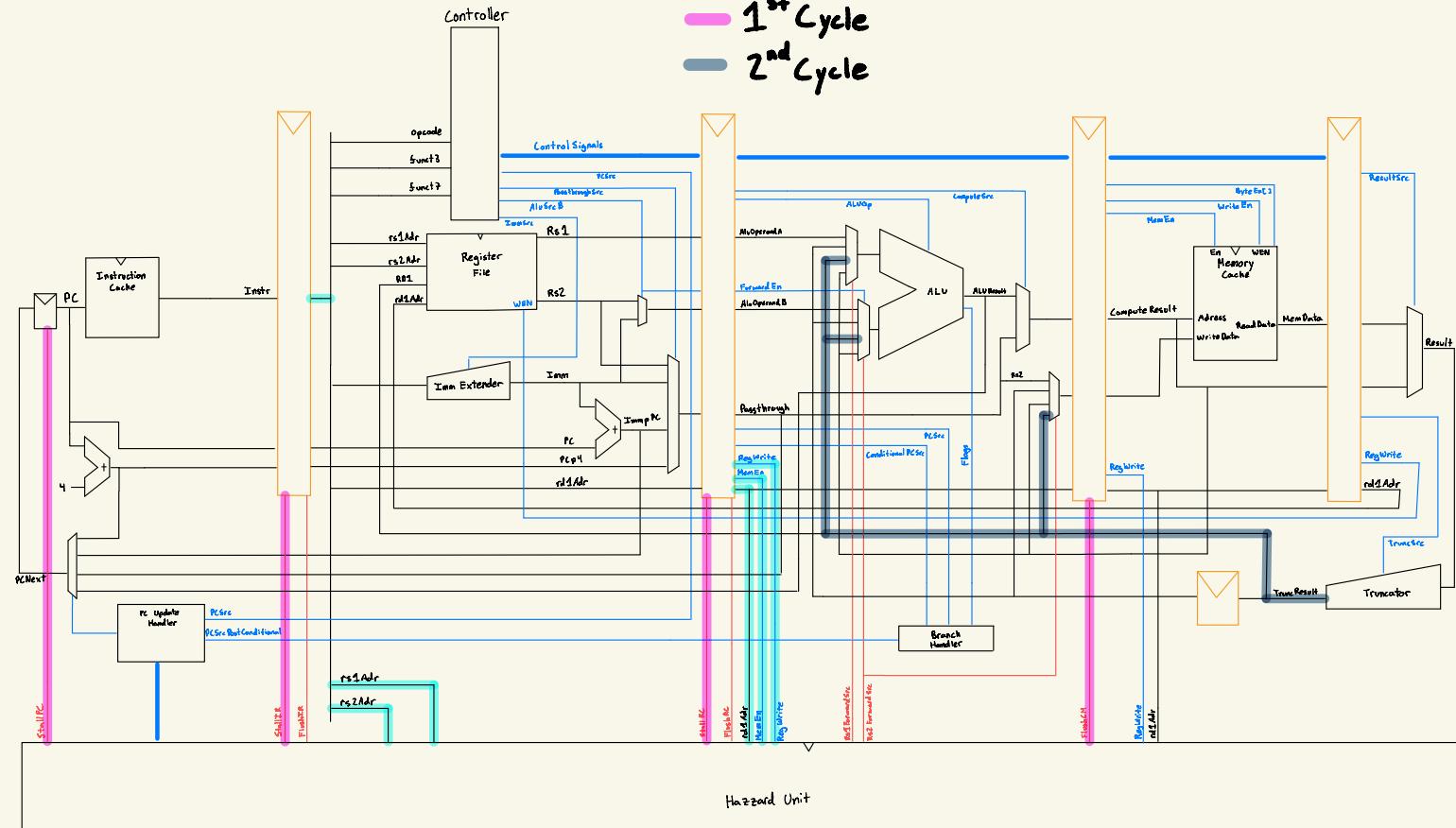
Computational

- Compute Result
- Trunc Result
- Both



Load

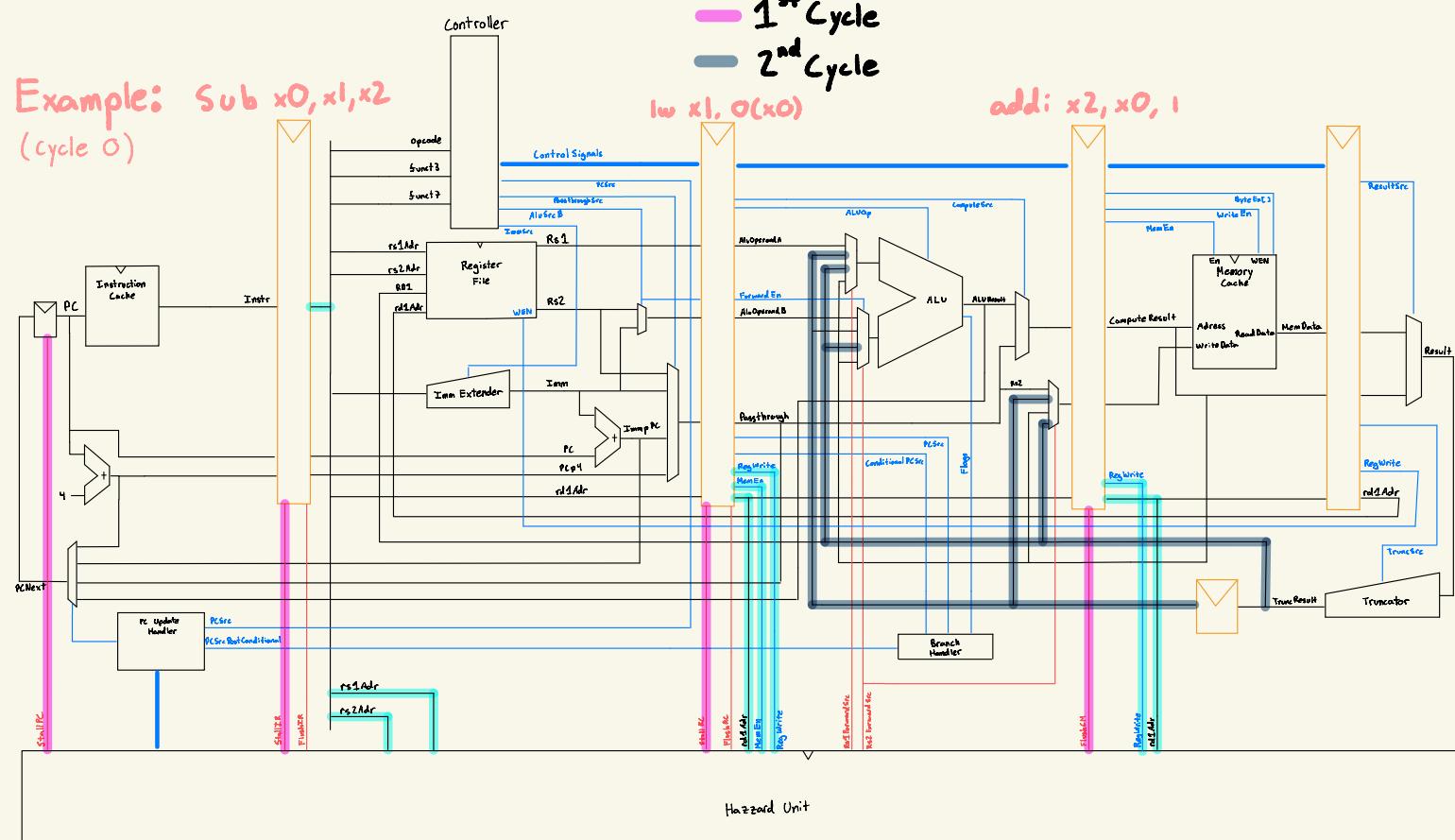
- 0th Cycle
- 1st Cycle
- 2nd Cycle



Load After Computational Exception

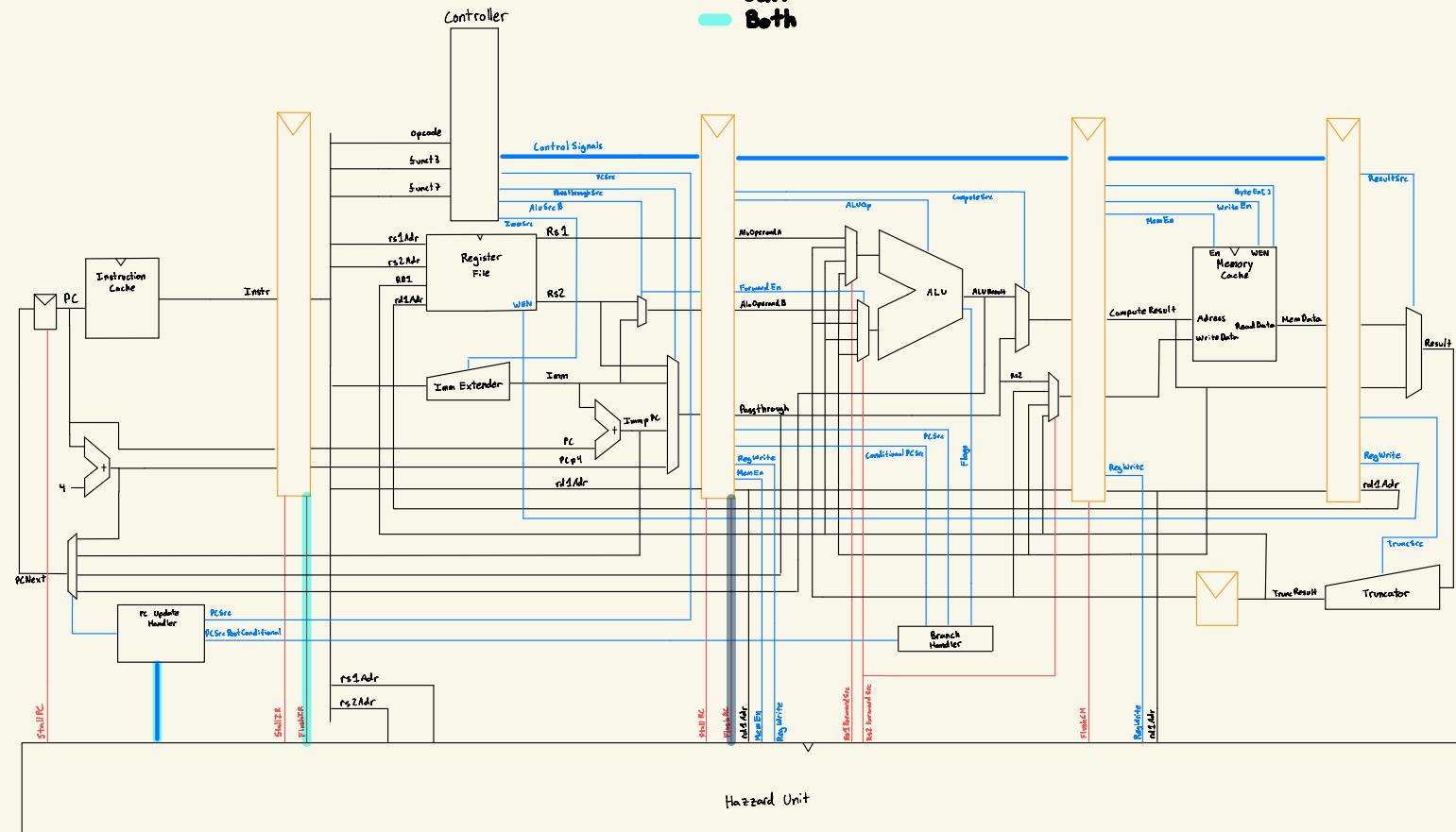
- 0th Cycle
- 1st Cycle
- 2nd Cycle

Example: Sub x0, x1, x2
(cycle 0)



Jumps

Jal
Jair
Beth



Branches

