CSCI 210
HOMEWORK ASSIGNMENT 06

GETTING STARTED WITH THE NIOS II EMBEDDED SOFT PROCESSOR

In this homework you will complete the "Introduction to the Altera Qsys System Integration Tool" tutorial, which is available in the materials folder in Moodle in the file `Introduction_to_the_Altera_Qsys_Tool.pdf`. You should instantiate the NIOS II processor with Verilog (not VHDL). The tutorial has both versions in it.

At the end of this tutorial, you'll get to the point where you run an assembly program on the NIOS II. Using that code as a starting point, modify that given code to maintain and display a running sum of the numbers input from the switches, rather than just outputting directly the numbers that were input.

Submission: (no late work accepted)

Prior to the due date and time posted in Moodle, upload your project into Moodle. This will be a zip file which contains the entire project directory structure. Your submission should be named userid-210-HW06.zip, where userid is your userid. Make sure to check two things after submitting your assignment:

(1) Your file has successfully been uploaded into Moodle.
(2) Download your file from Moodle, unpack the file, load and execute it on your board. If this doesn't work for me, you will loose significant credit on the assignment.