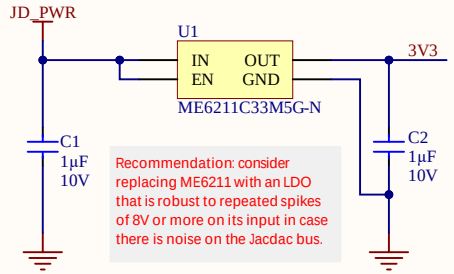
3V3 Regulator

This component is a power-consumer.

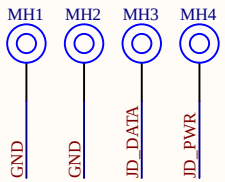


LDO provides 3V3 for diode clamps and optionally powers the prototype module through D1.

Recommendation: consider replacing ME6211 with an LDO that is robust to repeated spikes of 8V or more on its input in case there is noise on the Jacdac bus.

U1 alternative parts:
ME6212C33M5G 6V 260mV @ 200mA Iout 350mA
NCP114ASN330T1G 5.5V 225mV @ 300mA Iout 300mA
NCP114BSN330T1G 5.5V 225mV @ 300mA Iout 300mA
...and many other LDOs.

Mounting holes

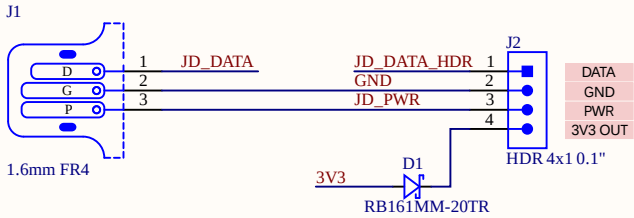


Mounting holes are electrically connected to the Jacdac bus nets so they can be used as an alternative to the PCB edge connector. Please use the following reference designators and net mapping:

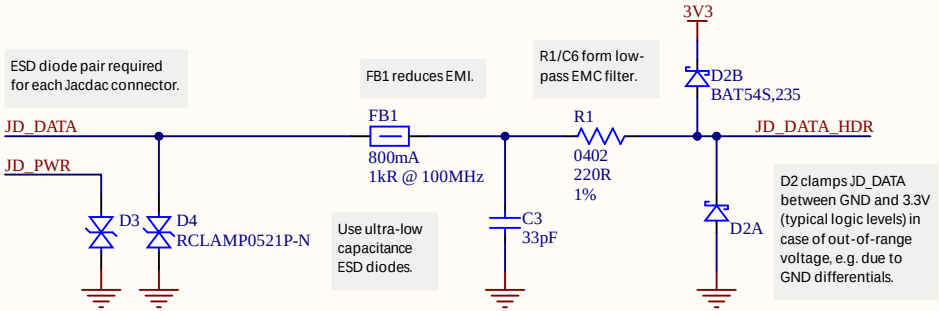
MH1 & MH2: GND
MH3: JD_DATA
MH4: JD_PWR

This design uses Jacdac 'small' mounting holes: PTH with finished diameter of 2.1mm, annular copper ring of 3.0mm diameter & copper/component keepout of 5.0mm. The mounting holes must be on 2.5mm pitch. Mounting holes should have appropriate silkscreen marker, and MH1 should have a pin 1 marker on the top side.

Jacdac interface



D1 prevents back-powering U1 from external source, but has forward voltage drop of 350mV @1A.



ESD diode pair required for each Jacdac connector.

FB1 reduces EMI.

R1/C6 form low-pass EMC filter.

Use ultra-low capacitance ESD diodes.

D2 clamps JD_DATA between GND and 3.3V (typical logic levels) in case of out-of-range voltage, e.g. due to GND differentials.

This reference design is a guideline. Please refer to the Jacdac docs online at https://aka.ms/jacdac for the definitive and most up-to-date information.

Silkscreen should include text to identify the module type and revision, and optionally a QR code.

This design uses a 'cute' board shape.

Silkscreen & layout notes

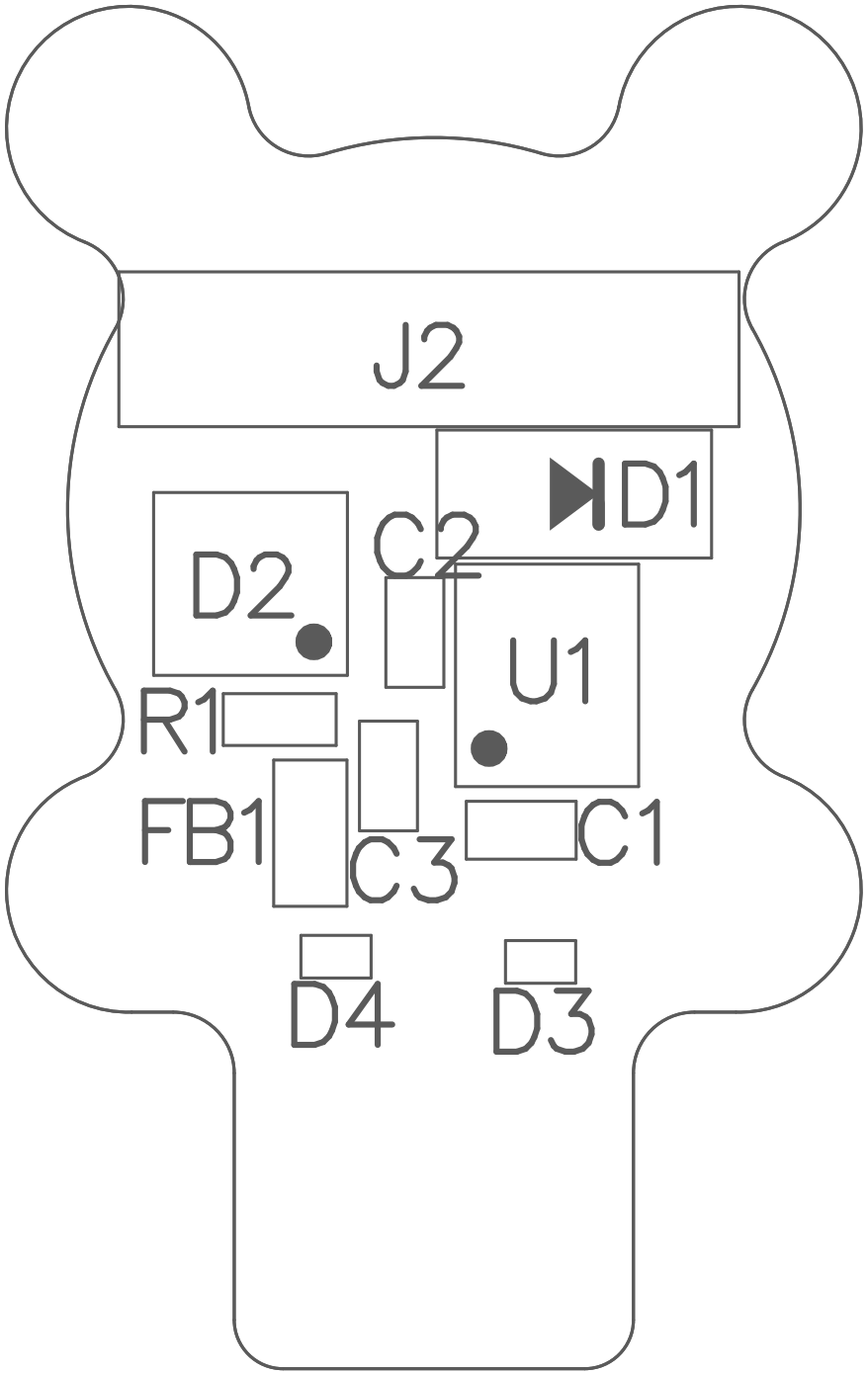
Block name

Design notes

When this PDF is viewed with Adobe Reader, clicking on components shows part numbers and other details.

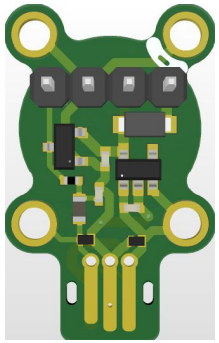
PROJECT FILENAME JacdacPinHeaders 45.PrjPCB	PROJECT CODENAME JacdacPinHeader	Microsoft	PROJECT DESCRIPTION Jacdac bus breakout for module prototyping
SHEET FILENAME JacdacPinHeaders 45.SchDoc	LICENCE Attribution 4.0 International (CC BY 4.0)	LAST MODIFIED 10/01/2022	PAGE 1 OF 1
		DRAWN BY GD, JD, SH	SHEET DESCRIPTION Complete design
			REVISION 0.3 PCB ID 45-0.3

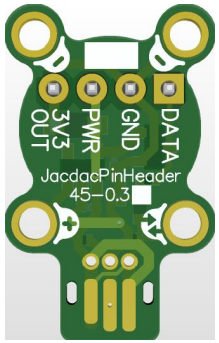
Board Outline
Top Assy



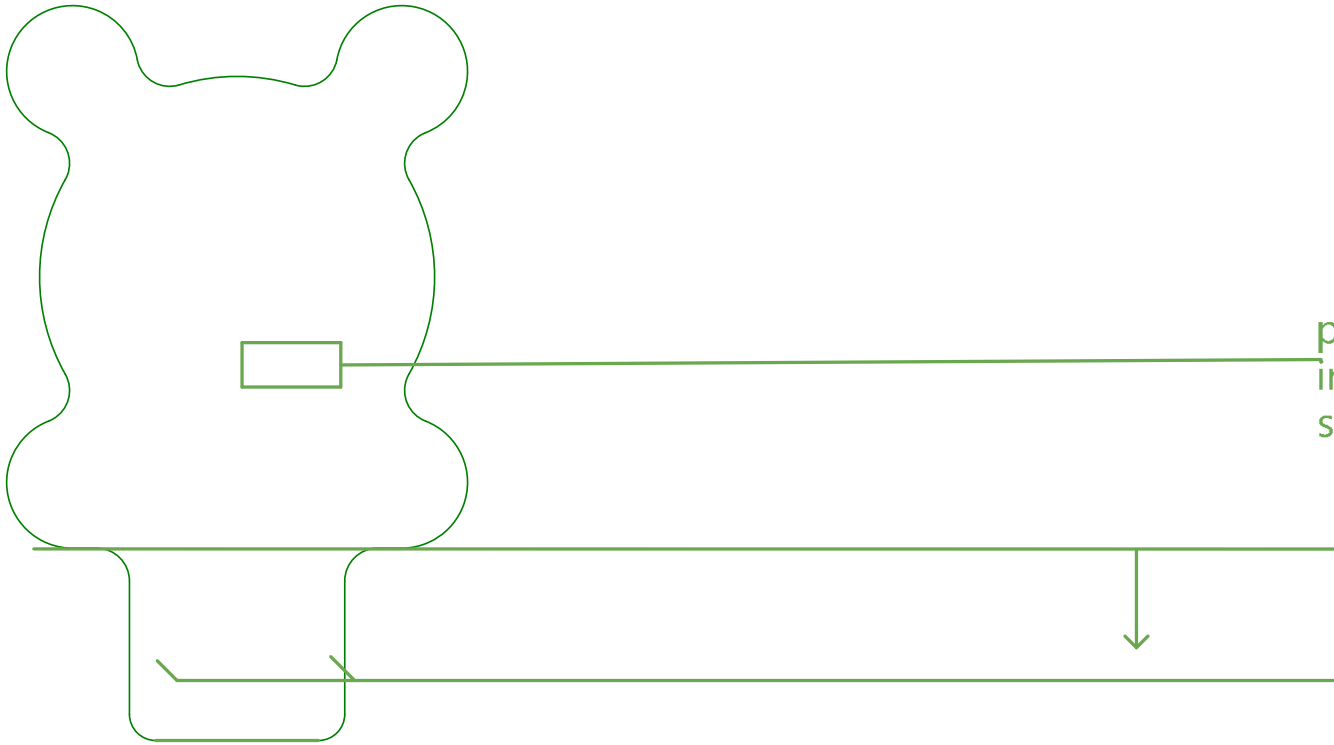
Board Outline

Bottom Assy



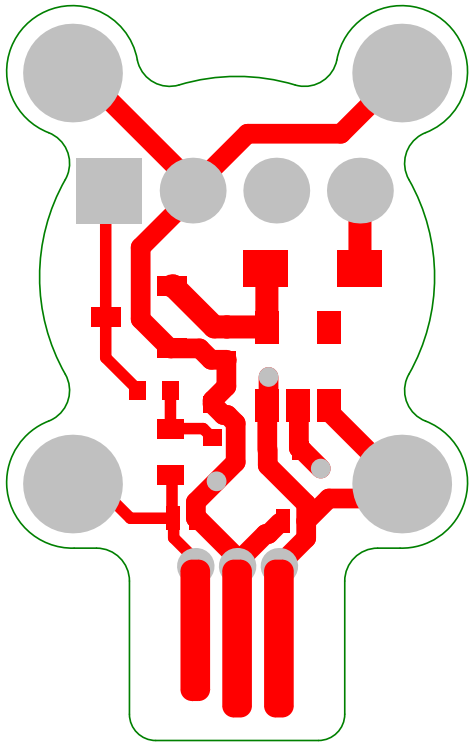

3V3
OUT
PWR
GND
DATA
JacdacPinHeader
45-0.3

Fabrication Notes
Board Outline



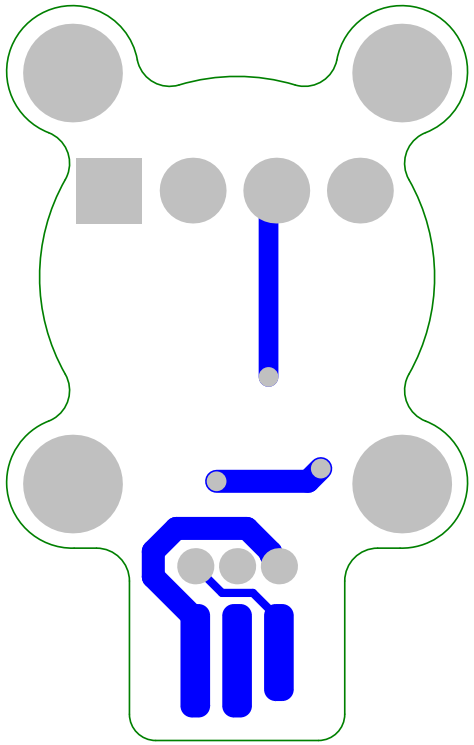
Top Layer

Board Outline



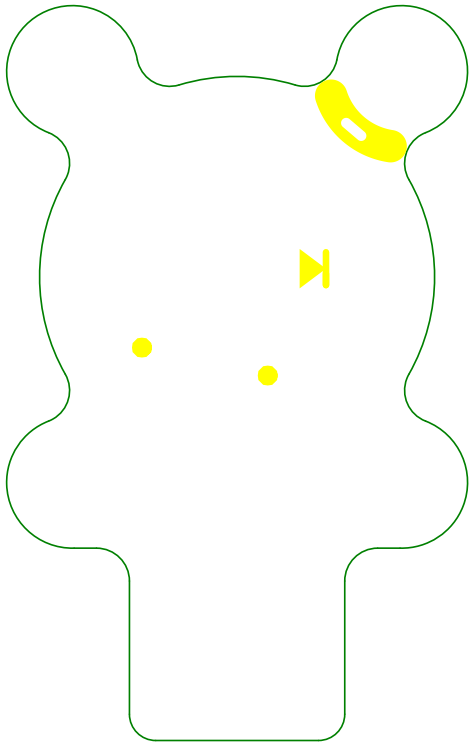
Bottom Layer

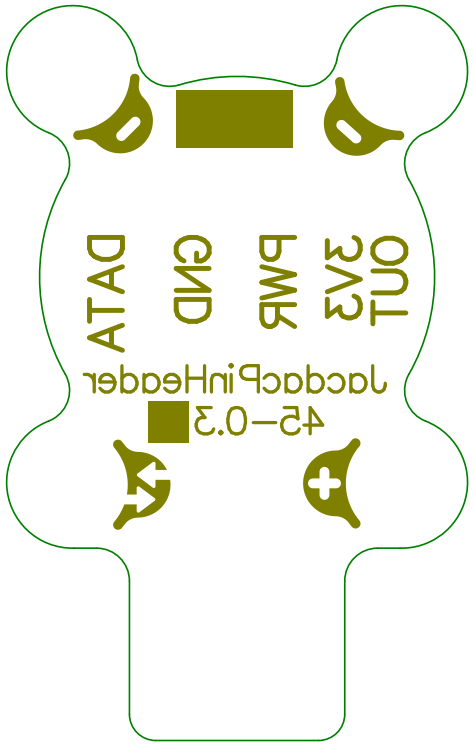
Board Outline



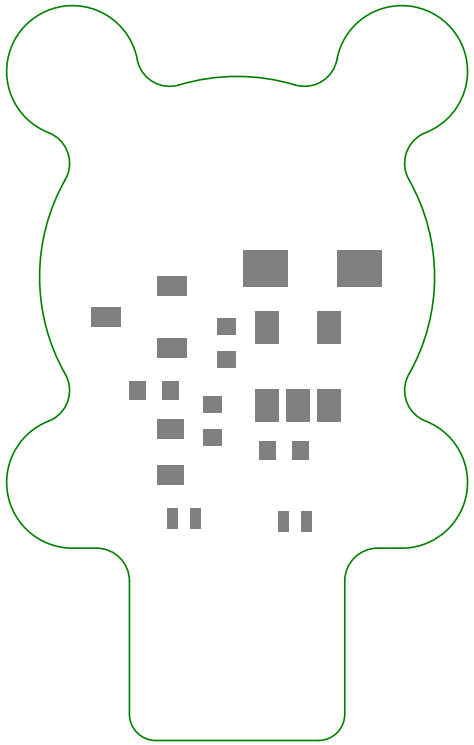
Board Outline

Top Overlay



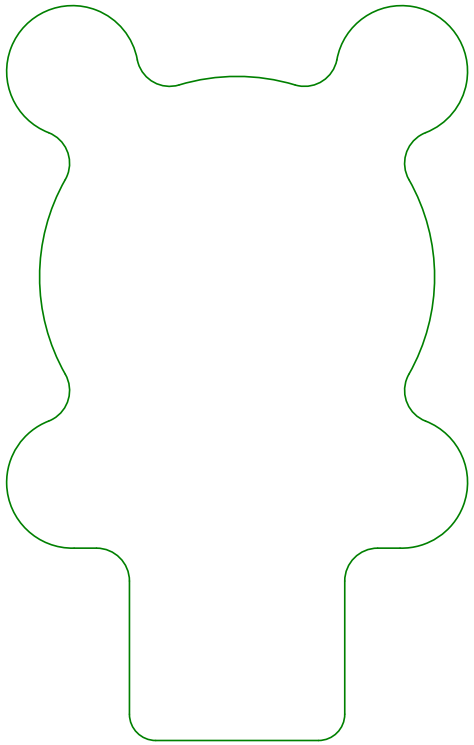

Board Outline
Bottom Overlay
DATA
GND
PWR
3V3 OUT
JacdacPinHeader
4.5–0.3

Board Outline



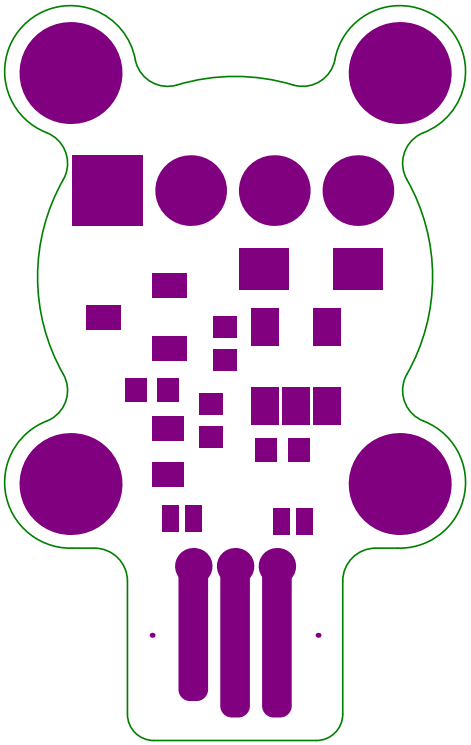
Top Paste

Board Outline



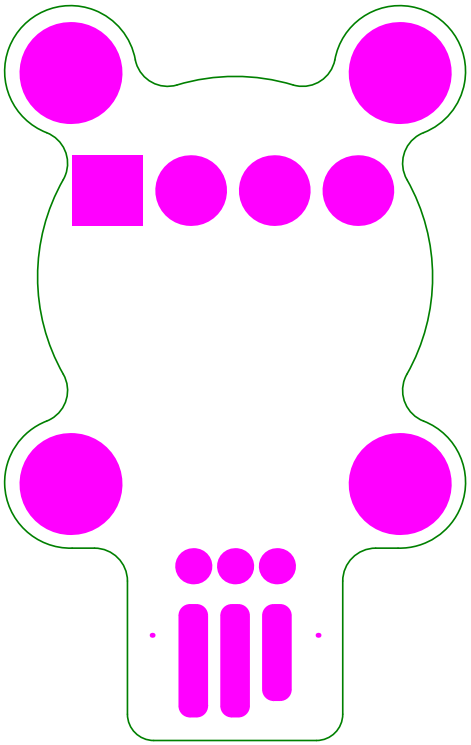
Bottom Paste

Board Outline



Top Solder (resist)

Board Outline



Bottom Solder (resist)

Board Outline