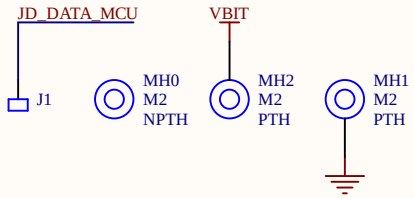
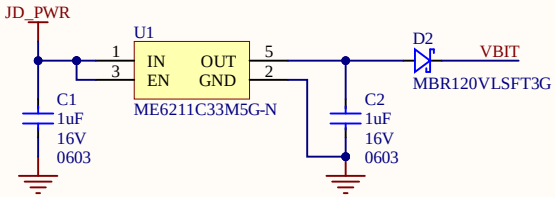
micro:bit connections

190 mA max current draw from micro:bit V2.



Power supply



Jacdac interface

Jacdac (https://aka.ms/jacdac) is a new "plug and play" protocol for connecting microcontrollers and peripherals. Its flexible topology, dynamic discovery and power delivery provide a great user experience for makers and students.

Jacdac provides 1Mbps communications and power delivery. JD_DATA uses 3.3V logic, JD_PWR is nominally 5V.

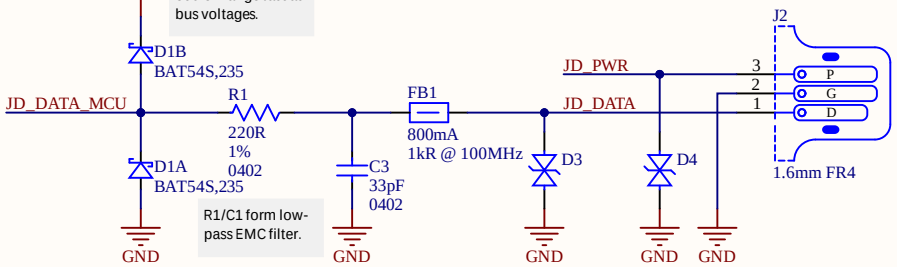
Please refer to the Jacdac docs online at https://aka.ms/jacdac for the definitive and most up-to-date information.

This component is a power consumer.

D1 clamp JD_DATA between GND and VBIT in case of out-of-range Jacdac bus voltages.

FB1 filter reduces EMI.

Use ultra-low cap ESD diodes, capacitance <10pF.

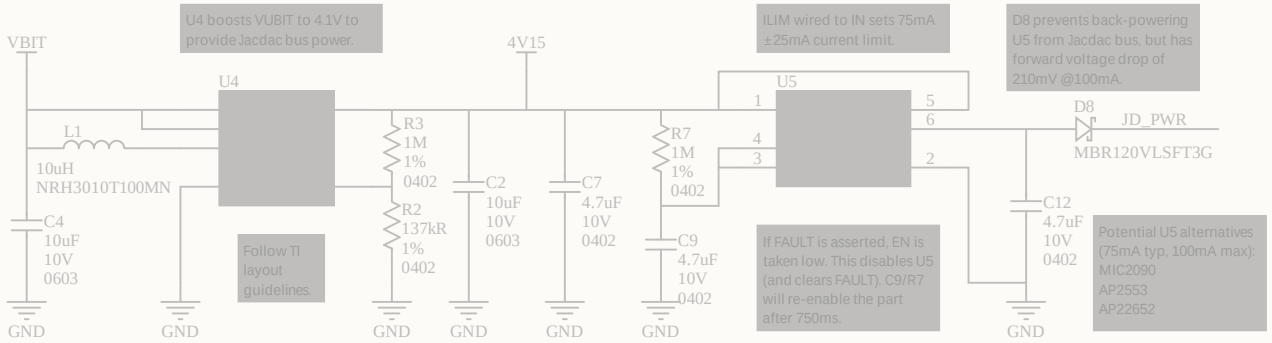


R1/C1 form low-pass EMC filter.

Jacdac power delivery is optional. Spec requires current limiting with auto retry, and that nothing gets hot! This shield delivers 75mA typical, 100mA max.

Since JD_PWR supplies up to 100mA, ≥3.85V is needed at the connector, resulting in at least 3.7V at each module.Therefore U5 output must be 4.1V. This draws 145mA from 3.3V VUBIT supply.

Check Jacdac spec for information about higher currents and MCU-based 'high current power providers'.



Key:

- Silkscreen & layout notes
- Block name
- Design notes

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When this PDF is viewed with Adobe Reader, clicking on components shows part numbers and other details.

PROJECT FILENAME JacdacMicroBitBackPack 94.PrjPCB	PROJECT CODENAME JacdacMicroBitBackPack	Microsoft	PROJECT DESCRIPTION Compact Jacdac adapter for the BBC micro:bit V2
SHEET FILENAME JacdacMicroBitBackPack 94.SchDoc	LICENCE Attribution 4.0 International (CC BY 4.0)	LAST MODIFIED 08/04/2022	PAGE 1 OF 2
DRAWN BY Steve Hodges	SHEET DESCRIPTION complete design	REVISION 0.1	PCB ID 94-0.1