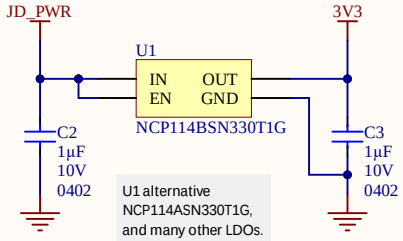
3V3 regulator

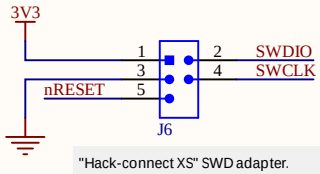


Recommendation: consider replacing NCP114 with an LDO that is robust to repeated spikes of 8V or more on its input in case there is noise on the Jacdac bus.

This component is a power-consumer.

U1 alternative NCP114ASN330T1G, and many other LDOs.

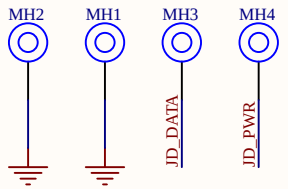
Programming/debug connector



"Hack-connect XS" SWD adapter.

https://arcade.makecode.com/hardware/dbg

Mounting holes

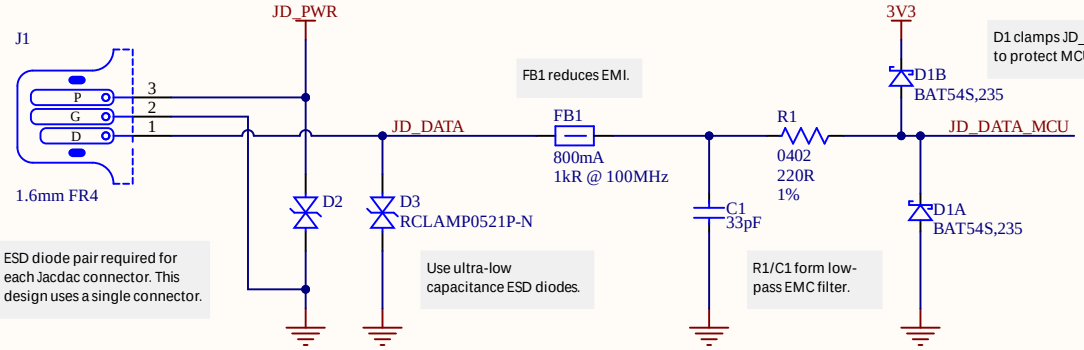


Mounting holes are electrically connected to the Jacdac bus nets so they can be used as an alternative to the PCB edge connector. Please use the following reference designators and net mapping:

MH1 & MH2: GND
MH3: JD_DATA
MH4: JD_PWR

This design uses Jacdac 'small' mounting holes: PTH with finished diameter of 2.1mm, annular copper ring of 3.0mm diameter & copper/component keepout of 5.0mm. The mounting holes must be on 2.5mm pitch. Mounting holes should have appropriate silkscreen marker, and MH1 should have a pin 1 marker on the top side.

Jacdac connector

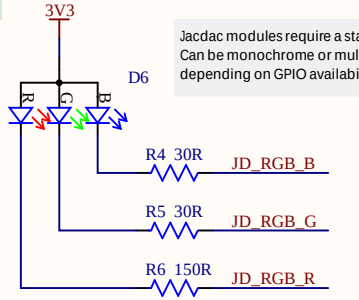


ESD diode pair required for each Jacdac connector. This design uses a single connector.

Use ultra-low capacitance ESD diodes.

R1/C1 form low-pass EMC filter.

Status LED



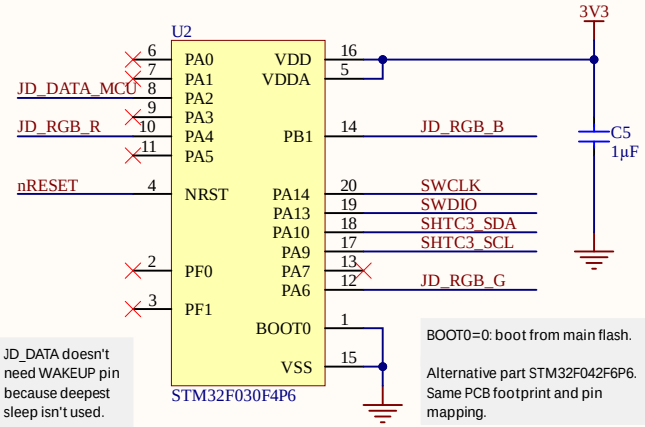
Jacdac modules require a status LED. Can be monochrome or multicolor depending on GPIO availability.

Tuoahan TZ-P4-1615RGBTCA1-0.55T RGB is footrpint-compatible alternative for D6. If using alternative part recalculate R4-R6.

MCU

U3 critical pin mappings:

PA2 USART1_TX for JD data	PA10 SHTC3_SDA
PA4 TIM14_CH1 for RGB_R	PA9 SHTC3_SCL
PA6 TIM16_CH1 for RGB_G	
PB1 TIM3_CH4 for JD_RGB_B	

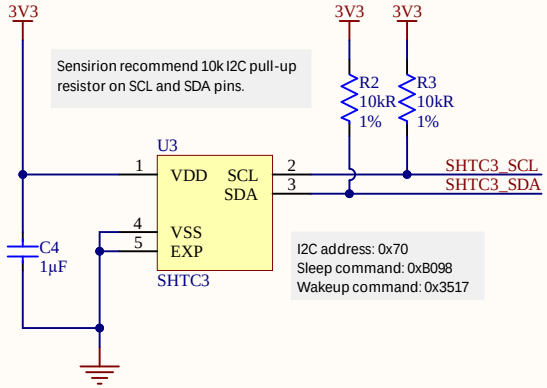


JD_DATA doesn't need WAKEUP pin because deepest sleep isn't used.

BOOT0=0: boot from main flash.

Alternative part STM32F042F6P6. Same PCB footprint and pin mapping.

Relative humidity & temperature sensor



I2C address: 0x70
Sleep command: 0xB098
Wakeup command: 0x3517

This reference design is a guideline. Please refer to the Jacdac docs online at https://aka.ms/jacdac for the definitive and most up-to-date information.

Silkscreen should include text to identify the module type and revision, and optionally a QR code.

This design uses a 'cute' board shape.

Silkscreen & layout notes

Block name

Design notes

When this PDF is viewed with Adobe Reader, clicking on components shows part numbers and other details.

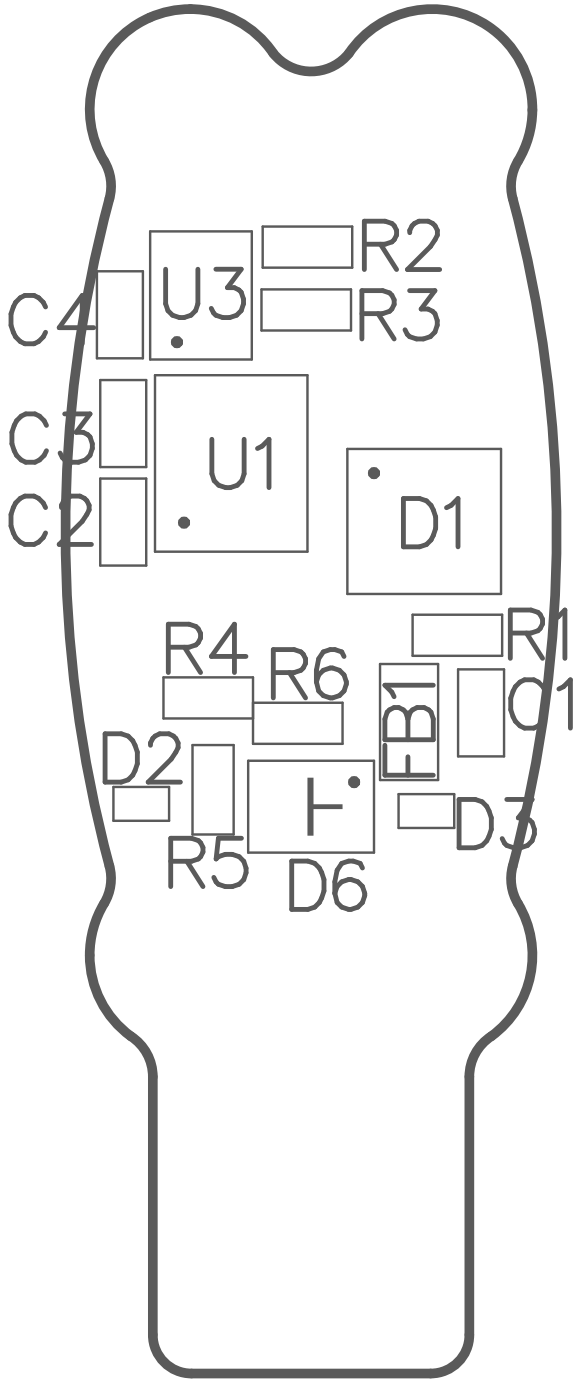
Microsoft

PROJECT DESCRIPTION: Jacdac relative humidity and temperature module

SHEET DESCRIPTION: Complete design

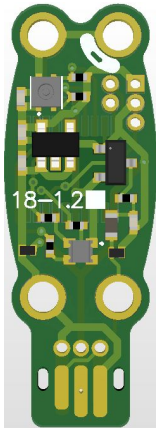
PROJECT FILENAME JacdacRHTemp 18.PrjPCB	PROJECT CODENAME JacdacRHTemp				
SHEET FILENAME JacdacRHTemp 18.SchDoc	LICENCE Attribution 4.0 International (CC BY 4.0)	LAST MODIFIED 03/12/2021	PAGE 1 OF 1	DRAWN BY D. Gakure & S. Hodges	REVISION 1.2 PCB ID 18-1.2

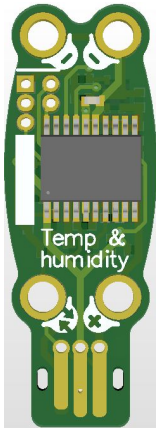
Board Outline
Top Assy



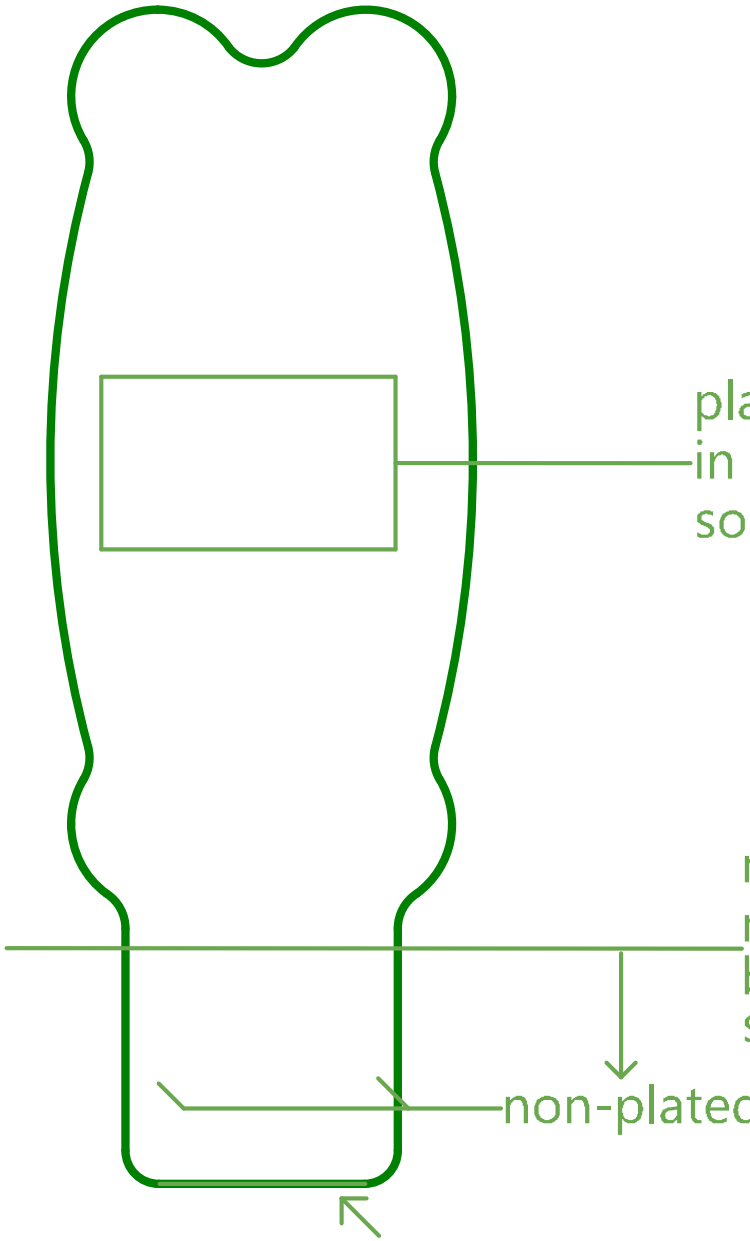
Board Outline

Bottom Assy


18−1.2


Temp &
humidity

Fabrication Notes
Board Outline



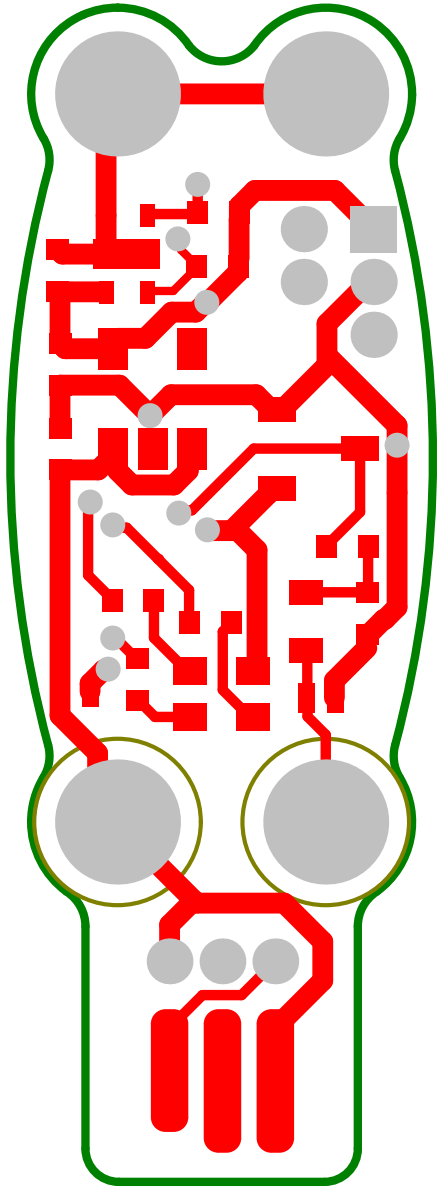
place any PCB manufacturer identifiers
in this region on bottom layer,
so they will be underneath the TSSOP

no board edge pips/
rat's teeth/mouse bites
below this line - make
sure board edge is clean

non-plated slots x2

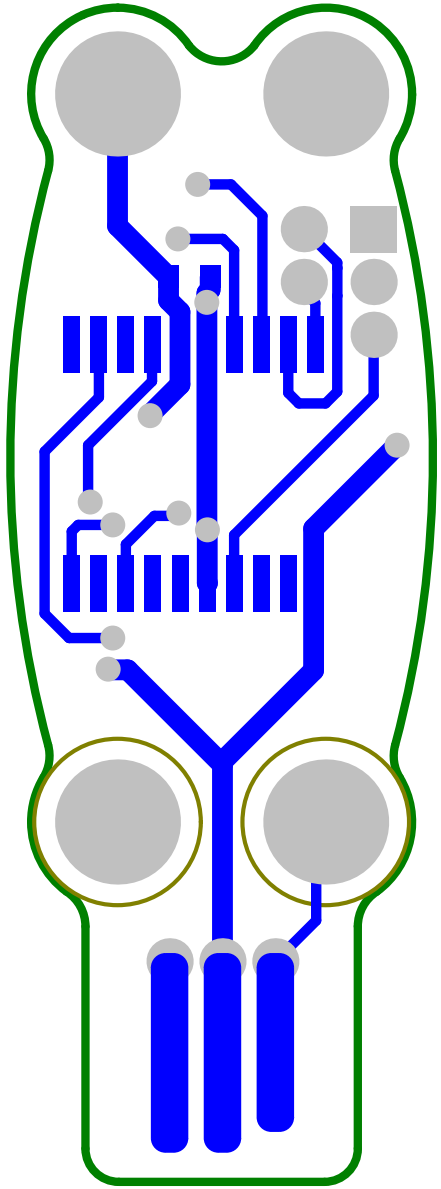
Top Layer

Board Outline



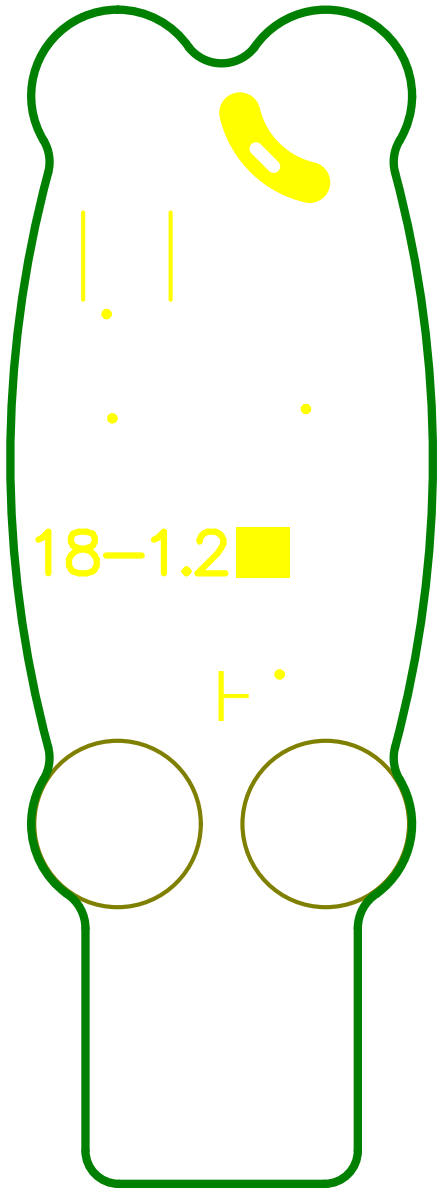
Bottom Layer

Board Outline



Board Outline

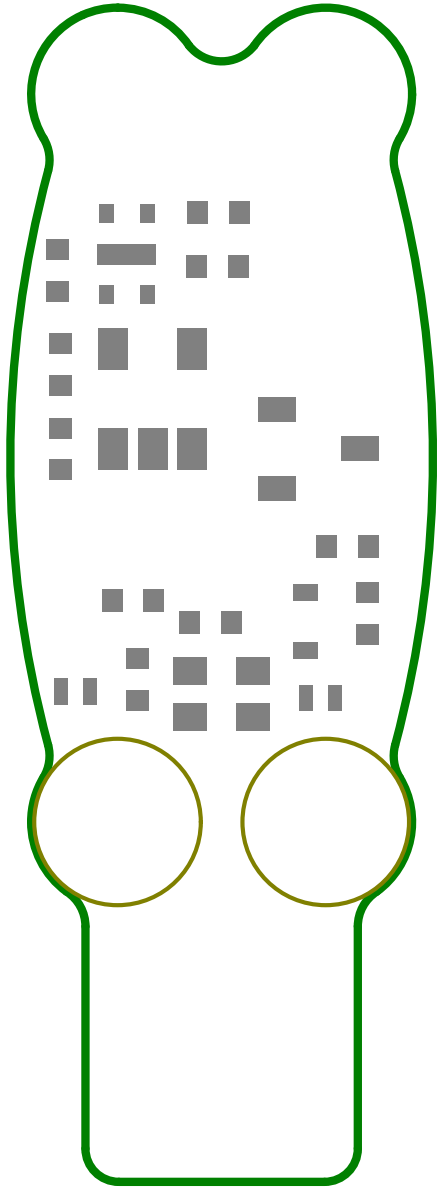
Top Overlay



Board Outline

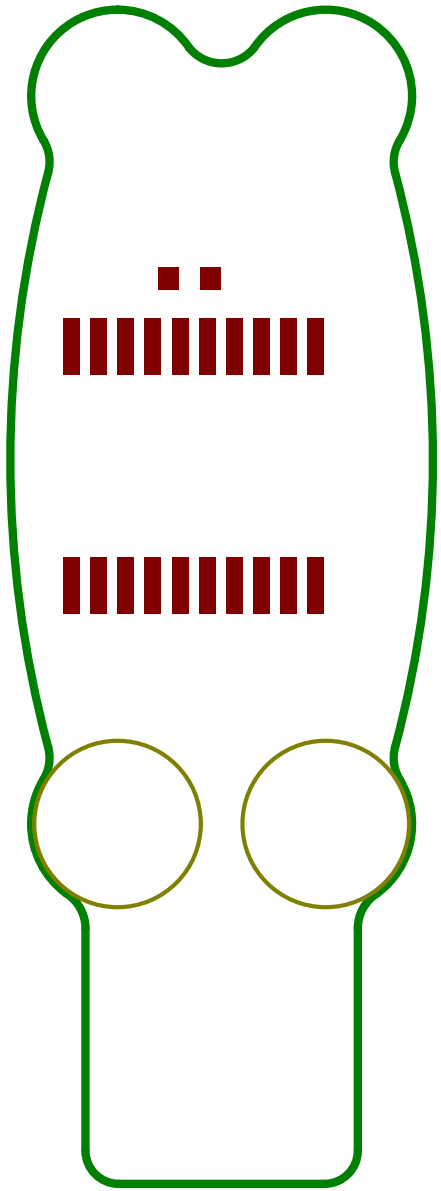
Bottom Overlay

Board Outline



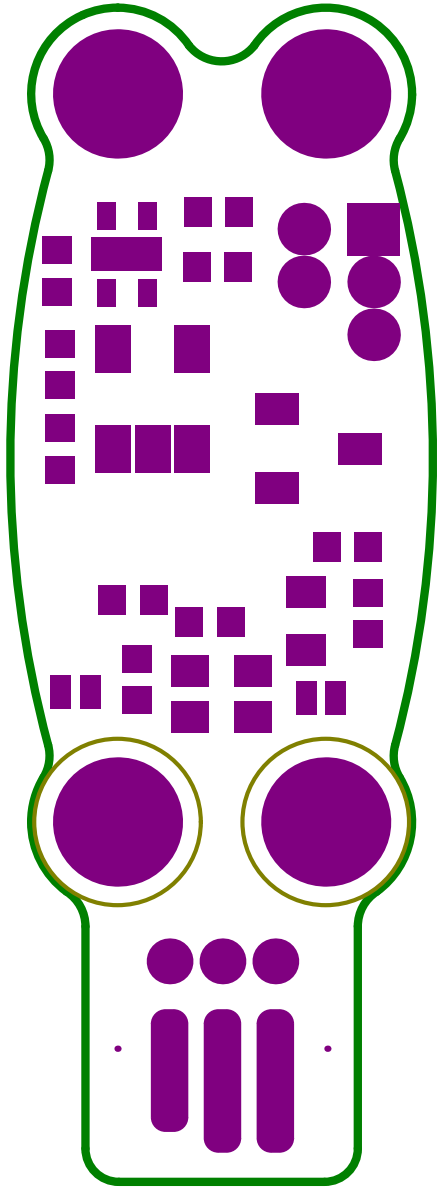
Top Paste

Board Outline



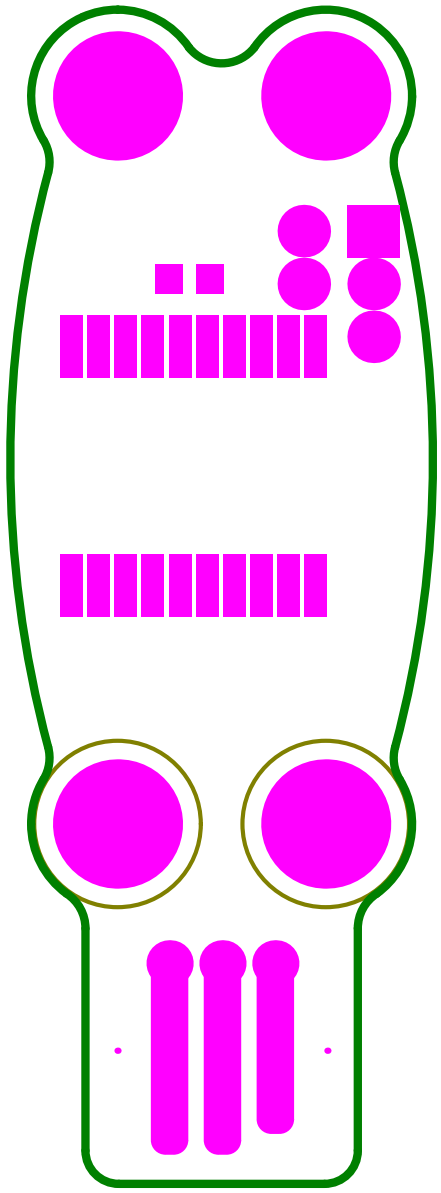
Bottom Paste

Board Outline



Top Solder (resist)

Board Outline



Bottom Solder (resist)

Board Outline