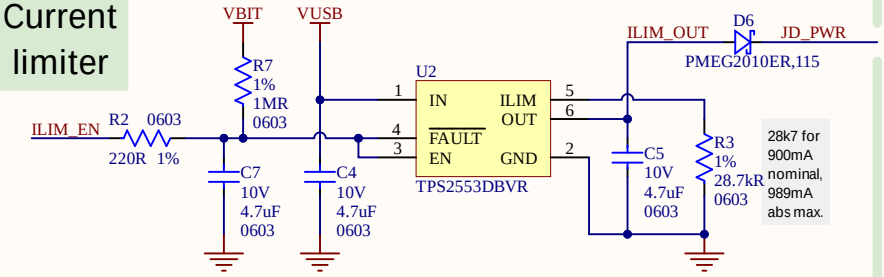
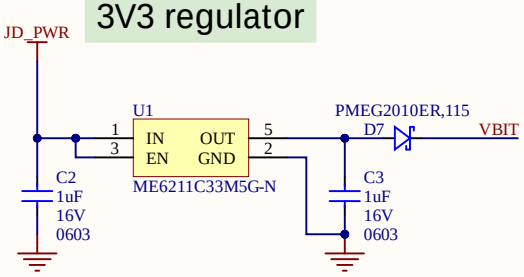
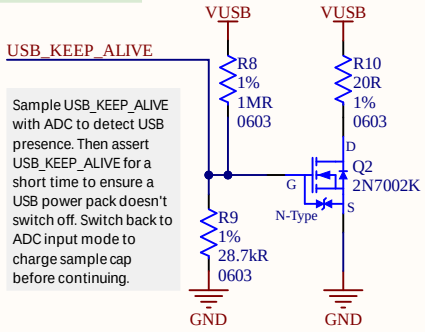
Current limiter



3V3 regulator

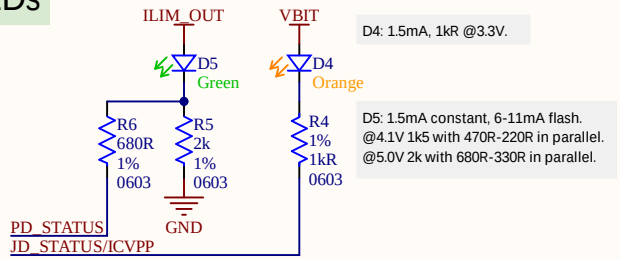


Mounting holes



Sample USB_KEEP_ALIVE with ADC to detect USB presence. Then assert USB_KEEP_ALIVE for a short time to ensure a USB power pack doesn't switch off. Switch back to ADC input mode to charge sample cap before continuing.

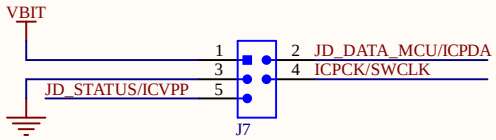
Status LEDs



D4: 1.5mA, 1kR @3.3V.

D5: 1.5mA constant, 6-11mA flash.
@4.1V 1k5 with 470R-220R in parallel.
@5.0V 2k with 680R-330R in parallel.

Programming header

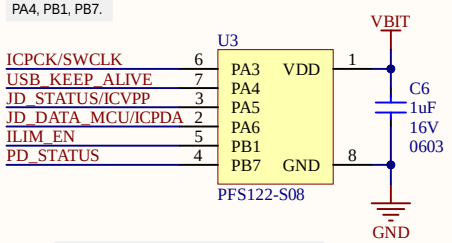


"JacConnect" programming adapter for PADAUK.
https://microsoft.github.io/jacdac-docs/ddk/firmware/jac-connect/

Power service MCU

This component is dynamically powered. It provides power when VUSB is greater than JD_PWR and recieves power otherwise.

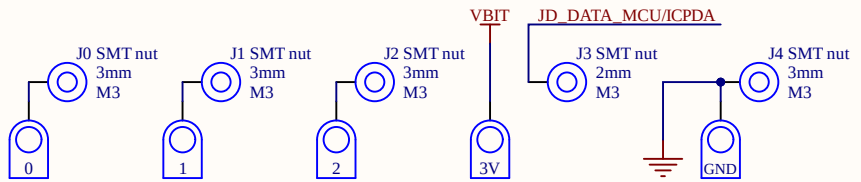
ADC on PA3, PA4, PB1, PB7.



MCU runs power service to prevent power delivery from multiple providers. Must sample VBUS to know if it's providing power or consuming power.

micro:bit V2 interface

Five M3 SMT nuts for mounting the back pack to the micro:bit.
Note that J3 is 1mm shorter to avoid contact with 3V.

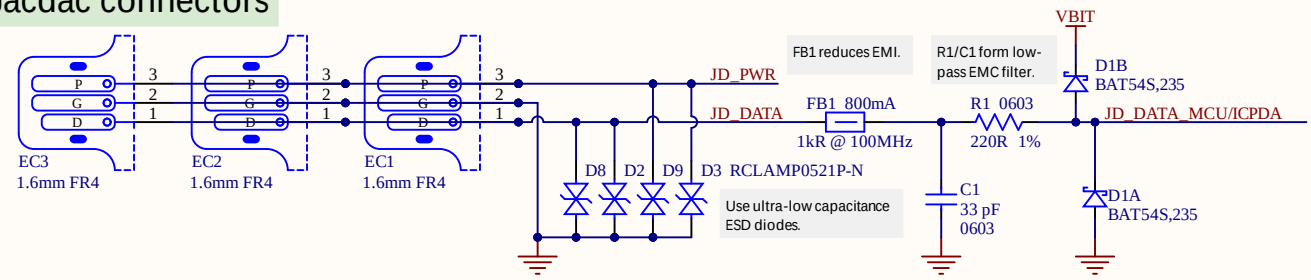


Pick up VUSB from micro:bit test point.

J5 VUSB
Pogo pin
2.9mm

J6 VBIT
Pogo pin
2.9mm

Jacdac connectors



FB1 reduces EMI.

R1/C1 form low-pass EMC filter.

Use ultra-low capacitance ESD diodes.

This reference design is a guideline. Please refer to the Jacdac docs online at https://aka.ms/jacdac for the definitive and most up-to-date information.

Silkscreen should include text to identify the module type and revision, and optionally a QR code.

This design uses an EC30 board shape.

Silkscreen & layout notes

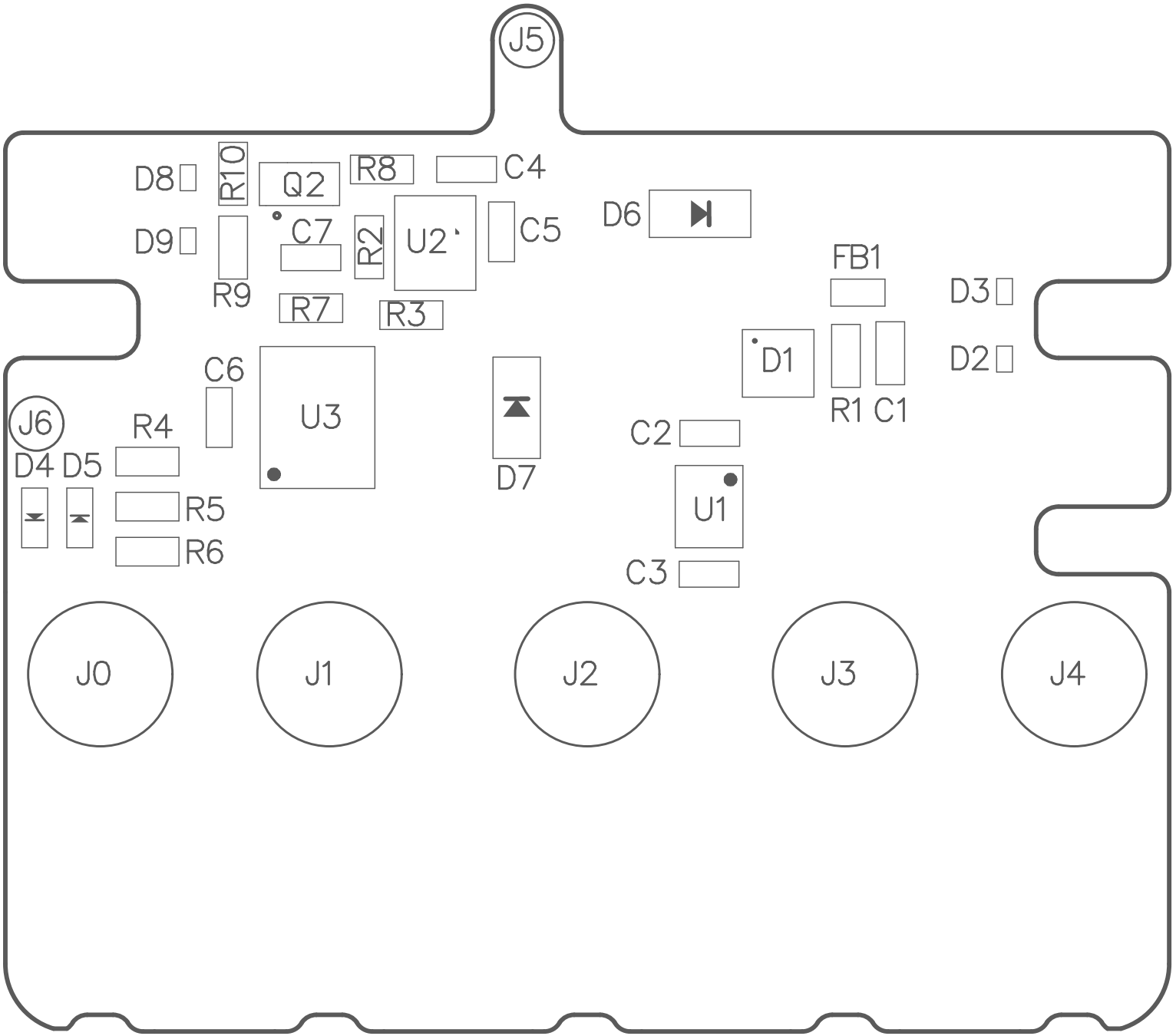
Block name

Design notes

This information is provided "as-is". You bear the risk of using it. Some information relates to pre-released specification which may change without notice. Microsoft makes no warranties, express or implied, with respect to the information provided here.

When this PDF is viewed with Adobe Reader, clicking on components shows part numbers and other details.

PROJECT FILENAME JacdacMicroBitBackPackHi 119.PrjPCB	PROJECT CODENAME JacdacMicroBitBackPackHi	Microsoft	PROJECT DESCRIPTION High power Jacdaptor for micro:bit
SHEET FILENAME JacdacMicroBitBackPackHi-Alt0 119.SchDoc	LICENCE Attribution 4.0 International (CC BY 4.0)	LAST MODIFIED 02/12/2022 / PAGE 1 OF 1 / DRAWN BY SH	SHEET DESCRIPTION Complete design / REVISION 0.1 / PCB ID 119-0.1

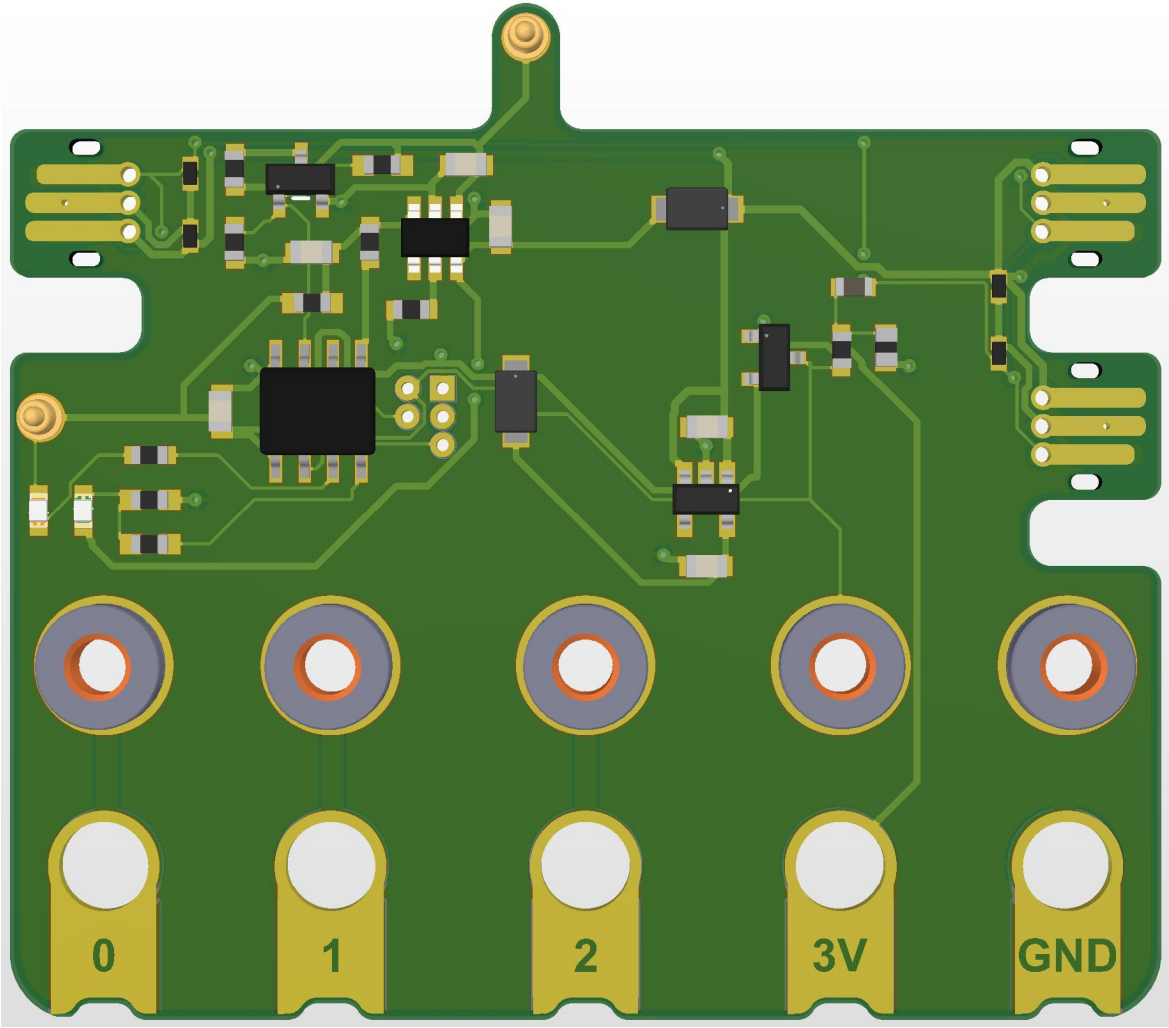


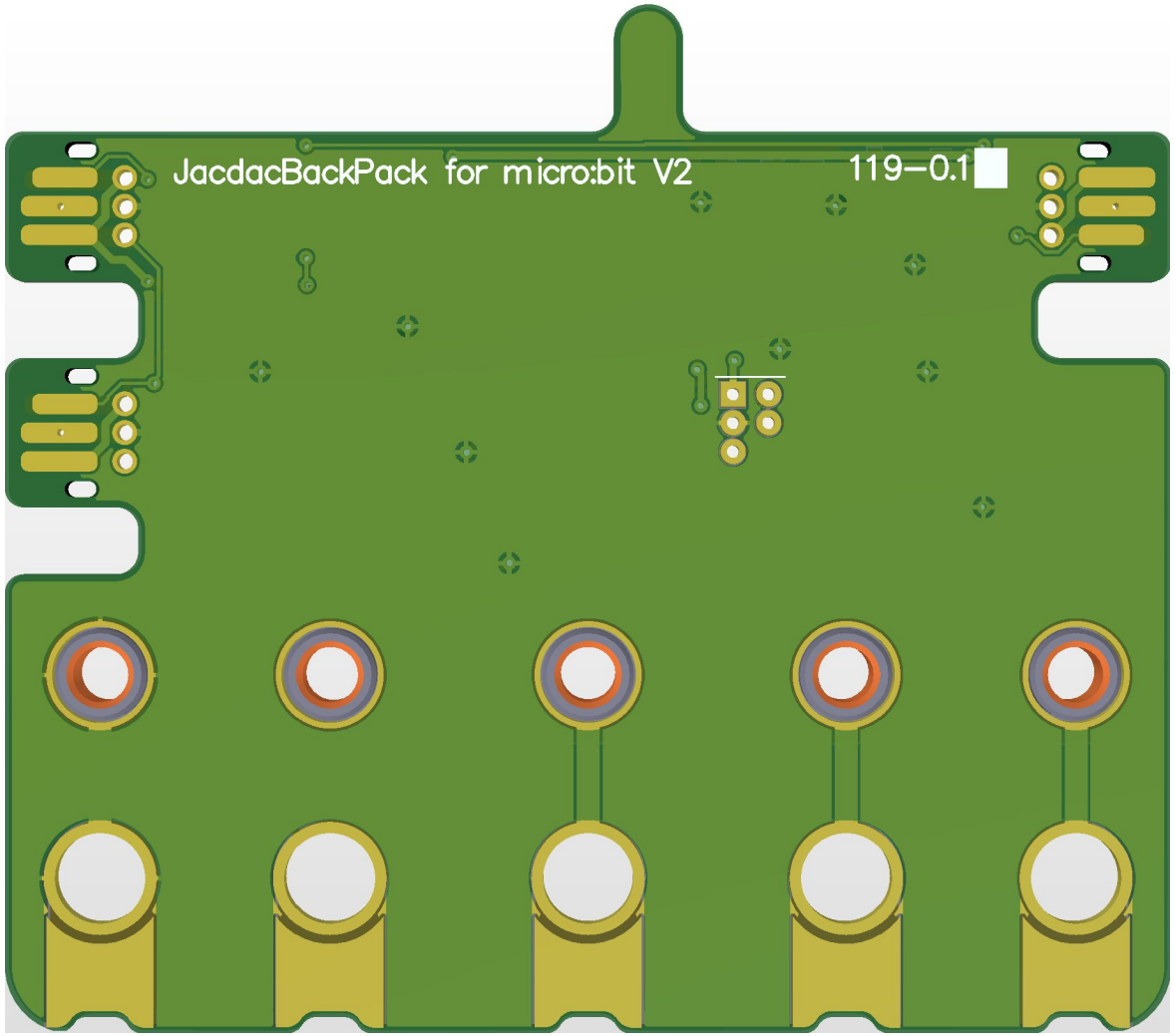
Board Outline

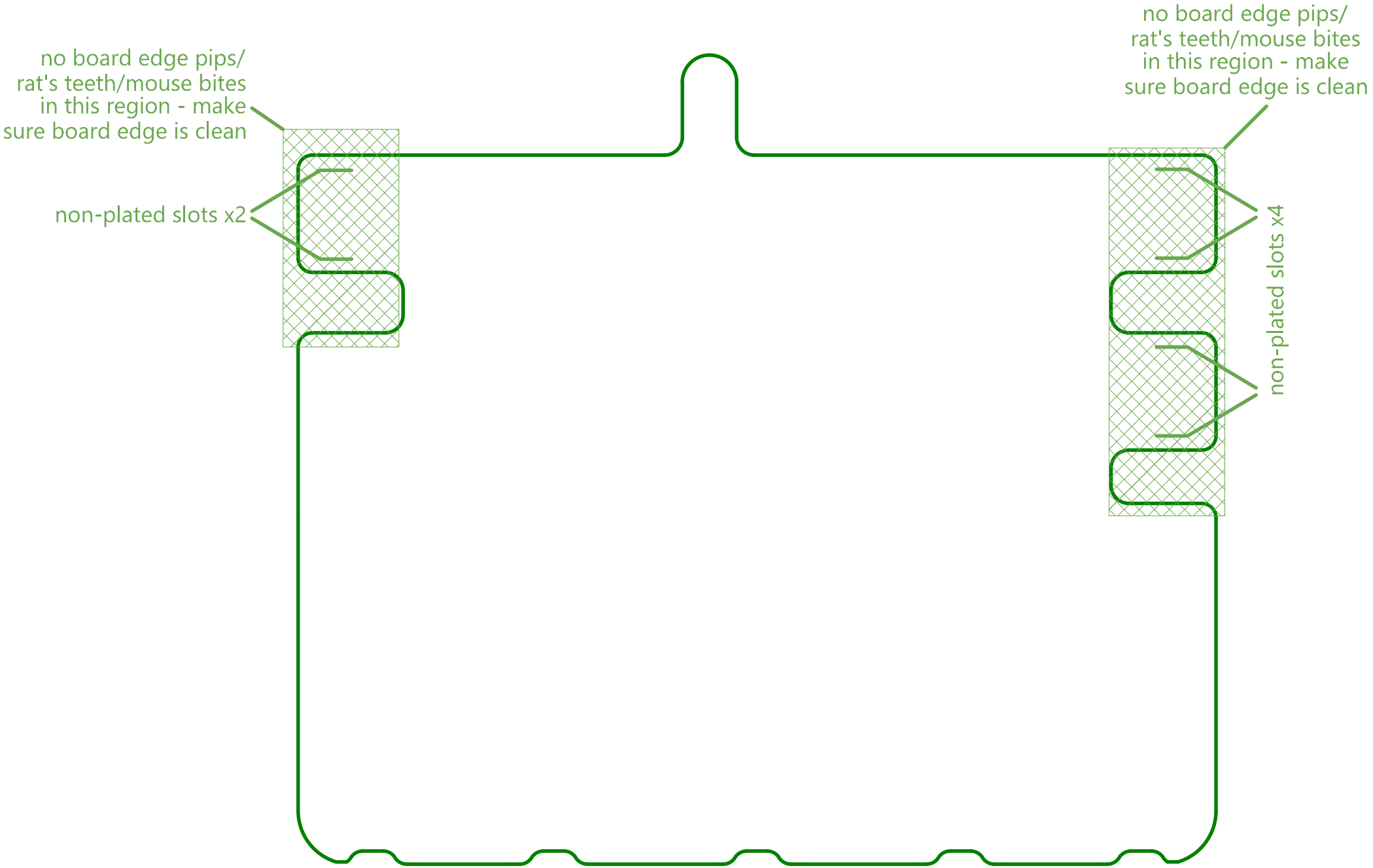
Top Assy

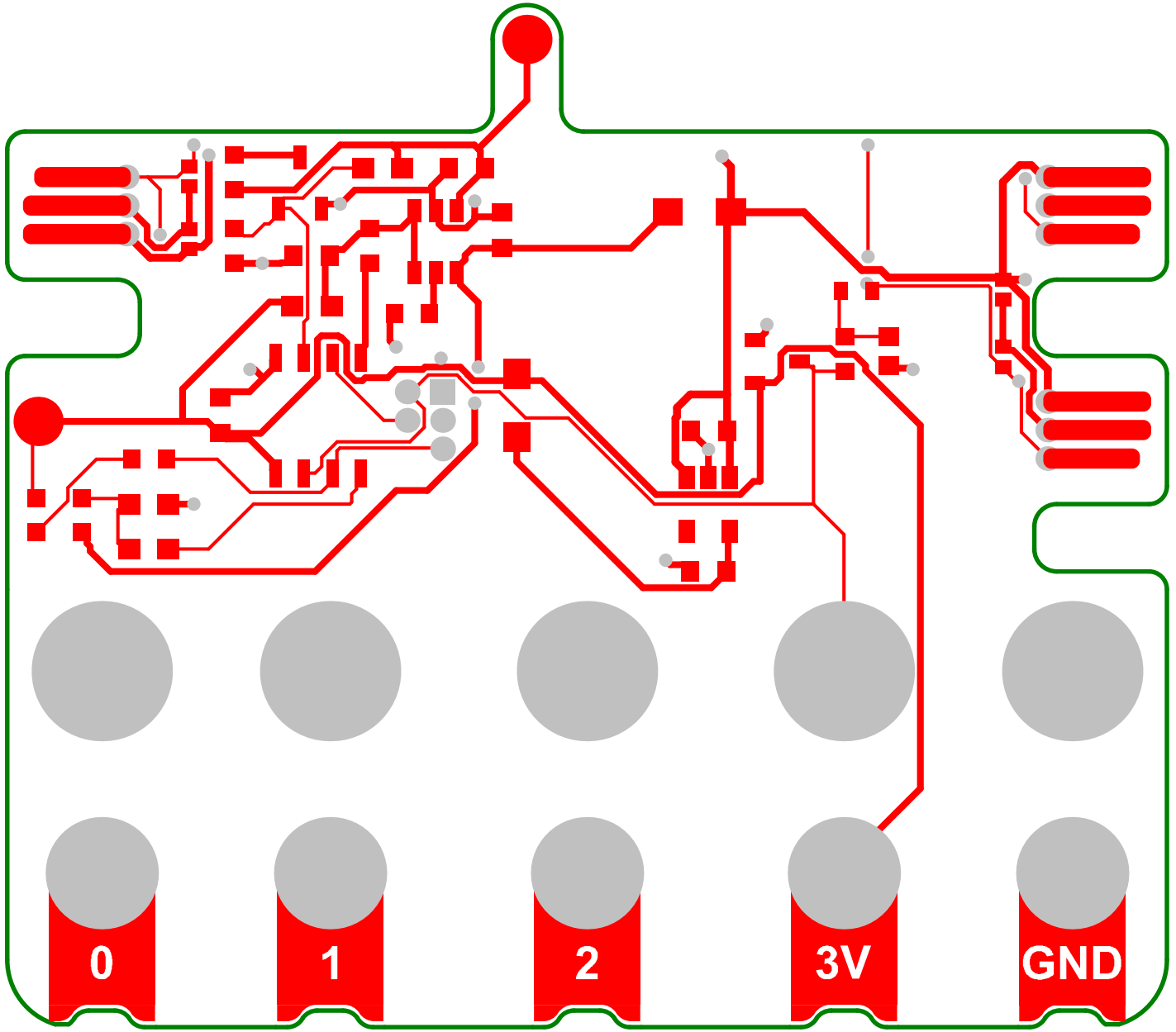
Board Outline

Bottom Assy


0
1
2
3V
GND

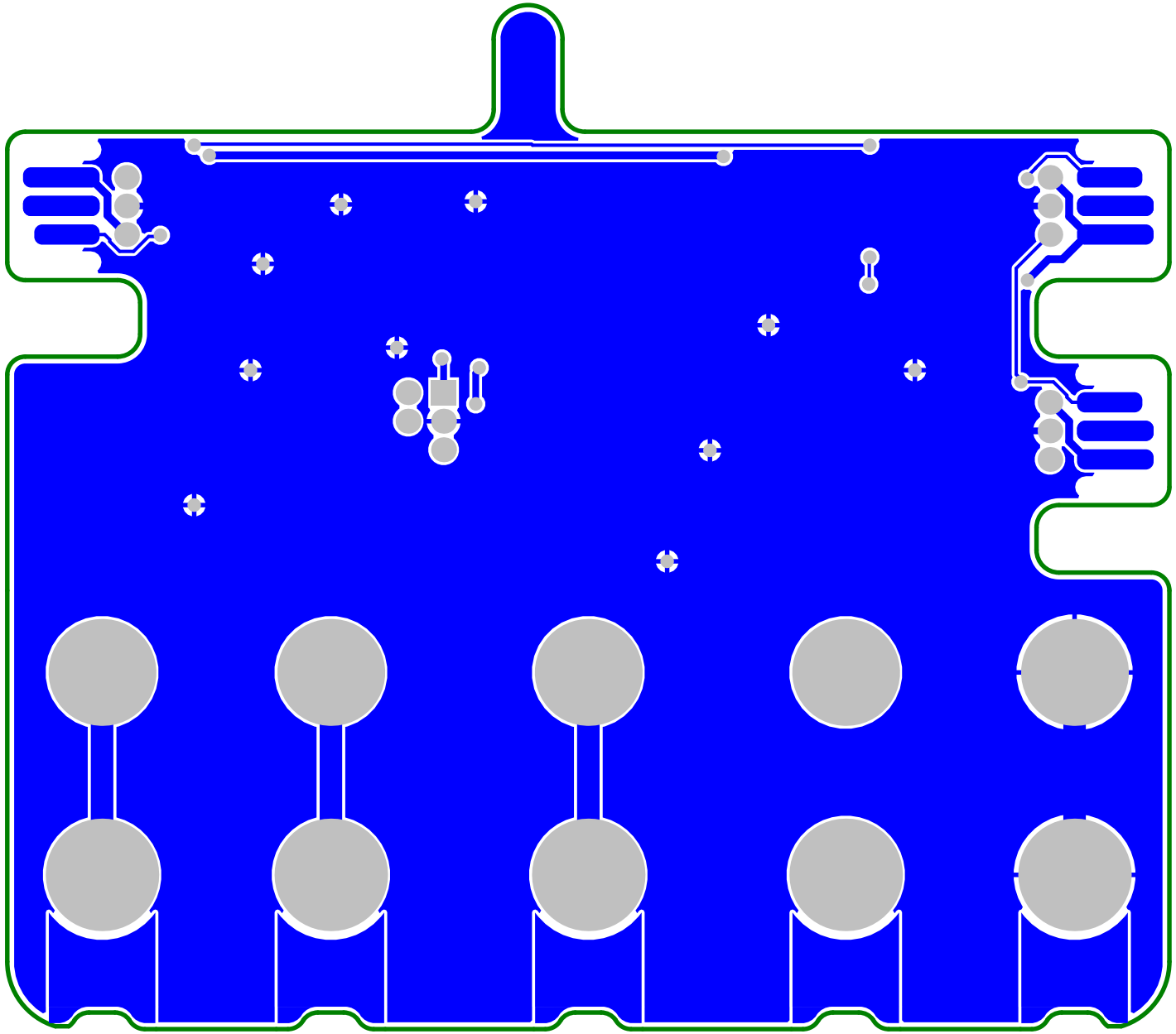

JacdacBackPack for micro:bit V2
119-0.1


no board edge pips/
rat's teeth/mouse bites
in this region - make
sure board edge is clean
non-plated slots x2
no board edge pips/
rat's teeth/mouse bites
in this region - make
sure board edge is clean
non-plated slots x4
Fabrication Notes
Board Outline



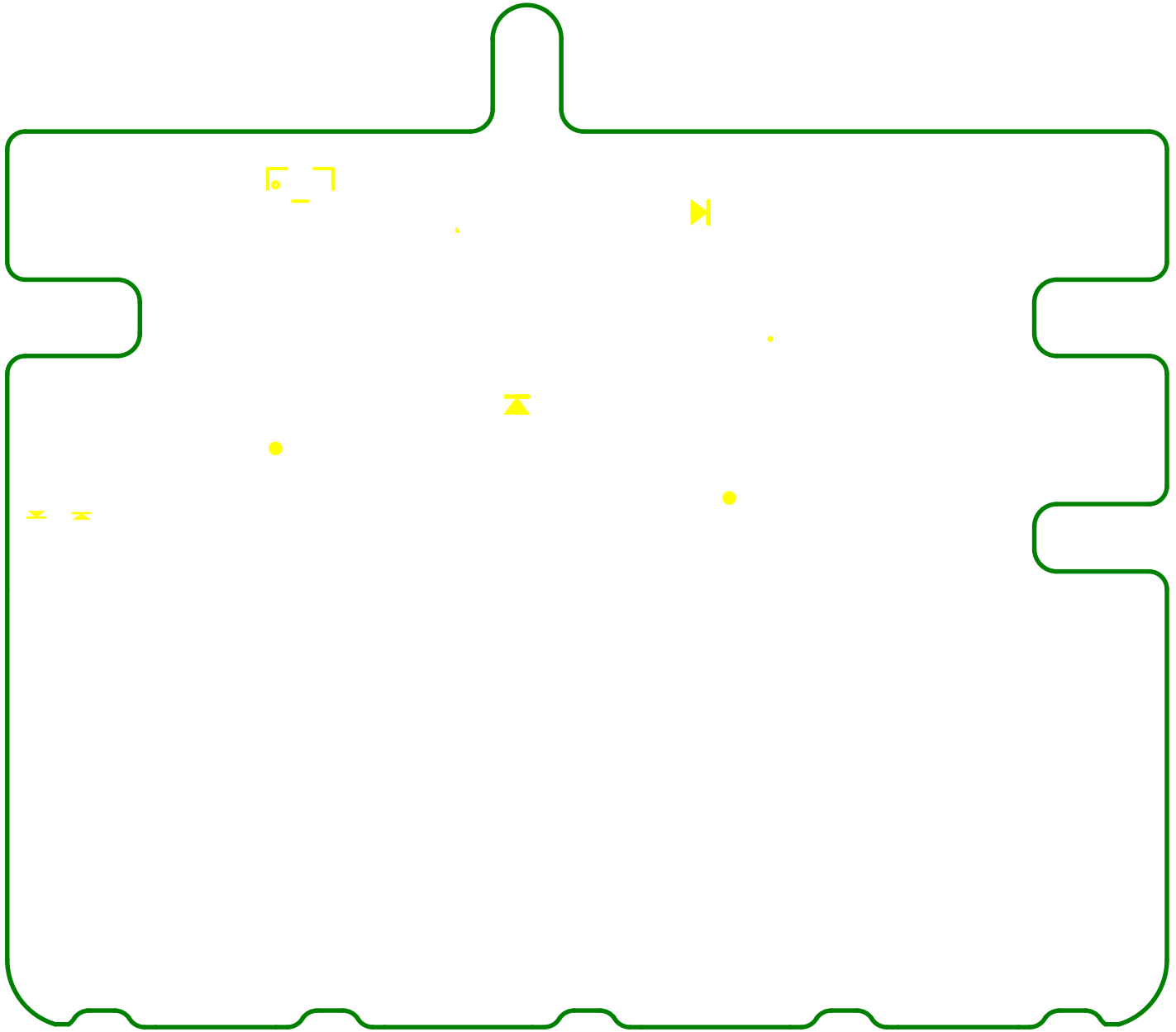
Top Layer

Board Outline



Bottom Layer

Board Outline

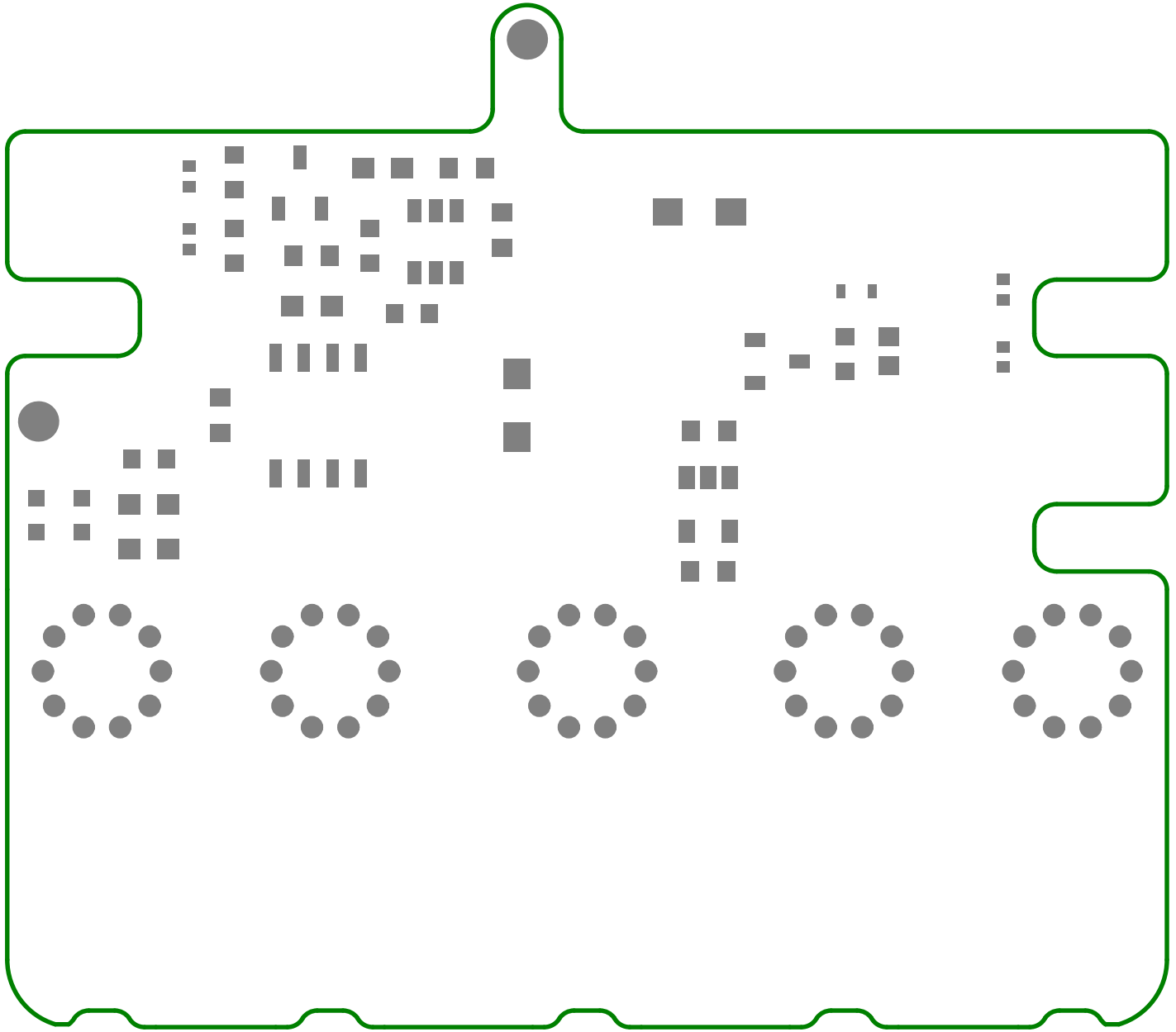


Board Outline

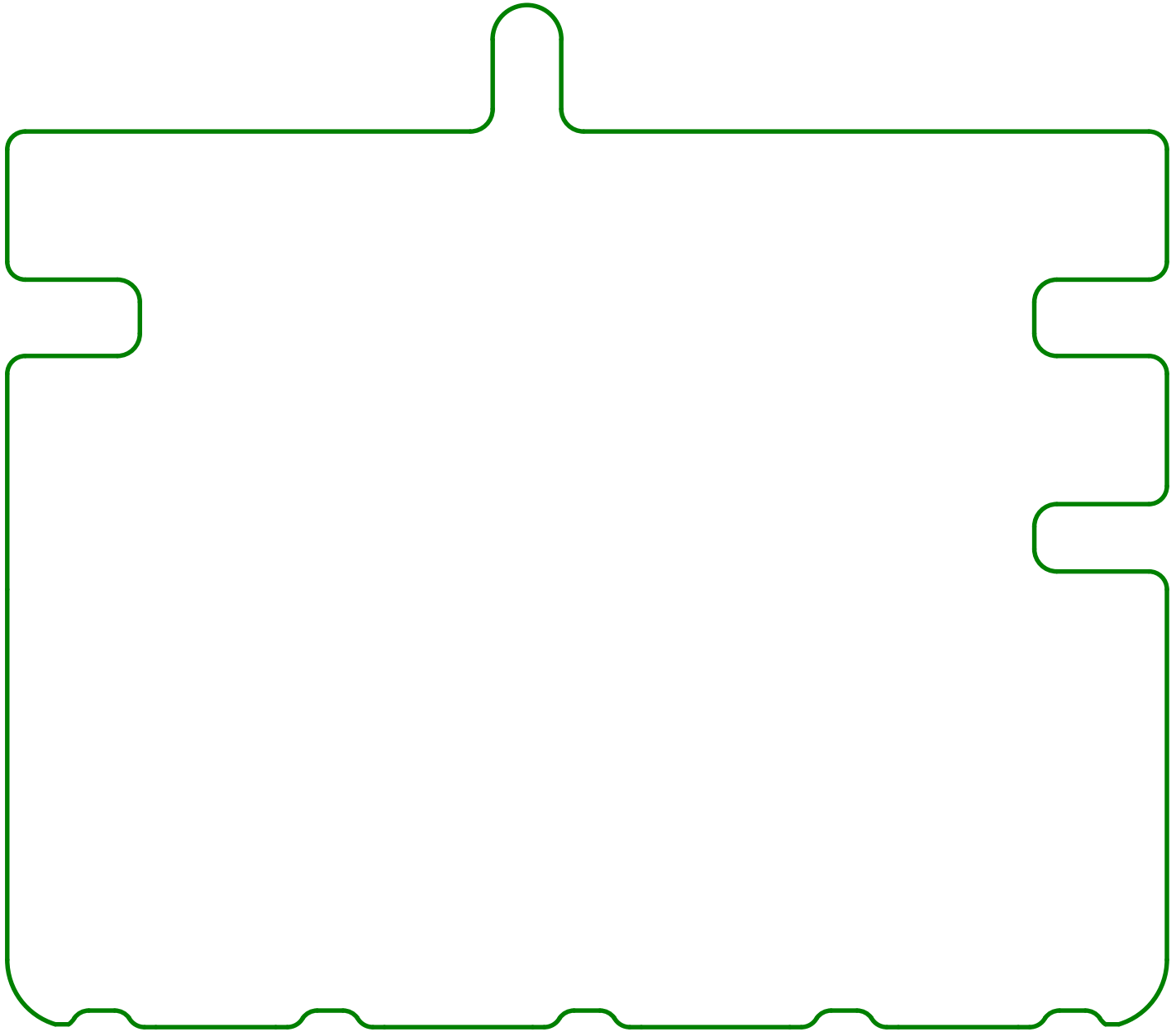
Top Overlay

Bottom Overlay

Board Outline

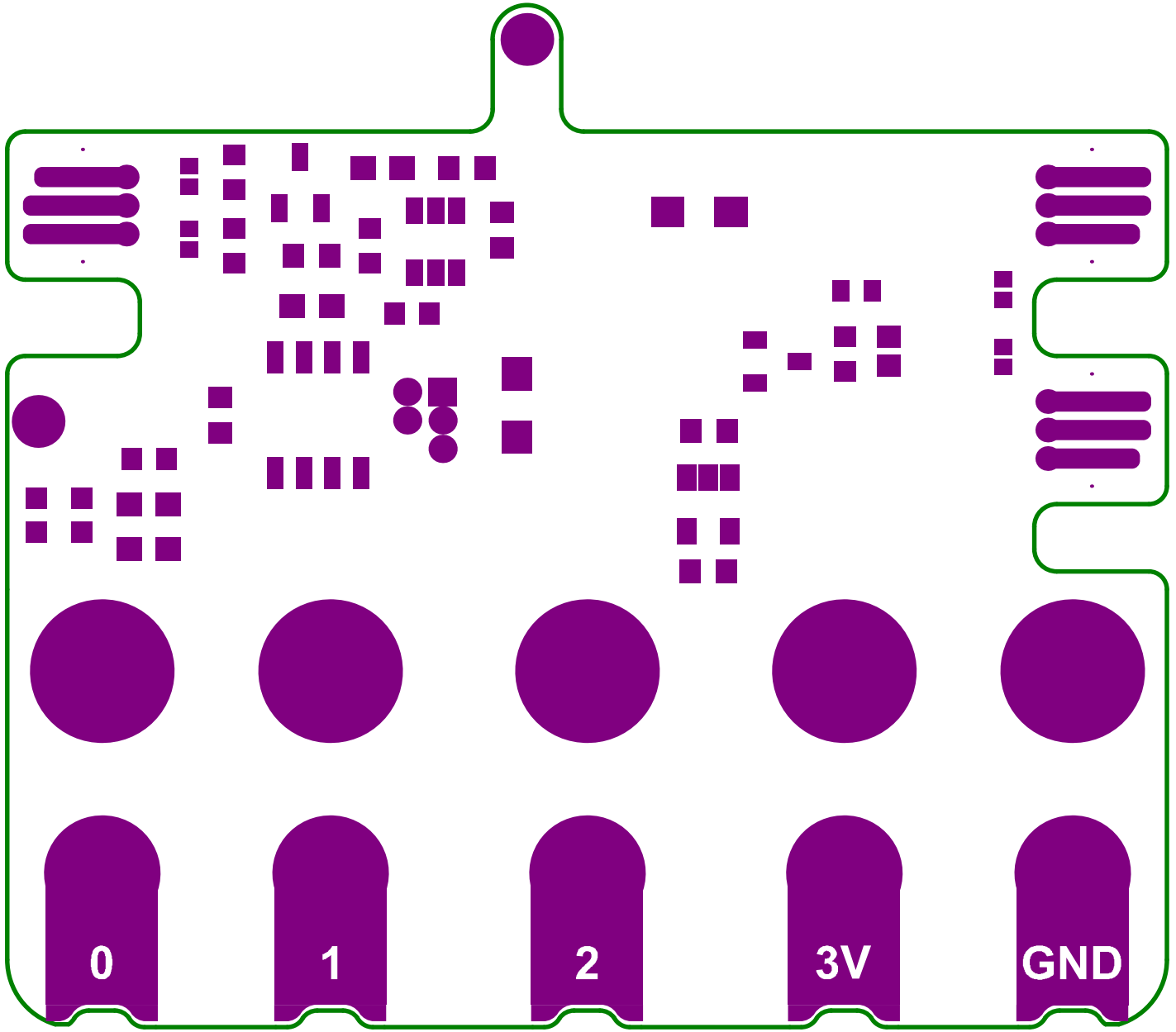


Top Paste Board Outline



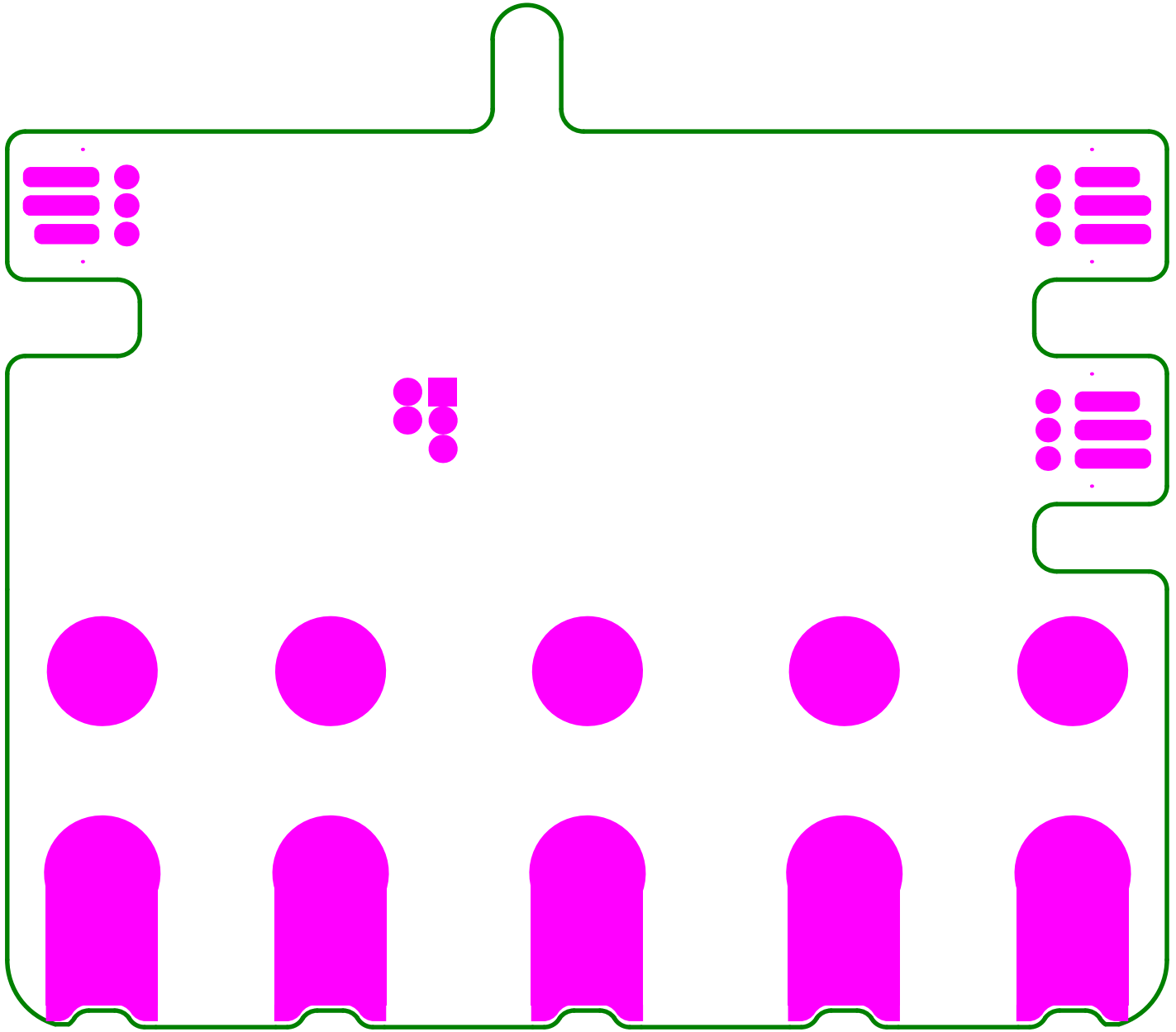
Board Outline

Bottom Paste



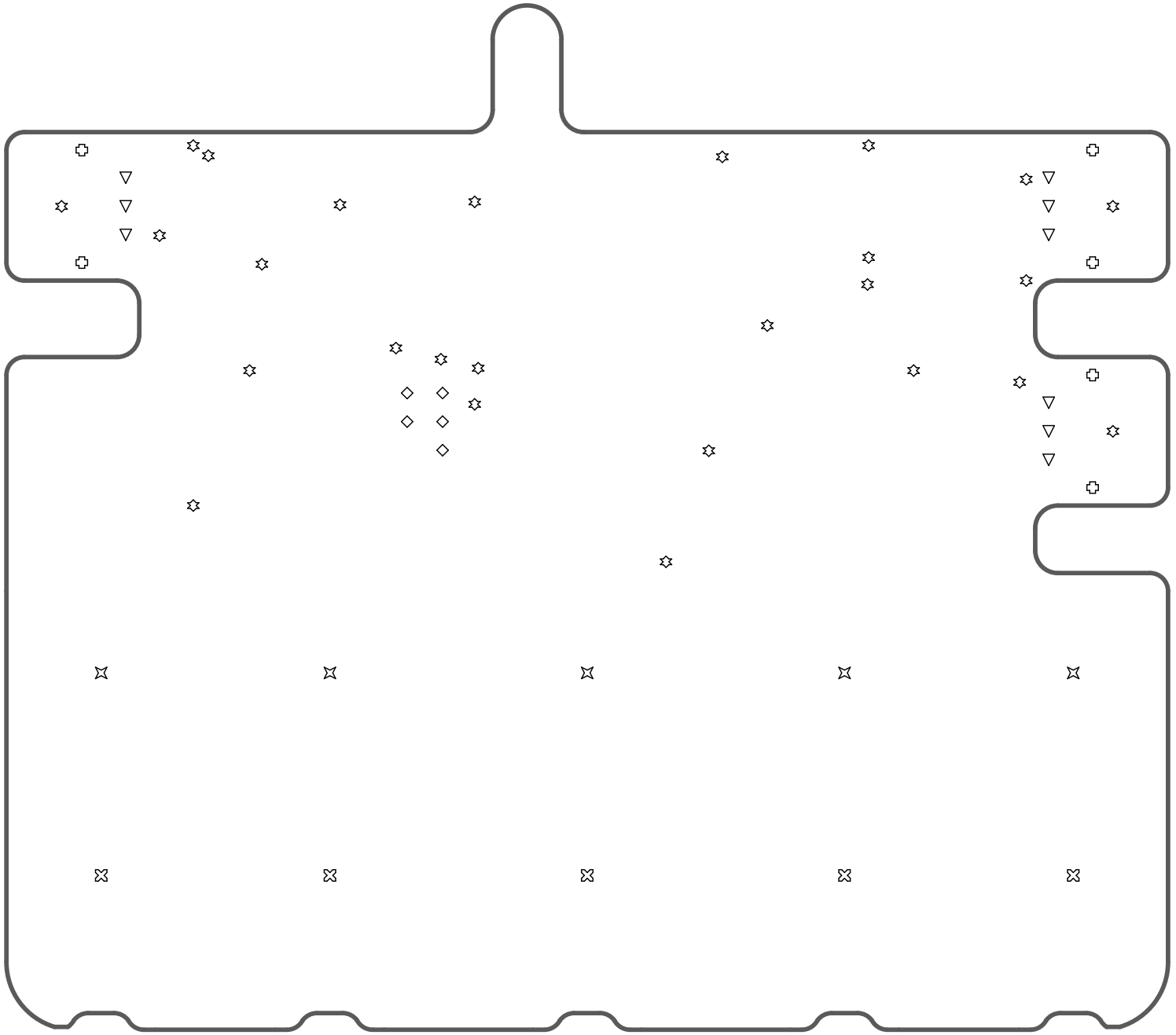
Board Outline

Top Solder (resist)



Board Outline

Bottom Solder (resist)



Board Outline

Drill Drawing