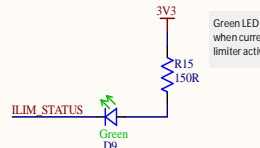
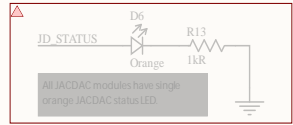
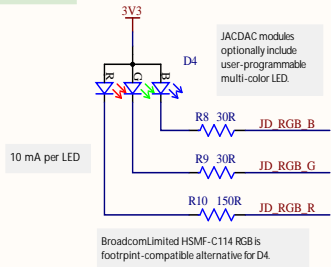
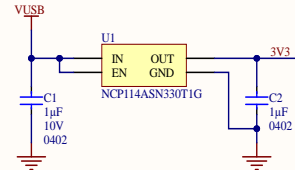


## Status LEDs

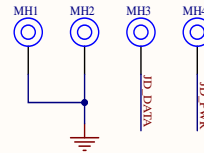


## 3V3 regulator



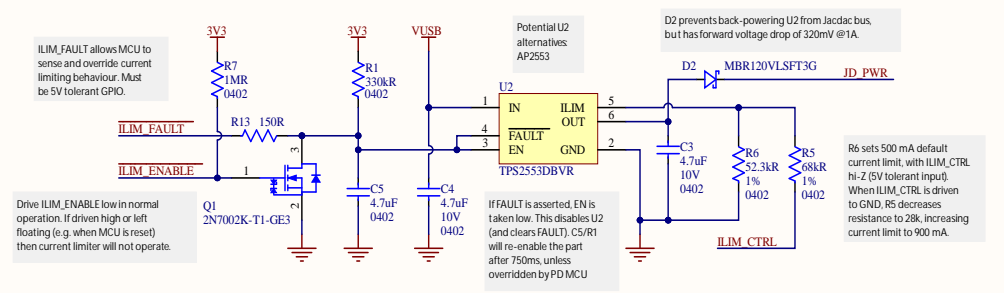
## Mounting holes

MH1, 2 connects to GND.  
MH3 connects to JD\_DATA, and  
MH4 connects to JD\_PWR.

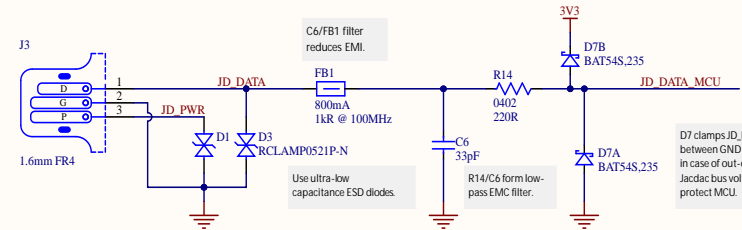


JACDAC mounting holes plated through hole, finished diameter of 2.2mm and annular ring of 3.2mm diameter.

## Current limiter



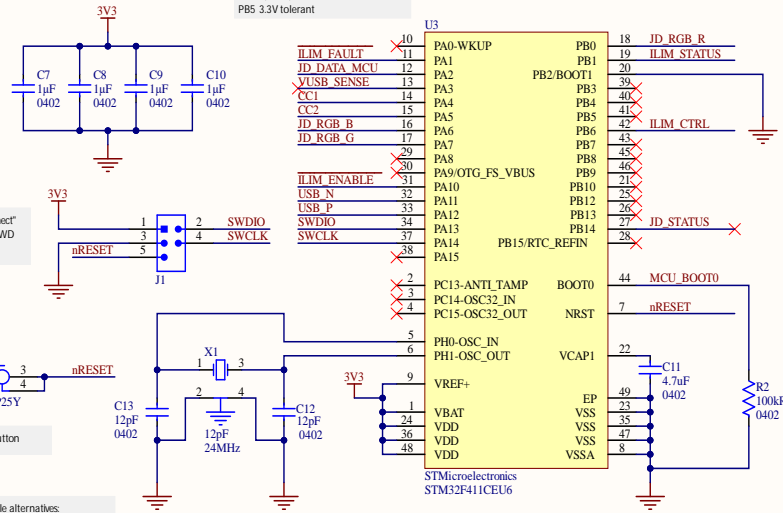
## Jaccdac interface



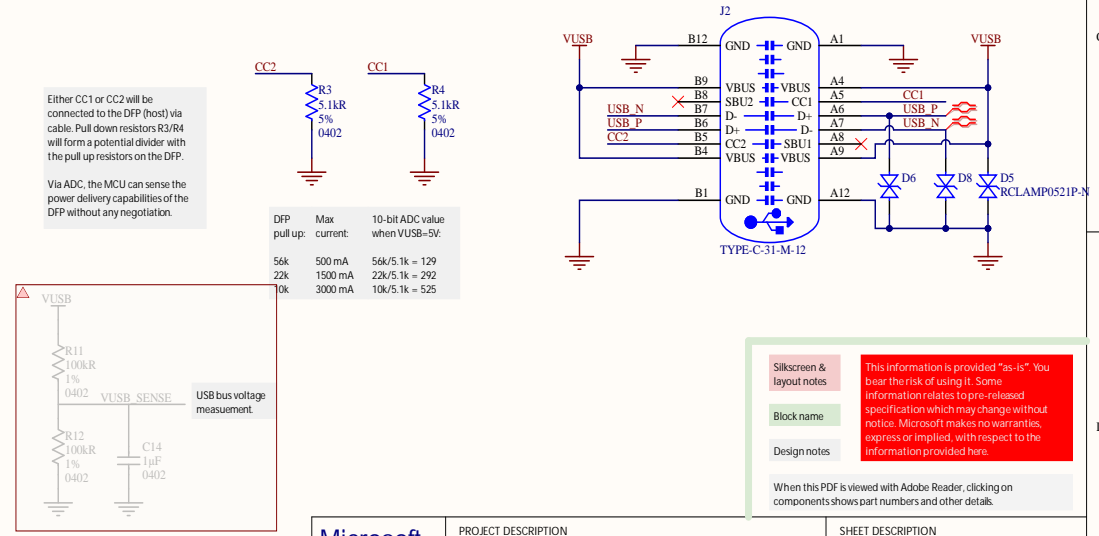
## Brain & power delivery MCU

PA0-7 and PB0-2 are ADC.

PA0 3.3V tolerant  
PA1-15 5V tolerant  
PB0-4 6-10, 12-15 5V tolerant  
PB5 3.3V tolerant



## USB interface



Microsoft

PROJECT DESCRIPTION  
Jaccdac STM32F411CEU6 brain

SHEET DESCRIPTION  
complete design

SHEET FILENAME JaccdacBrainF4 41.SchDoc

PROJECT FILENAME JaccdacBrainF4 41.PrjPCB

PROJECT CODENAME JaccdacBrainF4

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DRAWN BY JD, SH & DG

REVISION 0.2 PCB ID 41-0.2