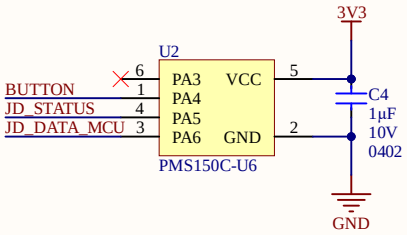
MCU

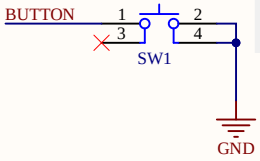


U2 must be programmed before being soldered down due to restrictive in-circuit programming requirements.

JD_STATUS is PWM-capable GPIO.

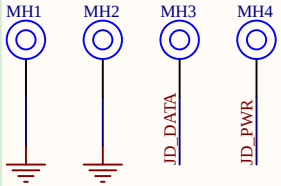
Button

MCU must have internal pull-up on BUTTON GPIO.



SW1 pin 4 is grounded to aid routing.

Mounting holes



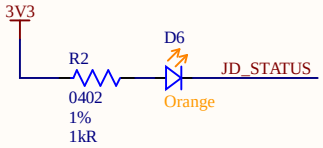
JACDAC mounting holes are plated through hole, finished diameter of 2.1mm, annular ring of 3.0mm diameter and copper/component keepout of 5.0mm. The mounting holes should be on 2.5mm pitch.

MH1 & MH2 : GND
MH3 : JD_DATA
MH4 : JD_PWR

Mounting holes should have appropriate silkscreen marker, and MH1 should have a pin 1 marker on the top side.

Jacdac modules require mounting holes. Modules mounting holes are electrically connected so that modules can be mounted on top of other PCBs without using cables.

Status LED



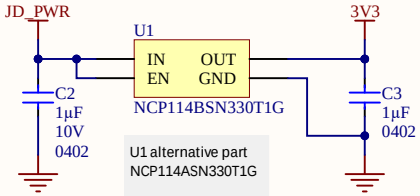
D6
Alternative part
SML-D12D
E6C0603SEAC1UDA
NCD0603O1

Jacdac modules require a status LED.

The LED can be monochrome or multicolor depending on GPIO availability

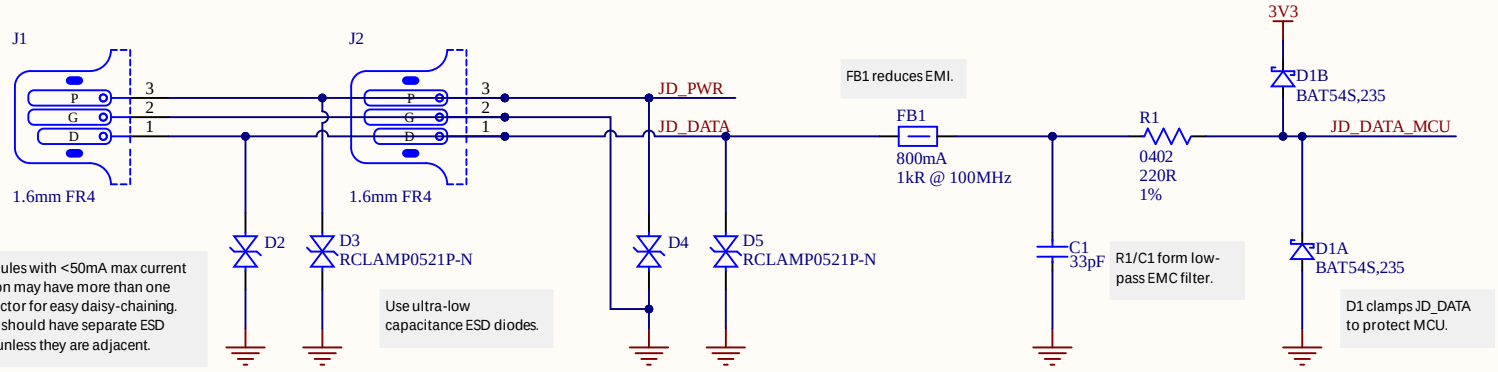
If using alternative part recalculate the resistor values R2

3V3 Regulator



U1 alternative part
NCP114ASN330T1G

Jacdac connector



FB1 reduces EMI.

Jacdac modules with <50mA max current consumption may have more than one edge connector for easy daisy-chaining. Connectors should have separate ESD protection unless they are adjacent.

ESD diode pair required for each Jacdac connector.

Use ultra-low capacitance ESD diodes.

R1/C1 form low-pass EMC filter.

D1 clamps JD_DATA to protect MCU.

Silkscreen & layout notes

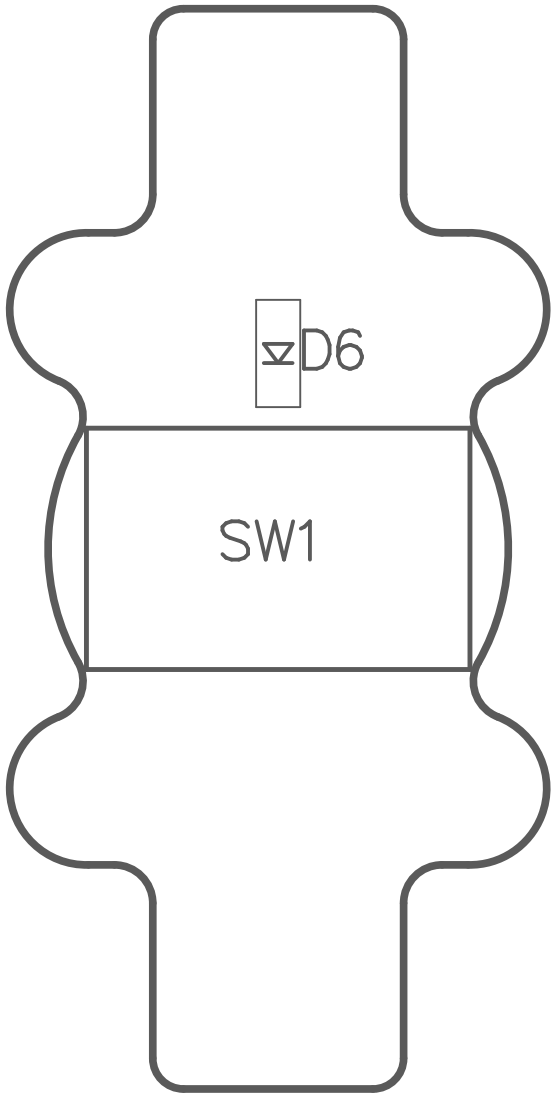
Block name

Design notes

When this PDF is viewed with Adobe Reader, clicking on components shows part numbers and other details.

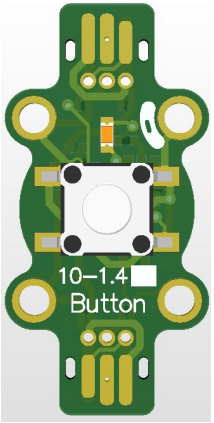
PROJECT FILENAME JacdacButton 10.PrjPCB	PROJECT CODENAME JacdacButton	Microsoft	PROJECT DESCRIPTION Jacdac button based on low-cost OTP PADAUK MCU / SHEET DESCRIPTION Complete design
SHEET FILENAME JacdacButton 10.SchDoc	LICENCE Attribution 4.0 International (CC BY 4.0)	LAST MODIFIED 10/11/2021 / PAGE 1 OF 1 / DRAWN BY DG, JD & SH	REVISION 1.4 / PCB ID 10-1.4

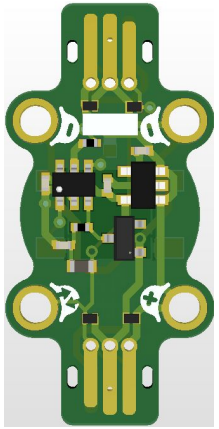
Board Outline
Top Assy



Board Outline

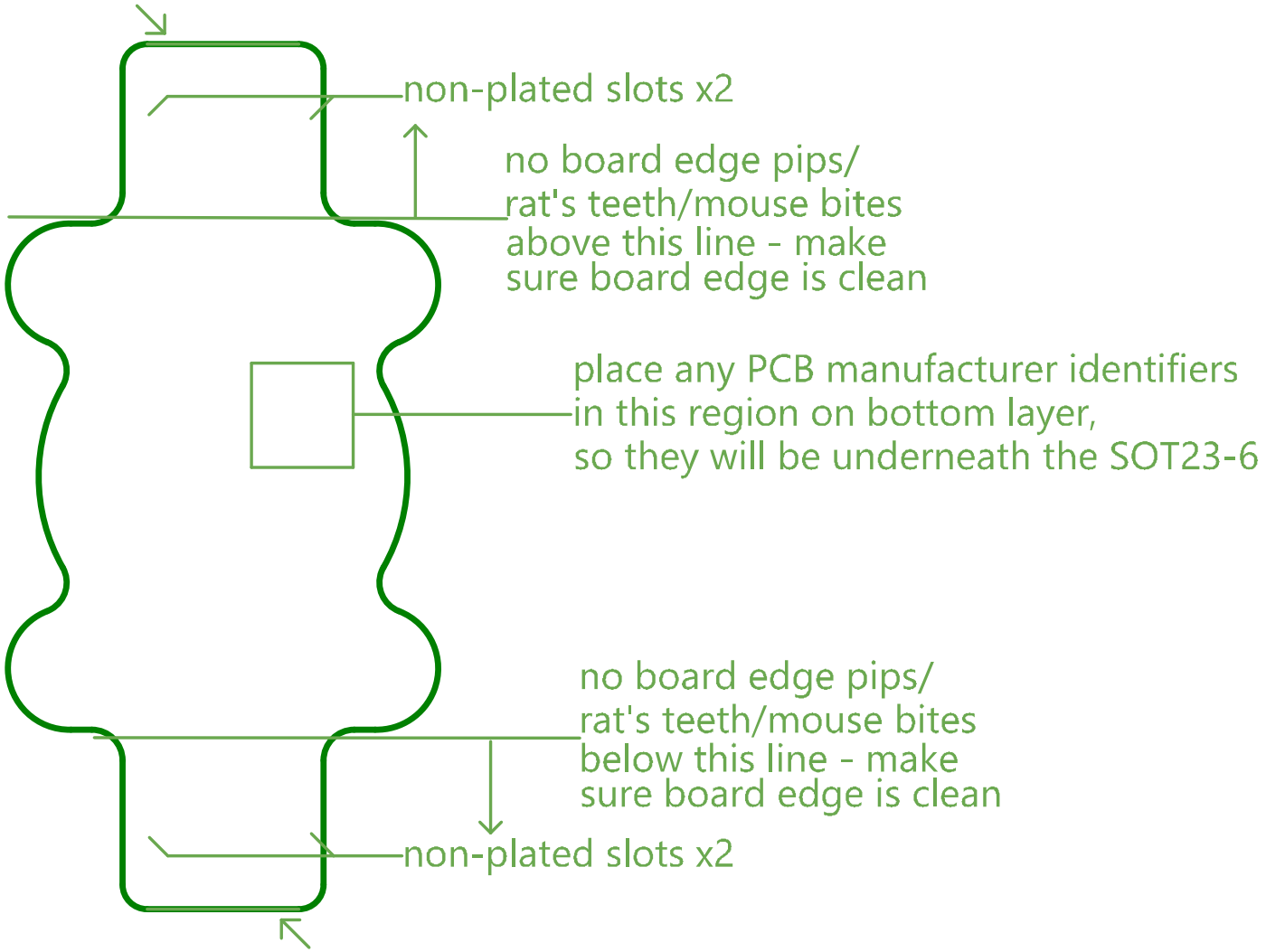
Bottom Assy


10-1.4
Button



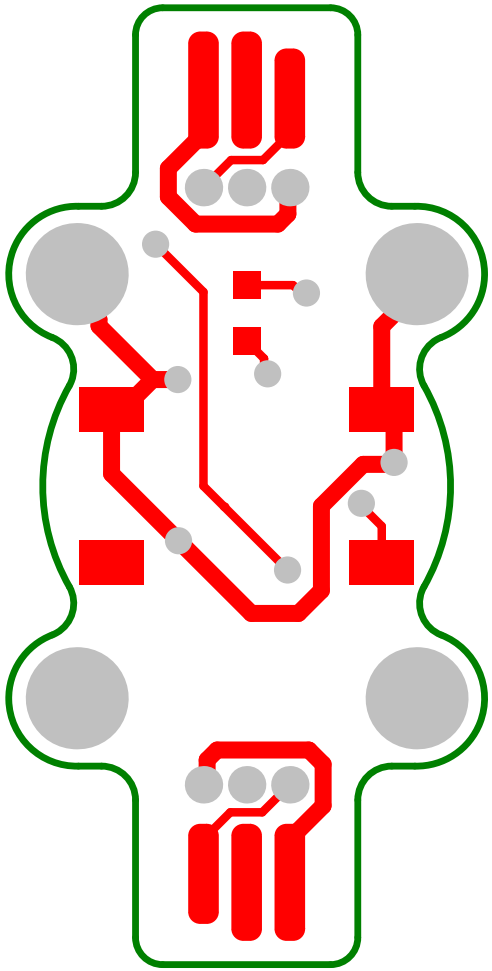
Fabrication Notes

Board Outline



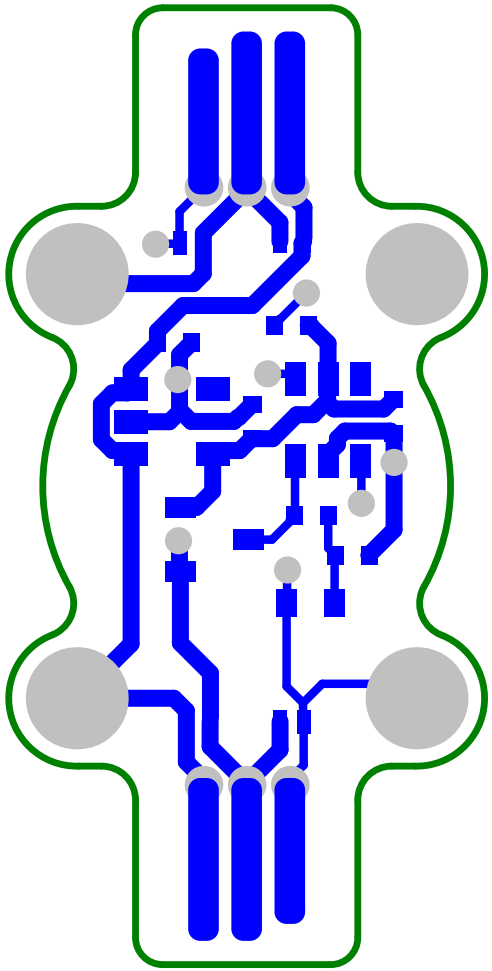
Top Layer

Board Outline



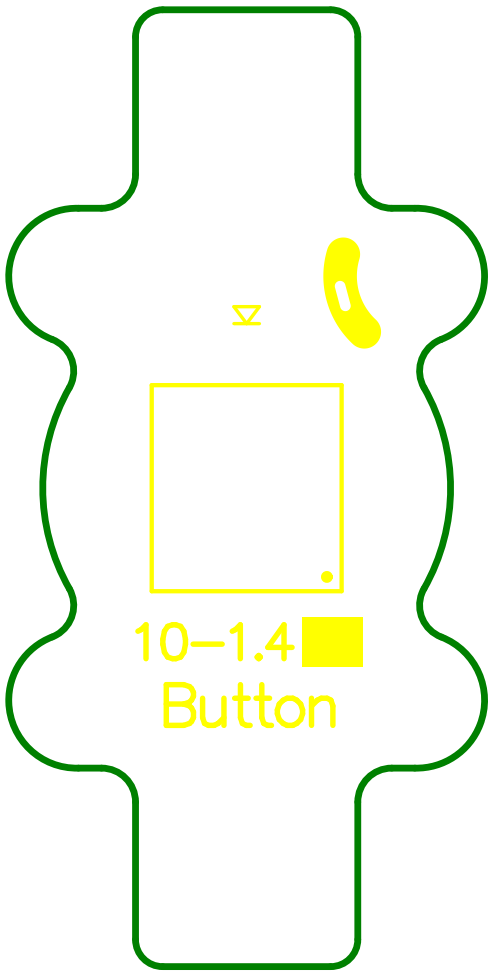
Bottom Layer

Board Outline



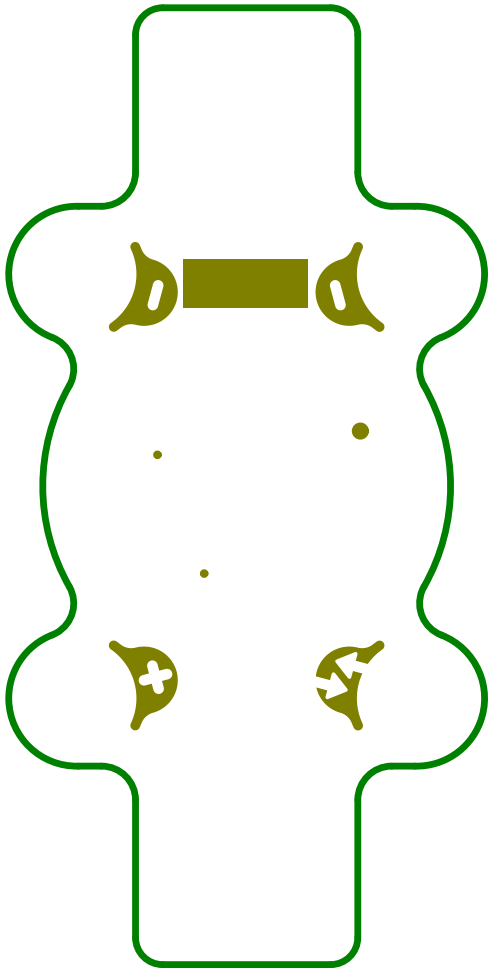
Board Outline

Top Overlay



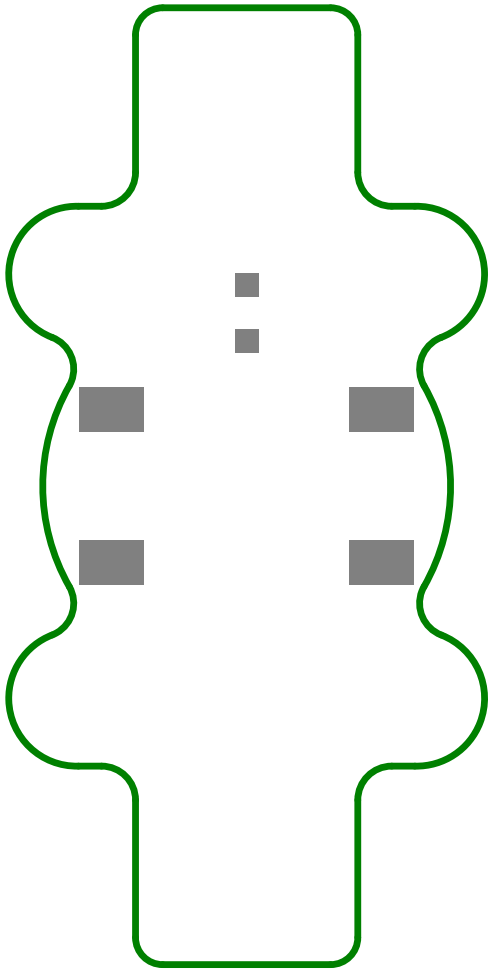
Board Outline

Bottom Overlay



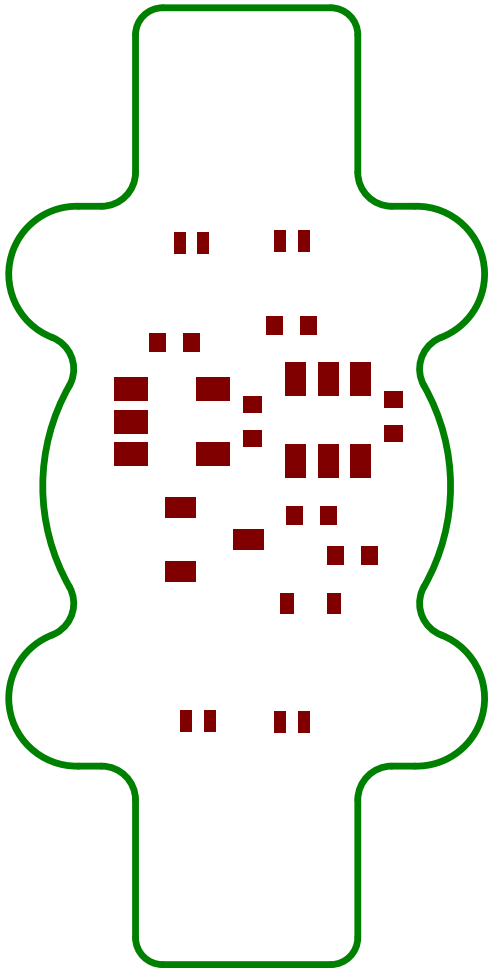
Board Outline

Top Paste



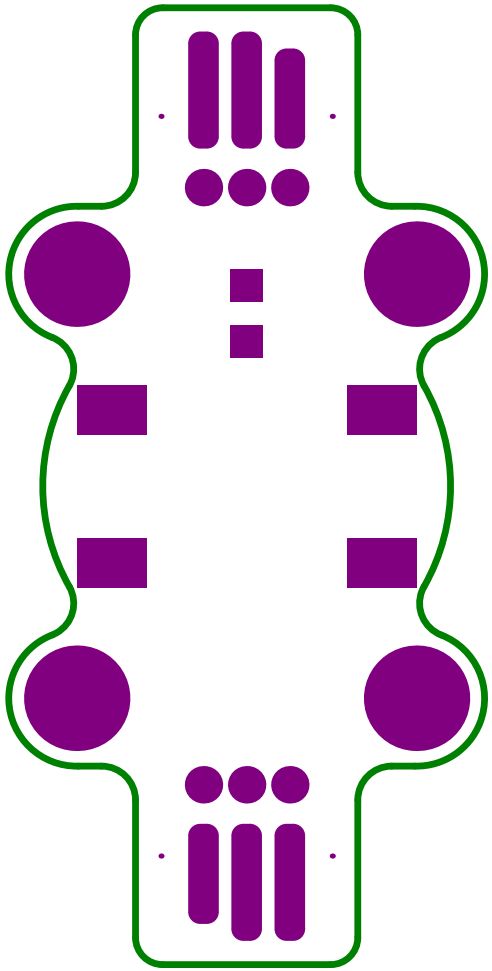
Board Outline

Bottom Paste



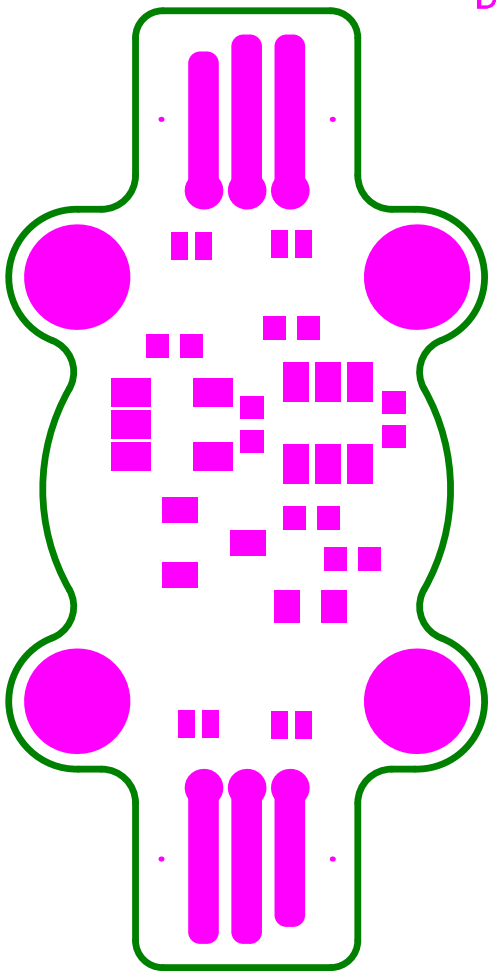
Board Outline

Top Solder (resist)



Board Outline

Bottom Solder (resist)



Board Outline