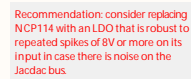
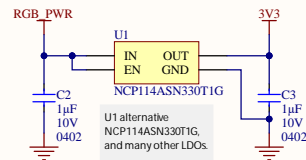


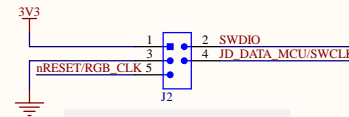
3V3 regulator



This component is either a power-consumer, or can be independently powered through the USB connector.

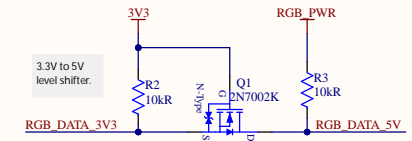


Programming/debug connector

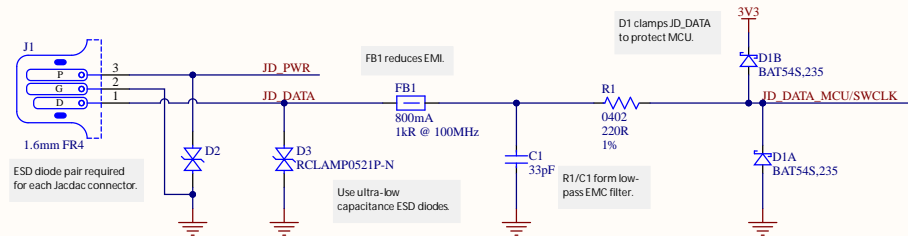


"Hack-connect XS" SWD adapter.
<https://arcade.makecode.com/hardware/dbg>

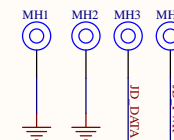
Independent power and RGB LED interfaces



Jacdac connector



Mounting holes



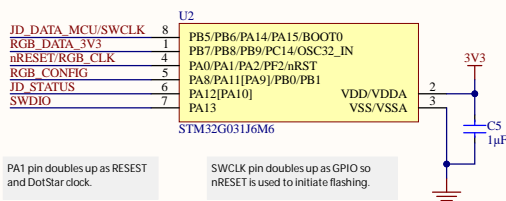
Mounting holes are electrically connected to the Jacdac bus nets so they can be used as an alternative to the PCB edge connector. Please use the following reference designators and net mapping:

MH1 & MH2: G
MH3: JD_DATA
MH4: JD_PWR

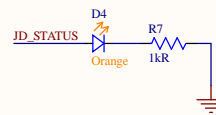
MCU

U2 critical pin mappings:
PB6 USART1_TX for JD data PB7 RGB strip data
PA12 JD monochromatic LED PA8 RGB strip config

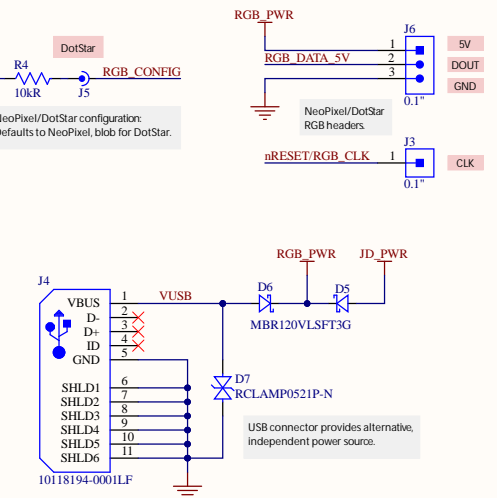
JD_DATA doesn't need WAKEUP pin because deepest sleep isn't used.



Status LED



The LED can be monochrome or multi-colour depending on GPIO availability.



This reference design is a guideline. Please refer to the Jacdac docs online at <https://aka.ms/jacdac> for the definitive and most up-to-date information.

Silkscreen should include text to identify the module type and revision, and optionally a QR code.

This design uses a 'cute' board shape

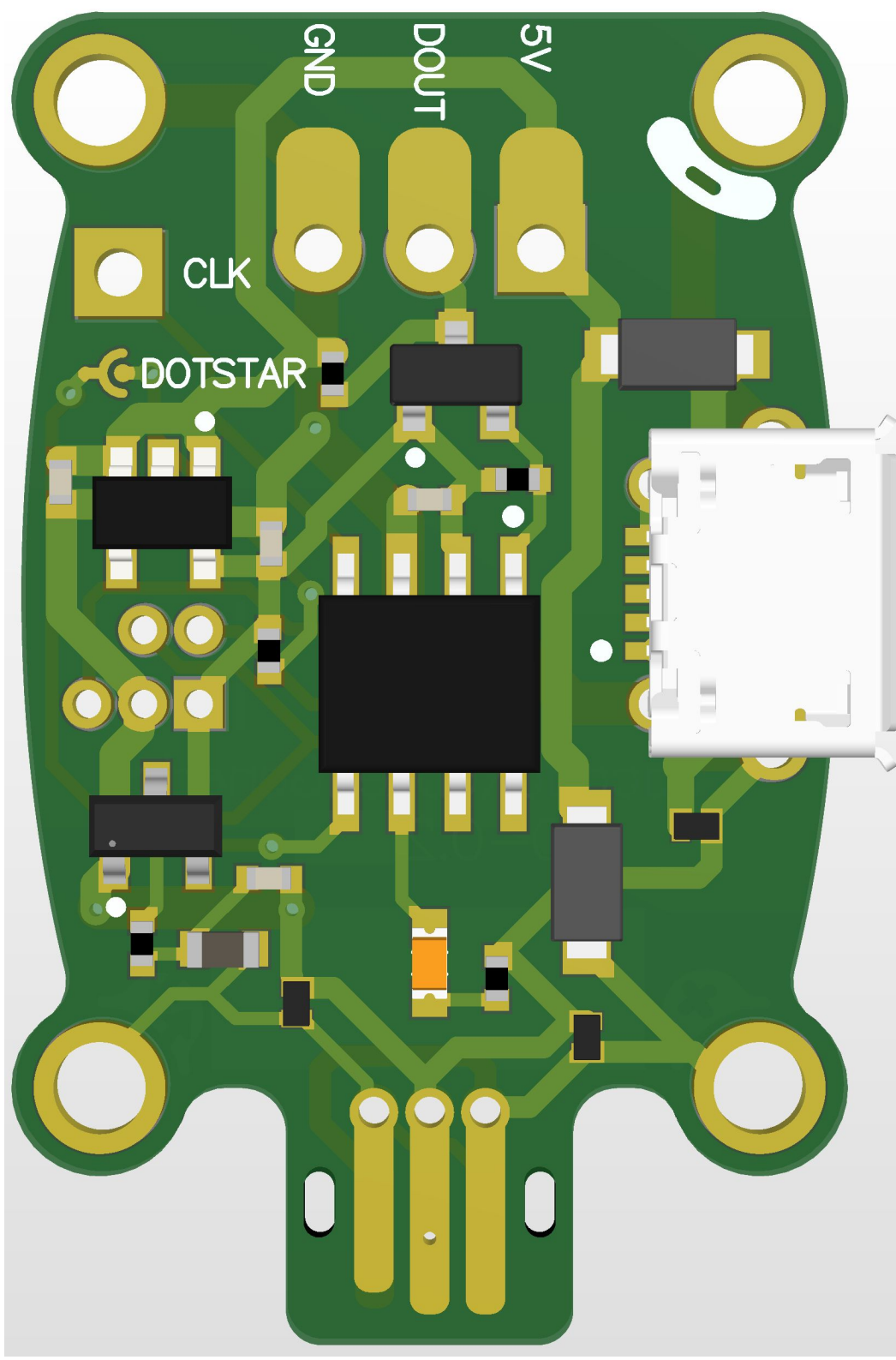
Silkscreen &

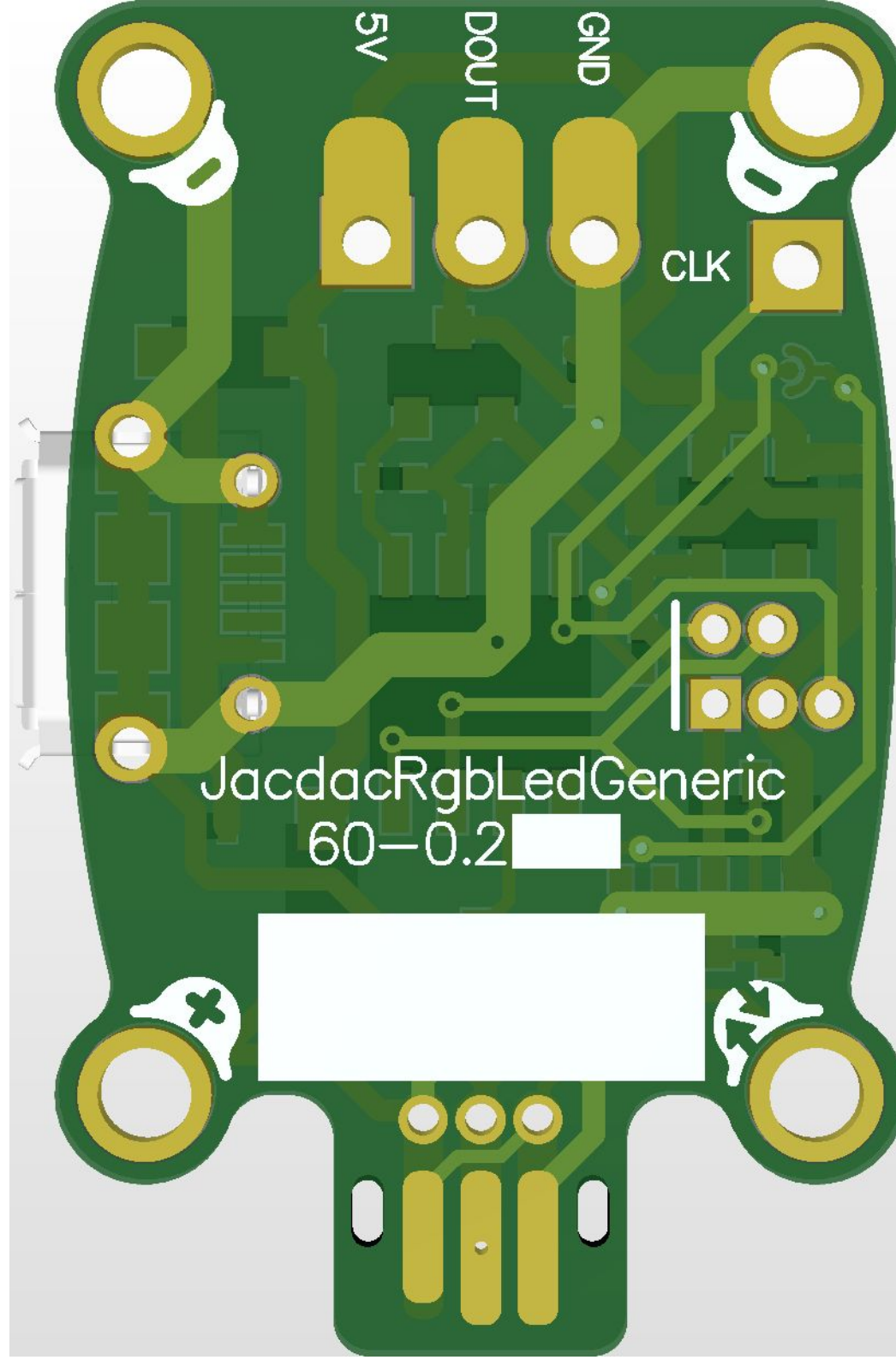
Block name

Design notes

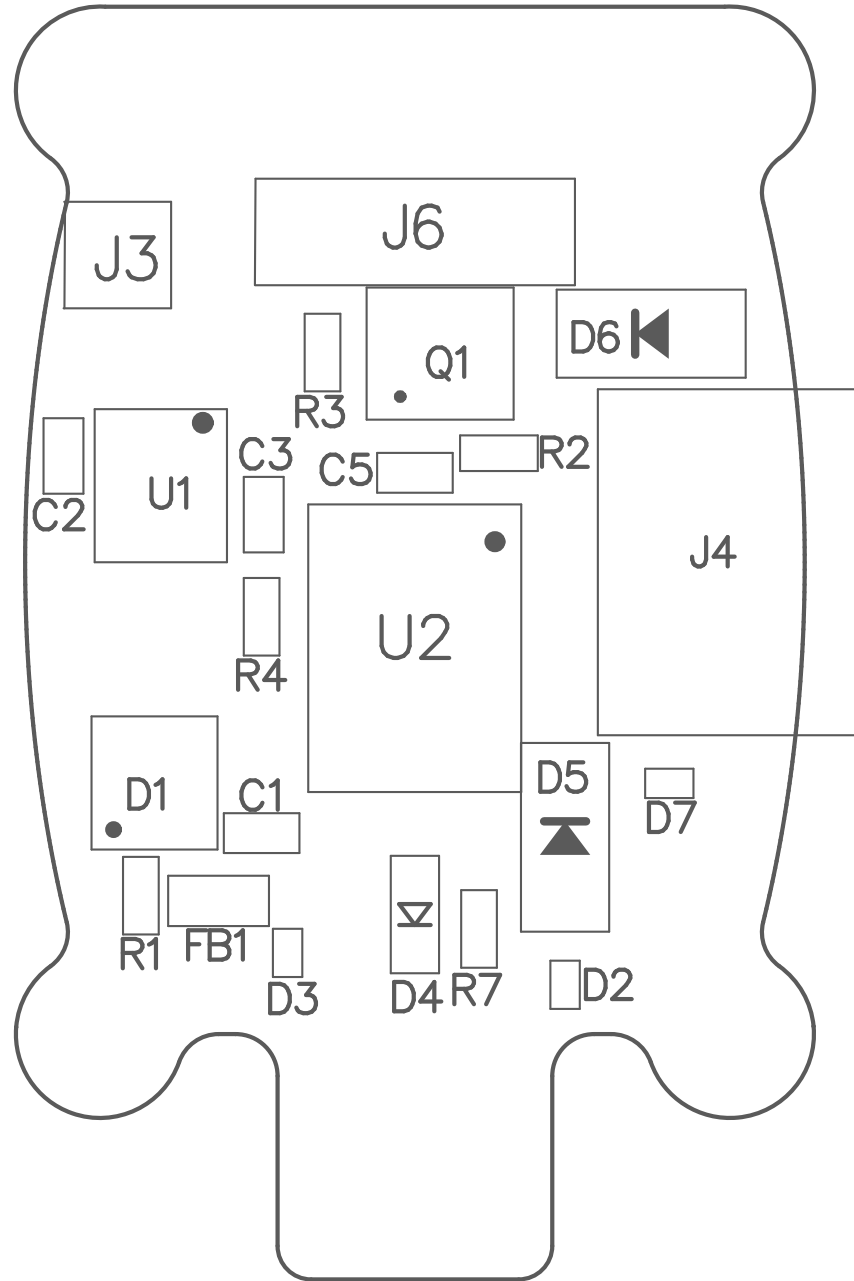
This information is provided "as-is". You bear the risk of using it. Some information relates to pre-released specification which may change without notice. Microsoft makes no warranties, express or implied, with respect to the information provided.

When this PDF is viewed with Adobe Reader, clicking on components shows part numbers and other details.



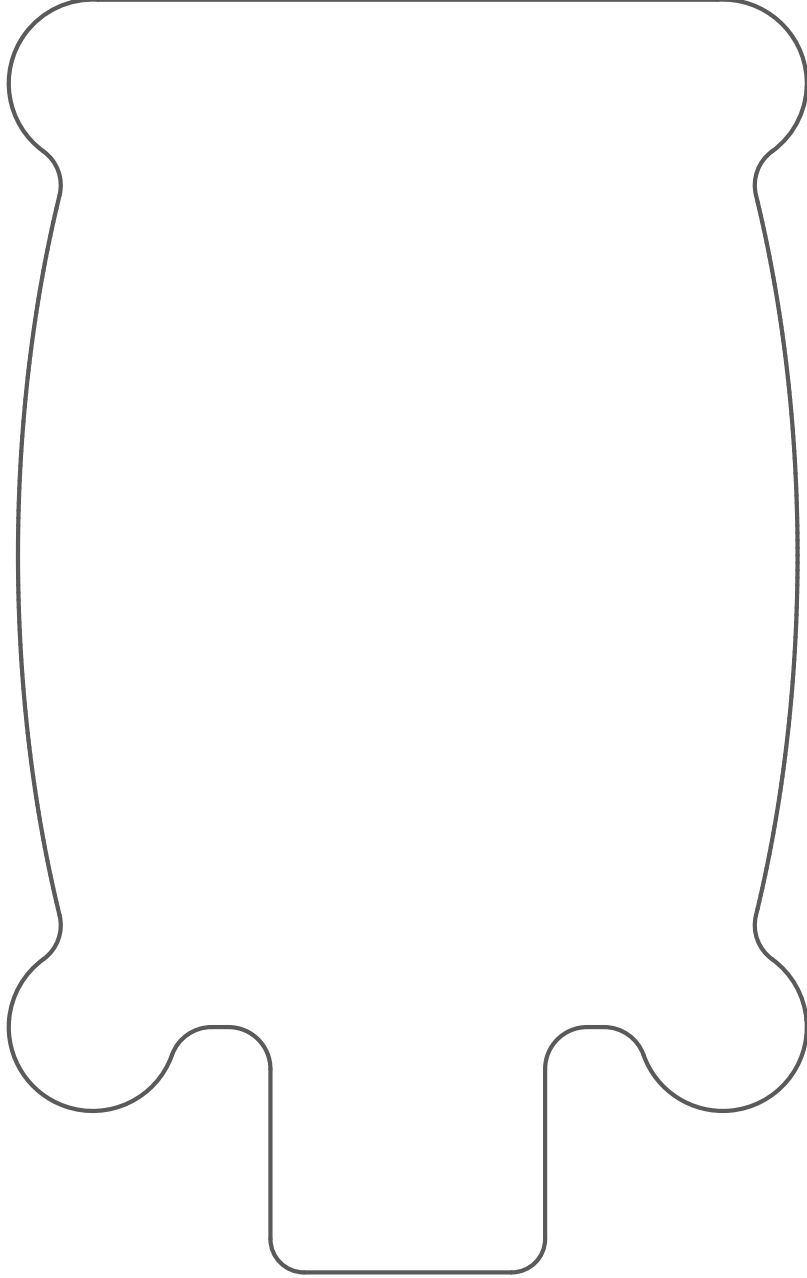


Board Outline Top Assy

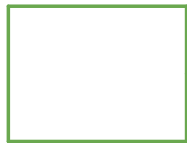


Board Outline

Bottom Assy



Fabrication Notes Board Outline



place any PCB manufacturer identifiers
in this region on top layer,
so they will be underneath the 8-SOIC

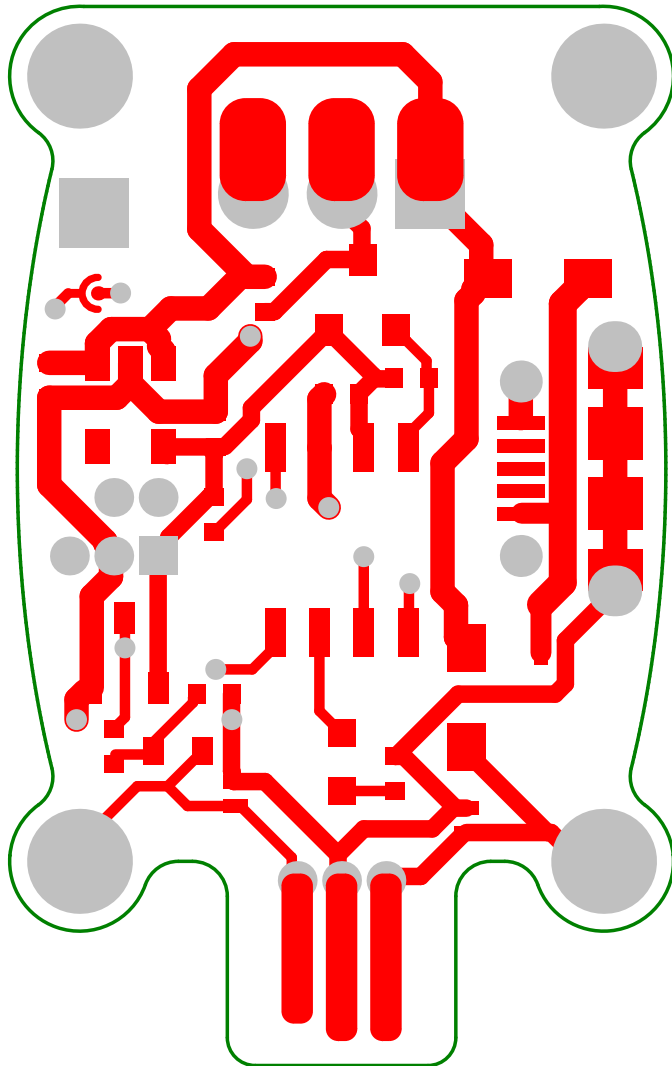
no board edge pips/
rat's teeth/mouse bites
below this line - make
sure board edge is clean

non-plated slots x2



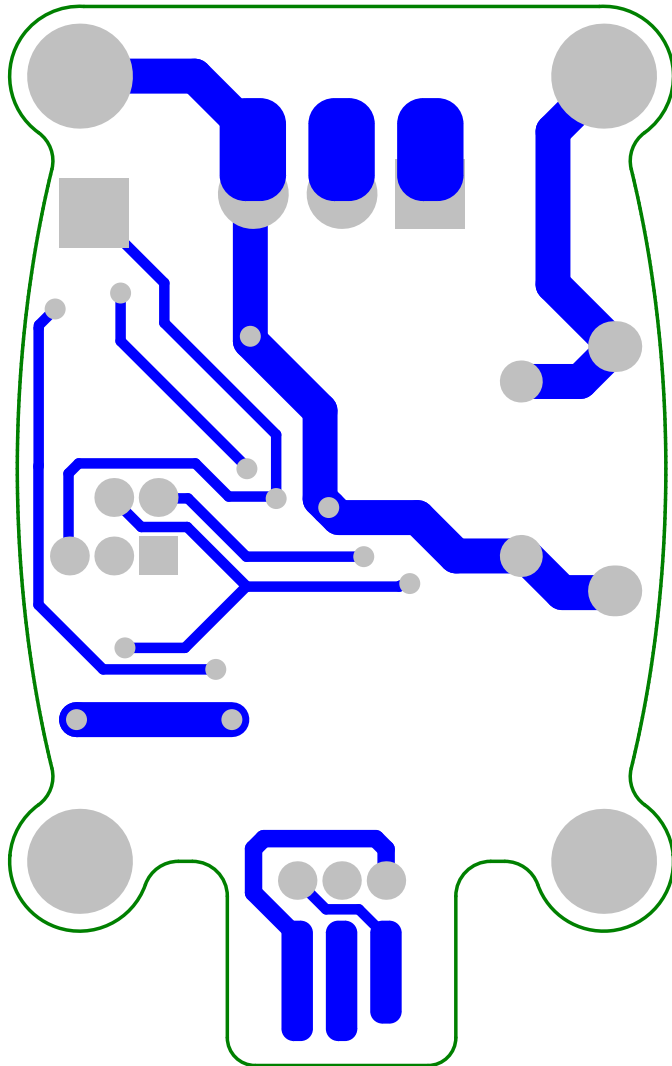
Top Layer

Board Outline



Bottom Layer

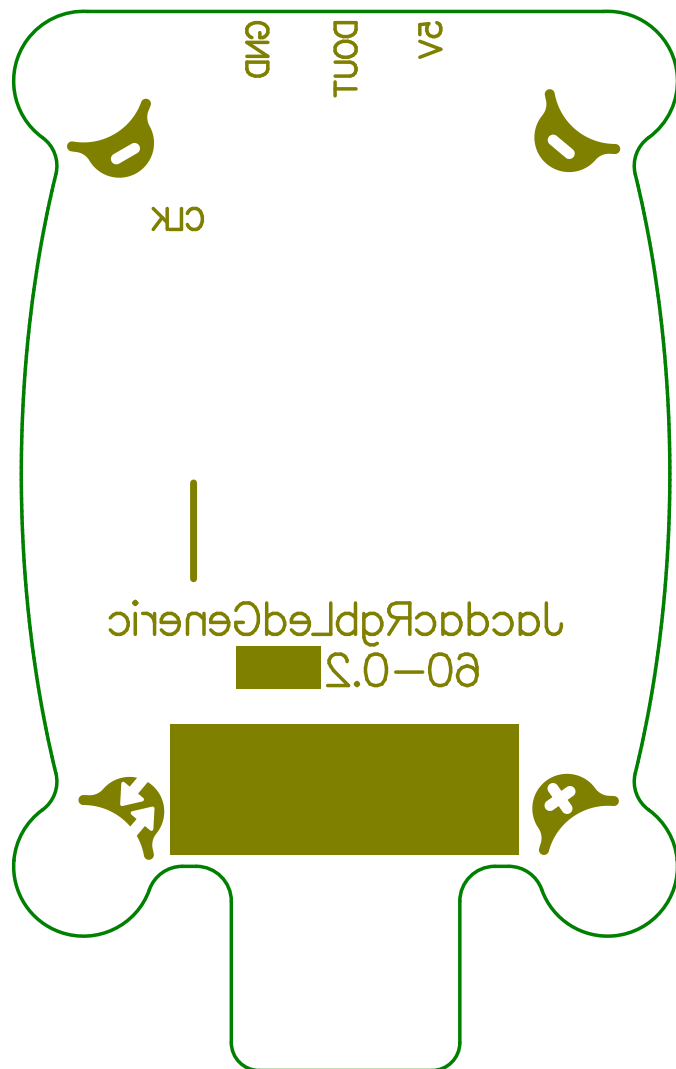
Board Outline



Board Outline

Top Overlay

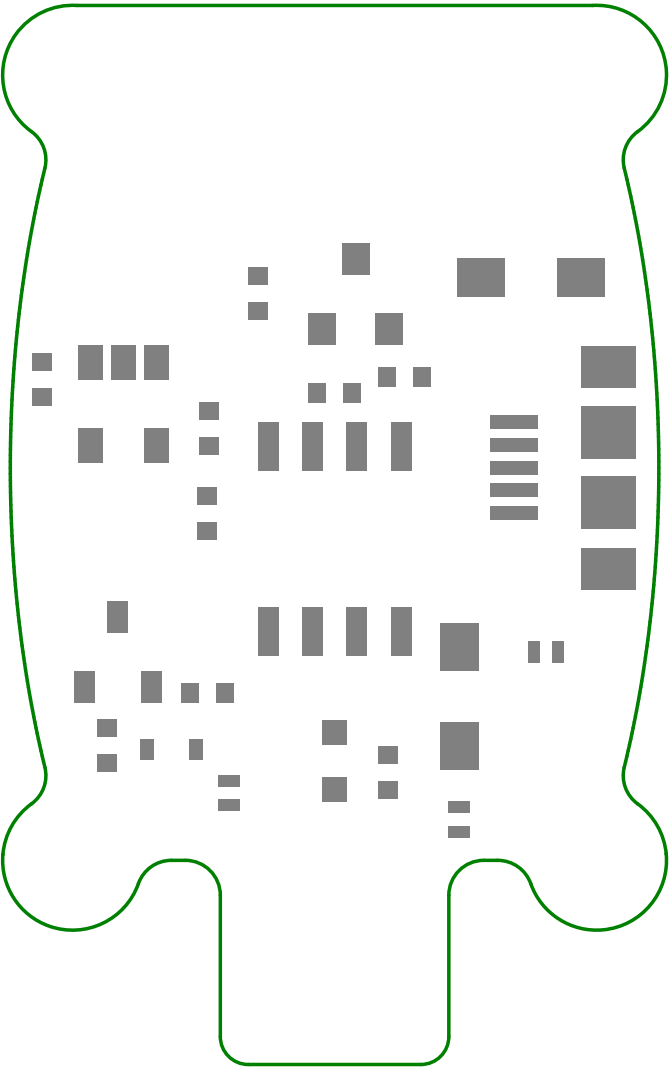




Board Outline

Bottom Overlay

Board Outline

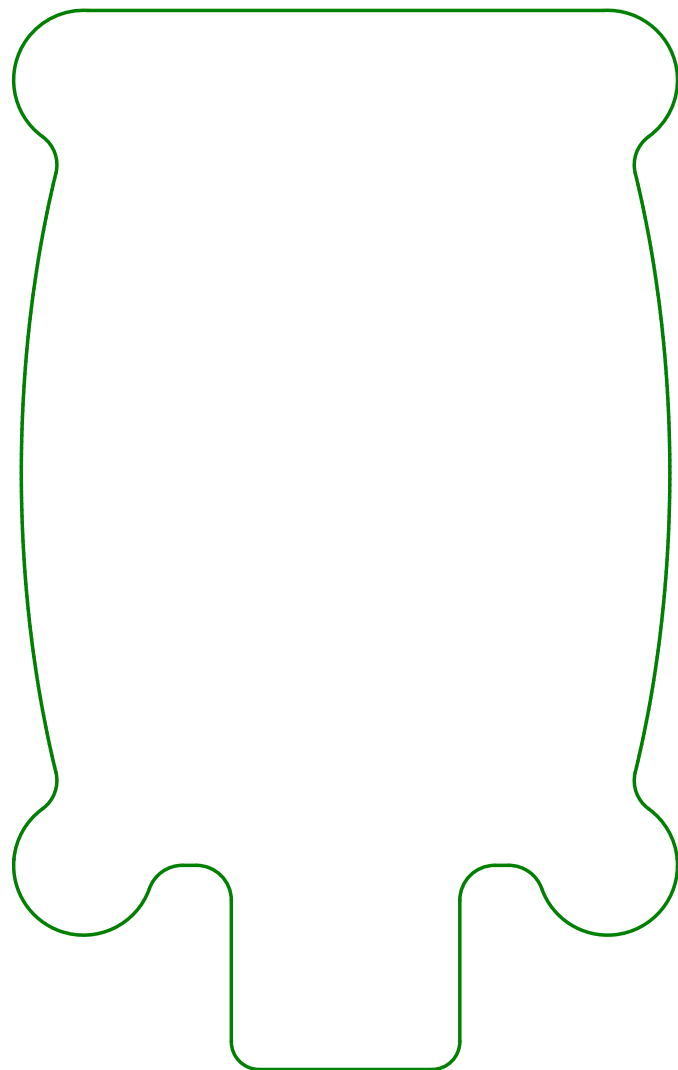


Top Paste

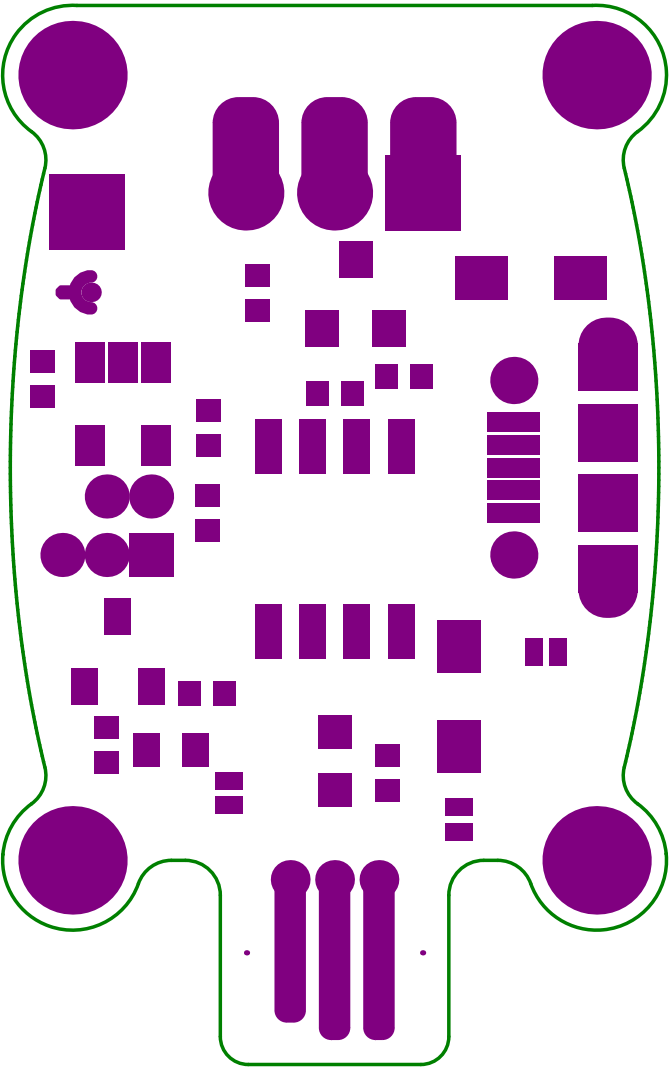


Board Outline

Bottom Paste



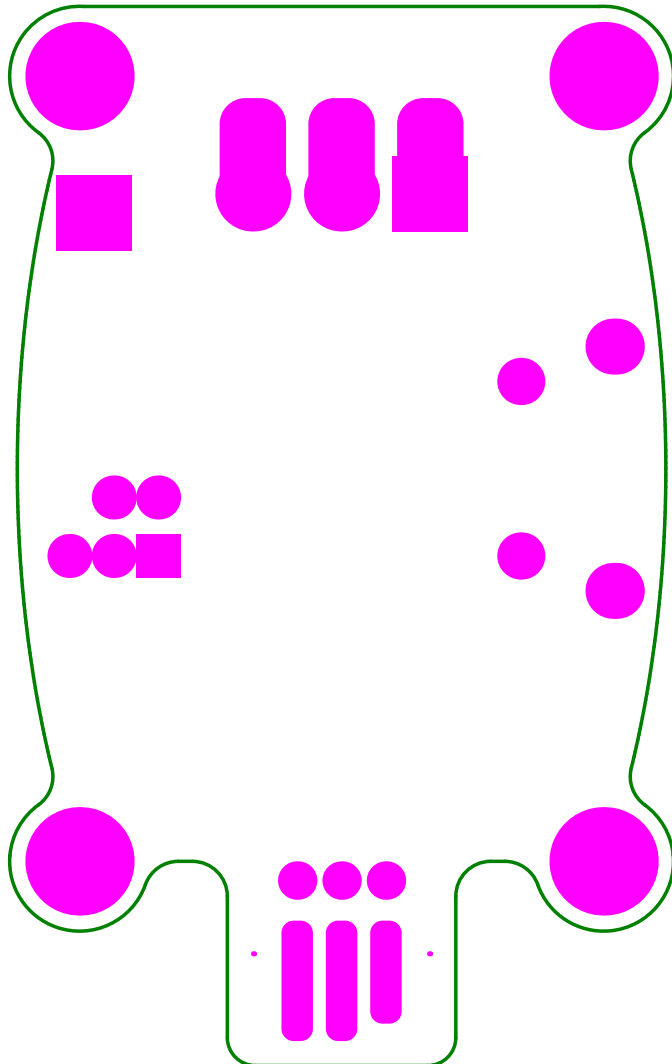
Board Outline



Top Solder (resist)



Board Outline



Bottom Solder (resist)

Board Outline

