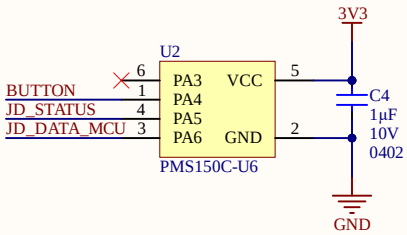
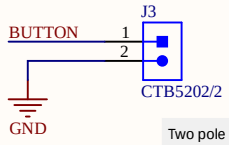
MCU



U2 must be programmed before being soldered down due to restrictive in-circuit programming requirements. JD_STATUS is PWM-capable GPIO.

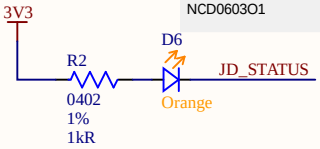
Button



MCU must have internal pull-up on BUTTON GPIO.

Two pole terminal block

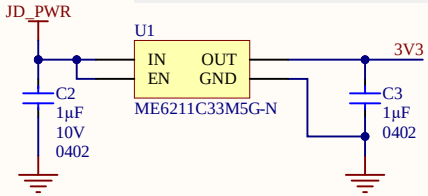
Status LED



D6
Alternative part
SML-D12D
E6C0603SEAC1UDA
NCD0603O1

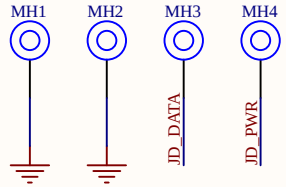
All Jacdac modules have Jacdac status LED. Relatively large R2 value limits current consumption.

3V3 Regulator



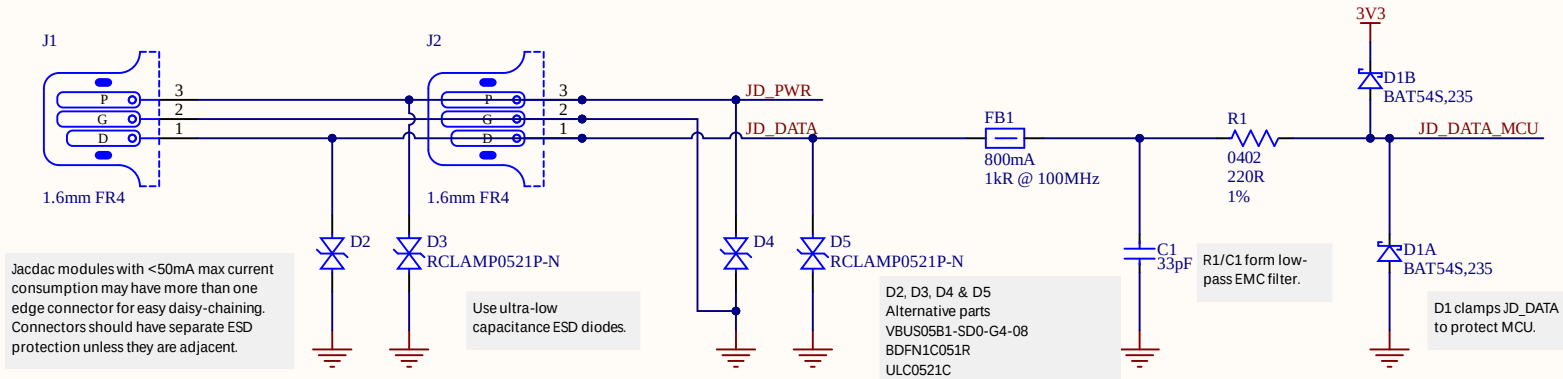
U1 alternative parts:
ME6212C33M5G 6V 260mV @ 200mA Iout 350mA
NCP114ASN330T1G 5.5V 225mV @ 300mA Iout 300mA
NCP114BSN330T1G 5.5V 225mV @ 300mA Iout 300mA

Mounting holes



JACDAC mounting holes are grounded plated through hole, finished diameter of 2.2mm and annular ring of 3.2mm diameter.

Jacdac connector



Jacdac modules with <50mA max current consumption may have more than one edge connector for easy daisy-chaining. Connectors should have separate ESD protection unless they are adjacent.

Use ultra-low capacitance ESD diodes.

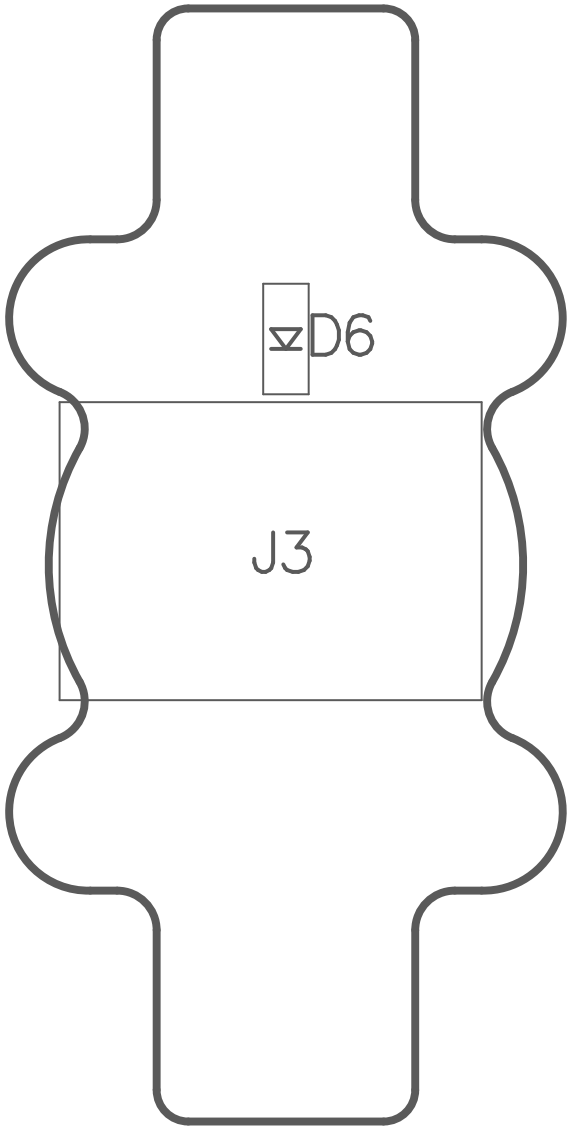
D2, D3, D4 & D5
Alternative parts
VBUS05B1-SD0-G4-08
BDFN1C051R
ULC0521C
ESD5311Z-2/TR

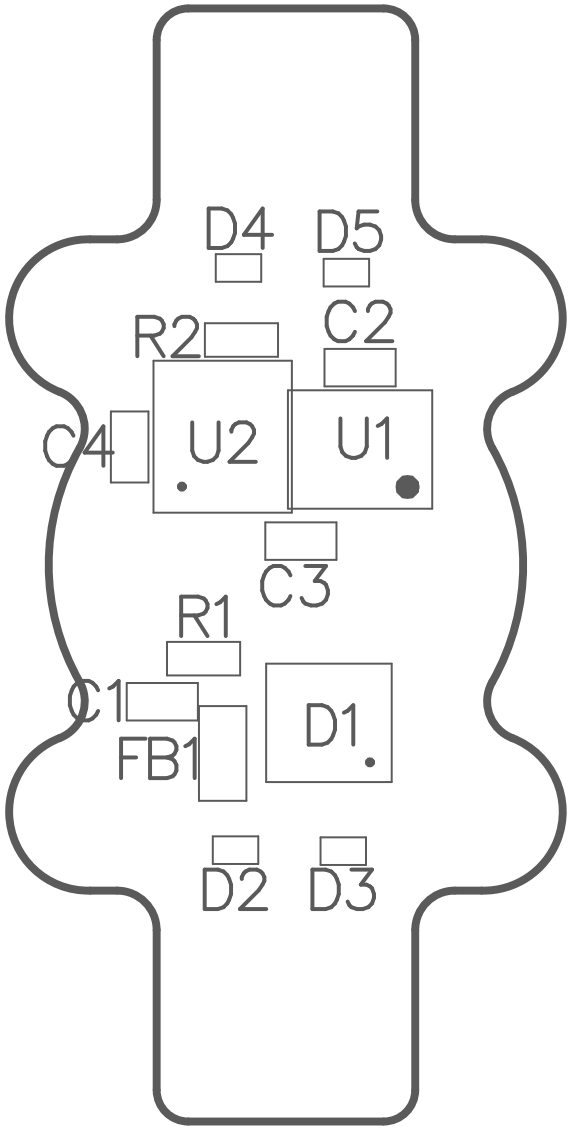
R1/C1 form low-pass EMC filter.

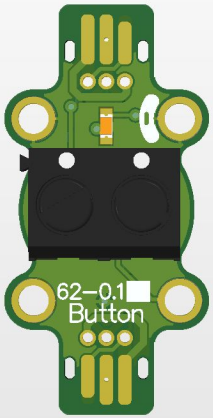
D1 clamps JD_DATA to protect MCU.

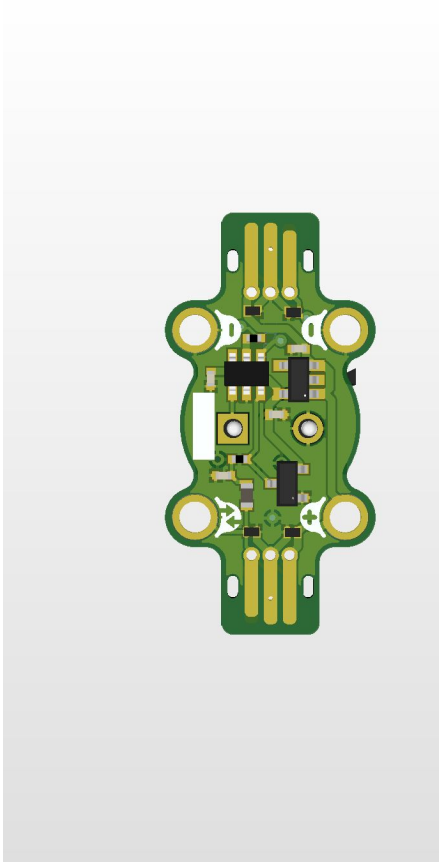
Key:
- Silkscreen & layout notes
- Block name
- Design notes

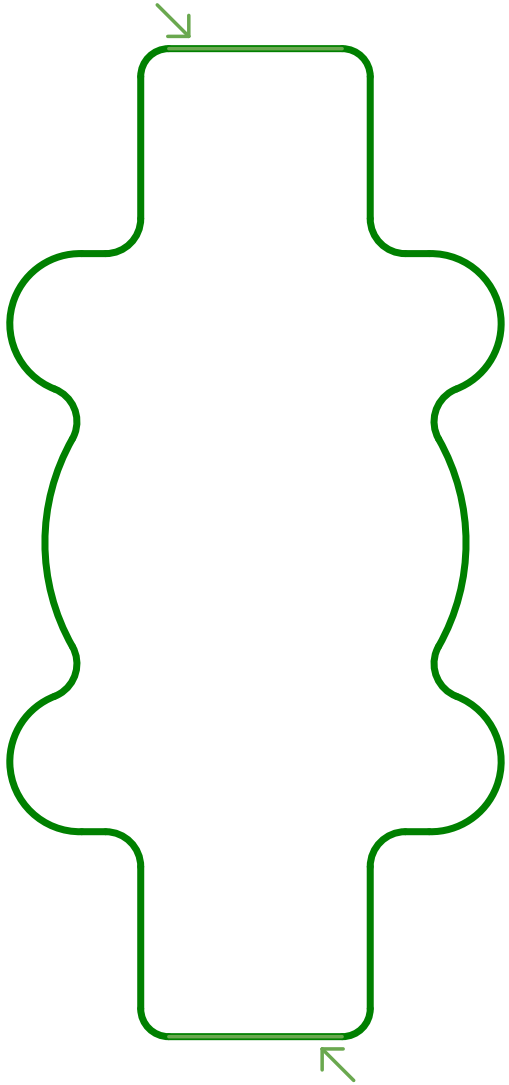
PROJECT FILENAME JacdacTBlockButton 62.PrjPCB	PROJECT CODENAME JacdacTBlockButton	Microsoft	PROJECT DESCRIPTION Jacdac button based on low-cost OTP PADAUK MCU
SHEET FILENAME JacdacTBlockButton 62.SchDoc	LICENCE Attribution 4.0 International (CC BY 4.0)	LAST MODIFIED 03/09/2021	PAGE 1 OF 1
		DRAWN BY NT	SHEET DESCRIPTION Complete design
		REVISION 0.1	PCB ID 62-0.1

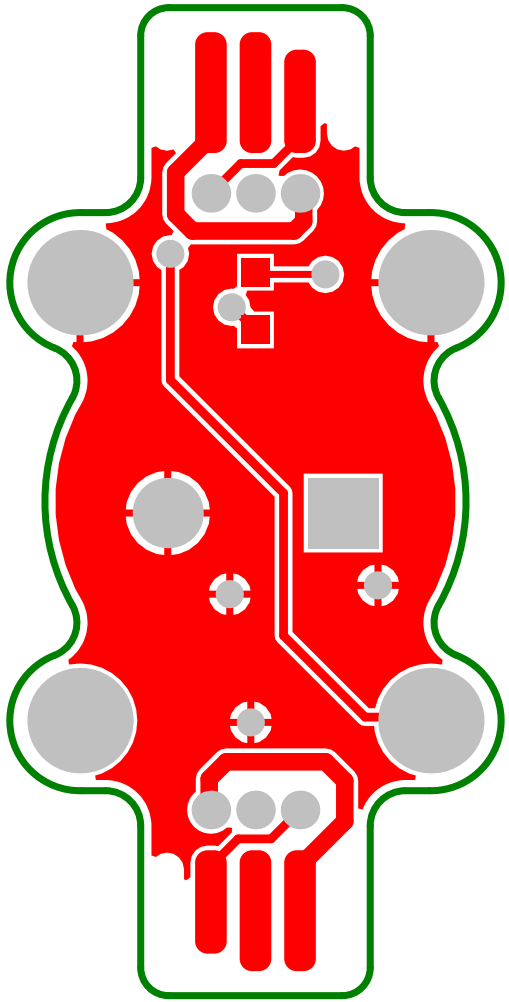

D6
J3

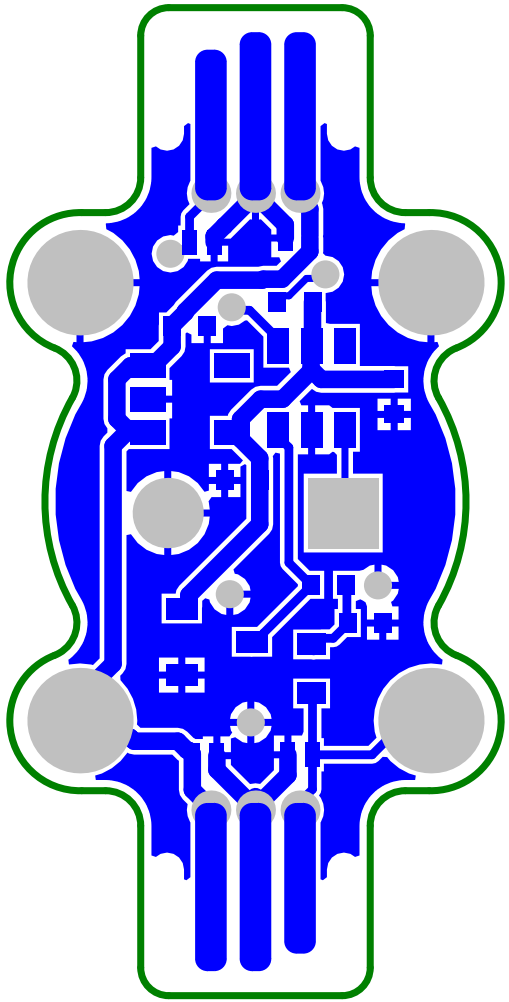

D4
D5
R2
C2
C4
U2
U1
C3
R1
C1
FB1
D1
D2
D3

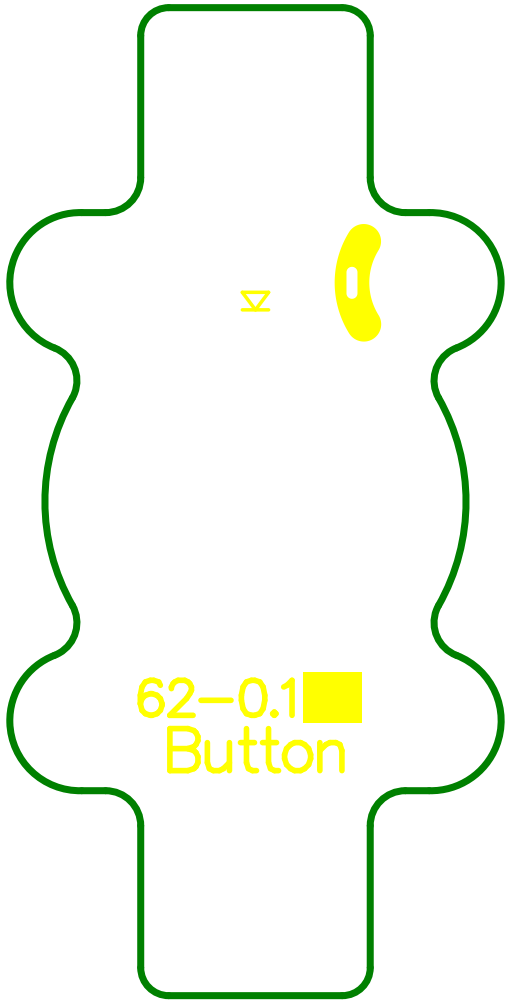

62-0.1
Button










62–0.1
Button