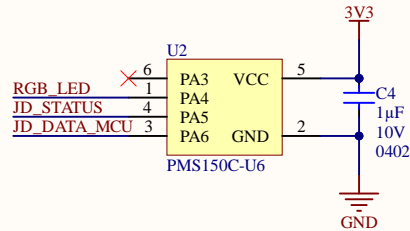
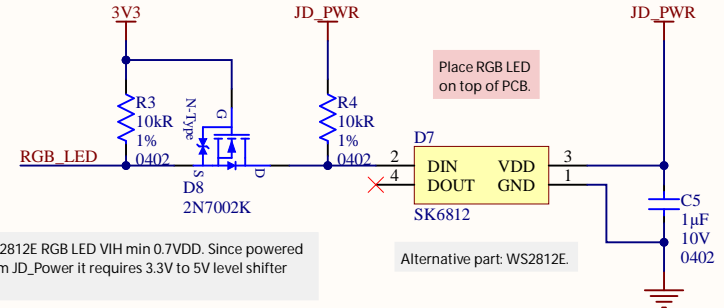


## MCU



U2 must be programmed before being soldered down due to restrictive in-circuit programming requirements. JD\_STATUS is PWM-capable GPIO.

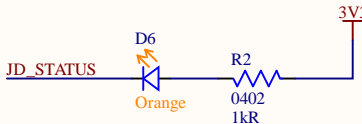
## RGB addressable LED



WS2812E RGB LED VIH min 0.7VDD. Since powered from JD\_Power it requires 3.3V to 5V level shifter

Alternative part: WS2812E.

## Status LED



Place status LED on bottom of PCB.

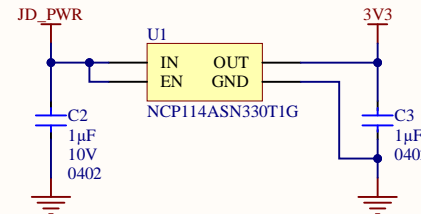
D6  
Alternative part  
SML-D12D  
E6C0603SEAC1UDA  
NCD060301

Jacdac modules require a status LED.

The LED can be monochrome or multicolor depending on GPIO availability

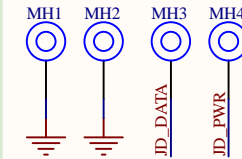
If using alternative part recalculate the resistor values R2

## 3V3 Regulator



U1 alternative parts:  
ME6212C33M5G 6V 260mV @ 200mA Iout 350mA  
NCP114BSN330T1G 5.5V 225mV @ 300mA Iout 300mA

## Mounting holes



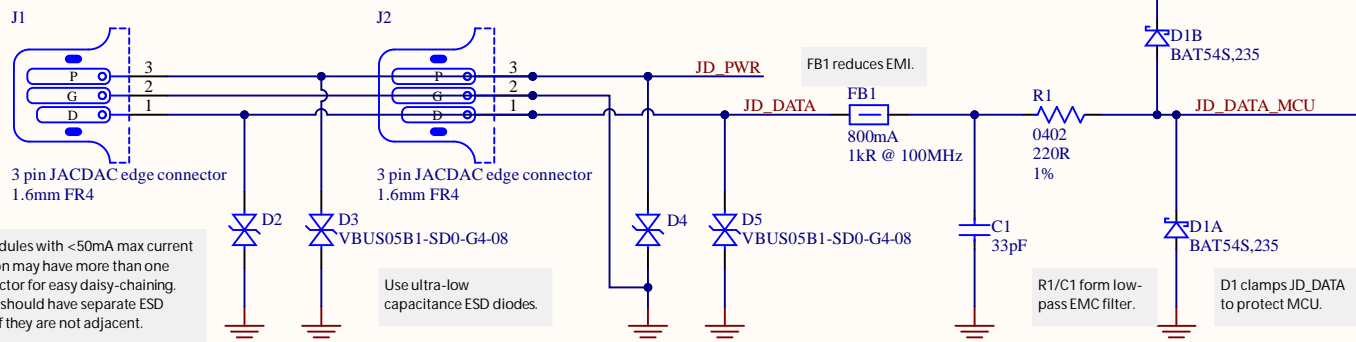
JACDAC mounting holes are plated through hole, finished diameter of 2.1mm, annular ring of 3.0mm diameter and copper/component keepout of 5.0mm. The mounting holes should be on 2.5mm pitch.

MH1 & MH2 : GND  
MH3 : JD\_DATA  
MH4 : JD\_PWR

Mounting holes should have appropriate silkscreen marker, and MH1 should have a pin 1 marker on the top side.

Jacdac modules require mounting holes. Modules mounting holes are electrically connected so that modules can be mounted on top of other PCBs without using cables.

## JacDac connector



JACDAC modules with <50mA max current consumption may have more than one edge connector for easy daisy-chaining. Connectors should have separate ESD protection if they are not adjacent.

Use ultra-low capacitance ESD diodes.

ESD diode pair required for each Jacdac connector.

Microsoft

PROJECT DESCRIPTION  
Jacdac Padauk single Addressable RGB LED

SHEET DESCRIPTION  
Complete design

PROJECT FILENAME JacdacSingleRgbLed 42.PrjPCB

PROJECT CODENAME JacdacSingleRgbLed

LAST MODIFIED 10/11/2021

PAGE 1 OF 1

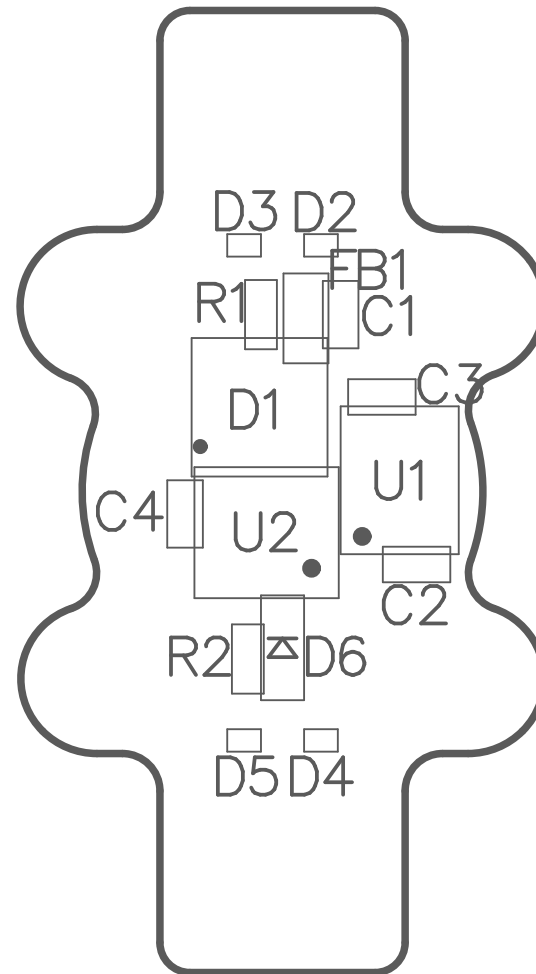
DRAWN BY GD, JD, SH & DG

SHEET FILENAME JacdacSingleRgbLed 42.SchDoc

LICENCE Attribution 4.0 International (CC BY 4.0)

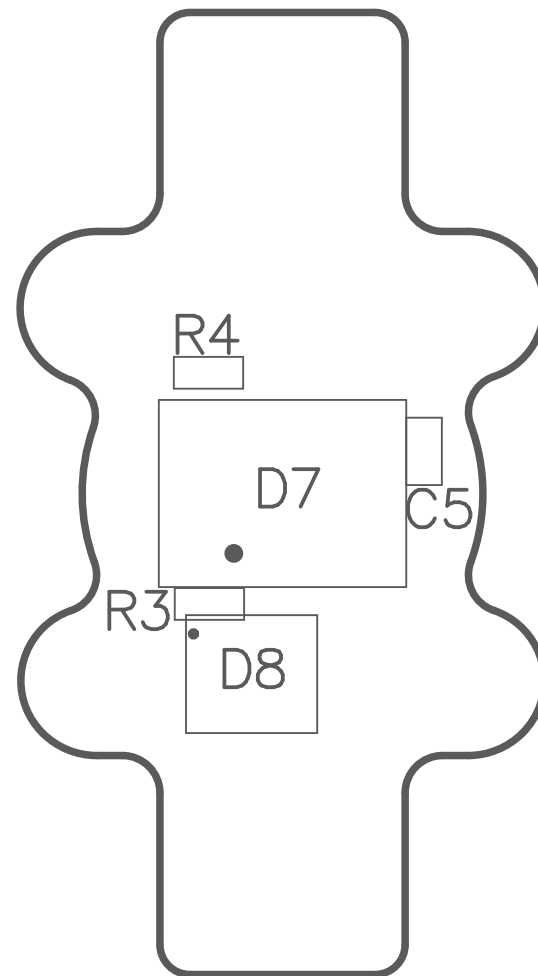
REVISION 0.3 PCB ID 42-0.3

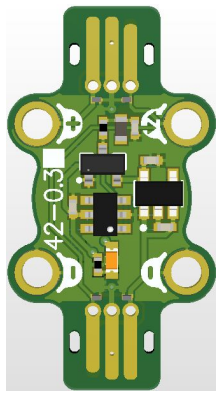
# Board Outline Top Assy



Board Outline

Bottom Assy

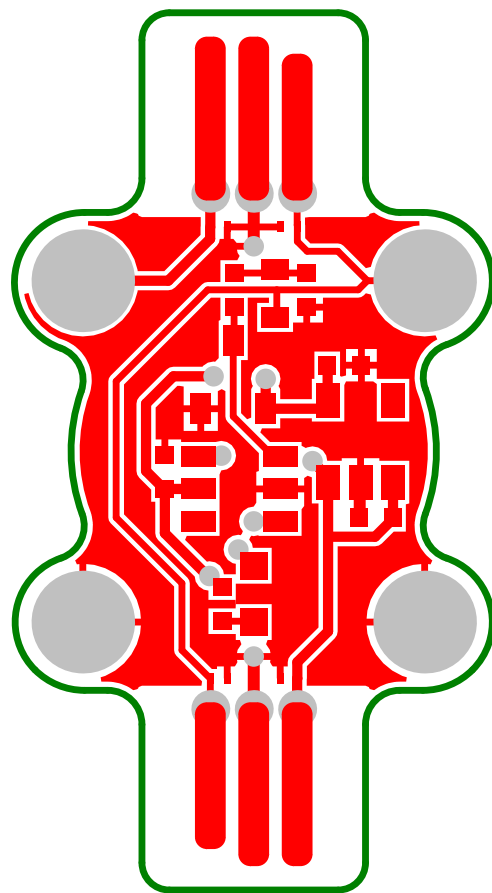






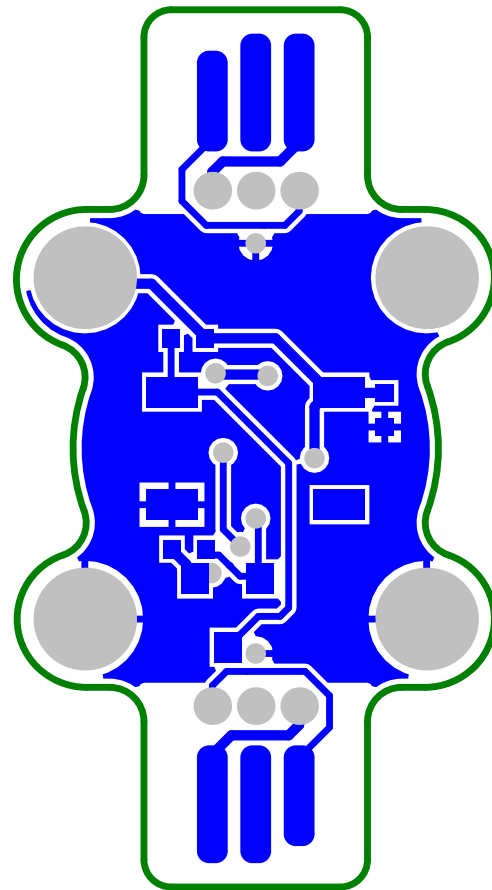
Top Layer

Board Outline

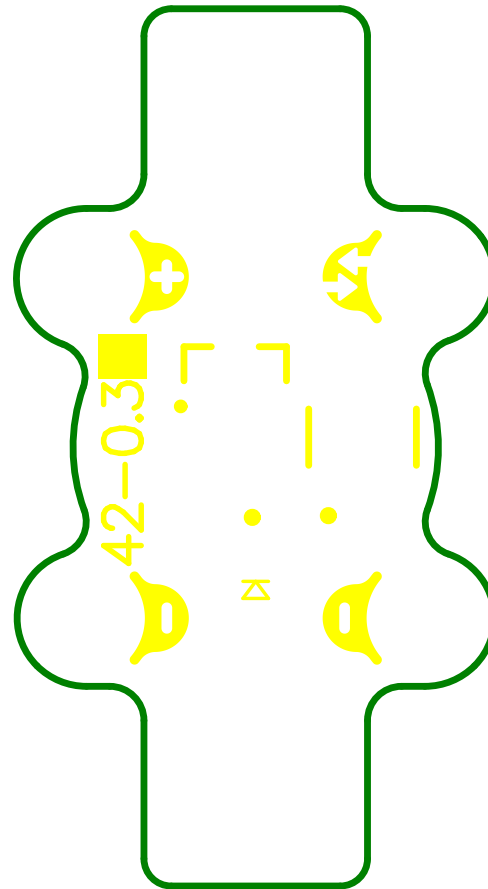


Bottom Layer

Board Outline



## Board Outline





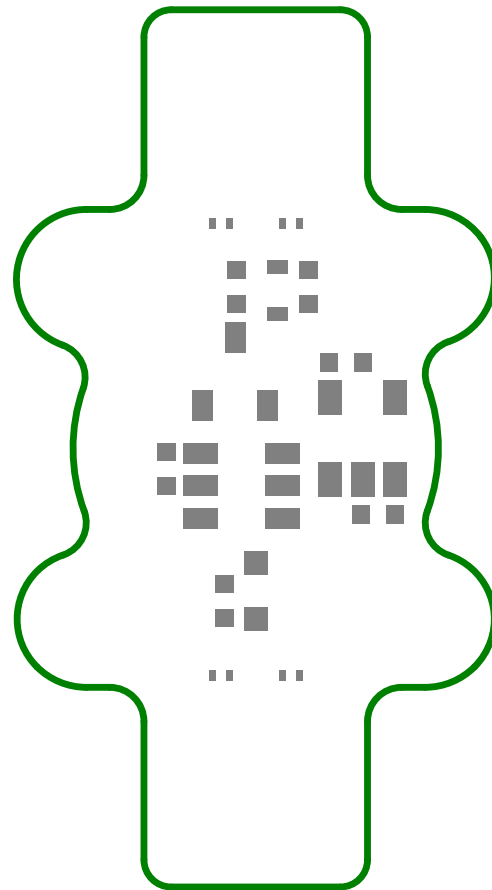
Board Outline

Bottom Overlay



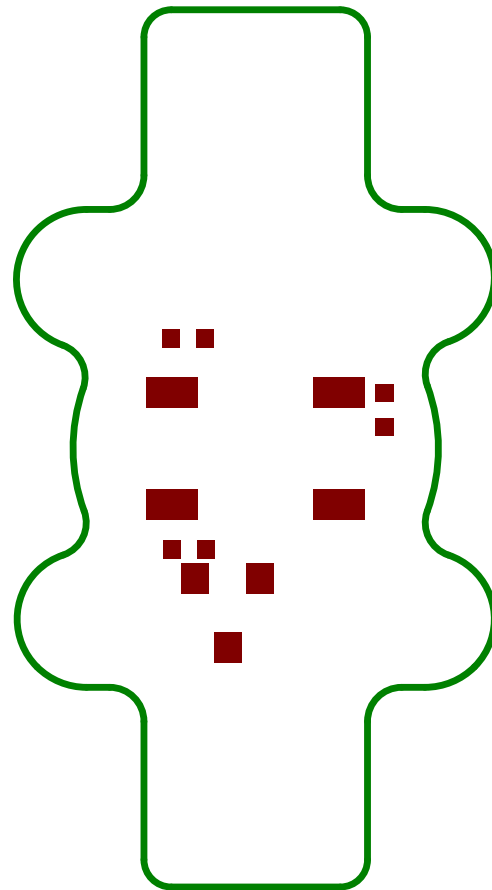
Board Outline

Top Paste



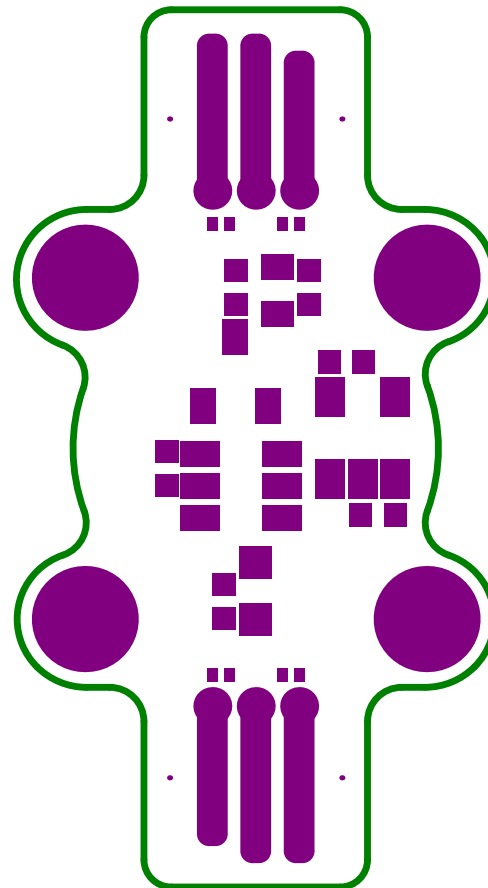
Board Outline

Bottom Paste



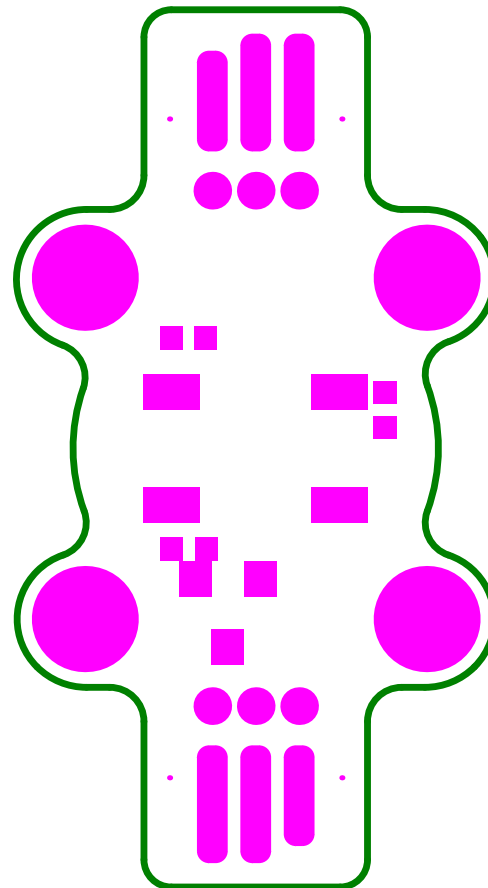
Board Outline

Top Solder (resist)



Board Outline

Bottom Solder (resist)



## Board Outline

