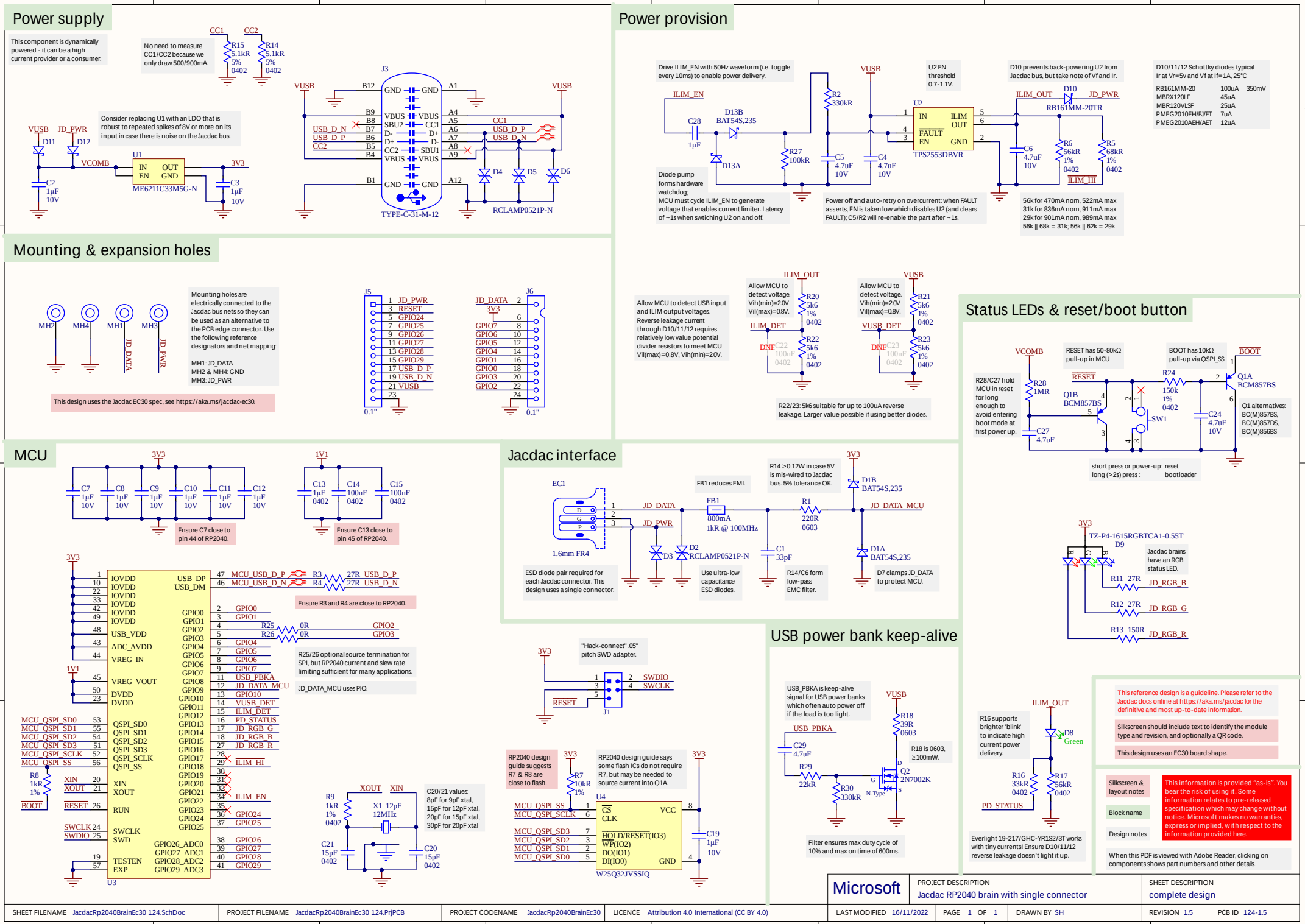
Power supply
This component is dynamically powered - it can be a high current provider or a consumer.
No need to measure CC1/CC2 because we only draw 500/900mA.
CC1 CC2
R15 5.1kR 5% 0402
R14 5.1kR 5% 0402
Consider replacing U1 with an LDO that is robust to repeated spikes of 8V or more on its input in case there is noise on the Jacdac bus.
VUSB JD_PWR
D11 D12
VCOMB
U1
IN OUT
EN GND
ME6211C33M5G-N
3V3
C2 1µF 10V
C3 1µF 10V
J3
TYPE-C-31-M-12
RCLAMP0521P-N
D4 D5 D6
USB_D_N USB_D_P CC2
CC1
Power provision
Drive ILIM_EN with 50Hz waveform (i.e. toggle every 10ms) to enable power delivery.
ILIM_EN
C28 1µF
D13B BAT54S,235
D13A
R2 330kR
R27 100kR
C5 4.7uF 10V
C4 4.7uF 10V
U2 EN threshold 0.7-1.1V.
U2
IN ILIM OUT
FAULT
EN GND
TPS2553DBVR
D10 prevents back-powering U2 from Jacdac bus, but take note of Vf and Ir.
ILIM_OUT D10 JD_PWR
RB161MM-20TR
C6 4.7uF 10V
R6 56kR 1% 0402
R5 68kR 1% 0402
ILIM_HI
D10/11/12 Schottky diodes typical Ir at Vr=5v and Vf at If=1A, 25°C
RB161MM-20 100uA 350mV
MBRX120LF 45uA
MBR120VLSF 25uA
PMEG2010EH/EJ/ET 7uA
PMEG2010AEH/AET 12uA
Diode pump forms hardware watchdog; MCU must cycle ILIM_EN to generate voltage that enables current limiter. Latency of ~1s when switching U2 on and off.
Power off and auto-retry on overcurrent: when FAULT asserts, EN is taken low which disables U2 (and clears FAULT); C5/R2 will re-enable the part after ~1s.
56k for 470mA nom, 522mA max
31k for 836mA nom, 911mA max
29k for 901mA nom, 989mA max
56k || 68k = 31k; 56k || 62k = 29k
Mounting & expansion holes
MH2 MH4 MH1 MH3
JD_DATA JD_PWR
Mounting holes are electrically connected to the Jacdac bus nets so they can be used as an alternative to the PCB edge connector. Use the following reference designators and net mapping:
MH1: JD_DATA
MH2 & MH4: GND
MH3: JD_PWR
This design uses the Jacdac EC30 spec, see https://aka.ms/jacdac-ec30.
J5
1 JD_PWR
3 RESET
5 GPIO24
7 GPIO25
9 GPIO26
11 GPIO27
13 GPIO28
15 GPIO29
17 USB_D_P
19 USB_D_N
21 VUSB
23
0.1"
J6
JD_DATA 2
3V3 6
GPIO7 8
GPIO6 10
GPIO5 12
GPIO4 14
GPIO1 16
GPIO0 18
GPIO3 20
GPIO2 22
24
0.1"
Allow MCU to detect USB input and ILIM output voltages. Reverse leakage current through D10/11/12 requires relatively low value potential divider resistors to meet MCU Vil(max)=0.8V, Vih(min)=2.0V.
Allow MCU to detect voltage. Vih(min)=2.0V Vil(max)=0.8V.
ILIM_OUT
R20 5k6 1% 0402
ILIM_DET
DNF C22 100nF 0402
R22 5k6 1% 0402
Allow MCU to detect voltage. Vih(min)=2.0V Vil(max)=0.8V.
VUSB
R21 5k6 1% 0402
VUSB_DET
DNF C23 100nF 0402
R23 5k6 1% 0402
R22/23: 5k6 suitable for up to 100uA reverse leakage. Larger value possible if using better diodes.
Status LEDs & reset/boot button
VCOMB
R28 1MR
C27 4.7uF
R28/C27 hold MCU in reset for long enough to avoid entering boot mode at first power up.
RESET has 50-80kΩ pull-up in MCU
RESET
Q1B BCM857BS
BOOT has 10kΩ pull-up via QSPI_SS
BOOT
R24 150k 1% 0402
Q1A BCM857BS
SW1
C24 4.7uF 10V
Q1 alternatives: BC(M)857BS, BC(M)857DS, BC(M)856BS
short press or power-up: reset
long (>2s) press: bootloader
MCU
3V3
C7 1µF 10V
C8 1µF 10V
C9 1µF 10V
C10 1µF 10V
C11 1µF 10V
C12 1µF 10V
Ensure C7 close to pin 44 of RP2040.
1V1
C13 1µF 0402
C14 100nF 0402
C15 100nF 0402
Ensure C13 close to pin 45 of RP2040.
IOVDD USB_VDD ADC_AVDD VREG_IN VREG_VOUT DVDD
USB_DP USB_DM
MCU_USB_D_P MCU_USB_D_N
R3 27R USB_D_P
R4 27R USB_D_N
Ensure R3 and R4 are close to RP2040.
GPIO0 GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7 GPIO8 GPIO9 GPIO10 GPIO11 GPIO12 GPIO13 GPIO14 GPIO15 GPIO16 GPIO17 GPIO18 GPIO19 GPIO20 GPIO21 GPIO22 GPIO23 GPIO24 GPIO25 GPIO26_ADC0 GPIO27_ADC1 GPIO28_ADC2 GPIO29_ADC3
R25 0R GPIO2
R26 0R GPIO3
R25/26 optional source termination for SPI, but RP2040 current and slew rate limiting sufficient for many applications.
USB_PBKA
JD_DATA_MCU
ILIM_DET
PD_STATUS
JD_RGB_G
JD_RGB_B
JD_RGB_R
ILIM_HI
ILIM_EN
GPIO24
GPIO25
GPIO26
GPIO27
GPIO28
GPIO29
JD_DATA_MCU uses PIO.
QSPI_SD0 QSPI_SD1 QSPI_SD2 QSPI_SD3 QSPI_SCLK QSPI_SS
MCU_QSPI_SD0 MCU_QSPI_SD1 MCU_QSPI_SD2 MCU_QSPI_SD3 MCU_QSPI_SCLK MCU_QSPI_SS
R8 1kR 1% BOOT
XIN XOUT
RESET
SWCLK SWDIO
RUN SWD TESTEN EXP
U3
XOUT XIN
R9 1kR 1% 0402
X1 12pF 12MHz
C21 15pF 0402
C20 15pF 0402
C20/21 values: 8pF for 9pF xtal, 15pF for 12pF xtal, 20pF for 15pF xtal, 30pF for 20pF xtal
Jacdac interface
EC1
D G P
1.6mm FR4
ESD diode pair required for each Jacdac connector. This design uses a single connector.
JD_DATA
JD_PWR
FB1 800mA 1kR @ 100MHz
FB1 reduces EMI.
D3 D2 RCLAMP0521P-N
Use ultra-low capacitance ESD diodes.
C1 33pF
R14/C6 form low-pass EMC filter.
R1 220R 0603
R14 >0.12W in case 5V is mis-wired to Jacdac bus. 5% tolerance OK.
3V3
D1B BAT54S,235
JD_DATA_MCU
D1A BAT54S,235
D7 clamps JD_DATA to protect MCU.
3V3
TZ-P4-1615RGBTCA1-0.55T
D9
Jacdac brains have an RGB status LED.
R11 27R JD_RGB_B
R12 27R JD_RGB_G
R13 150R JD_RGB_R
3V3
"Hack-connect" .05" pitch SWD adapter.
SWDIO SWCLK
RESET
J1
RP2040 design guide suggests R7 & R8 are close to flash.
3V3
R7 10kR 1%
RP2040 design guide says some flash ICs do not require R7, but may be needed to source current into Q1A.
3V3
U4
CS CLK
HOLD/RESET(IO3) WP(IO2) DO(IO1) DI(IO0)
VCC GND
W25Q32JVSSIQ
C19 1µF 10V
USB power bank keep-alive
USB_PBKA is keep-alive signal for USB power banks which often auto power off if the load is too light.
USB_PBKA
C29 4.7uF
R29 22kR
R30 330kR
VUSB
R18 39R 0603
R18 is 0603, ≥100mW.
Q2 2N7002K
N-Type
Filter ensures max duty cycle of 10% and max on time of 600ms.
R16 supports brighter 'blink' to indicate high current power delivery.
ILIM_OUT
D8 Green
R16 33kR 0402
R17 56kR 0402
PD_STATUS
Everlight 19-217/GHC-YR1S2/3T works with tiny currents! Ensure D10/11/12 reverse leakage doesn't light it up.
This reference design is a guideline. Please refer to the Jacdac docs online at https://aka.ms/jacdac for the definitive and most up-to-date information.
Silkscreen should include text to identify the module type and revision, and optionally a QR code.
This design uses an EC30 board shape.
Silkscreen & layout notes
Block name
Design notes
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PROJECT DESCRIPTION
Jacdac RP2040 brain with single connector
SHEET DESCRIPTION
complete design
SHEET FILENAME JacdacRp2040BrainEc30 124.SchDoc
PROJECT FILENAME JacdacRp2040BrainEc30 124.PrjPCB
PROJECT CODENAME JacdacRp2040BrainEc30
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