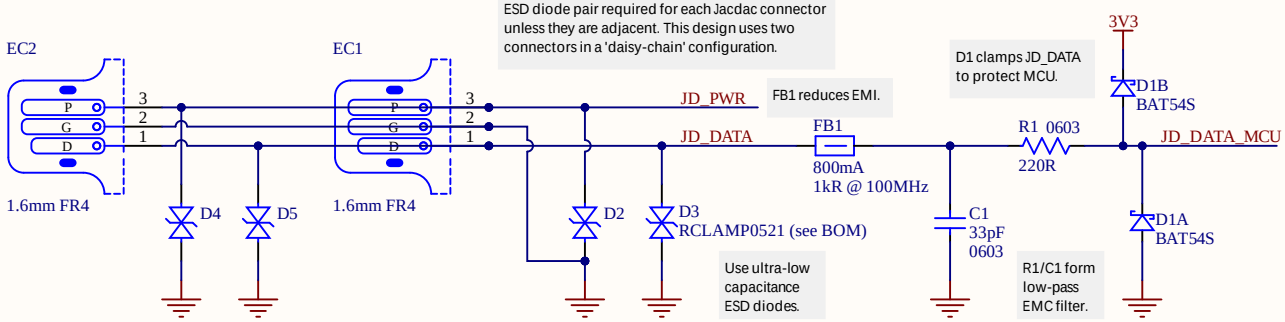
Jacdac connector



ESD diode pair required for each Jacdac connector unless they are adjacent. This design uses two connectors in a 'daisy-chain' configuration.

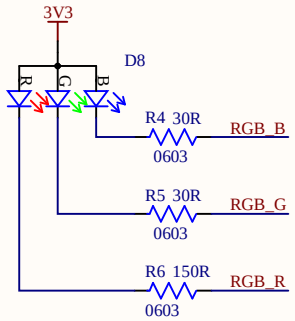
FB1 reduces EMI.

D1 clamps JD_DATA to protect MCU.

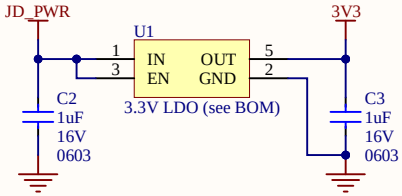
Use ultra-low capacitance ESD diodes.

R1/C1 form low-pass EMC filter.

RGB LED



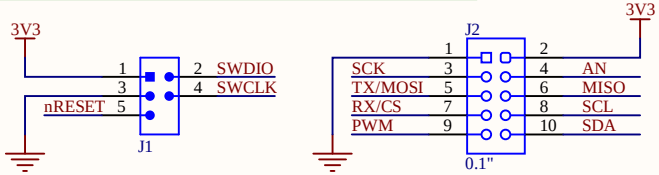
3V3 regulator



Consider using an LDO that is robust to spikes over 6V on input in case of noise on JD_PWR.

This component is a power-consumer.

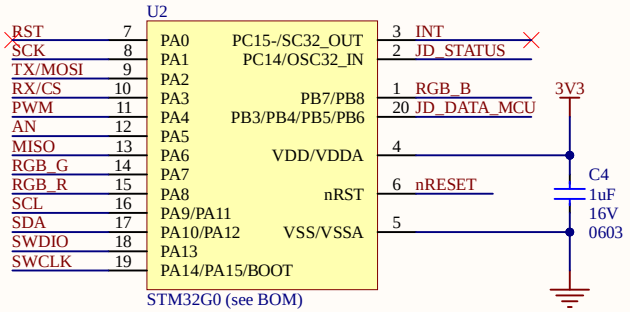
Programming/debug/expansion



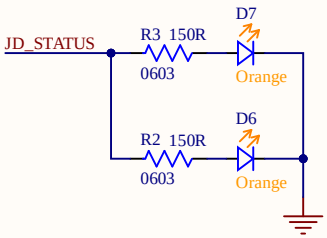
"Hack-connect" SWD adapter.
https://arcade.makecode.com/hardware/dbg

Label expansion header pins.

MCU

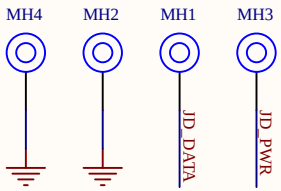


Status LED



Jacdac modules require a status LED per port (can be shared if ports are adjacent). Can be monochrome or multicolor depending on GPIO availability.

Mounting holes



Mounting holes are electrically connected to the Jacdac bus nets so they can be used as an alternative to the PCB edge connector. Please use the following reference designators and net mapping:

MH1 & MH2: GND
MH3: JD_DATA
MH4: JD_PWR

This design uses PTH mounting holes with finished diameter of 3.1mm, annular copper ring of 4.4mm diameter & copper/component keepout of 7.0mm. The mounting holes must be on 10mm pitch.
Mounting holes should have appropriate silkscreen marker, and MH1 should have a pin 1 marker in copper on the top side only.

This reference design is a guideline. Please refer to the Jacdac docs online at https://aka.ms/jacdac for the definitive and most up-to-date information.

This design uses an enclosure compatible board shape.

Silkscreen should include text to identify the module type and revision, and optionally a QR code.

Silkscreen & layout notes

Block name

Design notes

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When this PDF is viewed with Adobe Reader, clicking on components shows part numbers and other details.

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SHEET FILENAME JacdacDevRgbEc30 117.SchDoc	LICENCE Attribution 4.0 International (CC BY 4.0)		

Microsoft

PROJECT DESCRIPTION
G0-based single RGB LED/dev board

SHEET DESCRIPTION
Complete design

LAST MODIFIED 13/06/2022	PAGE 1 OF 1	DRAWN BY S. Hodges	REVISION 1.0	PCB ID 117-1.0