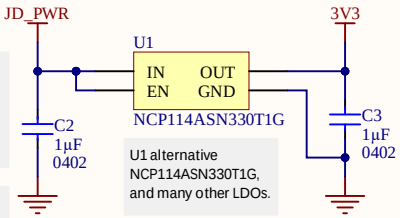
3V3 regulator

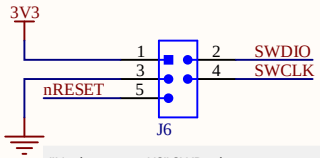


Recommendation: consider replacing NCP114 with an LDO that is robust to repeated spikes of 8V or more on its input in case there is noise on the Jacdac bus.

This component is a power-consumer.

U1 alternative NCP114ASN330T1G, and many other LDOs.

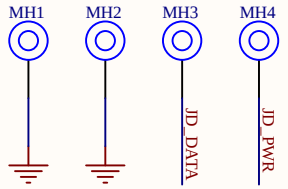
Programming/debug connector



"Hack-connect XS" SWD adapter.

https://arcade.makecode.com/hardware/dbg

Mounting holes

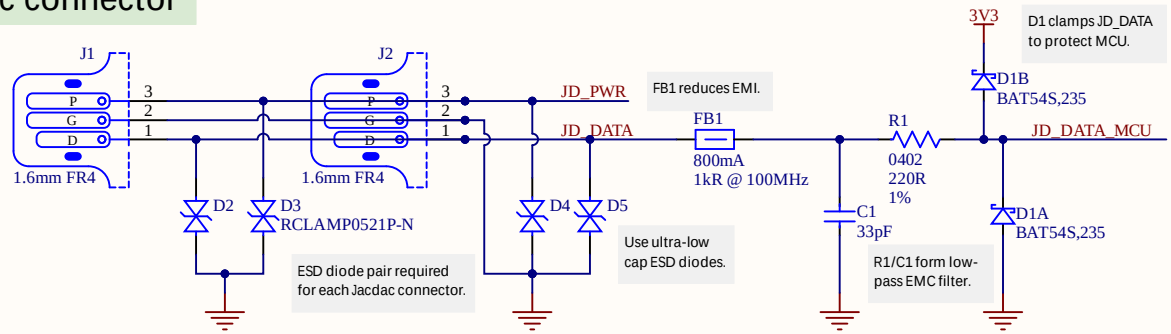


Mounting holes are electrically connected to the Jacdac bus nets so they can be used as an alternative to the PCB edge connector. Please use the following reference designators and net mapping:

MH1 & MH2: GND
MH3: JD_DATA
MH4: JD_PWR

This design uses Jacdac 'small' mounting holes: PTH with finished diameter of 2.1mm, annular copper ring of 3.0mm diameter & copper/component keepout of 5.0mm. The mounting holes must be on 2.5mm pitch. Mounting holes should have appropriate silkscreen marker, and MH1 should have a pin 1 marker on the top side.

Jacdac connector



D1 clamps JD_DATA to protect MCU.

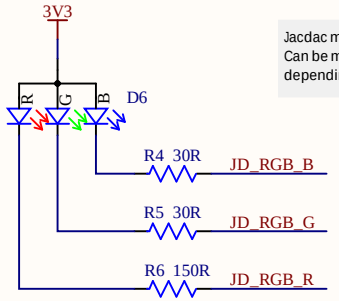
FB1 reduces EMI.

ESD diode pair required for each Jacdac connector.

Use ultra-low cap ESD diodes.

R1/C1 form low-pass EMC filter.

Status LED

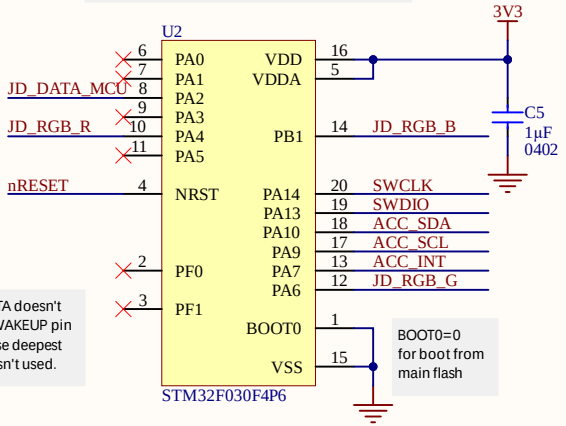


Jacdac modules require a status LED. Can be monochrome or multicolor depending on GPIO availability.

Tuoahan TZ-P4-1615RGBTCA1-0.55T RGB is footrpint-compatible alternative for D6. If using alternative part recalculate R4-R6.

MCU

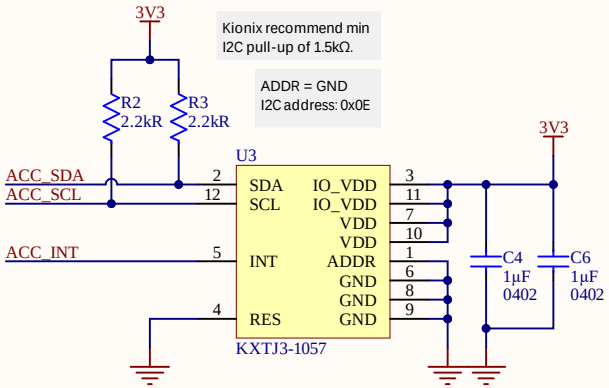
U3 critical pin mappings:
PA2 USART1_TX for JD data
PA4 TIM14_CH1 for RGB_R
PA6 TIM16_CH1 for RGB_G
PB1 TIM3_CH4 for JD_RGB_B
PA10 ACC_SDA
PA9 ACC_SCL



JD_DATA doesn't need WAKEUP pin because deepest sleep isn't used.

BOOT0=0 for boot from main flash

Accelerometer



Kionix recommend min I2C pull-up of 1.5kΩ.

ADDR = GND
I2C address: 0x0E

This reference design is a guideline. Please refer to the Jacdac docs online at https://aka.ms/jacdac for the definitive and most up-to-date information.

Silkscreen should include text to identify the module type and revision, and optionally a QR code.

This design uses a 'cute' board shape.

Silkscreen & layout notes

Block name

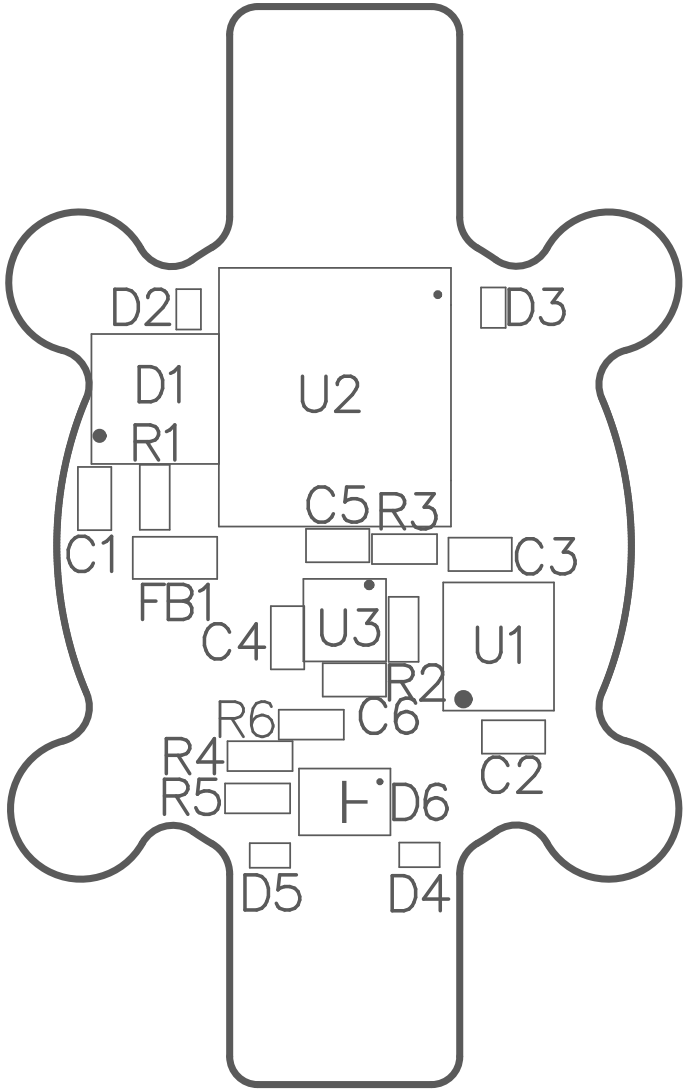
Design notes

This information is provided "as-is". You bear the risk of using it. Some information relates to pre-released specification which may change without notice. Microsoft makes no warranties, express or implied, with respect to the information provided here.

When this PDF is viewed with Adobe Reader, clicking on components shows part numbers and other details.

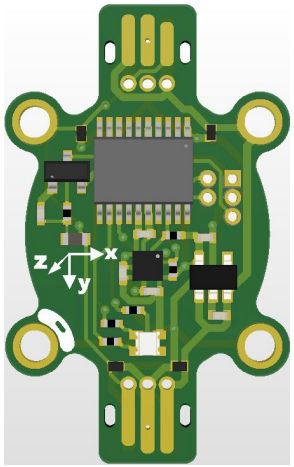
PROJECT FILENAME Jacdac Accelerometer 30.PrjPCB	PROJECT CODENAME Jacdac Accelerometer	Microsoft	PROJECT DESCRIPTION Jacdac accelerometer module / SHEET DESCRIPTION Complete design
SHEET FILENAME Jacdac Accelerometer 30.SchDoc	LICENCE Attribution 4.0 International (CC BY 4.0)	LAST MODIFIED 20/12/2021	PAGE 1 OF 1 / DRAWN BY DG, MM, JD, GD & SH / REVISION 1.1 / PCB ID 30-1.1

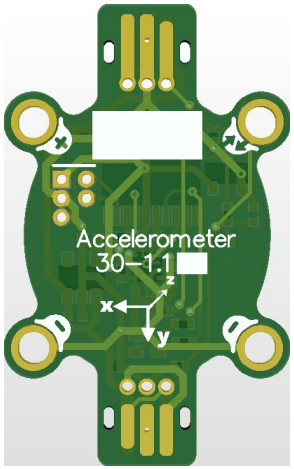
Board Outline
Top Assy



Board Outline

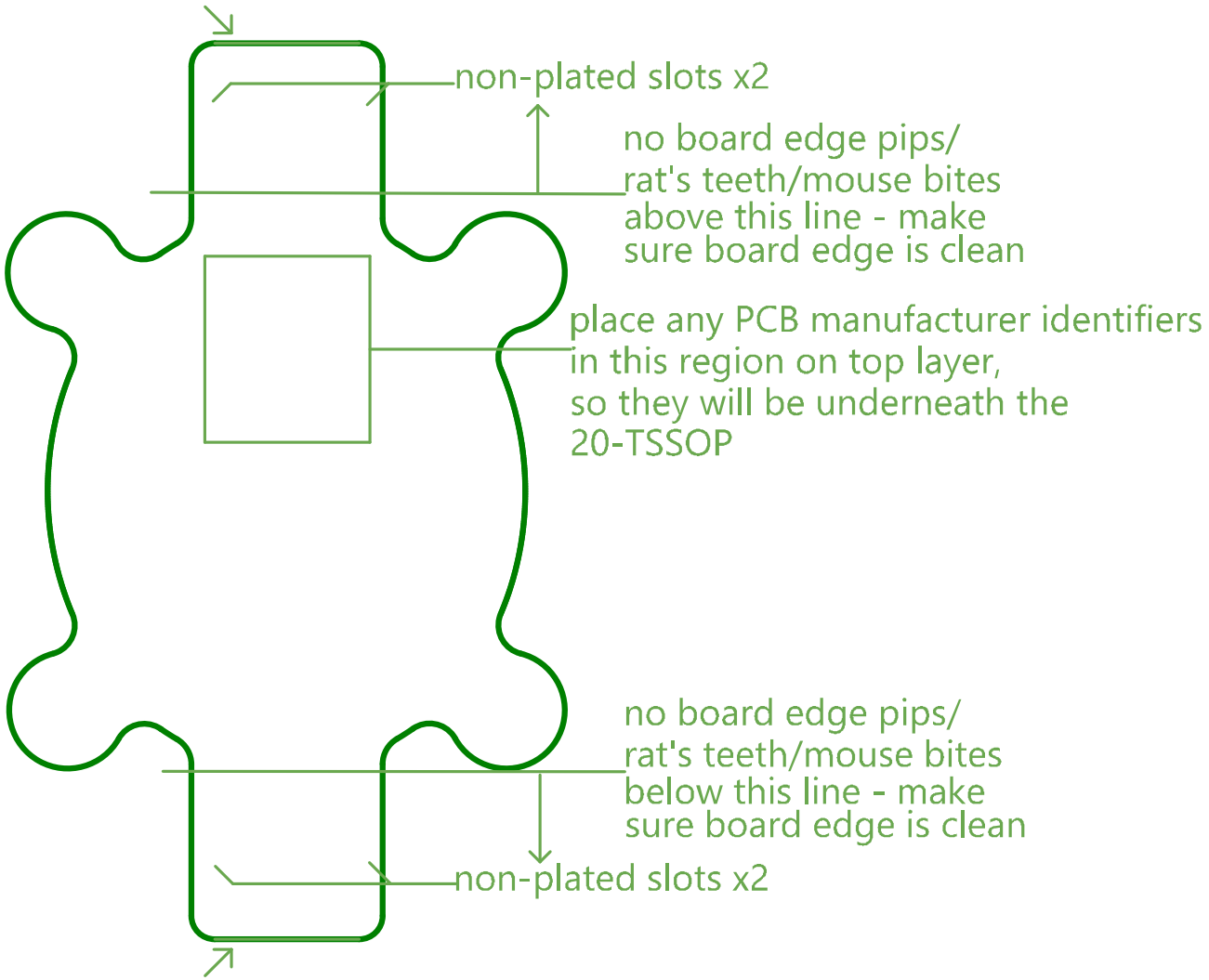
Bottom Assy


z
x
y


Accelerometer
30-1.1
z
x
y

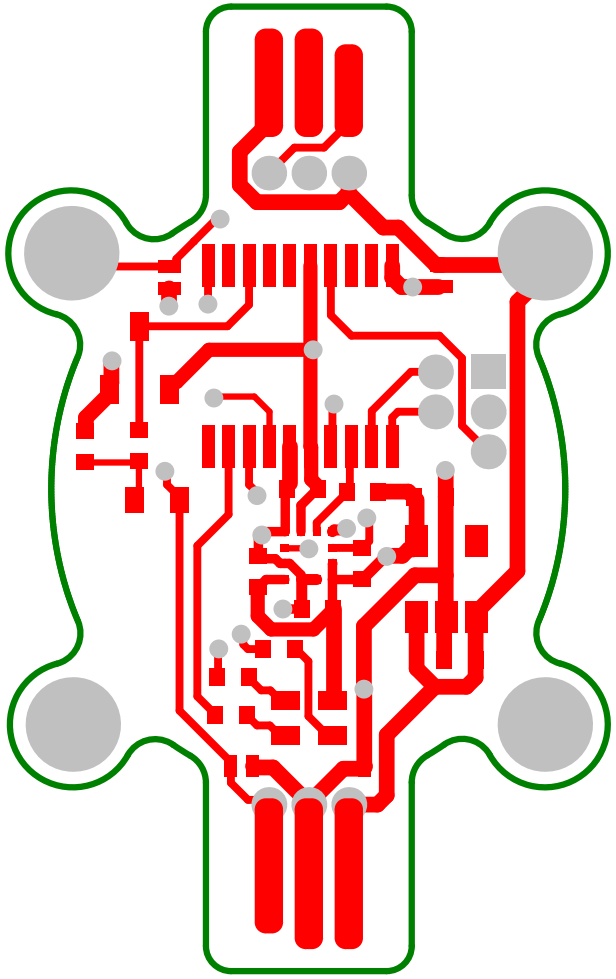
Fabrication Notes

Board Outline



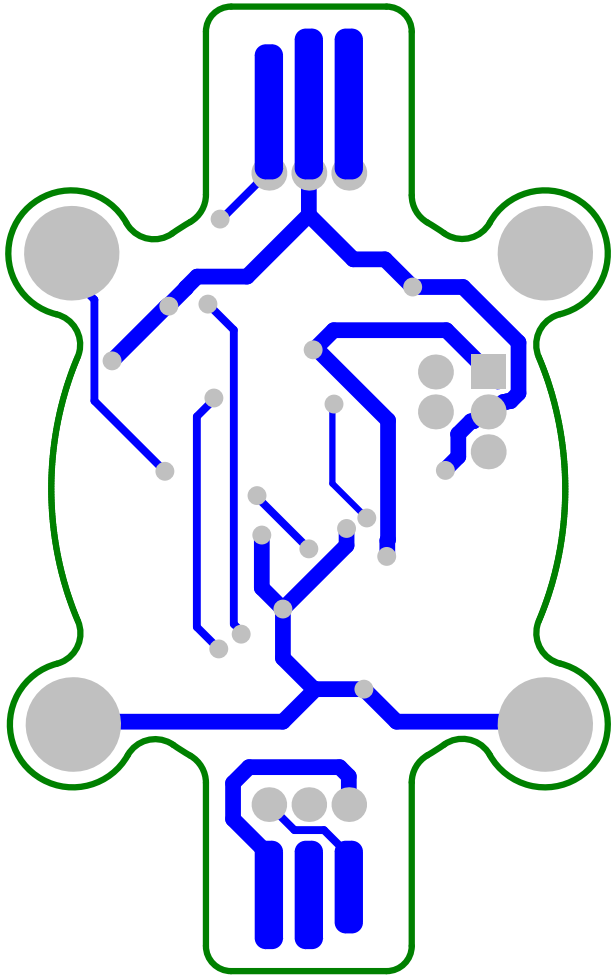
Top Layer

Board Outline



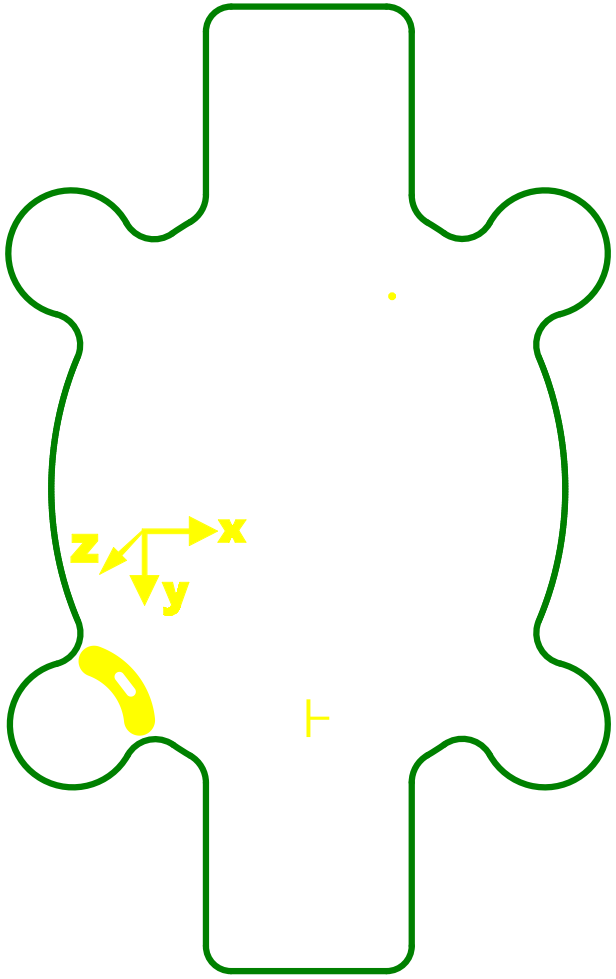
Bottom Layer

Board Outline



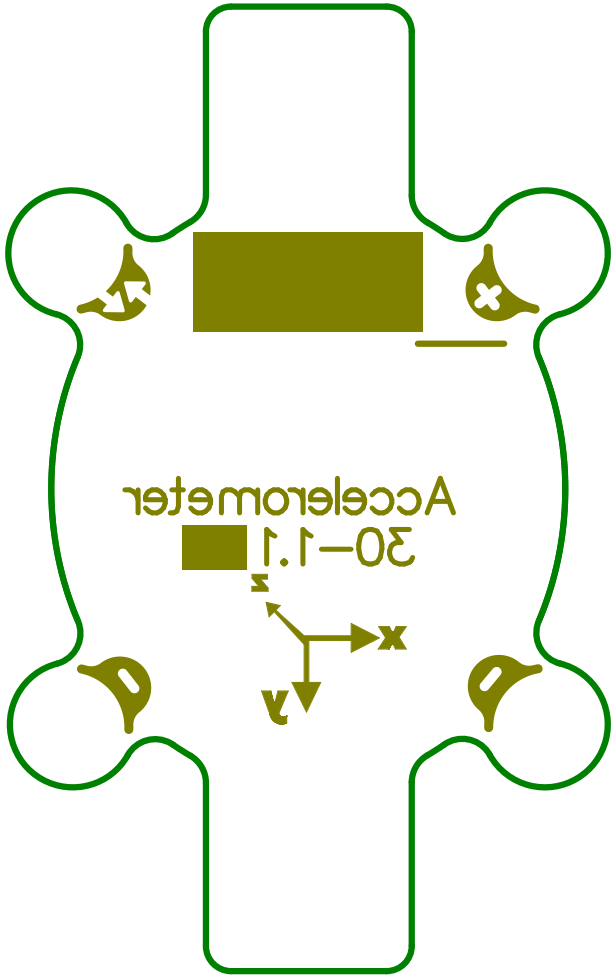
Board Outline

Top Overlay



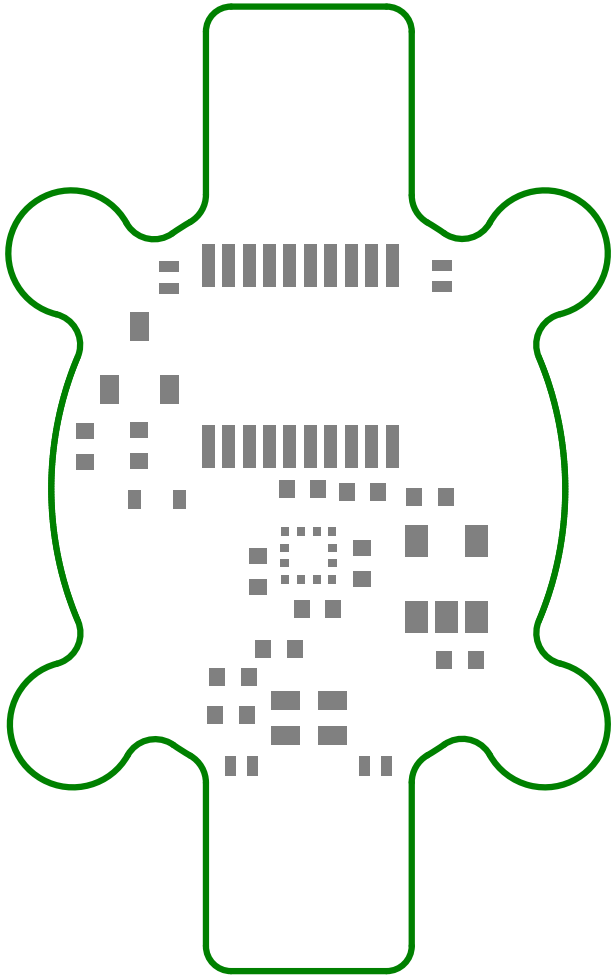
Board Outline

Bottom Overlay



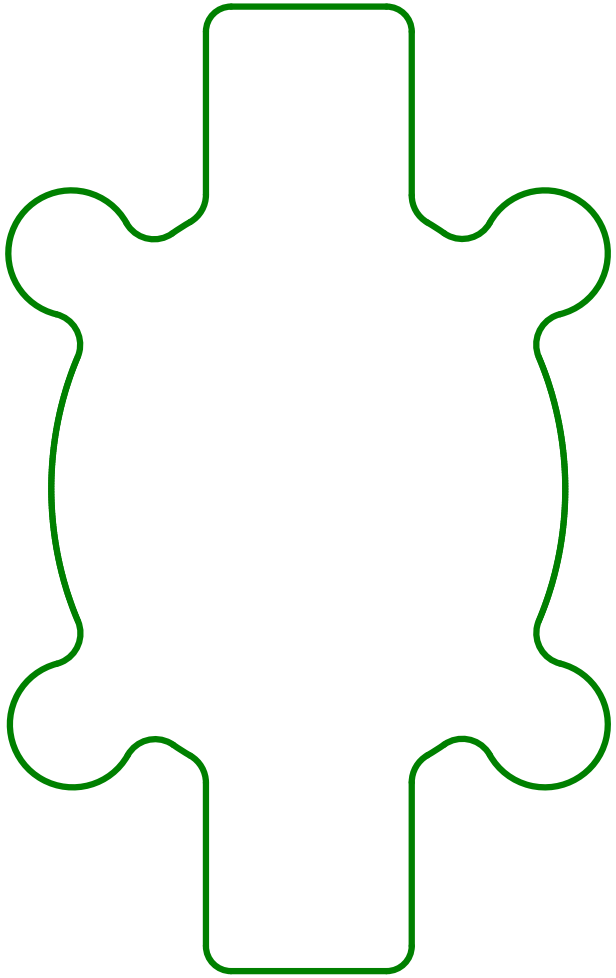
Board Outline

Top Paste



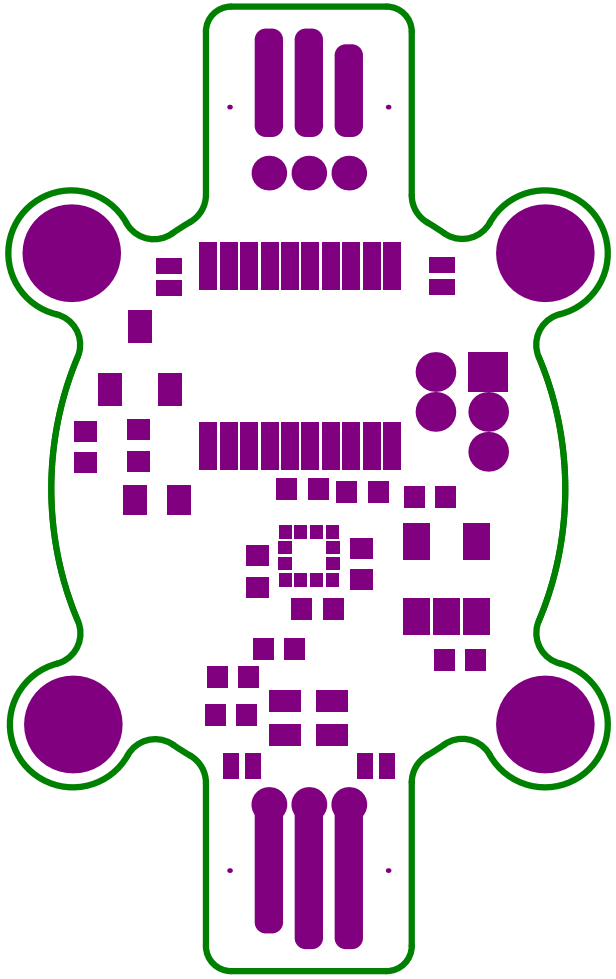
Board Outline

Bottom Paste



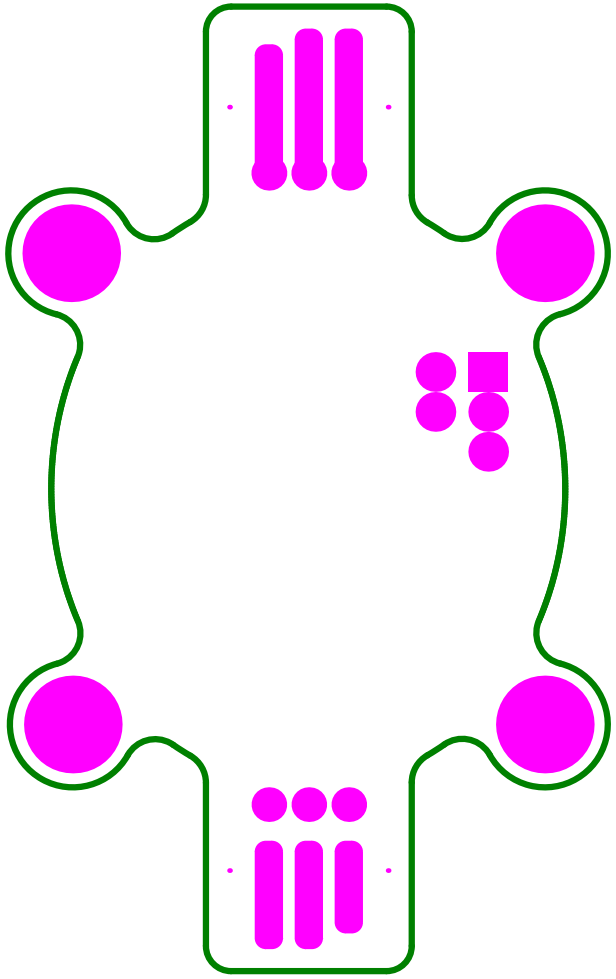
Board Outline

Top Solder (resist)



Board Outline

Bottom Solder (resist)



Board Outline