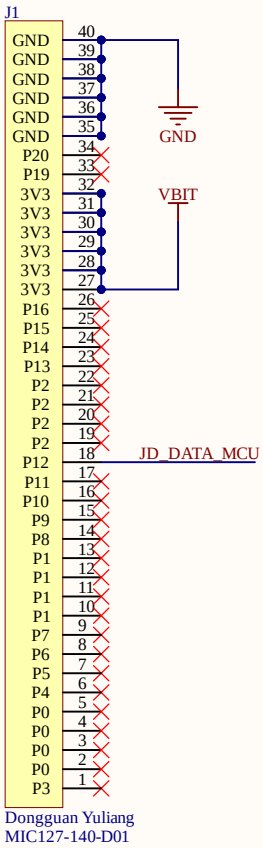
micro:bit connections

190 mA max current draw from micro:bit V2.



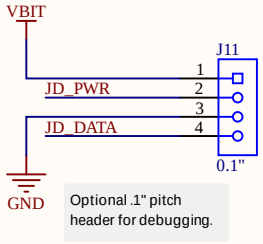
Jacdac interface

Jacdac (https://aka.ms/jacdac) is a new "plug and play" protocol for connecting microcontrollers and peripherals. Its flexibile topology, dynamic discovery and power delivery provide a great user experience for makers and students.

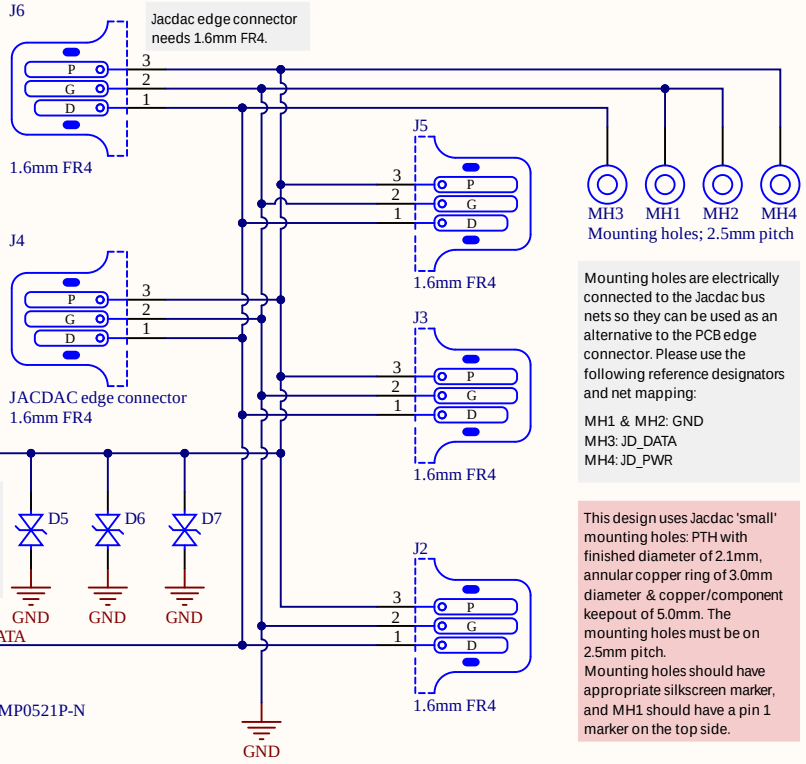
Jacdac provides 1Mbps communications and power delivery. JD_DATA uses 3.3V logic, JD_PWR is nominally 5V.

Please refer to the Jacdac docs online at https://aka.ms/jacdac for the definitive and most up-to-date information.

This component is a low current power provider.



Optional .1" pitch header for debugging.

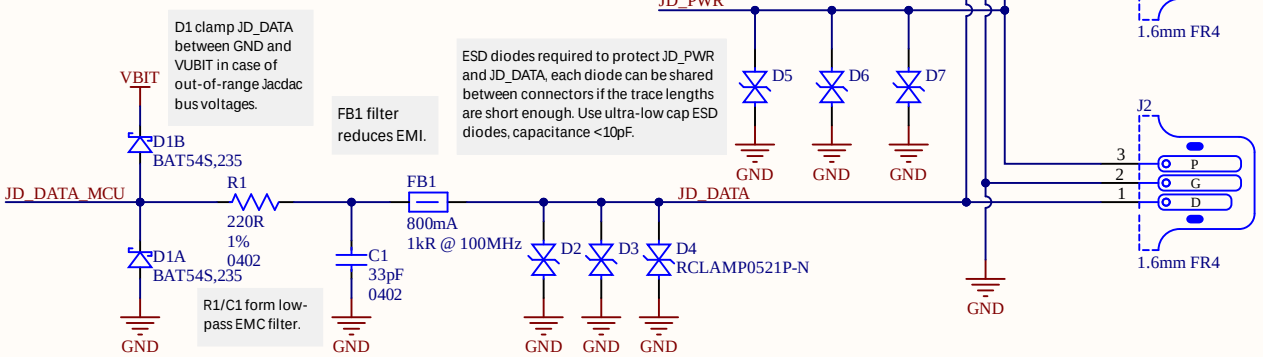


Jacdac edge connector needs 1.6mm FR4.

Mounting holes are electrically connected to the Jacdac bus nets so they can be used as an alternative to the PCB edge connector. Please use the following reference designators and net mapping:

MH1 & MH2: GND
MH3: JD_DATA
MH4: JD_PWR

This design uses Jacdac 'small' mounting holes: PTH with finished diameter of 2.1mm, annular copper ring of 3.0mm diameter & copper/component keepout of 5.0mm. The mounting holes must be on 2.5mm pitch.
Mounting holes should have appropriate silkscreen marker, and MH1 should have a pin 1 marker on the top side.



D1 clamp JD_DATA between GND and VUBIT in case of out-of-range Jacdac bus voltages.

FB1 filter reduces EMI.

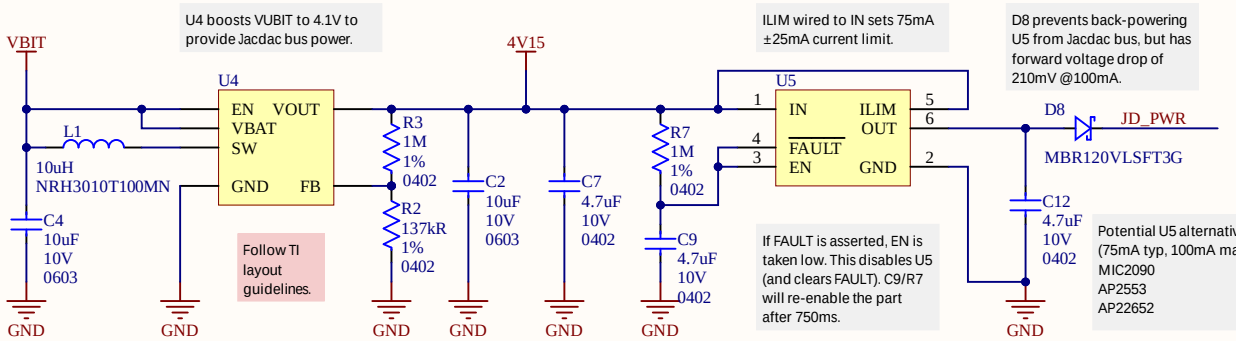
ESD diodes required to protect JD_PWR and JD_DATA, each diode can be shared between connectors if the trace lengths are short enough. Use ultra-low cap ESD diodes, capacitance <10pF.

R1/C1 form low-pass EMC filter.

Jacdac power delivery is optional. Spec requires current limiting with auto retry, and that nothing gets hot! This shield delivers 75mA typical, 100mA max.

Since JD_PWR supplies up to 100mA, ≥3.85V is needed at the connector, resulting in at least 3.7V at each module.Therefore U5 output must be 4.1V. This draws 145mA from 3.3V VUBIT supply.

Check Jacdac spec for information about higher currents and MCU-based 'high current power providers'.



U4 boosts VUBIT to 4.1V to provide Jacdac bus power.

Follow TI layout guidelines.

ILIM wired to IN sets 75mA ±25mA current limit.

If FAULT is asserted, EN is taken low. This disables U5 (and clears FAULT). C9/R7 will re-enable the part after 750ms.

D8 prevents back-powering U5 from Jacdac bus, but has forward voltage drop of 210mV @100mA.

Potential U5 alternatives (75mA typ, 100mA max):
MIC2090
AP2553
AP22652

Key:

Silkscreen & layout notes

Block name

Design notes

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When this PDF is viewed with Adobe Reader, clicking on components shows part numbers and other details.

PROJECT FILENAME JacDacMicroBitShieldLP 29.PrjPCB	PROJECT CODENAME JacdacMicroBitShieldLP	Microsoft	PROJECT DESCRIPTION Jacdac adapter reference design for the BBC micro:bit V2
SHEET FILENAME JacDacMicroBitShieldLP 29.SchDoc	LICENCE Attribution 4.0 International (CC BY 4.0)	LAST MODIFIED 03/12/2021 PAGE 1 OF 2 DRAWN BY JD, SH & DG	SHEET DESCRIPTION complete design REVISION 0.6 PCB ID 29-0.6