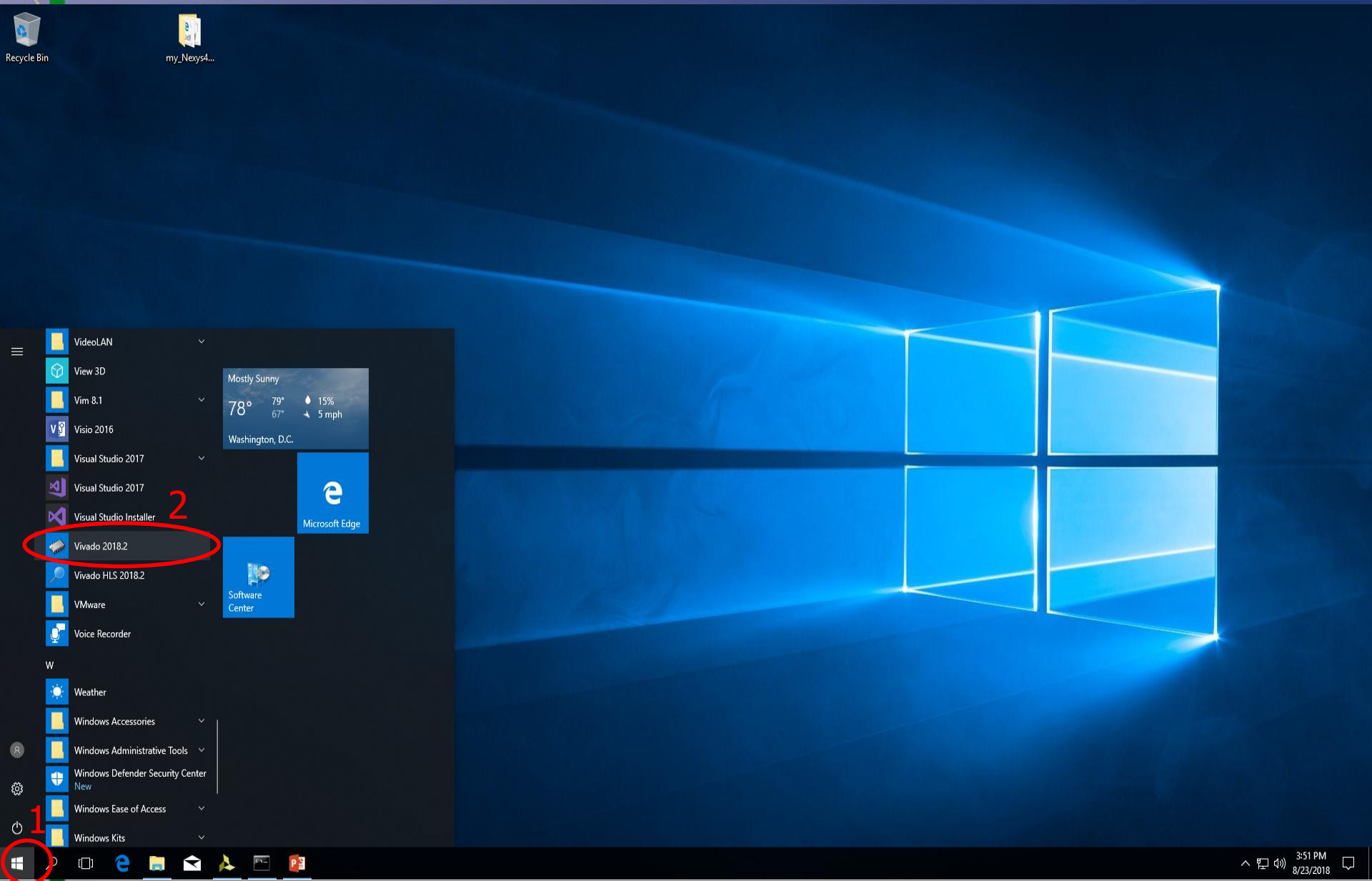


Functional Simulation using Xilinx Vivado 2019.2

- 1) Create a **blank** Vivado **project**
 - Project **name**
 - Project destination **folder**
 - Choose **default** settings
- 2) Add **source files**
 - **Design** file(s)
 - **Simulation** files
 - Testbench
 - Waveform configuration
- 3) Run **behavioral/functional simulation**
 - **Simulation settings**, e.g., simulation time
 - Edit **waveform configuration**, e.g., waveform style (digital, analog), add signals, add dividers, signal radix, etc.



Xilinx Vivado 2019.2 – (1) Create Project



Xilinx Vivado 2019.2 – (1) Create Project

The screenshot displays the Xilinx Vivado 2019.2 software interface. On the left, the 'Quick Start' panel is visible, with the 'Create Project >' option highlighted by a red circle and a red number '1'. The 'Tasks' and 'Learning Center' panels are also visible. In the center, the 'New Project' wizard is open, titled 'Create a New Vivado Project'. The wizard text states: 'This wizard will guide you through the creation of a new project. To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.' At the bottom of the wizard, the 'Next >' button is highlighted by a red circle and a red number '2'. The 'Recent Projects' panel on the right shows a project named 'Single_Cycle/vivado_project'. The 'Tcl Console' at the bottom left contains the command 'start_gui'. The bottom status bar indicates 'New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.'



Xilinx Vivado 2019.2 – (1) Create Project

Vivado 2017.2

File Flow Tools Window Help Quick Access

VIVADO HLx Editions

XILINX ALL PROGRAMMABLE

Quick Start

- Create Project >
- Open Project >
- Open Example Project >

Tasks

- Manage IP >
- Open Hardware Manager >
- Xilinx Tcl Store >

Learning Center

- Documentation and Tutorials >
- Quick Take Videos >
- Release Notes Guide >

Recent Projects

Single_Cycle/vivado_project

New Project

Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

Project name: vivado_project

Project location: C:/Users/e190a104

☒ Create project subdirectory

Project will be created at: C:/Users/e190a104/vivado_project

Choose a directory for project file and associated data files

< Back Next > Finish Cancel

Tcl Console

```
start_gui
```

Type a Tcl command here

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Xilinx Vivado 2019.2 – (1) Create Project

The screenshot displays the Xilinx Vivado 2017.2 software interface. The main window shows the 'Quick Start' panel with links to 'Create Project', 'Open Project', and 'Open Example Project'. The 'Tasks' panel includes 'Manage IP', 'Open Hardware Manager', and 'Xilinx Tcl Store'. The 'Learning Center' panel provides links to 'Documentation and Tutorials', 'Quick Take Videos', and 'Release Notes Guide'. A 'Recent Projects' list on the right shows 'Single_Cycle/vivado_project'. The 'New Project' wizard is active, with the 'Choose Project Location' dialog box open. The dialog shows the 'Project Name' field and the 'Choose Project Location' section. The 'Recent' list shows 'C:/Users/e190a104'. The 'Directory' field shows 'C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter'. The file tree shows the 'n_bit_up_down_counter' folder selected, indicated by a red circle and the number '1'. The 'Select' button is also circled in red and marked with a red circle and the number '2'. The 'Tcl Console' at the bottom shows the command 'start_gui'.

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.



Xilinx Vivado 2019.2 – (1) Create Project

The screenshot shows the Xilinx Vivado 2017.2 interface. The main window has a sidebar with 'Quick Start', 'Tasks', and 'Learning Center' sections. The 'Quick Start' section includes links for 'Create Project', 'Open Project', and 'Open Example Project'. The 'Tasks' section includes links for 'Manage IP', 'Open Hardware Manager', and 'Xilinx Tcl Store'. The 'Learning Center' section includes links for 'Documentation and Tutorials', 'Quick Take Videos', and 'Release Notes Guide'. The main area displays 'Recent Projects' with a list containing 'Single_Cycle/vivado_project'. A 'New Project' dialog box is open in the center. It has a title bar 'New Project' and a close button. The dialog contains the following fields and controls:

- Project Name:** A text field containing 'vivado_project'. It is circled in red with a red '1' above it.
- Project location:** A text field containing 'C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter'. It is circled in red with a red '2' above it.
- Create project subdirectory:** A checkbox that is checked.
- Project will be created at:** A text field containing 'C:/.../HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project'.
- Buttons:** At the bottom, there are four buttons: '< Back', 'Next >', 'Finish', and 'Cancel'. The 'Next >' button is circled in red with a red '3' above it.

The background interface also shows a 'Tcl Console' at the bottom with a search bar and a list of commands including 'start_gui'. The status bar at the very bottom indicates 'New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.' and shows the system clock as 8:17 PM on 8/22/2017.

Xilinx Vivado 2019.2 – (1) Create Project

The screenshot displays the Xilinx Vivado 2019.2 software interface. The top menu bar includes File, Flow, Tools, Window, and Help. The main workspace is divided into several panels: 'Quick Start' on the left with links to 'Create Project', 'Open Project', and 'Open Example Project'; 'Tasks' below it with links to 'Manage IP', 'Open Hardware Manager', and 'Xilinx Tcl Store'; and 'Learning Center' at the bottom left with links to 'Documentation and Tutorials', 'Quick Take Videos', and 'Release Notes Guide'. On the right, the 'Recent Projects' panel shows a project named 'Single_Cycle/vivado_project'. In the center, the 'New Project' dialog box is open, titled 'Project Type'. It prompts the user to 'Specify the type of project to create.' and lists five options: 'RTL Project' (selected), 'Post-synthesis Project', 'I/O Planning Project', 'Imported Project', and 'Example Project'. Each option has a brief description. The 'Next >' button at the bottom of the dialog is circled in red. The 'Tcl Console' at the bottom left shows the command 'start_gui' entered. The bottom status bar indicates 'New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.'

Vivado 2017.2

File Flow Tools Window Help

Quick Access

VIVADO HLx Editions

XILINX ALL PROGRAMMABLE

Quick Start

Create Project >

Open Project >

Open Example Project >

Tasks

Manage IP >

Open Hardware Manager >

Xilinx Tcl Store >

Learning Center

Documentation and Tutorials >

Quick Take Videos >

Release Notes Guide >

Recent Projects

Single_Cycle/vivado_project

New Project

Project Type

Specify the type of project to create.

☒ RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
☐ Do not specify sources at this time

☐ Post-synthesis Project
You will be able to add sources, view device resources, run design analysis, planning and implementation.
☐ Do not specify sources at this time

☐ I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.

☐ Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ Example Project
Create a new Vivado project from a predefined template.

< Back Next > Finish Cancel

Tcl Console

start_gui

Type a Tcl command here

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Xilinx Vivado 2019.2 – (1) Create Project

The screenshot shows the Xilinx Vivado 2017.2 interface. The 'New Project' wizard is open, and the 'Add Sources' step is highlighted with a red circle and the number '1'. The 'Target language' dropdown is set to 'VHDL' and is also circled with a red circle and the number '2'. The 'Next >' button is circled with a red circle and the number '2'.

Quick Start

- Create Project >
- Open Project >
- Open Example Project >

Tasks

- Manage IP >
- Open Hardware Manager >
- Xilinx Tcl Store >

Learning Center

- Documentation and Tutorials >
- Quick Take Videos >
- Release Notes Guide >

Recent Projects

- Single_Cycle/vivado_project

New Project

Add Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

Use Add Files, Add Directories or Create File buttons below

☐ Scan and add RTL include files into project

☐ Copy sources into project

☒ Add sources from Vivado libraries

Target language: **VHDL** Simulator language: Mixed

Tcl Console

```
start_gui
```

Type a Tcl command here

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Xilinx Vivado 2019.2 – (1) Create Project

The screenshot shows the Xilinx Vivado 2017.2 software interface. The top menu bar includes File, Flow, Tools, Window, and Help. The main workspace is divided into several panels: Quick Start (with links to Create Project, Open Project, and Open Example Project), Tasks (with links to Manage IP, Open Hardware Manager, and Xilinx Tcl Store), and Learning Center (with links to Documentation and Tutorials, Quick Take Videos, and Release Notes Guide). A 'Recent Projects' panel on the right shows a project named 'Single_Cycle/vivado_project'. The 'New Project' wizard is open, displaying the 'Add Constraints (optional)' step. The wizard prompts the user to 'Specify or create constraint files for physical and timing constraints.' Below this, there is a large empty box with the text 'Use Add Files or Create File buttons below'. At the bottom of the wizard, there are two buttons: 'Add Files' and 'Create File'. A checkbox labeled 'Copy constraints files into project' is also present. The 'Next >' button is circled in red, indicating the next step in the wizard. The bottom status bar shows the 'New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.'

Xilinx Vivado 2019.2 – (1) Create Project

Vivado 2017.2

File Flow Tools Window Help Quick Access

VIVADO HLx Editions

XILINX ALL PROGRAMMABLE

Quick Start

- Create Project >
- Open Project >
- Open Example Project >

Tasks

- Manage IP >
- Open Hardware Manager >
- Xilinx Tcl Store >

Learning Center

- Documentation and Tutorials >
- Quick Take Videos >
- Release Notes Guide >

Recent Projects

Single_Cycle/vivado_project

New Project

Default Part
Choose a default Xilinx part or board for your project. This can be changed later.

Select: ☒ Parts ☐ Boards

Filter

Product category: All Speed grade: All

Family: All Temp grade: All

Package: All

Reset All Filters

Search: Q

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Gb Transceivers	GTPE2 Transc
xc7vx485tffg1157-2L	1,157	600	303600	607200	1030	0	2800	20	0
xc7vx485tffg1157-1	1,157	600	303600	607200	1030	0	2800	20	0
xc7vx485tffg1158-3	1,158	350	303600	607200	1030	0	2800	48	0
xc7vx485tffg1158-2	1,158	350	303600	607200	1030	0	2800	48	0
xc7vx485tffg1158-2L	1,158	350	303600	607200	1030	0	2800	48	0
xc7vx485tffg1158-1	1,158	350	303600	607200	1030	0	2800	48	0
xc7vx485tffg1761-3	1,761	700	303600	607200	1030	0	2800	28	0

< >

? < Back Next > Finish Cancel

Tcl Console

```
start_gui
```

Type a Tcl command here

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.



Xilinx Vivado 2019.2 – (1) Create Project

The screenshot displays the Xilinx Vivado 2019.2 software interface. The top menu bar includes File, Flow, Tools, Window, and Help. The main workspace is divided into several sections: 'Quick Start' with links to Create Project, Open Project, and Open Example Project; 'Tasks' with links to Manage IP, Open Hardware Manager, and Xilinx Tcl Store; and 'Learning Center' with links to Documentation and Tutorials, Quick Take Videos, and Release Notes Guide. A 'Recent Projects' panel on the right shows a project named 'Single_Cycle/vivado_project'. In the center, the 'New Project' wizard is open, displaying the 'New Project Summary' dialog. The dialog lists the following information: a new RTL project named 'vivado_project' will be created; no source files or directories will be added; no constraints files will be added; and the default part and product family for the new project are: Default Part: xc7vx485tffg1157-1, Product: Virtex-7, Family: Virtex-7, Package: ffg1157, and Speed Grade: -1. At the bottom of the dialog, the 'Finish' button is circled in red, indicating the next step to create the project. The 'Tcl Console' at the bottom left shows the command 'start_gui' entered. The status bar at the bottom indicates the time is 8:29 PM on 8/22/2017.

Vivado 2017.2

File Flow Tools Window Help

Quick Access

VIVADO HLx Editions

XILINX ALL PROGRAMMABLE.

Quick Start

Create Project >

Open Project >

Open Example Project >

Recent Projects

Single_Cycle/vivado_project

Tasks

Manage IP >

Open Hardware Manager >

Xilinx Tcl Store >

Learning Center

Documentation and Tutorials >

Quick Take Videos >

Release Notes Guide >

New Project

VIVADO HLx Editions

XILINX ALL PROGRAMMABLE.

New Project Summary

- A new RTL project named 'vivado_project' will be created.
- No source files or directories will be added. Use Add Sources to add them later.
- No constraints files will be added. Use Add Sources to add them later.
- The default part and product family for the new project:
Default Part: xc7vx485tffg1157-1
Product: Virtex-7
Family: Virtex-7
Package: ffg1157
Speed Grade: -1

To create the project, click Finish

< Back Next > Finish Cancel

Tcl Console

```
start_gui
```

Type a Tcl command here

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Type here to search

8:29 PM 8/22/2017

Xilinx Vivado 2019.2 – (2) Add Sources

vivado_project - [C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project/vivado_project.xpr] - Vivado 2019.2

File Edit Flow Tools Window Layout View Help Quick Access

Flow Navigator PROJECT MANAGER - vivado_project

PROJECT MANAGER 1

- Settings
- Add Sources**
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Sources

- Design Sources
- Constraints
- Simulation Sources
 - sim_1

Project Summary

Settings Edit

Project name: vivado_project

Project location: C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project

Product family: Virtex-7

Project part: xc7vx485tffg1157-1

Add Sources

This guides you through the process of adding and creating sources for your project

- ☐ Add or create constraints
- ☒ **Add or create design sources** 2
- ☐ Add or create simulation sources

3

< Back **Next >** Finish Cancel

Not started

No errors or warnings

xc7vx485tffg1157-1

Vivado Implementation Defaults

File: None

Run Implementation to see timing results

Run Implementation to see power results

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed	Strategy	Part	Description
▼ ▷ synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2017)	xc7vx485tffg1157-1	Vivado Synthesis Defaults
▷ impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2017)	xc7vx485tffg1157-1	Default settings for Imple

Specify and/or create source files to add to the project

Type here to search

8:32 PM 8/22/2017

Xilinx Vivado 2019.2 – (2) Add Sources

vivado_project - [C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project/vivado_project.xpr] - Vivado 2019.2

File Edit Flow Tools Window Layout View Help Quick Access

Flow Navigator PROJECT MANAGER - vivado_project

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Sources

- Design Sources
- Constraints
- Simulation Sources
 - sim_1

Project Summary

Settings Edit

Project name: vivado_project
Project location: C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project
Product family: Virtex-7
Project part: xc7vx485tffg1157-1

Add Sources

Add or Create Design Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.

Use Add Files, Add Directories or Create File buttons below

Add Files Add Directories Create File

☐ Scan and add RTL include files into project
☐ Copy sources into project
☒ Add sources from subdirectories

< Back Next > Finish Cancel

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	Strategy	Part	Description
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2017)	xc7vx485tffg1157-1	Vivado Synthesis Defaults
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2017)	xc7vx485tffg1157-1	Default settings for Imple

Specify and/or create source files to add to the project

Type here to search

8:37 PM 8/22/2017

Xilinx Vivado 2019.2 – (2) Add Sources

vivado_project - [C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project/vivado_project.xpr] - Vivado 2019.2

File Edit Flow Tools Window Layout View Help Quick Access

Flow Navigator PROJECT MANAGER - vivado_project

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Sources

- Design Sources
- Constraints
- Simulation Sources
 - sim_1

Project Summary

Settings Edit

Project name: vivado_project

Project location: C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project

Product family: Virtex-7

Project part: xc7vx485tffg1157-1

Add Sources

Add Source Directories

Recent: C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_d...

Directory: C:\Users\190a104\Desktop\HW01_VSim_Tutorial_EI-Araby\n_bit_up_down_counter\design_sources

Public

a347f353

a687u420

b359p792

d679d929

e190a104

Xilinx

Contacts

Desktop

HW01_VSim_Tutorial_EI-Araby

n_bit_up_down_counter

design_sources

Simulation Sources

vivado_project

Documents

Downloads

Favorites

Links

Music

OneDrive

Select

Cancel

Not started

No errors or warnings

xc7vx485tffg1157-1

Vivado Implementation Defaults

File: None

Run Implementation to see timing results

Run Implementation to see power results

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed	Strategy	Part	Description
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2017)	xc7vx485tffg1157-1	Vivado Synthesis Defaults
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2017)	xc7vx485tffg1157-1	Default settings for Implem

Specify and/or create source files to add to the project

Xilinx Vivado 2019.2 – (2) Add Sources

vivado_project - [C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project/vivado_project.xpr] - Vivado 2019.2

File Edit Flow Tools Window Layout View Help Quick Access

Flow Navigator PROJECT MANAGER - vivado_project

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Sources

- Design Sources
- Constraints
- Simulation Sources
 - sim_1

Project Summary

Settings Edit

Project name: vivado_project
Project location: C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project
Product family: Virtex-7
Project part: xc7vx485tffg1157-1

Add Sources

Add or Create Design Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.

Index	Name	Library	Location
1	design_sources	xil_defaultlib	C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter

☐ Scan and add RTL include files into project
☐ Copy sources into project
☒ Add sources from subdirectories

1

< Back Next > Finish Cancel

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed	Strategy	Part	Description
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2017)	xc7vx485tffg1157-1	Vivado Synthesis Defaults
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2017)	xc7vx485tffg1157-1	Default settings for Imple

Specify and/or create source files to add to the project

Type here to search

8:43 PM 8/22/2017

Xilinx Vivado 2019.2 – (2) Add Sources

vivado_project - [C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project/vivado_project.xpr] - Vivado 2019.2

File Edit Flow Tools Window Layout View Help Quick Access

Flow Navigator PROJECT MANAGER - vivado_project

PROJECT MANAGER 1

- Settings
- Add Sources**
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Sources

- Design Sources (1)
 - n_bit_up_down_counter(behavioral) (n_bit_up_down_counter)
- Constraints
- Simulation Sources (1)
 - sim_1 (1)

Project Summary

Settings Edit

Project name: vivado_project
Project location: C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project
Product family: Virtex-7
Project part: xc7vx485tffg1157-1

Add Sources

This guides you through the process of adding and creating sources for your project

- ☐ Add or create constraints
- ☐ Add or create design sources
- ☒ Add or create simulation sources 2

3

< Back Next > Finish Cancel

Not started
No errors or warnings
xc7vx485tffg1157-1
Vivado Implementation Defaults
File: None

Run Implementation to see timing results

Run Implementation to see power results

Tcl Console Messages Log Reports Design Runs x

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed	Strategy	Part	Description
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2017)	xc7vx485tffg1157-1	Vivado Synthesis Defaults
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2017)	xc7vx485tffg1157-1	Default settings for Implem

Xilinx Vivado 2019.2 – (2) Add Sources

vivado_project - [C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project/vivado_project.xpr] - Vivado 2019.2

File Edit Flow Tools Window Layout View Help Quick Access

Flow Navigator PROJECT MANAGER - vivado_project

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Sources

- Design Sources (1)
 - n_bit_up_down_counter(behavioral) (n_bit_up_down_co
- Constraints
- Simulation Sources (1)
 - sim_1 (1)

Project Summary

Settings Edit

Project name: vivado_project
Project location: C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project
Product family: Virtex-7
Project part: xc7vx485tffg1157-1

Add Sources

Add or Create Simulation Sources

Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.

Specify simulation set: sim_1

Use Add Files, Add Directories or Create File buttons below

Add Files Add Directories Create File

☐ Scan and add RTL include files into project
☐ Copy sources into project
☒ Add sources from subdirectories
☒ Include all design sources for simulation

? < Back Next > Finish Cancel

Properties

Select an object to see properties

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed	Strategy	Part	Description
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2017)	xc7vx485tffg1157-1	Vivado Synthesis Defaults
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2017)	xc7vx485tffg1157-1	Default settings for Imple

Specify and/or create source files to add to the project

Type here to search

8:49 PM 8/22/2017

Xilinx Vivado 2019.2 – (2) Add Sources

vivado_project - [C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project/vivado_project.xpr] - Vivado 2019.2

File Edit Flow Tools Window Layout View Help Quick Access

Flow Navigator PROJECT MANAGER - vivado_project

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Sources

- Design Sources (1)
 - n_bit_up_down_counter(behavioral) (n_bit_up_down_counter.vhd)
- Constraints
- Simulation Sources (1)

Project Summary

Settings Edit

Project name: vivado_project

Project location: C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project

Product family: Virtex-7

Add Source Files

Look in: simulation_sources 1

OSDISK (C:)

Users

e190a104

Desktop

HW01_VSim_Tutorial_EI-Araby

n_bit_up_down_counter

simulation_sources 2

USB Drive (D:)

File name: "n_bit_up_down_counter_tb.vhd" "n_bit_up_down_counter_wave.wcfg"

Files of type: Design Source Files (.vhd, .vhdl, .vhf, .vhdp, .vho, .v, .verilog, .vr, .vg, .vb, .tf, .vlog, .vp, .vm, .veo, .svo, .vh, .h, .svh, .vhp, .svhp, .edn, .edf, .edif, .ngc, .nc, .svp, .bmm, .mif, .mem, .elf, .dcp, .bd, .wcfg)

OK Cancel

```
END n_bit_up_down_counter_tb;

ARCHITECTURE Behavioral OF n_bit_up_down_counter_tb IS

    -- Component Declaration for the Unit Under Test (UUT)
    COMPONENT n_bit_up_down_counter
        GENERIC (n_bits : NATURAL := 8);
        PORT (up_down : IN STD_LOGIC; -- direction of
              clk, rst : IN STD_LOGIC;
              count : OUT STD_LOGIC_VECTOR(n_bits-1 downto 0));
    END COMPONENT;

    -- Clock period definitions
    constant clk_period : time := 10 ns;
```

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed	Strategy	Part	Description
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2017)	xc7vx485tffg1157-1	Vivado Synthesis Defaults
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2017)	xc7vx485tffg1157-1	Default settings for Implementation

Specify and/or create source files to add to the project

Xilinx Vivado 2019.2 – (2) Add Sources

vivado_project - [C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project/vivado_project.xpr] - Vivado 2017.2

File Edit Flow Tools Window Layout View Help Quick Access

Flow Navigator PROJECT MANAGER - vivado_project

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Sources

- Design Sources (1)
 - n_bit_up_down_counter(behavioral) (n_bit_up_down_co
- Constraints
- Simulation Sources (1)

Project Summary

Settings Edit

Project name: vivado_project

Project location: C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project

Product family: Virtex-7

Add Source Files

Look in: simulation_sources

n_bit_up_down_counter_tb.vhd 1

n_bit_up_down_counter_wave.wcfg

Recent Directories

C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n...

File Preview

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY n_bit_up_down_counter_tb IS
END n_bit_up_down_counter_tb;

ARCHITECTURE Behavioral OF n_bit_up_down_counter_tb IS

    -- Component Declaration for the Unit Under Test (UUT)
    COMPONENT n_bit_up_down_counter
        GENERIC (n_bits : NATURAL := 8);
        PORT (up_down : IN STD_LOGIC; -- direction of
              clk, rst : IN STD_LOGIC;
              count : OUT STD_LOGIC_VECTOR(n_bits-1 d
              );
    END COMPONENT;

    -- Clock period definitions
```

File name: "n_bit_up_down_counter_tb.vhd" "n_bit_up_down_counter_wave.wcfg"

Files of type: Design Source Files (.vhd, vhdl, vhf, vhdp, vho, v, vf, verillog, vr, vg, vb, tf, vlog, vp, vm, veo, svo, vh, h, svh, vhp, svhp, edn, edf, edif, ngc, sv, svp, bmm, mif, mem, elf, dcp, bd, wcfg)

OK 2 Cancel

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed	Strategy	Part	Description
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2017)	xc7vx485tffg1157-1	Vivado Synthesis Defaults
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2017)	xc7vx485tffg1157-1	Default settings for Imple

Specify and/or create source files to add to the project

Type here to search

8:52 PM 8/22/2017

Xilinx Vivado 2019.2 – (2) Add Sources

vivado_project - [C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project/vivado_project.xpr] - Vivado 2017.2

File Edit Flow Tools Window Layout View Help Quick Access

Flow Navigator PROJECT MANAGER - vivado_project

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Sources

- Design Sources (1)
 - n_bit_up_down_counter (behavioral) (n_bit_up_down_counter)
- Constraints
- Simulation Sources (1)
 - sim_1 (1)

Project Summary

Settings Edit

Project name: vivado_project

Project location: C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project

Product family: Virtex-7

Project part: xc7vx485tffg1157-1

Add Sources

Add or Create Simulation Sources

Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.

Specify simulation set: sim_1

Index	Name	Library	Location
1	n_bit_up_down_counter_tb.vhd	xil_defaultlib	C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/simulation_sources
2	n_bit_up_down_counter_wave.wcfg	N/A	C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/simulation_sources

Add Files Add Directories Create File

☐ Scan and add RTL include files into project

☐ Copy sources into project

☒ Add sources from subdirectories

☒ Include all design sources for simulation

1

< Back Next > Finish Cancel

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed	Strategy	Part	Description
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2017)	xc7vx485tffg1157-1	Vivado Synthesis Defaults
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2017)	xc7vx485tffg1157-1	Default settings for Imple

Specify and/or create source files to add to the project

Type here to search

9:01 PM 8/22/2017

Xilinx Vivado 2019.2 – (2) Add Sources

vivado_project - [C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project/vivado_project.xpr] - Vivado 2019.2

File Edit Flow Tools Window Layout View Help Quick Access

Flow Navigator PROJECT MANAGER - vivado_project

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Sources

- Design Sources (1)
 - n_bit_up_down_counter(behavioral) (n_bit_up_down_counter)
- Constraints
- Simulation Sources (2)
 - sim_1 (2)
 - n_bit_up_down_counter_tb(behavioral) (n_bit_up_down_counter)
 - uut: n_bit_up_down_counter(behavioral) (n_bit_up_down_counter)
 - Waveform Configuration File (1)
 - n_bit_up_down_counter_wave.wcfg

Project Summary

Settings Edit

Project name: vivado_project
Project location: C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project
Product family: Virtex-7
Project part: xc7vx485tffg1157-1
Top module name: n_bit_up_down_counter
Target language: VHDL
Simulator language: Mixed

Synthesis

Status: Not started
Messages: No errors or warnings
Part: xc7vx485tffg1157-1
Strategy: Vivado Synthesis Defaults

Implementation

Status: Not started
Messages: No errors or warnings
Part: xc7vx485tffg1157-1
Strategy: Vivado Implementation Defaults
Incremental compile: None

DRC Violations

Run Implementation to see DRC results

Timing

Run Implementation to see timing results

Utilization

Run Synthesis to see utilization results

Power

Run Implementation to see power results

Properties

Select an object to see properties

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed	Strategy	Part	Description
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2017)	xc7vx485tffg1157-1	Vivado Synthesis Defaults
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2017)	xc7vx485tffg1157-1	Default settings for Implem



Xilinx Vivado 2019.2 – (2) Add Sources

vivado_project - [C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project/vivado_project.xpr] - Vivado 2019.2

File Edit Flow Tools Window Layout View Help Quick Access

Flow Navigator PROJECT MANAGER - vivado_project

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Sources

- Design Sources (1)
 - n_bit_up_down_counter(behavioral)(n_bit_up_down_co**
- Constraints
- Simulation Sources (2)
 - sim_1 (2)
 - n_bit_up_down_counter_tb(Behavioral)(n_bit_up_d
 - uut: n_bit_up_down_counter(behavioral)(n_bit_up
 - Waveform Configuration File (1)
 - n_bit_up_down_counter_wave.wcfg

Source File Properties

n_bit_up_down_counter.vhd

- ☒ Enabled
- Location: C:/Users/e190a104/Desktop/HW01_VSim_Tutor
- Type: VHDL
- Library: xil_defaultlib
- Size: 0.6 KB
- Modified: Wednesday 08/24/16 10:14:27 PM
- Read-only: No
- Encrypted: No

Project Summary

n_bit_up_down_counter.vhd

C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/design_sources/n_bit_up_down_counter.vhd

```
1 LIBRARY ieee;
2 USE ieee.std_logic_1164.all;
3 USE ieee.std_logic_signed.all;
4
5 ENTITY n_bit_up_down_counter IS
6     GENERIC (n_bits : NATURAL := 8);
7     PORT (up_down : IN STD_LOGIC; -- direction of count, 1 --> counting up, 0 --> counting down
8           clk, rst : IN STD_LOGIC;
9           count : OUT STD_LOGIC_VECTOR(n_bits-1 downto 0)
10        );
11 END n_bit_up_down_counter;
12
13 ARCHITECTURE behavioral OF n_bit_up_down_counter IS
14
15     -- Architecture declarations
16
17
18     -- Internal signal declarations
19
20
21 BEGIN
22
23     -- insert your design here --
24
25     -----
26
27 END behavioral;
```

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed	Strategy	Part	Description
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2017)	xc7vx485tffg1157-1	Vivado Synthesis Defaults
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2017)	xc7vx485tffg1157-1	Default settings for Imple

13:0 Insert VHDL 9:08 PM 8/22/2017

Xilinx Vivado 2019.2 – (2) Add Sources

vivado_project - [C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project/vivado_project.xpr] - Vivado 2019.2

File Edit Flow Tools Window Layout View Help Quick Access

Flow Navigator PROJECT MANAGER - vivado_project

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Sources

- Design Sources (1)
 - n_bit_up_down_counter(behavioral) (n_bit_up_down_counter.vhd)
- Constraints
- Simulation Sources (2)
 - sim_1(0)
 - n_bit_up_down_counter_tb(Behavioral) (n_bit_up_down_counter_tb.vhd)**
 - Waveform Configuration File (1)
 - n_bit_up_down_counter_wave.wcfg

Source File Properties

n_bit_up_down_counter_tb.vhd

- Enabled
- Location: C:/Users/e190a104/Desktop/HW01_VSim_Tutorial
- Type: VHDL
- Library: xil_defaultlib
- Size: 1.6 KB
- Modified: Wednesday 08/24/16 09:34:05 PM
- Read-only: No
- Encrypted: No

Project Summary

n_bit_up_down_counter.vhd n_bit_up_down_counter_tb.vhd

C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/simulation_sources/n_bit_up_down_counter_tb.vhd

```
1 LIBRARY ieee;
2 USE ieee.std_logic_1164.ALL;
3
4 ENTITY n_bit_up_down_counter_tb IS
5 END n_bit_up_down_counter_tb;
6
7 ARCHITECTURE Behavioral OF n_bit_up_down_counter_tb IS
8
9 -- Component Declaration for the Unit Under Test (UUT)
10 COMPONENT n_bit_up_down_counter
11   GENERIC (n_bits : NATURAL := 8);
12   PORT (up_down : IN STD_LOGIC; -- direction of count, 1 --> counting up, 0 --> counting down
13         clk, rst : IN STD_LOGIC;
14         count : OUT STD_LOGIC_VECTOR(n_bits-1 downto 0)
15       );
16 END COMPONENT;
17
18 -- Clock period definitions
19 CONSTANT n_bits : NATURAL := 5;
20 CONSTANT clk_period : time := 10 ns;
21
22 --Inputs
23 SIGNAL up_down : STD_LOGIC := '1';
24 SIGNAL clk : STD_LOGIC := '0';
25 SIGNAL rst : STD_LOGIC := '0';
26
27 --Outputs
28 SIGNAL count : STD_LOGIC_VECTOR(n_bits-1 downto 0);
29
30 BEGIN
31
32 -- Instantiate the Unit Under Test (UUT)
33 uut : n_bit_up_down_counter
34   GENERIC MAP (n_bits => n_bits)
35   PORT MAP (up_down => up_down,
36            clk => clk,
37            rst => rst,
```

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed	Strategy	Part	Description
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2017)	xc7vx485tffg1157-1	Vivado Synthesis Defaults
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2017)	xc7vx485tffg1157-1	Default settings for Implem

7.0 Insert VHDL 9:12 PM 8/22/2017

Xilinx Vivado 2019.2 – (3) Run Behavioral Simulation

vivado_project - [C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project/vivado_project.xpr] - Vivado 2017.2

1. **Flow** 2. **Settings** 3. **Simulation Settings...**

Source File Properties

n_bit_up_down_counter_tb.vhd

☒ Enabled

Location: C:/Users/e190a104/Desktop/HW01_VSim_Tutorial

Type: VHDL

Library: xil_defaultlib

Size: 1.6 KB

Modified: Wednesday 08/24/16 09:34:05 PM

Read-only: No

Encrypted: No

General Properties

Simulation Settings

Simulation

Simulation Settings

Simulation Settings

```
1 LIBRARY ieee;
2 USE ieee.std_logic_1164.ALL;
3
4 ENTITY n_bit_up_down_counter_tb IS
5 END n_bit_up_down_counter_tb;
6
7 ARCHITECTURE Behavioral OF n_bit_up_down_counter_tb IS
8
9 -- Component Declaration for the Unit Under Test (UUT)
10 COMPONENT n_bit_up_down_counter
11   GENERIC (n_bits : NATURAL := 8);
12   PORT (up_down : IN STD_LOGIC; -- direction of count, 1 --> counting up, 0 --> counting down
13         clk, rst : IN STD_LOGIC;
14         count : OUT STD_LOGIC_VECTOR(n_bits-1 downto 0)
15       );
16 END COMPONENT;
17
18 -- Clock period definitions
19 CONSTANT n_bits : NATURAL := 5;
20 CONSTANT clk_period : time := 10 ns;
21
22 --Inputs
23 SIGNAL up_down : STD_LOGIC := '1';
24 SIGNAL clk : STD_LOGIC := '0';
25 SIGNAL rst : STD_LOGIC := '0';
26
27 --Outputs
28 SIGNAL count : STD_LOGIC_VECTOR(n_bits-1 downto 0);
29
30 BEGIN
31
32 -- Instantiate the Unit Under Test (UUT)
33 uut : n_bit_up_down_counter
34   GENERIC MAP (n_bits => n_bits)
35   PORT MAP (up_down => up_down,
36            clk => clk,
37            rst => rst,
```

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed	Strategy	Part	Description
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2017)	xc7vx485tffg1157-1	Vivado Synthesis Defaults
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2017)	xc7vx485tffg1157-1	Default settings for Implem

Open simulation settings to change options



Xilinx Vivado 2019.2 – (3) Run Behavioral Simulation

vivado_project - [C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project/vivado_project.xpr] - Vivado 2017.2

File Edit Flow Tools Window Layout View Help Quick Access

Flow Navigator PROJECT MANAGER - vivado_project

PROJECT MANAGER

- Settings
- Add Sources
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- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
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- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG
 - Generate Bitstream
 - Open Hardware Manager

Sources

- Design Sources (1)
 - n_bit_up_down_counter (behavioral) (n_bit_up_down_co
- Constraints
- Simulation Sources (2)
 - sim_1 (2)
 - n_bit_up_down_counter_tb (Beha
 - Waveform Configuration File (1)
 - n_bit_up_down_counter_wave.v

Hierarchy Libraries Compile Order

Source File Properties

n_bit_up_down_counter_tb.vhd

Enabled

Location: C:/Users/e190a104/Desktop/H

Type: VHDL

Library: xil_defaultlib

Size: 1.6 KB

Modified: Wednesday 08/24/16 09:34:05

Read-only: No

Encrypted: No

General Properties

Tcl Console Messages Log Reports

Project Summary

n_bit_up_down_counter.vhd

n_bit_up_down_counter_tb.vhd

C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/simulation_sources/n_bit_up_down_counter_tb.vhd

```
1: LIBRARY ieee;  
2: USE ieee.std_logic_1164.ALL;
```

Settings

Simulation

Specify various settings associated to Simulation

Target simulator: Vivado Simulator

Simulator language: Mixed

Simulation set: sim_1

Simulation top module name: n_bit_up_down_counter_tb

☒ Clean up simulation files

Compilation Elaboration **Simulation** Netlist Advanced

xsim.simulate.tcl.post

xsim.simulate.runtime 1000ns

xsim.simulate.log_all_signals ☒

xsim.simulate.custom_tcl

xsim.simulate.wdb

xsim.simulate.saif_scope

xsim.simulate.runtime

Specify simulation run time

OK Cancel Apply Restore...

Tcl Console Messages Log Reports

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	Strategy	Part	Description
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2017)	xc7vx485tfg1157-1	Vivado Synthesis Defaults
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2017)	xc7vx485tfg1157-1	Default settings for Imple

Xilinx Vivado 2019.2 – (3) Run Behavioral Simulation

vivado_project - [C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project/vivado_project.xpr] - Vivado 2019.2

File Edit Flow Tools Window Layout View Help Quick Access

Flow Navigator PROJECT MANAGER - vivado_project

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation**
 - Run Behavioral Simulation**
 - Run Post-Synthesis Functional Simulation
 - Run Post-Synthesis Timing Simulation
 - Run Post-Implementation Functional Simulation
 - Run Post-Implementation Timing Simulation
- RTL ANALYSIS
 - Open Elaboration
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG
 - Generate Bitstream
 - Open Hardware Manager

Sources

- Design Sources (1)
 - n_bit_up_down_counter(behavioral) (n_bit_up_down_counter.vhd)
- Constraints
- Simulation Sources (2)
 - sim_1 (2)
 - n_bit_up_down_counter_tb(behavioral) (n_bit_up_down_counter_tb.vhd)
 - Waveform Configuration File (1)
 - n_bit_up_down_counter_wave.wcfg

Project Summary

n_bit_up_down_counter.vhd n_bit_up_down_counter_tb.vhd

C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/simulation_sources/n_bit_up_down_counter_tb.vhd

```
1 LIBRARY ieee;
2 USE ieee.std_logic_1164.ALL;
3
4 ENTITY n_bit_up_down_counter_tb IS
5 END n_bit_up_down_counter_tb;
6
7 ARCHITECTURE Behavioral OF n_bit_up_down_counter_tb IS
8
9 -- Component Declaration for the Unit Under Test (UUT)
10 COMPONENT n_bit_up_down_counter
11   GENERIC (n_bits : NATURAL := 8);
12   PORT (up_down : IN STD_LOGIC; -- direction of count, 1 --> counting up, 0 --> counting down
13         clk, rst : IN STD_LOGIC;
14         count : OUT STD_LOGIC_VECTOR(n_bits-1 downto 0)
15       );
16 END COMPONENT;
17
18 -- Clock period definitions
19 CONSTANT n_bits : NATURAL := 5;
20 CONSTANT clk_period : time := 10 ns;
21
22 --Inputs
23 SIGNAL up_down : STD_LOGIC := '1';
24 SIGNAL clk : STD_LOGIC := '0';
25 SIGNAL rst : STD_LOGIC := '0';
26
27 --Outputs
28 SIGNAL count : STD_LOGIC_VECTOR(n_bits-1 downto 0);
29
30 BEGIN
31
32 -- Instantiate the Unit Under Test (UUT)
33 uut : n_bit_up_down_counter
34   GENERIC MAP (n_bits => n_bits)
35   PORT MAP (up_down => up_down,
36            clk => clk,
37            rst => rst,
```

General Properties

Enabled

Location: C:/Users/e190a104/Desktop/HW01_VSim_Tutorial

Type: VHDL

Library: xil_defaultlib

Size: 1.6 KB

Modified: Wednesday 08/24/16 09:34:05 PM

Read-only: No

Encrypted: No

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed	Strategy	Part	Description
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2017)	xc7vx485tffg1157-1	Vivado Synthesis Defaults
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2017)	xc7vx485tffg1157-1	Default settings for Implemen

Vivado Simulator

Type here to search



Xilinx Vivado 2019.2 – (3) Run Behavioral Simulation

vivado_project - [C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project/vivado_project.xpr] - Vivado 2019.2

File Edit Flow Tools Window Layout View Help Quick Access

Flow Navigator PROJECT MANAGER - vivado_project

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Sources

- Design Sources (1)
 - n_bit_up_down_counter(behavioral) (n_bit_up_down_c...
- Constraints
- Simulation Sources (2)
 - sim_1 (2)
 - n_bit_up_down_counter_tb(behavioral) (n_bit_up_d...
 - Waveform Configuration File (1)
 - n_bit_up_down_counter_wave.wcfg

Source File Properties

n_bit_up_down_counter_tb.vhd

Enabled

Location: C:/Users/e190a104/Desktop/HW01_VSim_Tutor

Type: VHDL

Library: xil_defaultlib

Size: 1.6 KB

Modified: Wednesday 08/24/16 09:34:05 PM

Read-only: No

Encrypted: No

General Properties

Run Simulation

Executing elaborate step...

Background Cancel

```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.ALL;
3
4  ENTITY n_bit_up_down_counter_tb IS
5  END n_bit_up_down_counter_tb;
6
7  ARCHITECTURE Behavioral OF n_bit_up_down_counter_tb IS
8
9  -- Component Declaration for the Unit Under Test (UUT)
10 COMPONENT n_bit_up_down_counter
11   GENERIC (n_bits : NATURAL := 8);
12   PORT (up_down : IN  STD_LOGIC; -- direction of count, 1 --> counting up, 0 --> counting down
13         clk, rst : IN  STD_LOGIC;
14         count : OUT  STD_LOGIC_VECTOR(n_bits-1 downto 0)
15        );
16 END COMPONENT;
```

```
27  --Outputs
28  SIGNAL count : STD_LOGIC_VECTOR(n_bits-1 downto 0);
29
30 BEGIN
31
32  -- Instantiate the Unit Under Test (UUT)
33  uut : n_bit_up_down_counter
34    GENERIC MAP (n_bits => n_bits)
35    PORT MAP (up_down => up_down,
36             clk => clk,
37             rst => rst,
```

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed	Strategy	Part	Description
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2017)	xc7vx485tffg1157-1	Vivado Synthesis Defaults
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2017)	xc7vx485tffg1157-1	Default settings for Implem

Executing elaborate step...

Type here to search

9:26 PM 8/22/2017

Xilinx Vivado 2019.2 – (3) Run Behavioral Simulation

vivado_project - [C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project/vivado_project.xpr] - Vivado 2017.2

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SIMULATION - Behavioral Simulation - Functional - sim_1 - n_bit_up_down_counter_tb

Scope Sources

Name	Design Unit	Block Type
n_bit_up_down...	n_bit_up_d...	VHDL Entity
uut	n_bit_up_d...	VHDL Entity

Objects

Name	Value	Data Type
up_down	0	Logic
clk	0	Logic
rst	0	Logic
count[4:0]	UU	Array
n_bits	5	Integer
clk_period	10000 ps	Physical

n_bit_up_down_counter.vhd x n_bit_up_down_counter_tb.vhd x n_bit_up_down_counter_wave.wcfg x

2

1

1

Name	Value
Constants	
n_bits	5
clk_period	10000 ps
Inputs	
clk	0
rst	0
up_down	0
Outputs	
count[4:0]	U
count[4:0]	U

Tcl Console

Messages Log

```
INFO: [USF-XSim-96] XSim completed. Design snapshot 'n_bit_up_down_counter_tb_behav' loaded.  
INFO: [USF-XSim-97] XSim simulation ran for 1000ns  
launch_simulation: Time (s): cpu = 00:00:02 ; elapsed = 00:00:08 . Memory (MB): peak = 997.055 ; gain = 2.313
```

Type a Tcl command here

Sim Time: 1 us

9:28 PM 8/22/2017

Xilinx Vivado 2019.2 – (3) Run Behavioral Simulation

vivado_project - [C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project/vivado_project.xpr] - Vivado 2017.2

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SIMULATION - Behavioral Simulation - Functional - sim_1 - n_bit_up_down_counter_tb

n_bit_up_down_counter.vhd x n_bit_up_down_counter_tb.vhd **n_bit_up_down_counter_wave.wcfg** x

Name	Value
Constants	
n_bits	5
clk_period	10000 ps
Inputs	
clk	0
rst	0
up_down	0
Outputs	
count[4:0]	U
count[4:0]	U

0 ns 100 ns 200 ns 300 ns 400 ns 500 ns 600 ns 700 ns 800 ns 900 ns 1,000,000 ns

10000 ps

Sim Time: 1 us 9:32 PM 8/22/2017

Xilinx Vivado 2019.2 – (3) Run Behavioral Simulation

vivado_project - [C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project/vivado_project.xpr] - Vivado 2017.2

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PROGRAM AND DEBUG

- Generate Bitstream
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Scope

Sources

Objects

Simulation - Behavioral Simulation - Functional - sim_1 - n_bit_up_down_counter_tb

n_bit_up_down_counter.vhd x n_bit_up_down_counter_tb.vhd x n_bit_up_down_counter_wave.wcfg x

Search

Name	Value
Constants	
n_bits	5
clk_period	10000 ps
Inputs	
clk	0
rst	0
up_down	0
Outputs	
count[4:0]	

Right Click

Go To Source Code

Show in Object Window

Report Drivers

Force Constant...

Force Clock...

Remove Force

Cut Ctrl+X

Copy Ctrl+C

Paste Ctrl+V

Delete Delete

Find... Ctrl+F

Find Value... Ctrl+Shift+F

Select All Ctrl+A

Expand

Collapse

Ungroup

Rename F2

Name

Waveform Style

Signal Color

Object Color

Radix

Show as Enumeration

Reverse Bit Order

New Group

New Divider

New Virtual Bus

Default

Binary

Hexadecimal

Octal

ASCII

Unsigned Decimal

Signed Decimal

Signed Magnitude

Real

Real Settings...

0 ns 100 ns 200 ns 300 ns 400 ns 500 ns 600 ns 700 ns 800 ns 900 ns 1,000.000 ns

10000 ps

1 us

Signed Decimal

Sim Time: 1 us

9:35 PM 8/22/2017

Xilinx Vivado 2019.2 – (3) Run Behavioral Simulation

vivado_project - [C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_El-Araby/n_bit_up_down_counter/vivado_project/vivado_project.xpr] - Vivado 2019.2

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Right Click

Right Click

Simulation

- Run Simulation

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Simulation - Behavioral Simulation - Functional - sim_1 - n_bit_up_down_counter_tb

n_bit_up_down_counter.vhd x n_bit_up_down_counter_tb.vhd x n_bit_up_down_counter_wave.wcfg x

Scope

Sources

Objects

Name	Value
Constants	
n_bits	5
clk_period	10000 ps
Inputs	
clk	0
rst	0
up_down	0
Outputs	
count[4:0]	U

Go To Source Code

Show in Object Window

Report Drivers

Force Constant...

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Remove Force

Cut Ctrl+X

Copy Ctrl+C

Paste Ctrl+V

Delete

Delete

Find... Ctrl+F

Find Value... Ctrl+Shift+F

Select All Ctrl+A

Expand

Collapse

Ungroup

Rename F2

Name

Waveform Style

Signal Color

Divider Color

Radix

Show as Enumeration

Reverse Bit Order

New Group

New Divider

New Virtual Bus

Digital

Analog

Analog Settings...

0 ns 100 ns 200 ns 300 ns 400 ns 500 ns 600 ns 700 ns 800 ns 900 ns 1,000.000 ns

10000 ps

U

Sim Time: 1 us

9:39 PM 8/22/2017

Xilinx Vivado 2019.2 – (3) Run Behavioral Simulation

vivado_project - [C:/Users/e190a104/Desktop/HW01_VSim_Tutorial_EI-Araby/n_bit_up_down_counter/vivado_project/vivado_project.xpr] - Vivado 2019.2

File Edit Flow Tools Window Layout View Run Help Q Quick Access

Ready

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PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Scope

Objects

Simulation - Behavioral Simulation - Functional - sim_1 - n_bit_up_down_counter_tb

n_bit_up_down_counter.vhd x n_bit_up_down_counter_tb.vhd x n_bit_up_down_counter_wave.wcfg x

Right Click

Go To Source Code

Show in Object Window

Report Drivers

Force Constant...

Force Clock...

Remove Force

Cut Ctrl+X

Copy Ctrl+C

Paste Ctrl+V

Delete Delete

Find... Ctrl+F

Find Value... Ctrl+Shift+F

Select All Ctrl+A

Expand

Collapse

Ungroup

Rename F2

Name

Waveform Style

Signal Color

Divider Color

Radix

Show as Enumeration

Reverse Bit Order

New Group

New Divider

New Signal Bus

1,000.000 ns

100 ns

200 ns

300 ns

400 ns

500 ns

600 ns

700 ns

800 ns

900 ns

10000 ps

10 ns

Ctrl Console Messages Log

Sim Time: 1 us

9:42 PM 8/22/2017

HW01 (Vivado Simulator Tutorial)

- Describe in **behavioral VHDL** a ***modulo-m up/down counter*** with the following interface:
 - **Generics**
 - Modulo base (m with default value of 16)
 - **Inputs**
 - Clock (clk \rightarrow 1 bit)
 - Asynchronous reset (rst \rightarrow 1 bit)
 - Counting direction (up_down \rightarrow 1 bit)
 - 1 \rightarrow Counting up
 - 0 \rightarrow Counting down
 - **Outputs**
 - Count value (count $\rightarrow \lceil \log_2(m) \rceil$ bits)
- In Vivado
 - Create a project
 - Add source files
 - Run behavioral simulation
 - Your waveform configuration should be identical to the provided waveform snapshot.
- **NOTE:** Homework submission is a "**Single Attempt**", i.e., carefully review everything that you want to submit before hitting the "submit" button and make sure that you have uploaded all documents you want to submit and have not missed anything.
- **Due on Friday 09/04/2020 at 12:00pm (NOON) on Blackboard**

