RESUME

Jackson Melchert
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EDUCATION

Stanford University
PhD in Electrical Engineering, started in September 2019
Current GPA: 4.00/4.00

University of Wisconsin – Madison
Bachelor of Science in Computer Engineering, 2019
Graduated with Distinction
Double Major in Computer Engineering and Computer Science
GPA: 3.92/4.00

RESEARCH POSITIONS

Stanford University Department of Electrical Engineering Stanford, CA
PhD Student, Dr. Priyanka Raina, Advisor September 2019 – Present

- Currently researching efficient architectures for Course Grained Reconfigurable Architectures (CGRAs) as a part of the AHA Agile Hardware Project
- Created a generator to explore the design space of CGRA processing element architectures using novel domain specific languages
- Created an application analysis framework for extracting common computational blocks from applications and merging them together to create processing elements that accelerate those common computational blocks
- Helped to develop a domain specific language for designing processors and processing elements that utilizes formal methods for automatic compiler creation

University of Wisconsin – Madison Department of Computer Engineering Madison, WI
Undergraduate Research Assistant, Dr. Younghyun Kim, Supervisor May 2018 – May 2019

- Researched low power embedded system design and approximate computing
- Created an award-winning demonstration of a low power approximate serial bus (AxSerBus) by programming an FPGA and microcontroller using Verilog and C++
- Helped design a dynamically adjustable low power approximate division circuit (SAADI) using Verilog
- Simulated and synthesized this circuit using MATLAB, Modelsim, and Synopsis Design Compiler

University of Wisconsin – Madison Department of Computer Science Madison, WI
Web Developer, Dr. Suman Banerjee, Supervisor May 2018 – May 2019

- Worked with a development team on creating a website for GonioSense, a wearable-based system that can track and measure joint motions for patients undergoing physical therapy
- Created an intuitive website for patients and physicians to track and analyze goniometer measurements
- Developed and maintained the website using Angular as a front-end framework and Firebase as the back-end

University of Wisconsin – Madison Department of Computer Engineering Madison, WI
Undergraduate Research Assistant, Dr. Azadeh Davoodi, Supervisor May 2017 – May 2018

- Researched Electronic Design Automation through a Research Experiences for Undergraduates (REU) grant from the NSF
- Wrote programs in TCL and C++ to increase the security of microprocessor manufacturing as well as identify design rule violations
- Collected data using TCL scripting with the Olympus SoC tool from Mentor Graphics
- Designed and ran experiments using machine learning to aid in the routing of microprocessors
- Became familiar with neural network modeling tools such as Neupy and worked on modeling design rule violations using Deep Neural Networks

University of Wisconsin – Milwaukee Department of Physics Milwaukee, WI
Undergraduate Research Assistant, Dr. Daniel Agterberg, Supervisor May 2016 – August 2016

- Worked with a theoretical physicist and graduate student on the fermi surface representations of low temperature superconductors
- Independently created 3D representations of fermi surfaces in the superconducting state using Mathematica, MATLAB, and Python
- These visualizations were used to provide insight into the properties of these superconductors and how new low temperature superconductors could be identified

TEACHING EXPERIENCE

EE 272A: Design Projects in VLSI Systems I - Stanford University Stanford, CA
Teaching Assistant and Grader, Dr. Priyanka Raina, Professor Winter 2021 – Present

- Currently helping teach digital and mixed signal design and the electronic design automation (EDA) tools used for it.
- Students in this class write a deep neural network accelerator in Verilog and high-level synthesis.
- They take these designs and push them through all of the design tools needed to tape-out their accelerator, including synthesis, layout, place and route, power estimation, and more.

PUBLICATIONS

Priyanka Raina et al., "Creating an Agile Hardware Design Flow," ACM/IEEE Design Automation Conference (DAC), 2020

Jackson Melchert, Setareh Behroozi, Jingjie Li and Younghyun Kim, "SAADI-EC: A Quality-Configurable Approximate Divider for Energy Efficiency," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Nov. 2019

Setareh Behroozi, Jingjie Li, Jackson Melchert, and Younghyun Kim, “SAADI: A Scalable Accuracy Approximate Divider for Dynamic Energy-Quality Scaling”, Asia South Pacific Design Automation Conference (ASP-DAC ’19), 2019

Jackson Melchert, Boyu Zhang, and Azadeh Davoodi, "A comparative study of local net modeling using machine learning", ACM Great Lakes Symposium on VLSI (GLSVLSI'18), May 2018

Jonathon Magaña, Daohang Shi, Jackson Melchert, and Azadeh Davoodi, "Are Proximity Attacks a Threat to the Security of Split Manufacturing of Integrated Circuits?," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Dec. 2017