ECE 6140 Project Part 2: Design and Implement Deductive Fault Simulator

Due Nov 8th for all sections.

You are to design and implement a deductive fault simulator using list processing as discussed in class. You need to consider faults in the output nodes of all gates. For simplicity we will not consider faults in fanout branches as in the checkpointing theorem. What this means is that you have to consider each net stuck-at-0 or stuck-at-1 and not worry about whether it fans out to the inputs of more than one gate,

However, the fault simulator is to be designed with two options: (a) automatically simulating all the faults in all the nets and (b) taking as input a list of faults from a file for simulation purposes. This file must have the following format:

"Netno stuck-at-value"

1 0

2 1

3 0

4 1

…….

The output of the program must be directed to a file and must contain a list of all the detected faults from the set of vectors applied to the circuit under test as well as the number of faults detected.

Part (a): For the following vectors and circuits, find all the faults detected:

S27: 1101101

S27: 0101001

S298f_2: 10101011110010101

S298f_2: 11101110101110111

S344f_2: 101010101010111101111111

S344f_2: 111010111010101010001100

S349f_2: 101000000010101011111111

S349f_2: 111111101010101010001111

Part (b): Apply random test vectors to each of the above circuits and plot fault coverage vs. no of applied tests. How many vectors do you need to achieve more than 75% coverage ? How many random vectors do you need to achieve more than 90% coverage ?

Give a concise report (hand written will not be accepted) describing your implementation and results (as compact as possible). Upload directly to canvas by Nov 10th.