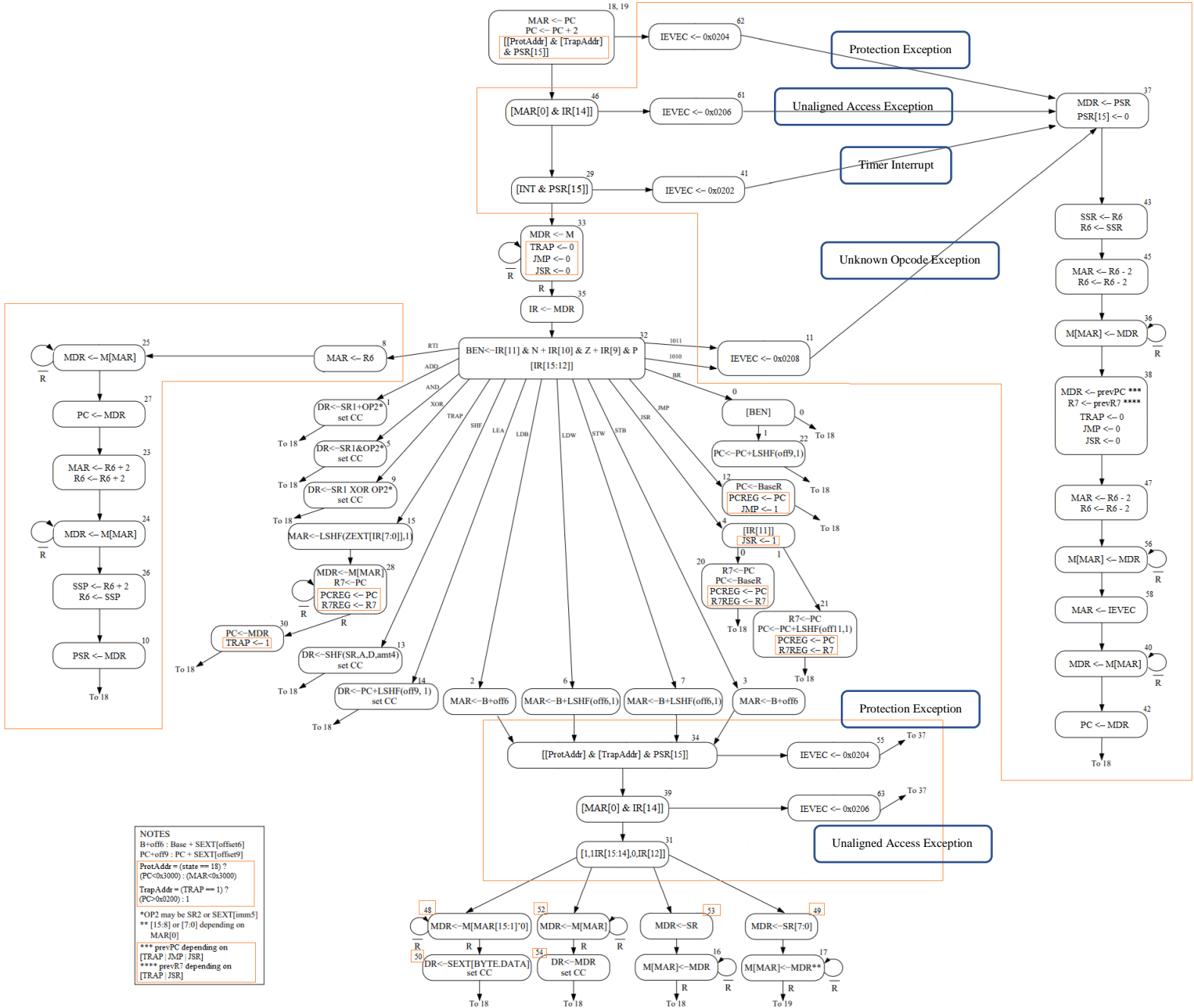
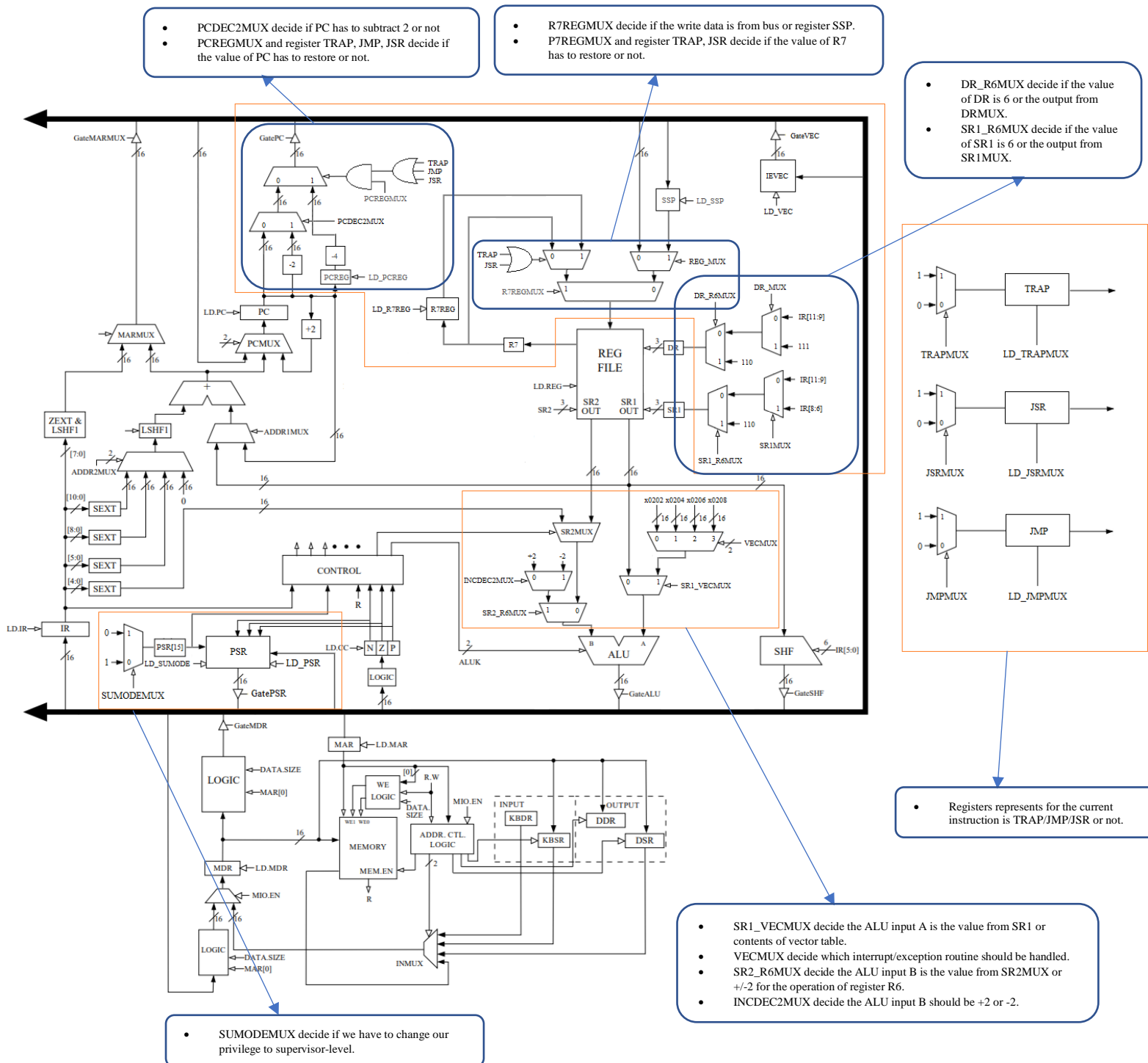


- State Diagram



- Datapath



- Control Signals

Signal Name	Signal Values	
COND(COND2/1, COND1, COND0):	101	;select protection exception
	110	;select unaligned access
	111	;select timer interrupt
LSIRD/1:	[0,0,IR[15:12]]	
	[1,1,IR[15:14],0,IR[12]]	
LD_PSR/1:	NO, LOAD	
LD_SSP/1:	NO, LOAD	
LD_VEC/1:	NO, LOAD	
LD_SUMODE/1:	NO, LOAD	
LD_TRAP/1:	NO, LOAD	
LD_JSR/1:	NO, LOAD	
LD_JMP/1:	NO, LOAD	
LD_R7REG/1:	NO, LOAD	
LD_PCREG/1:	NO, LOAD	
GateVEC/1:	NO, YES	
GatePSR/1:	NO, YES	
PCDEC2MUX/1:	PC	;select pc
	PC - 2	;select pc - 2
DR_R6MUX/1:	DRMUX	;select output from DRMUX
	R6	;select R6
SR1_R6MUX/1:	SR1MUX	;select output from SR1MUX
	R6	;select R6
SR2_R6MUX/1:	SR2MUX	;select output from SR2MUX
	INCDEC2MUX	;select output from INCDEC2MUX
REG_MUX/1:	BUS	;select value from bus
	SSP	;select value from SSP
INCDEC2MUX/1:	+2	
	-2	
VECMUX/2:	x0202	;select timer interrupt vector
	x0204	;select protection exception vector
	x0206	;select unaligned access exception vector
	x0208	;select unknown opcode exception vector
SR1_VECMUX/1:	SR1OUT	;select SR1OUT
	VECMUX	;select output from VECMUX
SUMODEMUX/1:	1	;select PSR[15] to user mode (1)
	0	;select PSR[15] to supervisor mode (0)
TRAPMUX/1:	0	
	1	
JSRMUX/1:	0	
	1	
JMPMUX/1:	0	
	1	
R7REGMUX/1:	REG_MUX	;select output from REG_MUX
	R7MUX	;select output from R7MUX
PCREGMUX/1:	PCDEC2MUX	;select output from PCDEC2MUX
	PCREG - 4	;select output from PCREG - 4

## • Microsequencer

