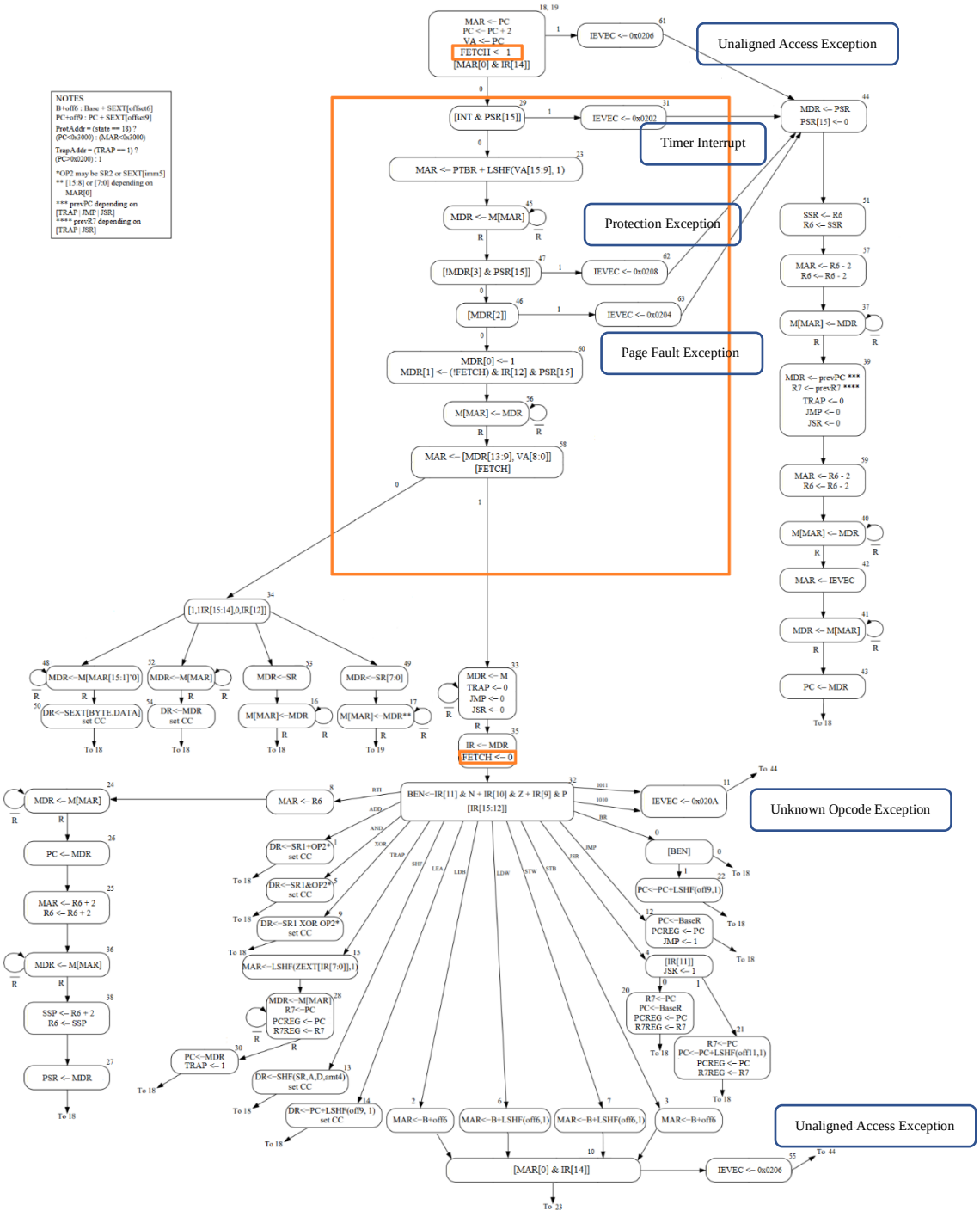
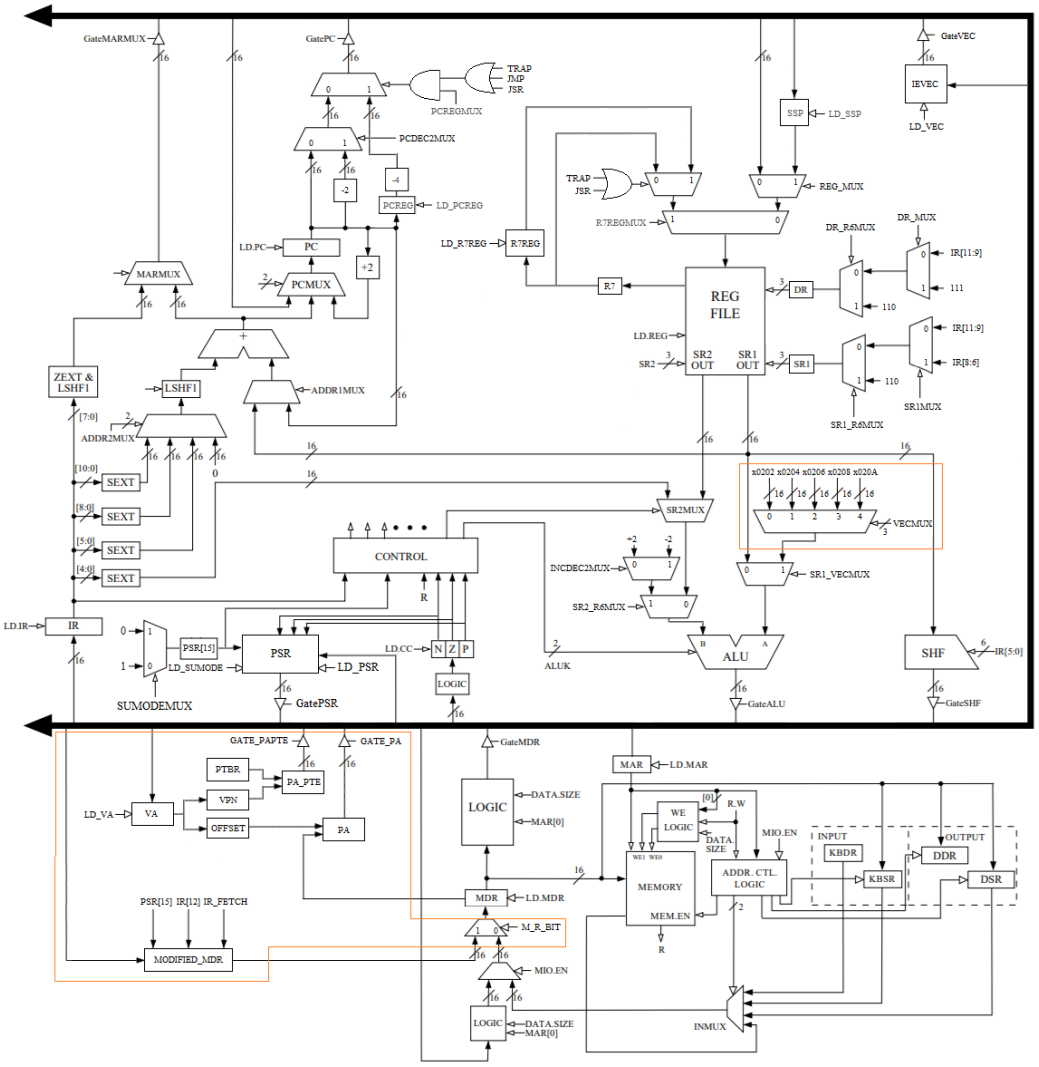
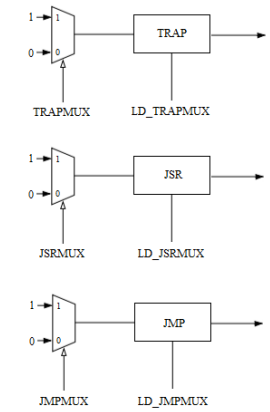
- State Diagram



- Datapath





- Registers represents for the current state is FETCH or not.

- VA stores virtual address from MAR.
- Get the physical address of PTE with known PTBR and VPN from VA.
- Get the physical address of virtual address with MDR and offset from VA.
- Modify the page table entry with reference and modified bit after accessing page table each time.

- Control Signals

Signal Name	Signal Values	
IRD2/1:	[0,0,IR[15:12]]	;select state w/ other situation
IRD3/1:	[1,1,IR[15:14],0,IR[12]]	;select state w/o other situation
PAGE_FAULT/1:	63	;select state w/ page fault exception
	60	;select state depends on FETCH
LD_IR_FETCH/1:	NO, LOAD	
LD_VA/1:	NO, LOAD	
Gate_PA/1:	NO, YES	
Gate_PAPTE/1:	NO, YES	
VECMUX/3:	x0202	;select timer interrupt vector
	x0204	;select page fault exception vector
	x0206	;select unaligned access exception vector
	x0208	;select protection exception vector
	x020A	;select unknown opcode exception vector
IR_FETCHMUX/1:	0	
	1	
M_R_BIT/1:		;select next MDR from BUS
		;modify MDR's reference and modified bit

- Microsequencer