Electronic Clock - Display Control

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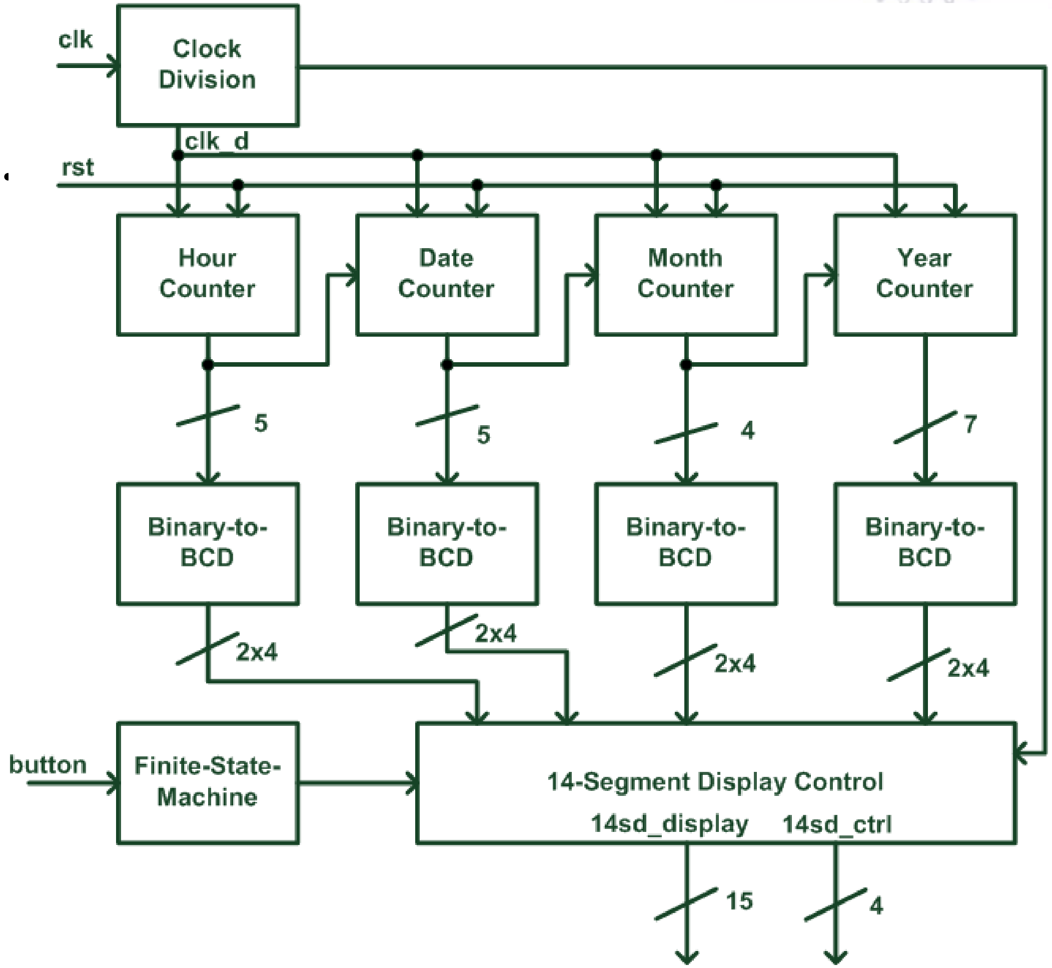
Timer

- Timer is a counter with carry propagation.
  - Hour : 0~23
  - Date: 0~28/30/31
  - Month: Jan(0)/Feb(1)/March(2)/……/November(10)/December(11)
  - Year: 00~99
- The carry propagation is determined not only by lower counter but also upper counters.
  - Leap month
  - Leap year

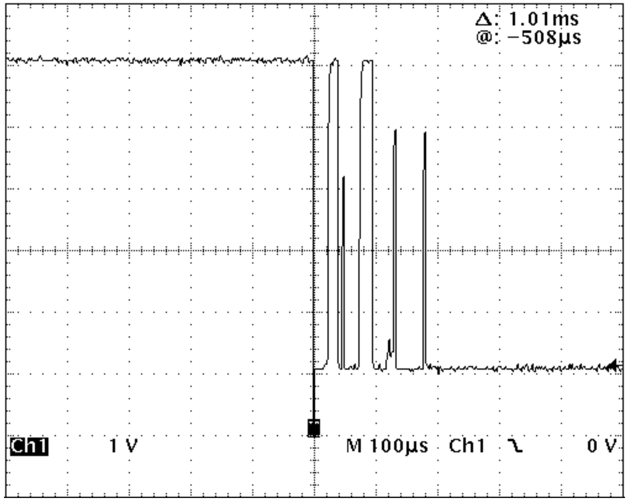
Display Control of Timer

- Finite-state-Machine
  - State determines the display modes of Timer.
    - 24hr or AM/PM
    - Month + Year
    - Date + Month
    - Year

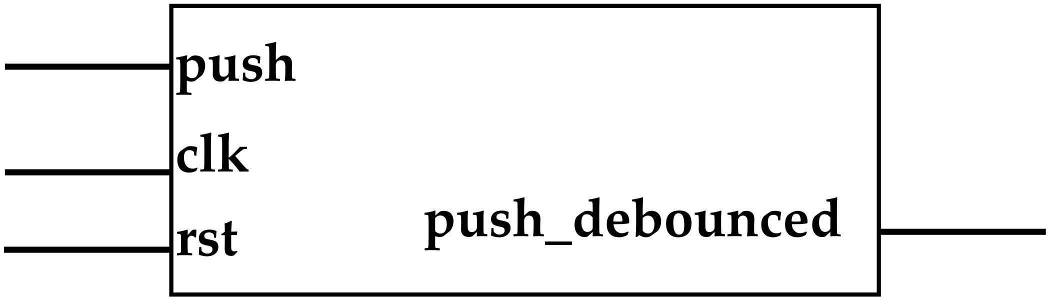


Switch Contact Bounce

- Pushbutton contains a metal spring
  - The switch contact will bounce several times before stabilization when buttons are pressed and released.
  - The random pulses causes instable results to the design.
  - The random pusles ranges in µs, but the FPGA is sensitive to pulses down to ns range.



Debounce Circuit



- N-bit shift register triggered with clock can be used as debounce circuit.
- When all 4 bits of the register are high (low), the output of the debounce circuit changes to high (low).

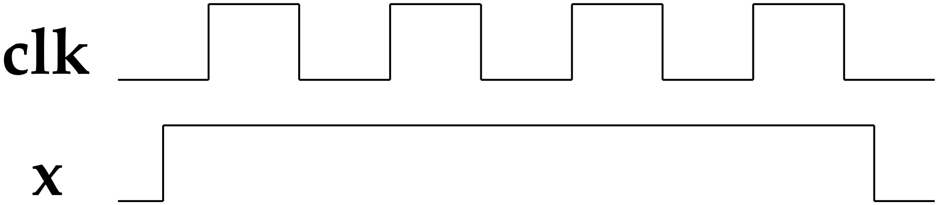
Debounce Design

```
module debounce (
 rst, clk, push, push_debounced );

input rst;
input clk;
input push;
output push_debounced;

// declare the outputs
reg push_debounced;

// declare the shifting registers
reg[3:0] push_window;
```

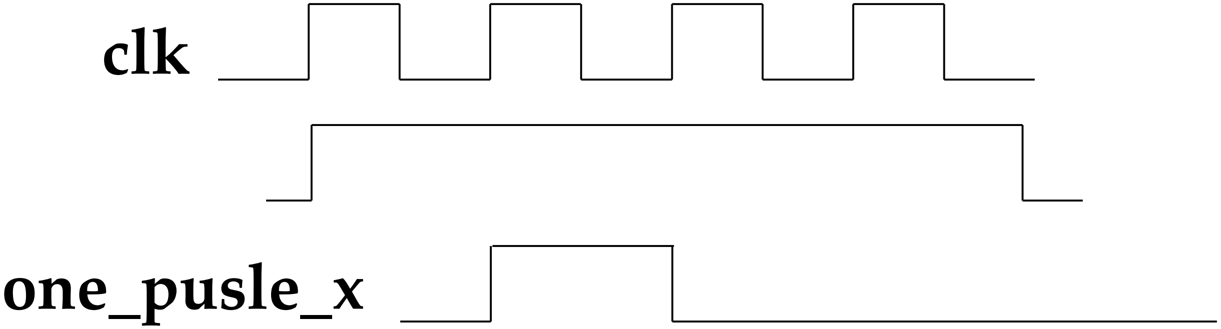
```
 always  @(posedge clk or posedge rst)
  begin
    if (rst) begin
      push_window <= 4'b0;
      push_debounced <= 1'b0;
    end else begin
      push_window<={push, push_window[3:1]};

     if (push_window[3:0] == 4'b1111) begin
        push_debounced <= 1'b1;
      end else begin
        push_debounced <= 1'b0;
      end
    end
  end
endmodule
```

One-Pulse Generation

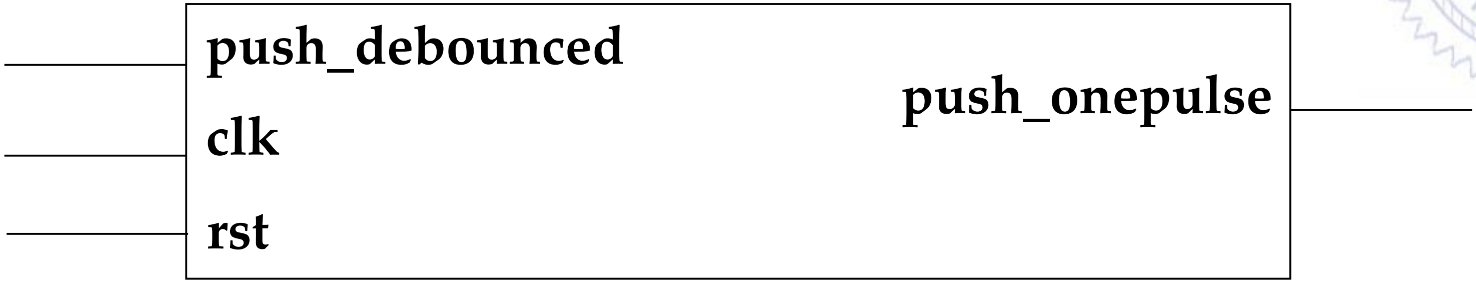
- Since the state of pressed is much longer than one clock period, the push-button usually recognizes one “pressed” event as successive cycles of “pressed”.



- Once a pushbutton is pressed (long or short), the one-pulse circuit generates only a one-clock-period-long pulse.



One-Pulse Generation



push_debounced

clk

rst

push_onepulse

- Inputs
  - – clk, rst : system clock and reset.
  - – push_debounced: debounced pushbutton signal
- Output
  - – push_onepulse: one-clock-cylce impulse when pushbuttone is pressed.

One-Pulse Design

```
module onepulse (
rst, clk, push_debounced, push_onepulse
);
  input clk, rst;
  input push_debounced;
  output push_onepulse;

  // internal registers
  reg push_onepulse_next;
  reg push_debounced_delay;

  always @* begin
    push_onepulse_next  =  push_debounced
     & ~push_debounced_delay;
  end
```

```
   always @(posedge clk or posedge rst)
      begin
    if (rst) begin

      push_onepulse <= 1'b0;
      push_debounced_delay <= 1'b0;

    end else begin

 push_onepulse <= push_onepulse_next;
push_debounced_delay <=push_debounced;

    end
   end
endmodule
```