Lab 4: Shifters

Objective

- ✓ Review sequential circuits.
- ✓ Review shift registers.

Prerequisite

- ✓ Fundamentals of logic gates.
- ✓ Clocking concepts
- ✓ Logic modeling in Verilog HDL.

Pre-labs

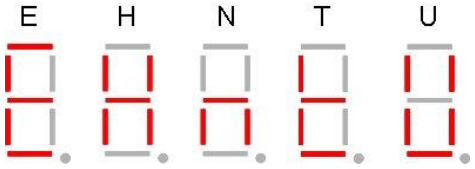
1. Cascade eight DFFs together as a shift register. Connect the output of the last DFF to the input of the first DFF as a ringer counter. Let the initial value of DFF output after reset be 01010101. Construct the Verilog RTL representation for the logics with verification.

Experiments

1 Implement pre-lab1 on FPGA platform with the LED pin assignments as output signal.

2 Construct a ring counter similar to that of pre-lab1 but the initial value of the DFFs can be set randomly.

3 Use the idea from pre-lab1. We can do something on the seven-segment display. Assume we have the pattern of E, H, N, T, U for seven-segment display as shown below. Try to implement the scrolling pre-stored pattern NTHUEE with the four seven-segment displays.



4 (Bonus) Display 1010 in the seven-segment display. Use the DIP switch (one bit to indicate left/right shift, three bits with one hot to display the kind of shift operation) as the control input to implement the functional/arithmetic/barrel shifter. Use one push button to control the display of the number before/after the shift operation.

TA: _____

