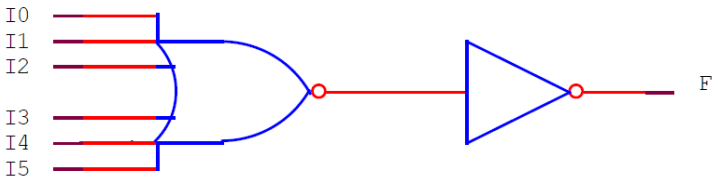
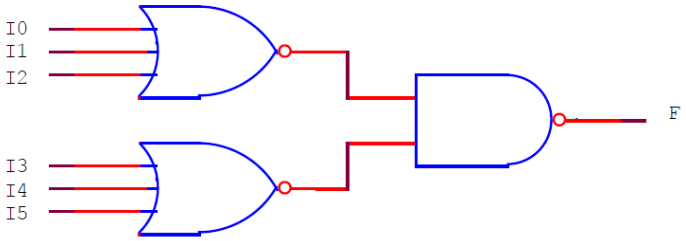
ISTM 214 Homework 2 (Due day: 10/4)

Name:_____ ID:_____

1. (20%) Show a **MOSFET-level diagram** for a 6-input OR gate realized using a 6-input NOR gate followed by a NOT gate. Label the inputs $I_0 \ldots I_5$ and the output F. Be sure to show the power (Vcc) and ground (GND) connections as well. Determine the total number of N- and P-channel MOSFETs required for this realization



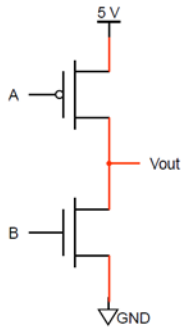
2. (20%) Show a **MOSFET-level diagram** for a 6-input OR gate realized using two 3-input NOR gates on the first level and a (single) 2-input NAND gate on the second level. Label the inputs $I_0 \ldots I_5$ and the output F. Determine the total number of N- and P-channel MOSFETs required for this realization. Be sure to show the power (Vcc) and ground (GND) connections as well.



3. (10%) Discuss the tradeoffs associated with the two 6-input OR functions realized in problems 1 and 2. Which is "better" (and why)?

4. (30%) Given that the P-channel device in the circuit below has ON and OFF resistances of100 Ω and 2 MΩ (respectively) and that the N-channel device has ON and OFF resistances of 50 Ω and 4 MΩ (respectively), complete the table listing the output voltages obtained for each input combination as well as the power dissipation (in milliwatts). Show your calculations

A	B	V_{out}	Power Dissipation
0V	0V		
0V	5V		
5V	0V		
5V	5V		



5. (20%) One of your “best friends from another major” found some N- and P-channel MOSFETs in your geek box and wired them together as shown below. Help your BFFAM figure out what they have created by determining V_{out} for all possible input combinations(for the sake of analysis, assume the ON resistance of each MOSFET (i.e., both P- and N-channel) is 10 Ω and that its OFF resistance is 1 MΩ.

A	B	V_{out}
0V	0V	
0V	5V	
5V	0V	
5V	5V