

Digital System Design Lab

Lab 10

Latch / Flip-Flop

Student ID: D1166506

Name: 周嘉禾

Date: 2023/11/29

1. Objectives

- To become familiar with the components of D flip-flop
- To become familiar with master-slave D flip-flop

2. Theorem

(1) Latch:

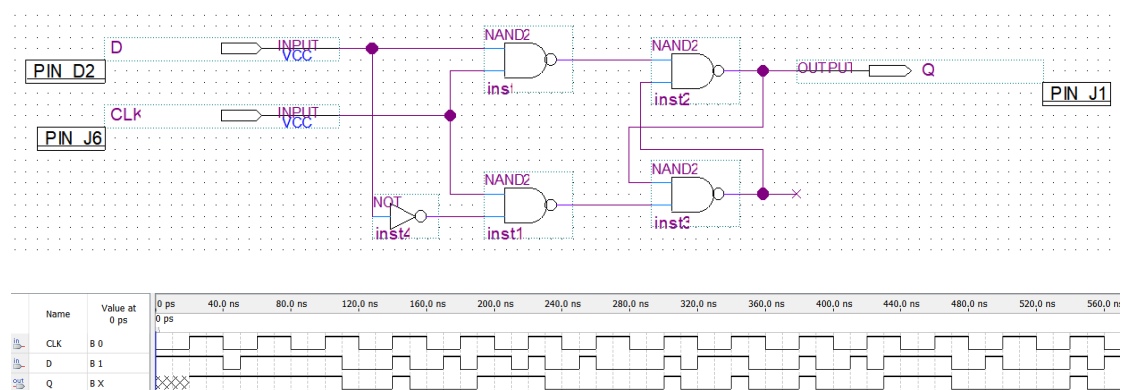
A latch is a basic memory element that can store a single bit of data. It's constructed using logic gates, typically using cross-coupled NAND or NOR gates. Latches are level-sensitive and can change their output state as long as the enabling signal is active. They're often used in temporary storage or simple control applications.

(2) Flip-Flop:

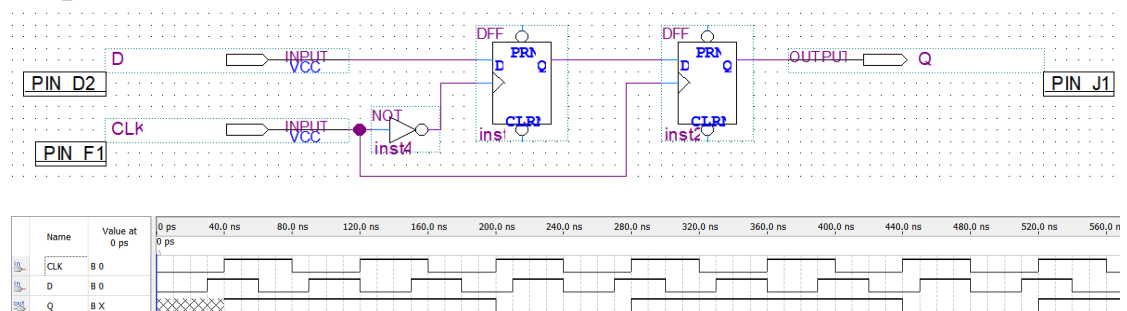
A flip-flop is a more stable and controlled version of a latch. It's edge-triggered, meaning it changes state based on the transition of a clock signal (rising or falling edge). Flip-flops come in different types like D-type, JK, SR, and T flip-flops, each with its own characteristics and use cases. They're commonly employed in digital systems for storing state information, forming the basis of sequential logic circuits like counters, registers, and memory elements in processors.

3. Experimental Results

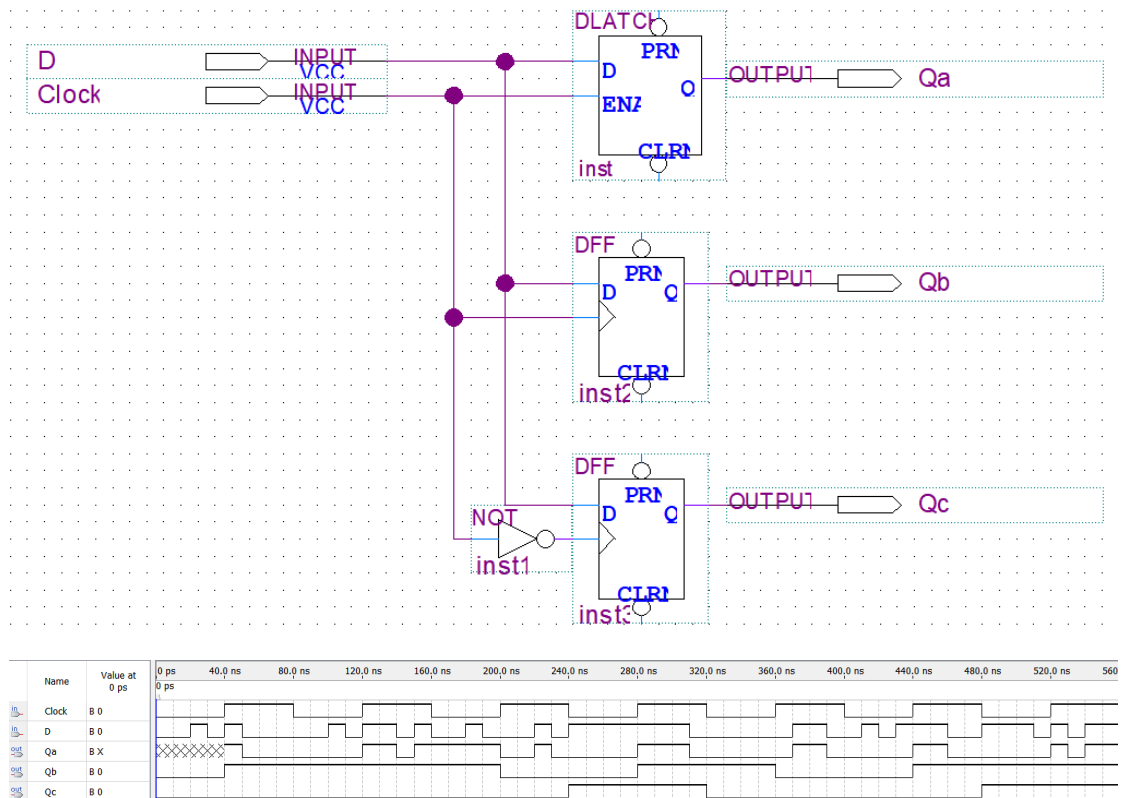
(1) Step 1



(2) Step 2



(3) Step 3



4. Comments

In step 3, Qa(D latch) will directly pass the value D had while the clock is high but will be indeterminate at when the circuit started since the clock hadn't opened beforehand.

On the other hand, Qb (positive edge D flip-flop) and Qc (negative edge D flip-flop) will only pass the value D on the edge (positive or negative), and the output will be constant until the edge changes.

5. Problems & Solutions

None

6. Feedback

None