
LEARNING OUTCOME #1: “an ability to analyze and design CMOS logic gates.”

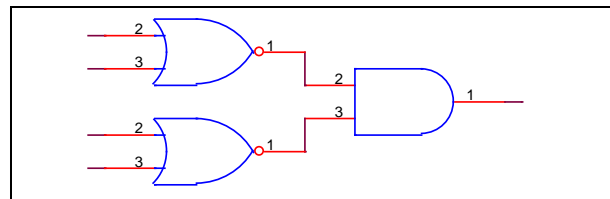
Multiple Choice – select the single most appropriate response for each question.

Note that “none of the above” MAY be a VALID ANSWER.

1. The **unsigned hexadecimal** number $(537)_{16}$ is equivalent to the following **unsigned binary** number:
- (A) $(101\ 11\ 111)_2$
 - (B) $(101\ 011\ 111)_2$
 - (C) $(101\ 0011\ 0111)_2$
 - (D) all of the above
 - (E) none of the above

2. The expression $(X+Y) \cdot (X+Z) = X + Y \cdot Z$ is an example of:
- (A) distributivity
 - (B) commutativity
 - (C) associativity
 - (D) consensus
 - (E) none of the above

3. A circuit consisting of a level of **NOR gates** followed by a level of **AND gates** is **logically equivalent** to:
- (A) a multi-input OR gate
 - (B) a multi-input AND gate
 - (C) a multi-input NOR gate
 - (D) a multi-input NAND gate
 - (E) none of the above



4. The **high impedance state** of a **tri-state buffer** is created by:
- (A) turning “off” the PMOS transistor and turning “on” the NMOS transistor at the output of the buffer
 - (B) turning “off” both the PMOS and the NMOS transistors at the output of the buffer
 - (C) turning “on” both the PMOS and the NMOS transistors at the output of the buffer
 - (D) turning “on” the PMOS transistor and turning “off” the NMOS transistor at the output of the buffer
 - (E) none of the above
5. The **direction that current flows** between the drain (D) and source (S) of N-channel and P-channel MOSFETS is as follows:
- (A) N-channel: $D \rightarrow S$; P-channel: $S \rightarrow D$
 - (B) N-channel: $S \rightarrow D$; P-channel: $D \rightarrow S$
 - (C) N-channel: $D \rightarrow S$; P-channel: $D \rightarrow S$
 - (D) N-channel: $S \rightarrow D$; P-channel: $S \rightarrow D$
 - (E) none of the above

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6. For most CMOS logic families, the **maximum acceptable V_{IL}** is:
- (A) 10% of the power supply voltage
 - (B) 30% of the power supply voltage
 - (C) 50% of the power supply voltage
 - (D) 70% of the power supply voltage
 - (E) 90% of the power supply voltage
7. The **nominal (minimum) case** for the **outputs of logic family “A”** to be able to successfully drive **the inputs of logic family “B”** is:
- (A) $\text{fanout}_{A \rightarrow B} \leq 1$ and $\text{DCNM}_{A \rightarrow B} < 0$
 - (B) $\text{fanout}_{A \rightarrow B} \leq 0$ and $\text{DCNM}_{A \rightarrow B} < 1$
 - (C) $\text{fanout}_{A \rightarrow B} \geq 1$ and $\text{DCNM}_{A \rightarrow B} > 0$
 - (D) $\text{fanout}_{A \rightarrow B} \geq 0$ and $\text{DCNM}_{A \rightarrow B} > 1$
 - (E) none of the above
8. If a CMOS **gate input voltage** is **50% of its V_{cc}** (power supply) voltage, then:
- (A) the logic gate will dissipate **less power** than it would if the input was 1% of its power supply voltage
 - (B) the logic gate will dissipate **less power** than it would if the input was 99% of its power supply voltage
 - (C) the logic gate will dissipate **more power** than it would if the input was *either 1% or 99%* of its power supply voltage
 - (D) the logic gate will dissipate **no power**
 - (E) none of the above
9. A microcontroller designed to operate over a power supply range of **2 V to 4 V** and a clock frequency range of **0 to 60 MHz** dissipates a maximum of **320 mW**. If the supply voltage used is **3 V** and the clock frequency is **40 MHz**, the power dissipation of the microcontroller will be reduced to:
- (A) 60 mW
 - (B) 120 mW
 - (C) 160 mW
 - (D) 180 mW
 - (E) none of the above
10. A microcontroller designed to operate over a power supply range of **2 V to 4 V** and a clock frequency range of **0 to 60 MHz** dissipates a maximum of **320 mW**. If the supply voltage used is **4 V** and the clock frequency is **1 Hz**, the power dissipation of the microcontroller will be reduced to:
- (A) 60 mW
 - (B) 120 mW
 - (C) 160 mW
 - (D) 180 mW
 - (E) none of the above

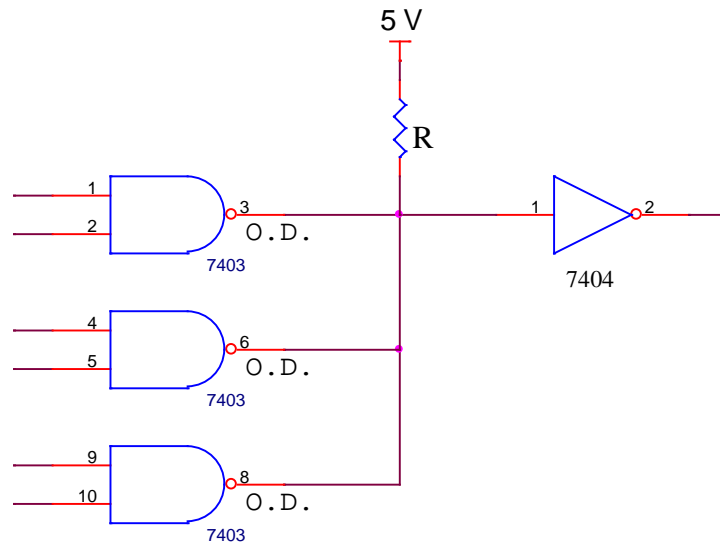
The following table applies to questions 11 through 14:

Table 1. DC Characteristics of a Hypothetical Logic Family.

$V_{CC} = 5 \text{ V}$	$V_{OH} = 3.50 \text{ V}$	$V_{OL} = 0.50 \text{ V}$	$V_{IH} = 2.50 \text{ V}$	$V_{IL} = 1.00 \text{ V}$
$V_{TH} = (V_{OH} - V_{OL})/2$	$I_{OH} = -5.0 \text{ mA}$	$I_{OL} = 10 \text{ mA}$	$I_{IH} = 500 \text{ }\mu\text{A}$	$I_{IL} = -2.0 \text{ mA}$

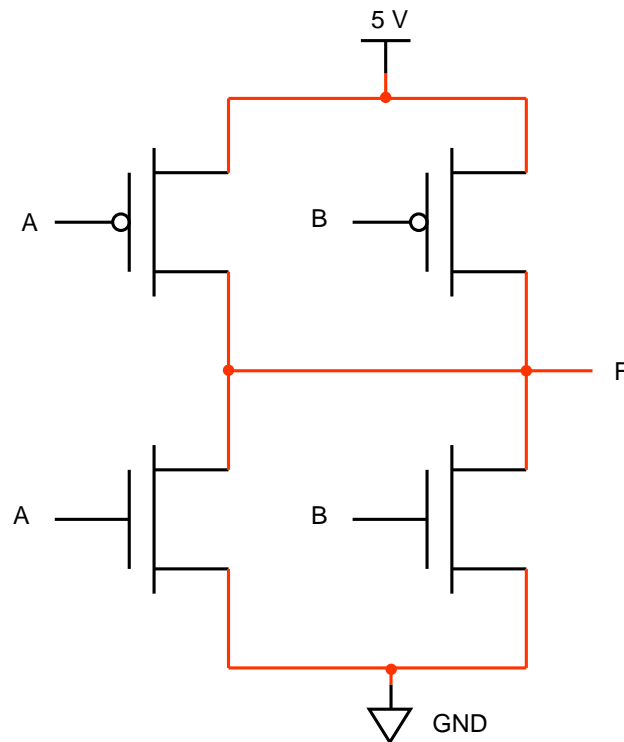
11. The **DC noise margin** for this logic family is:
- (A) 0.50 V
 - (B) 1.00 V
 - (C) 1.50 V
 - (D) 2.00 V
 - (E) none of the above
12. The **practical fanout** for this logic family is:
- (A) 1
 - (B) 2
 - (C) 5
 - (D) 10
 - (E) none of the above
13. When interfacing an **LED** that has a **forward voltage of 1.5 V** to this logic family in a **current sourcing** configuration, **maximum brightness** will be achieved (within the rated specifications) using a current limiting resistor of the value:
- (A) 200 Ω
 - (B) 300 Ω
 - (C) 400 Ω
 - (D) 500 Ω
 - (E) none of the above
14. When interfacing an **LED** that has a **forward voltage of 1.5 V** to this logic family in a **current sinking** configuration, **maximum brightness** will be achieved (within the rated specifications) using a current limiting resistor of the value:
- (A) 200 Ω
 - (B) 300 Ω
 - (C) 400 Ω
 - (D) 500 Ω
 - (E) none of the above

The following circuit applies to questions 15 through 17:



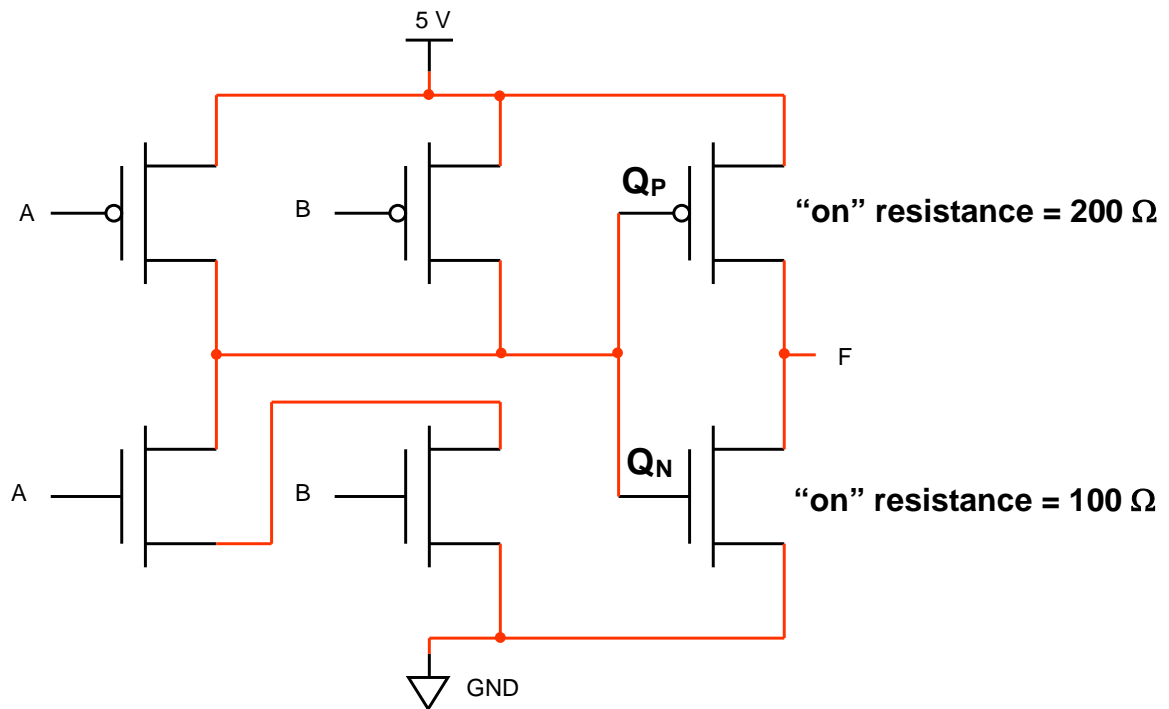
15. If the **minimum** value of pull-up resistor **R** used for this circuit is **1000 Ω** , the **I_{OLmax}** of each 7403 open-drain NAND gate is specified to be **+5 mA**, and the **I_{IL}** required by the 7404 inverter is **-0.5 mA**, then the **V_{IL}** provided to the 7404 input is guaranteed to be **no higher than**:
- (A) 0.1 V
 - (B) 0.5 V
 - (C) 4.5 V
 - (D) 5.0 V
 - (E) none of the above
16. If the **maximum** value of pull-up resistor **R** used for this circuit is **10,000 Ω** , the off-state leakage current of each of the 7403 open-drain NAND gate outputs is **+10 μA** , and the **I_{IH}** required by the 7404 inverter is **+20 μA** , then the **V_{IH}** provided to the 7404 input is guaranteed to be **no lower than**:
- (A) 0.1 V
 - (B) 0.5 V
 - (C) 4.5 V
 - (D) 5.0 V
 - (E) none of the above
17. A **valid reason** for choosing the **minimum value** of **R** (provided above) is:
- (A) to minimize the fall time (**t_{THL}**) of the circuit
 - (B) to minimize the rise time (**t_{TLH}**) of the circuit
 - (C) to minimize the power dissipation of the circuit
 - (D) to minimize the DC noise margin of the circuit
 - (E) none of the above

The following circuit applies to questions 18 through 20:



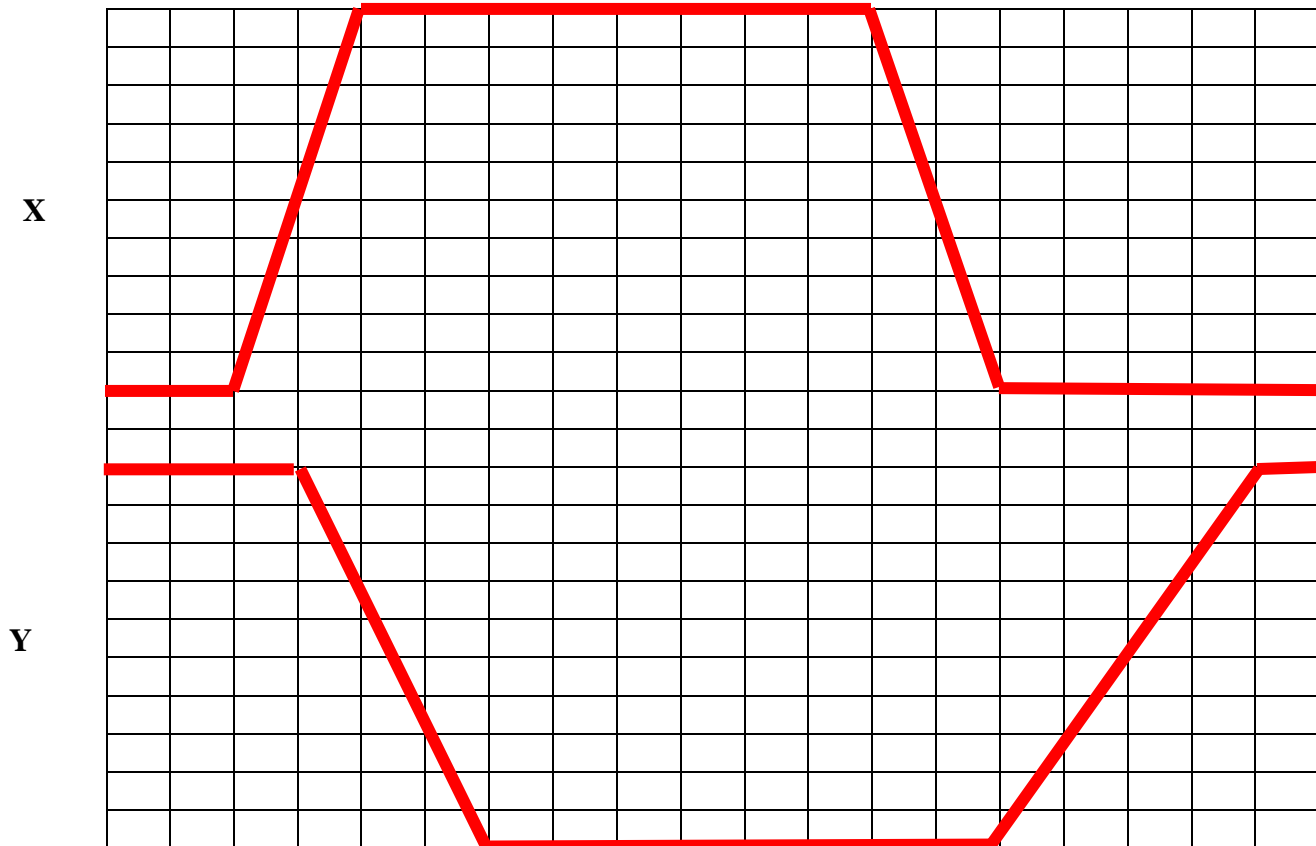
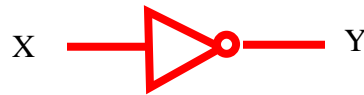
18. This circuit implements the following type of logic gate:
- (A) two-input OR
 - (B) two-input AND
 - (C) two-input NOR
 - (D) two-input NAND
 - (E) none of the above
19. If **A = 5V** and **B = 5V**, the output **F** will be:
- (A) disconnected ("floating" or high impedance)
 - (B) 0 V
 - (C) 2.5 V
 - (D) 5.0 V
 - (E) none of the above
20. If the "on" resistance of both the P-channel and N-channel MOSFETs is **50 Ω** , the amount of power this circuit will dissipate when input **A = 5V** and input **B = GND** is:
- (A) 25 mW
 - (B) 50 mW
 - (C) 250 mW
 - (D) 500 mW
 - (E) none of the above

The following circuit applies to questions 21 through 23:



21. This circuit implements the following type of logic gate:
- (A) two-input OR
 - (B) two-input AND
 - (C) two-input NOR
 - (D) two-input NAND
 - (E) none of the above
22. If the “on” resistance of the MOSFET labeled “ Q_P ” is **200 Ω** and the “on” resistance of the MOSFET labeled “ Q_N ” is **100 Ω** , then if **10 mA** of current is **sourced** in the high state, V_{OH} will be:
- (A) 1 V
 - (B) 2 V
 - (C) 3 V
 - (D) 4 V
 - (E) none of the above
23. If the “on” resistance of the MOSFET labeled “ Q_P ” is **200 Ω** and the “on” resistance of the MOSFET labeled “ Q_N ” is **100 Ω** , then if **10 mA** of current is **sunk** in the low state, V_{OL} will be:
- (A) 1 V
 - (B) 2 V
 - (C) 3 V
 - (D) 4 V
 - (E) none of the above

The following figure applies to questions 24 through 25 (assume each horizontal division is **1 nanosecond**):



  1 ns

24. Based on the definition provided in the course text, the **fall time** (t_{THL}) for the inverter is approximately:

- (A) 1.0 ns
- (B) 1.5 ns
- (C) 2.0 ns
- (D) 3.0 ns
- (E) none of the above

25. The **rise propagation delay** (t_{PLH}) for the inverter is approximately:

- (A) 1.0 ns
- (B) 1.5 ns
- (C) 2.0 ns
- (D) 3.0 ns
- (E) none of the above

26. A “floating” (unconnected) gate input will **most likely** cause the gate’s output to:
- (A) always be high
 - (B) always be low
 - (C) be one-half (50%) of the supply voltage
 - (D) be unpredictable
 - (E) none of the above
27. A CMOS circuit only consumes a **significant** amount of power:
- (A) when warming up
 - (B) when cooling off
 - (C) during output transitions
 - (D) during input transitions
 - (E) none of the above
28. The **primary purpose** of decoupling capacitors is to:
- (A) provide an instantaneous source of current during output transitions
 - (B) increase the output current sourcing/sinking capability
 - (C) prevent V_{OH} from falling below V_{OHmin}
 - (D) prevent V_{OL} from rising above V_{OLmax}
 - (E) none of the above
29. When a gate’s **rated I_{OL}** specification is **exceeded**, the following is likely to happen:
- (A) the V_{OH} of the gate will increase and the t_{TLH} of the gate will decrease
 - (B) the V_{OL} of the gate will decrease and the t_{THL} of the gate will increase
 - (C) the V_{OH} of the gate will decrease and the t_{TLH} of the gate will increase
 - (D) the V_{OL} of the gate will increase and the t_{THL} of the gate will increase
 - (E) none of the above
30. If a CMOS inverter drives a **capacitive load of 100 pF** and the “on” resistance of its P-channel MOSFET is **20 Ω** , then the gate’s output rise time (t_{TLH}) is approximately:
- (A) 0.2 ns
 - (B) 2 ns
 - (C) 20 ns
 - (D) 2000 ns
 - (E) none of the above

Answer key:
1-C, 2-A, 3-C, 4-B, 5-A, 6-B, 7-C, 8-C, 9-B, 10-E, 11-A, 12-C, 13-C, 14-B, 15-B,
16-C, 17-B, 18-E, 19-B, 20-C, 21-B, 22-C, 23-A, 24-A, 25-D, 26-D, 27-C, 28-A,
29-D, 30-B