

Digital System Design Lab

Lab 8

7-Segment Display Exercises

Student ID: D1166506

Name: 周嘉禾

Date: 2023/11/08

1. Objectives

- To learn how to use Verilog to control DE0 panel.

2. Theorem

(1) Verilog Syntax:

Verilog is a hardware description language used to model electronic systems. Its syntax resembles C programming language and is used to describe digital systems, primarily for simulation and synthesis. Verilog describes how digital circuits behave, allowing designers to model complex systems. It includes modules, variables, operators, and control structures, enabling the representation of hardware at various levels of abstraction.

(2) Common Cathode:

In electronics, a common cathode refers to a configuration where multiple diodes, LEDs, or other components share a common connection to the cathode (the negative terminal). For instance, in a common cathode LED display, all the cathodes of the individual LEDs are connected together and tied to the ground, while each LED's anode (the positive terminal) is connected to a separate pin for control.

(3) Common Anode:

Conversely, a common anode configuration involves components sharing a common connection to the anode (the positive terminal). In a common anode LED display, all the anodes of individual LEDs are tied together and connected to a positive voltage source, while each LED's cathode is connected to a separate pin for control.

3. Experimental Results

(1) Step 1

a. Think

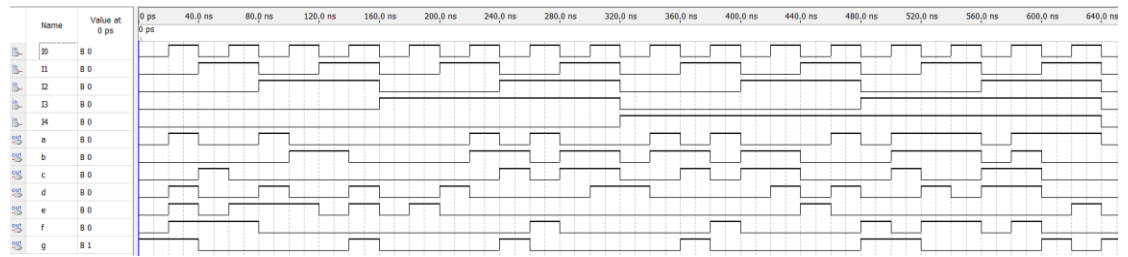
- i. Determine whether I4 is 0 or not.
- ii. According to I4, set led to corresponding pins.
- iii. Fill 7-segment led pins with corresponding graph.

b. Code

```
module step1(I0, I1, I2, I3, I4, a, b, c, d, e, f, g);
    input I0, I1, I2, I3, I4;
    output a, b, c, d, e, f, g;
    reg [6:0] led;

    always @(I0, I1, I2, I3, I4) begin
        if (I4==0)
            case({I3, I2, I1, I0})
                4'b0000: led = 7'b0000001; // 0
                4'b0001: led = 7'b1001111; // 1
                4'b0010: led = 7'b0010010; // 2
                4'b0011: led = 7'b0000110; // 3
                4'b0100: led = 7'b1001100; // 4
                4'b0101: led = 7'b0100100; // 5
                4'b0110: led = 7'b0100000; // 6
                4'b0111: led = 7'b0001101; // 7
                4'b1000: led = 7'b0000000; // 8
                4'b1001: led = 7'b0000100; // 9
                4'b1010: led = 7'b0001000; // A
                4'b1011: led = 7'b1100000; // B
                4'b1100: led = 7'b0110001; // C
                4'b1101: led = 7'b1000010; // D
                4'b1110: led = 7'b0110000; // E
                4'b1111: led = 7'b0111000; // F
                default: led = 7'b1111111; // default
            endcase
        else
            case({I3, I2, I1, I0})
                4'b0000: led = 7'b0001000; // A
                4'b0001: led = 7'b1100000; // B
                4'b0010: led = 7'b0110001; // C
                4'b0011: led = 7'b1000010; // D
                4'b0100: led = 7'b0110000; // E
                4'b0101: led = 7'b0111000; // F
                4'b0110: led = 7'b0000100; // G
                4'b0111: led = 7'b1001000; // H
                4'b1000: led = 7'b0000011; // J
                4'b1001: led = 7'b1110001; // L
                4'b1010: led = 7'b1101010; // N
                4'b1011: led = 7'b1100010; // O
                4'b1100: led = 7'b0001100; // P
                4'b1101: led = 7'b1111010; // R
                4'b1110: led = 7'b1000001; // U
                4'b1111: led = 7'b1000100; // Y
                default: led = 7'b1111111; // default
            endcase
        end
        assign {a, b, c, d, e, f, g} = led;
    end
endmodule
```

c. Simulation



(2) Step 2

a. Think

- Determine whether I0 is 0 or not.
- According to I4, set led to corresponding pins(U or A).
- Fill 7-segment led pins with corresponding graph
- Always show the greatest number if I0 is 1.

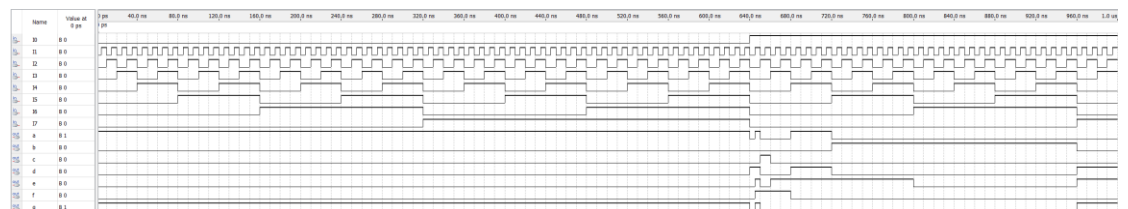
b. Code

```
module step2(I0, I1, I2, I3, I4, I5, I6, I7, a, b, c, d, e, f, g);
input I0, I1, I2, I3, I4, I5, I6, I7;
output a, b, c, d, e, f, g;
reg [6:0] led;

always @(I0, I1, I2, I3, I4, I5, I6, I7) begin
    if (I0==0)
        led = 7'b1000001;

    // U
    else
        casez({I7, I6, I5, I4, I3, I2, I1})
            7'b0000001: led = 7'b1001111; // 1
            7'b000001?: led = 7'b0010010; // 2
            7'b00001??: led = 7'b0000110; // 3
            7'b0001??: led = 7'b1001100; // 4
            7'b001??: led = 7'b0100100; // 5
            7'b01??: led = 7'b0100000; // 6
            7'b1??: led = 7'b0001101; // 7
            default: led = 7'b0001000; // A
        endcase
    end
    assign {a, b, c, d, e, f, g} = led;
endmodule
```

c. Simulation



4. Comments

The 7-segment display should be common anode since it uses sinking current to drive the display and makes leds lighted. (i.e. 0 to turn on led, and 1 to turn off led)

5. Problems & Solutions

None

6. Feedback

None