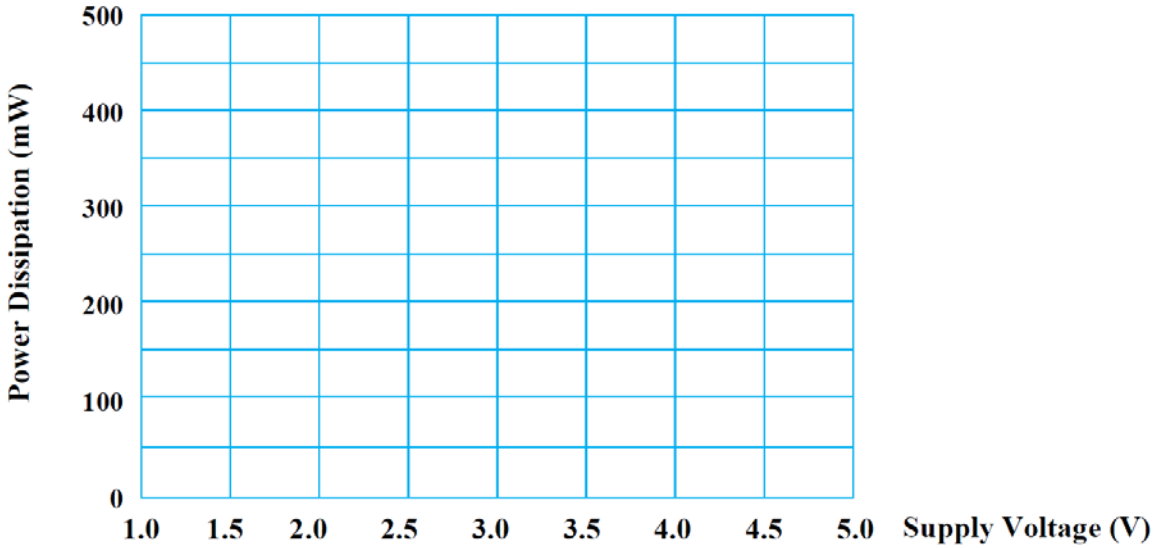
ISTM 214 Homework 4 (Due day: 10/24)

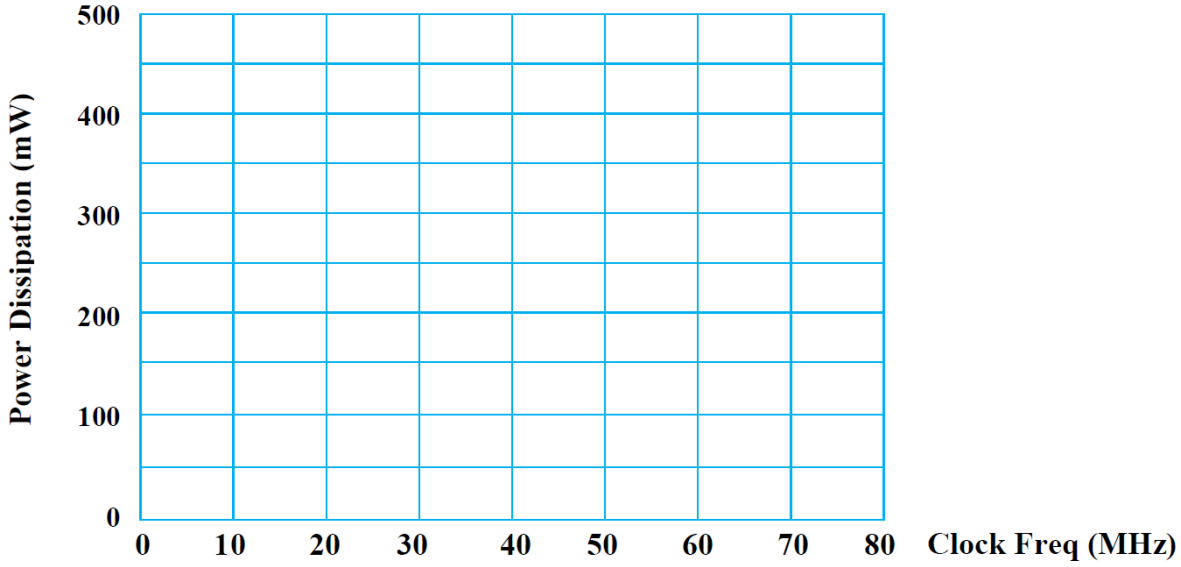
Name:_____ ID:_____

1. A particular CMOS microcontroller is designed to operate over a supply voltage range of **1.0 V** to **5.0 V** and at a maximum clock frequency of **80 MHz** (no minimum clock frequency is specified). The *maximum power dissipation* over this range of supply voltage and clock frequency is specified to be **450 milliwatts**.

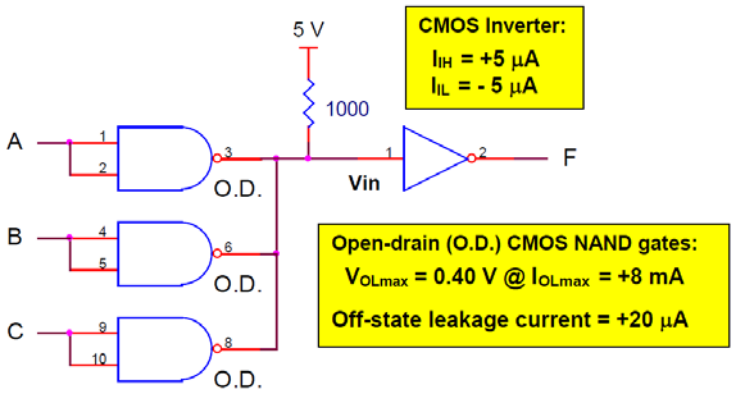
(a) Plot the relationship between power dissipation and supply voltage for this microcontroller



(b) Plot the relationship between power dissipation and clock frequency for this microcontroller



2. Given the circuit below, calculate V_{in} (the CMOS inverter input voltage) for each of the cases indicated along with the current individually sunk by each active open drain gate. Show your calculations.



A	B	C	O.D. Equivalent ON Resistance	V_{in} to Inverter	Current Sunk by Each Active O.D. Gate
0 V	0 V	0 V			
5 V	0 V	0 V			
5 V	5 V	0 V			
5 V	5 V	5 V			

3. Given the circuit, below, along with its Vi-Vo (input – output voltage) relationship, determine the following (show calculations where applicable):

a. estimate the ON resistance of the O.D. NAND gate

b. estimate the value of the pull-up resistor

c. estimate the t_{PHL} of the O.D. NAND gate

d. estimate the t_{PLH} of the O.D. NAND gate