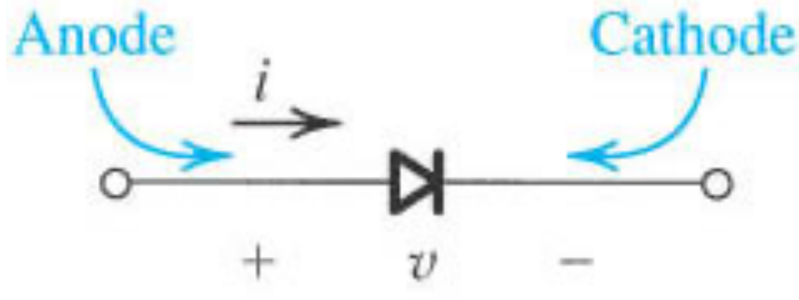
Topic 3

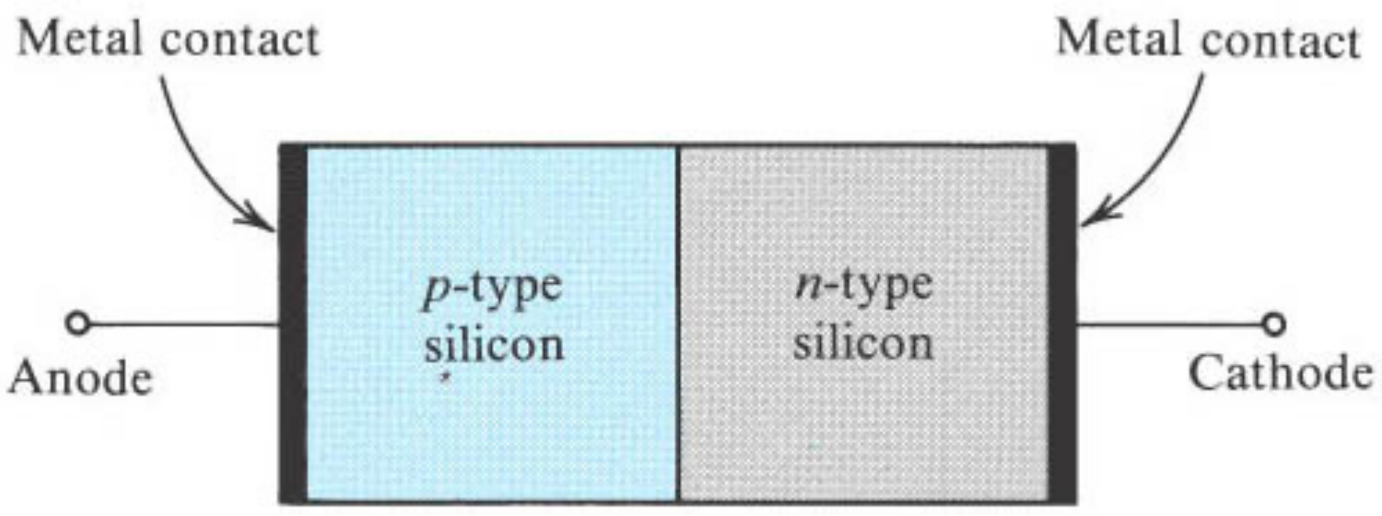
Semiconductors and the pn Junction

Physical Operation of Diodes

Symbol of Diode



Simplified physical structure of the junction diode



Semiconductor ?

3.1 Intrinsic Semiconductors

Intrinsic Semiconductors

- **silicon atom**
  - four valence electrons
  - requires four more to complete outermost shell
  - each pair of shared forms a covalent bond
  - the atoms form a lattice structure

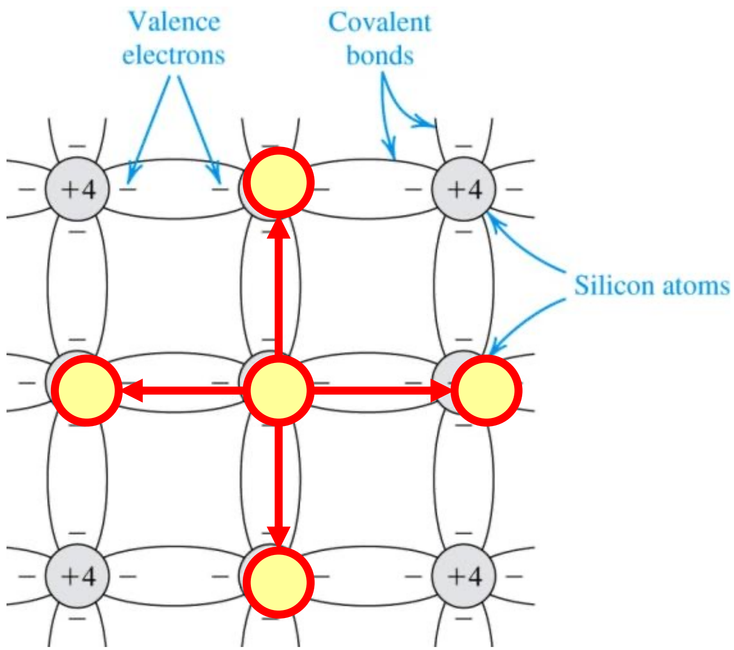


Figure 1.28 Two-dimensional representation of the silicon crystal. The circles represent the inner core of silicon atoms, with +4 indicating its positive charge of +4*q*, which is neutralized by the charge of the four valence electrons. Observe how the covalent bonds are formed by sharing of the valence electrons. At 0K, all bonds are intact and no free electrons are available for current conduction.

Figure 3.1 Two-dimensional representation of the silicon crystal. The circles represent the inner core of silicon atoms, with +4 indicating its positive charge of +4q, which is neutralized by the charge of the four valence electrons. Observe how the covalent bonds are formed by sharing of the valence electrons.

At 0 K, all bonds are intact and no free electrons are available for current conduction.

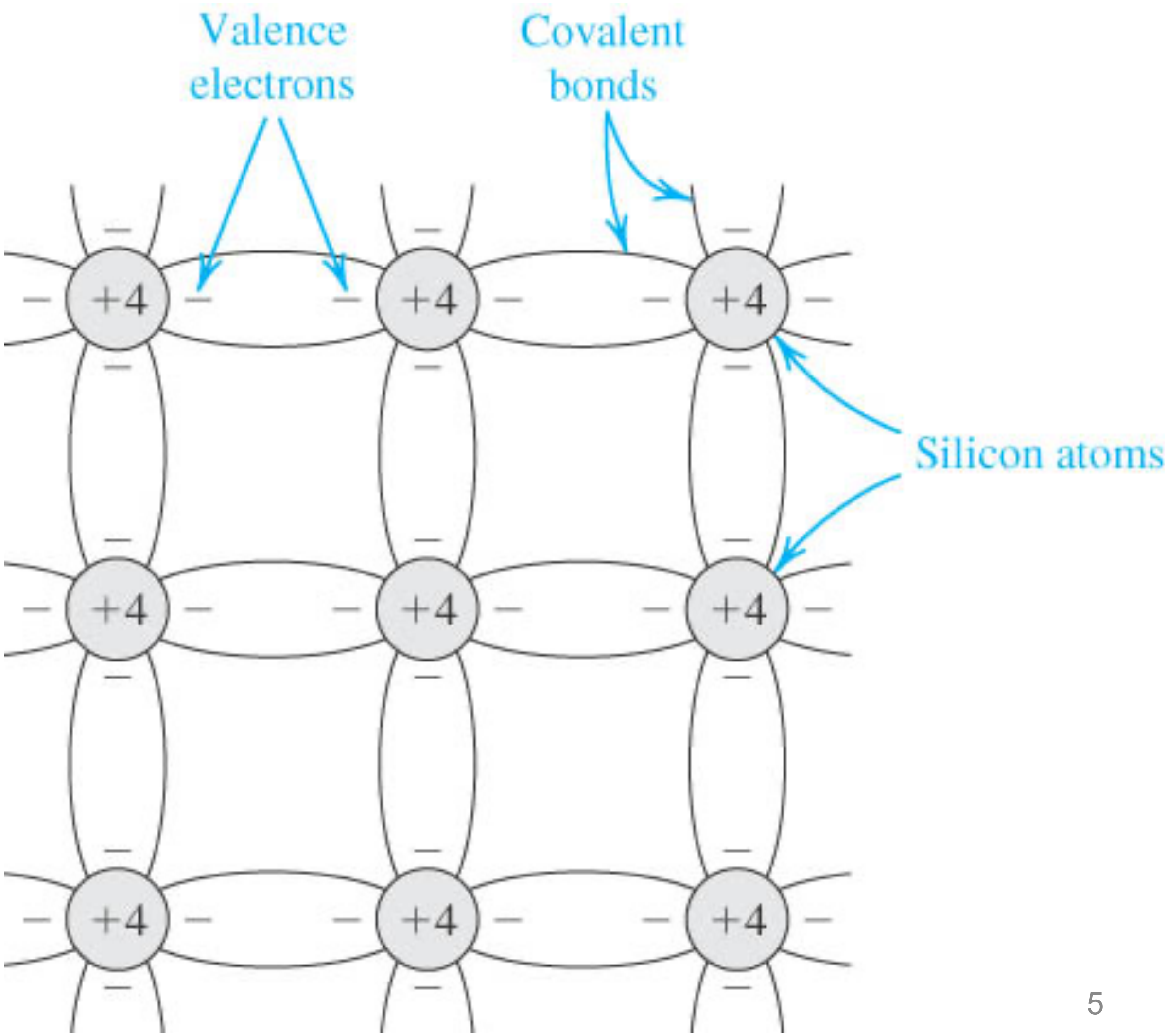
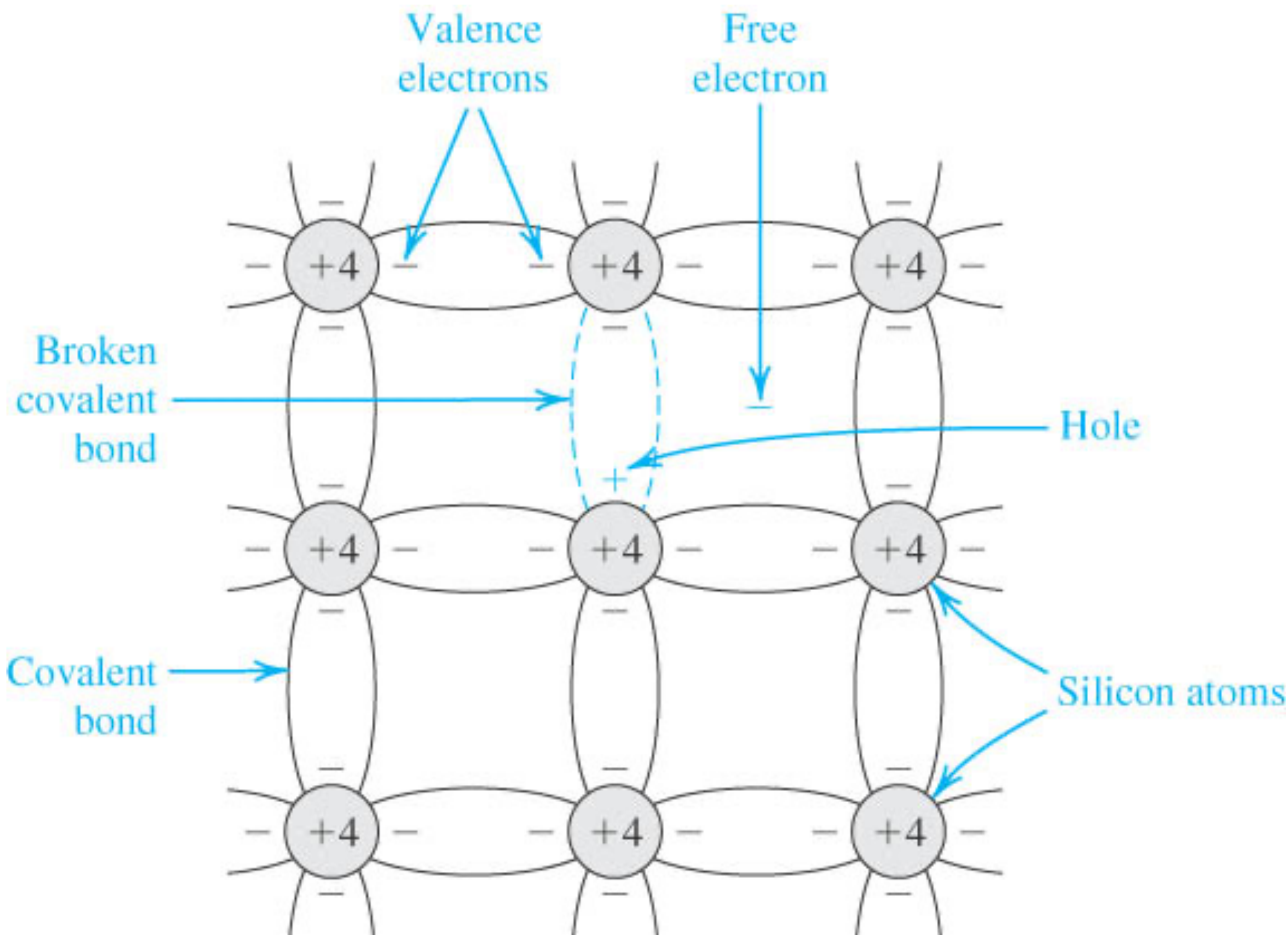
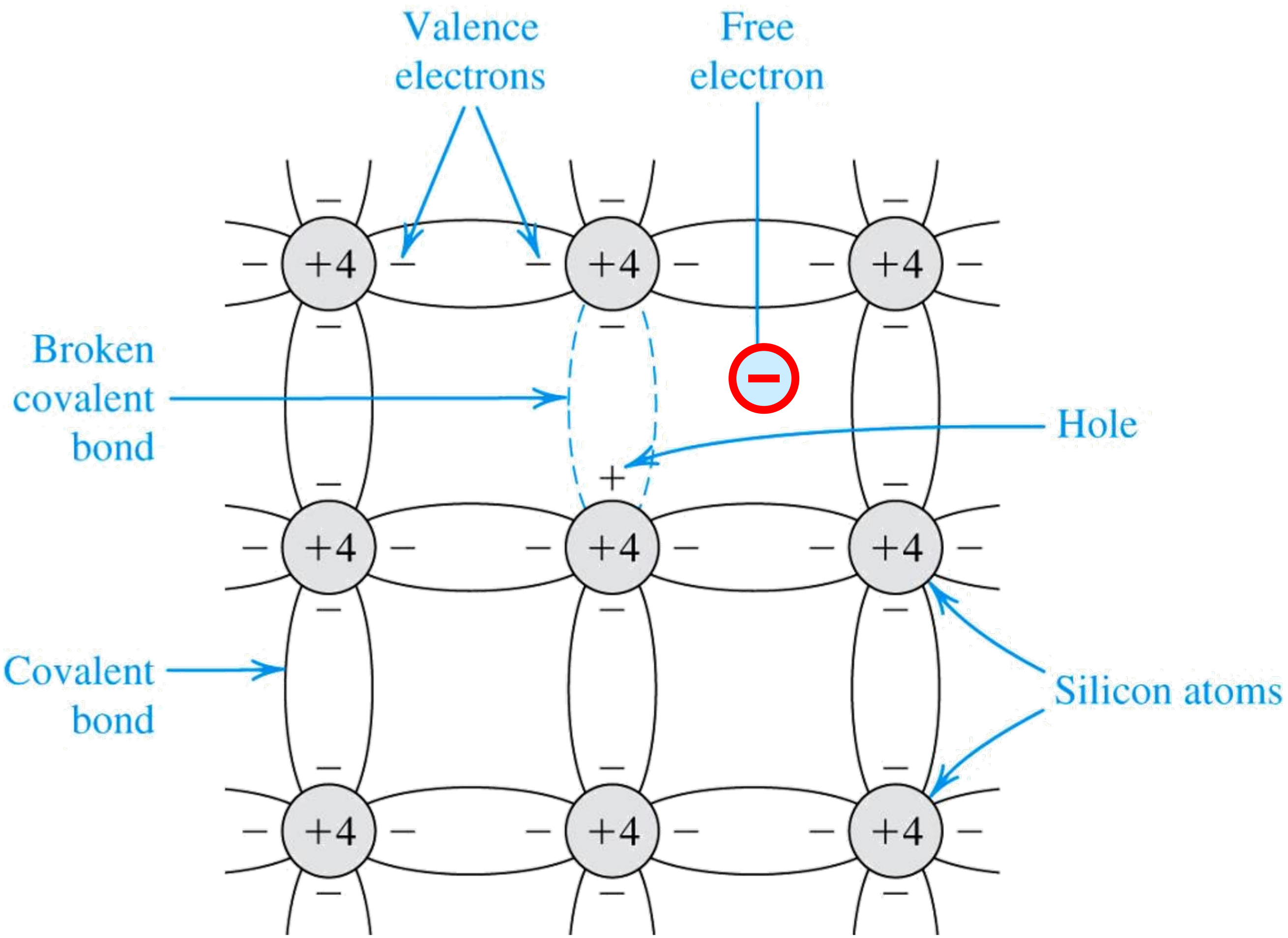


Figure 3.2 **At room temperature**, some of the covalent bonds are broken by thermal ionization. Each broken bond gives rise to a **free electron** and a **hole**, both of which become available for current conduction.




Valence electrons
Free electron
Broken covalent bond
Hole
Covalent bond
Silicon atoms
+4
+4
+4
+4
+4
+4
+4
+4
+4

Intrinsic Semiconductors

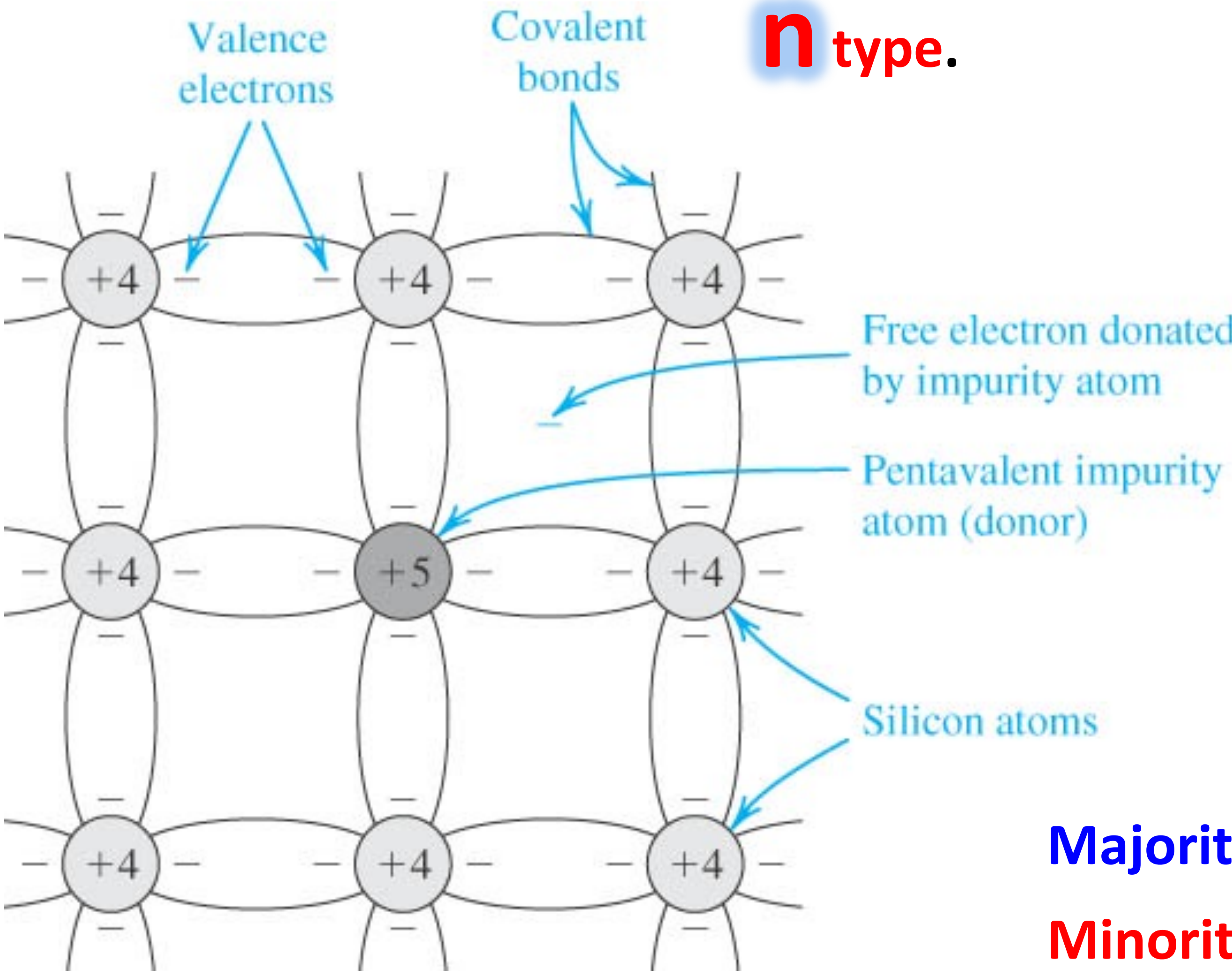
The process of freeing electrons, creating holes, and filling them **facilitates current flow**…

- silicon at low temps
  - all covalent bonds – are intact
  - no electrons – are available for conduction
  - conductivity – is zero
- silicon at room temp
  - some covalent bonds – break, freeing an electron creating hole, due to thermal energy
  - some electrons – will wander from thei oms, becoming available for conduction
  - conductivity – is greater than zero

3.2 Doped Semiconductors

Figure 3.3 A silicon crystal doped by a **pentavalent** element.

Each dopant atom donates a free electron and is thus called a donor. The doped semiconductor becomes **n** type.

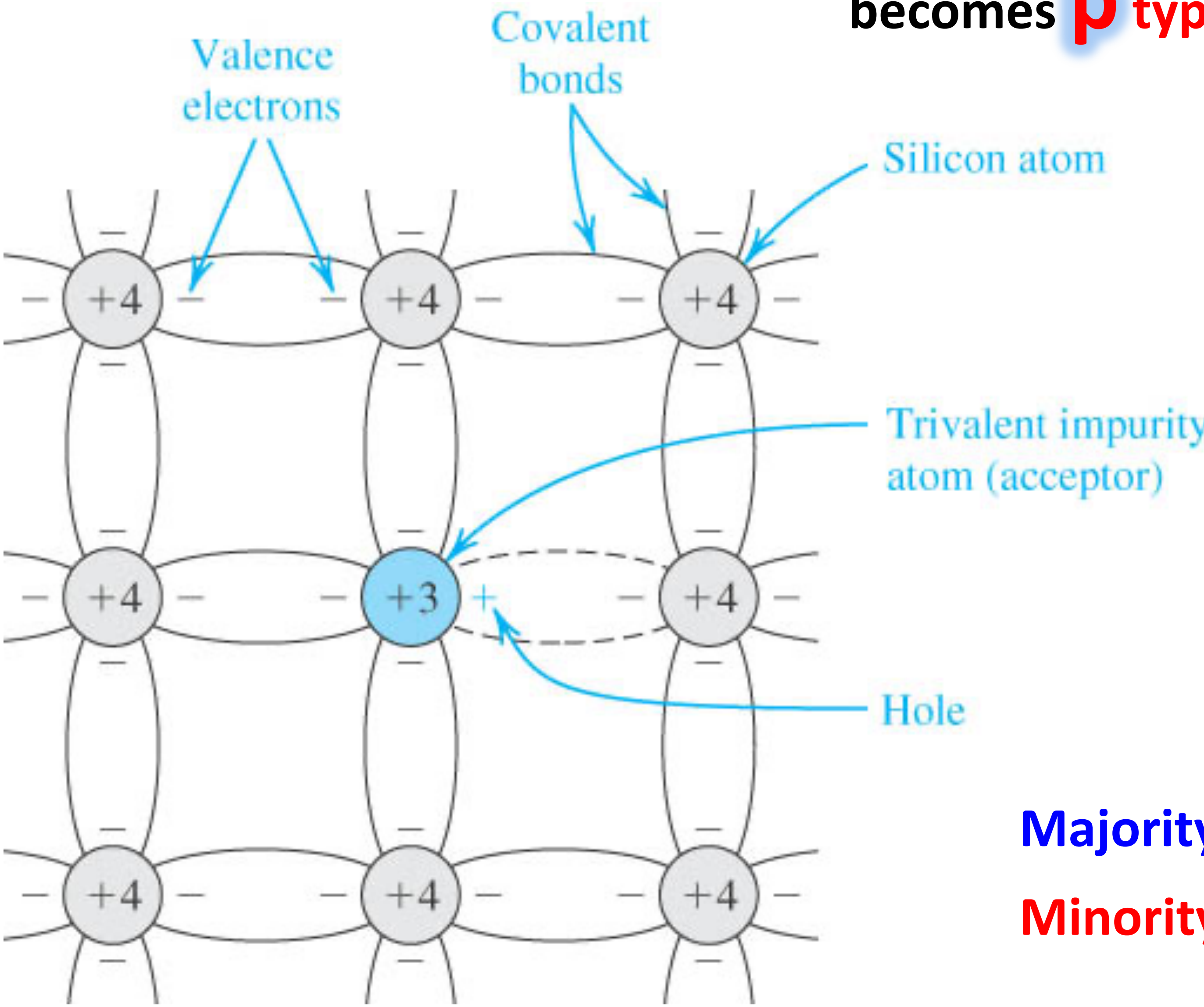


Majority: Electrons

Minority: Holes

Figure 3.4 crystal doped with a trivalent impurity.

Each dopant atom gives rise to a hole, and the semiconductor becomes p type.

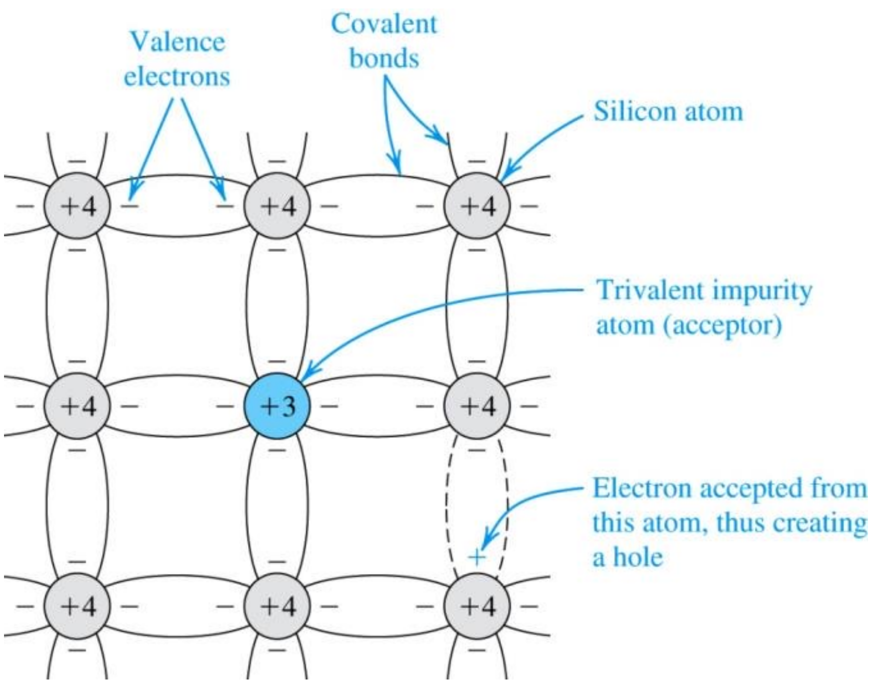


Majority: Holes

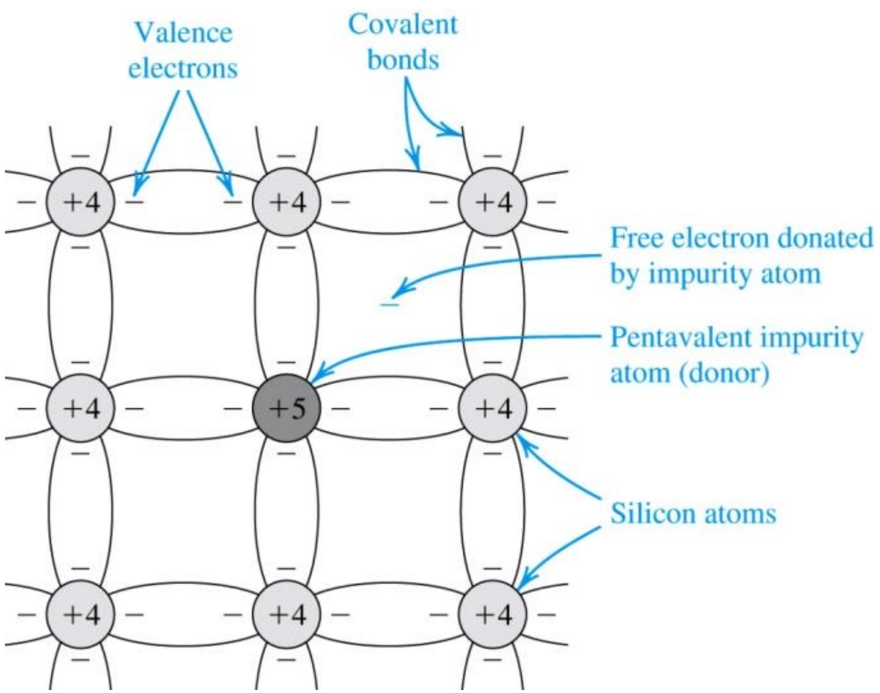
Minority: Electrons

Doped Semiconductors

- ***p*-type semiconductor**



- ***n*-type semiconductor**



3.3 Current Flow in Semiconductors

Figure 3.5 **A bar of intrinsic silicon (a) in which the hole concentration profile shown in (b) has been created along the *x*-axis by some unspecified mechanism.**

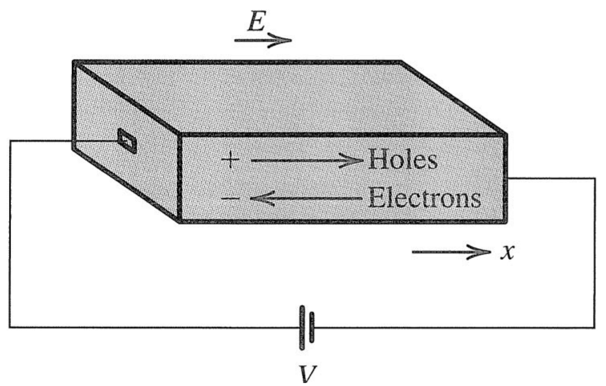
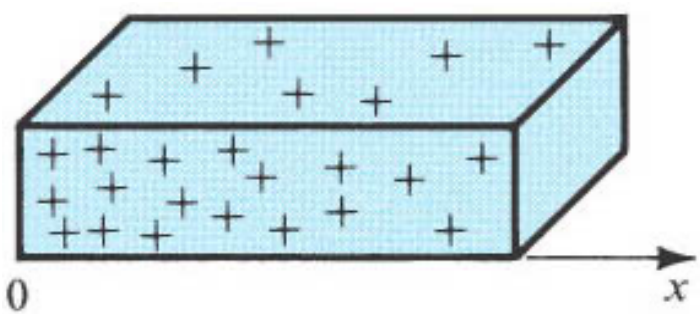
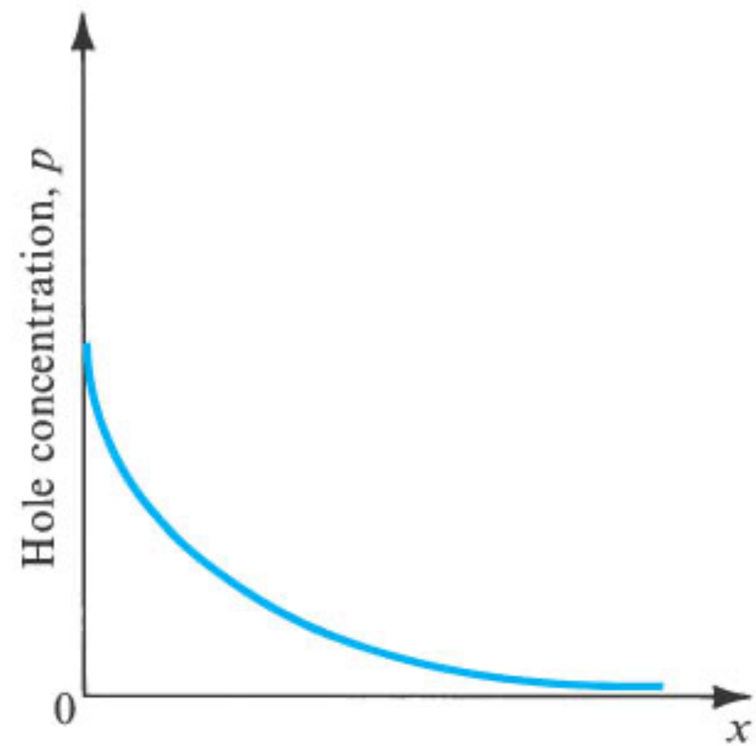


Figure 1.32 An electric field E established in a bar of silicon causes the holes to drift in the direction of E and the free electrons to drift in the opposite direction. Both the hole and electron drift currents are in the direction of E.



(a)



(b)

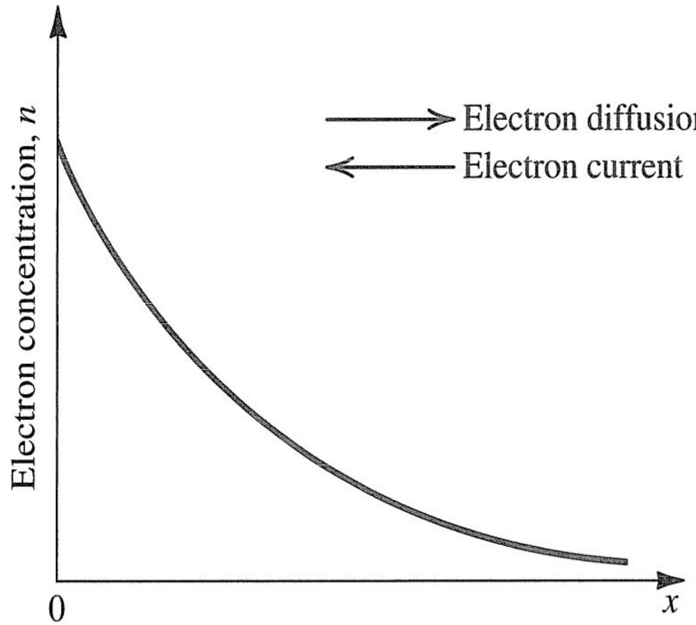


Figure 1.34 If the electron-concentration profile shown is established in a bar of silicon, electrons diffuse in the x direction, giving rise to an electron-diffusion current in the negative -x direction.

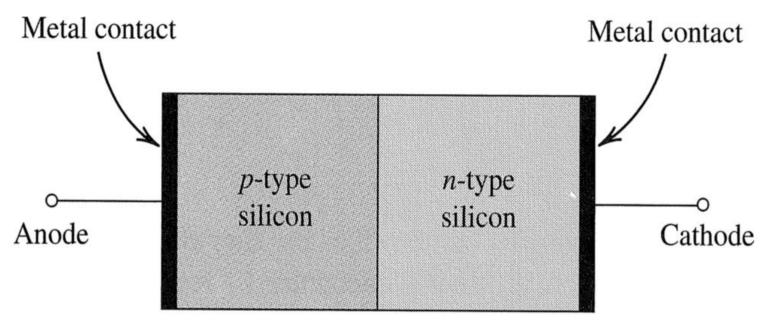


Figure 1.35 Simplified physical structure of the *pn* junction. (Actual geometries are given in Appendix A.) As the *pn* junction implements the junction diode, its terminals are labeled anode and cathode.

3.4 The pn Junction with open-circuit Terminals

3.4 The pn Junction with open-circuit Terminals

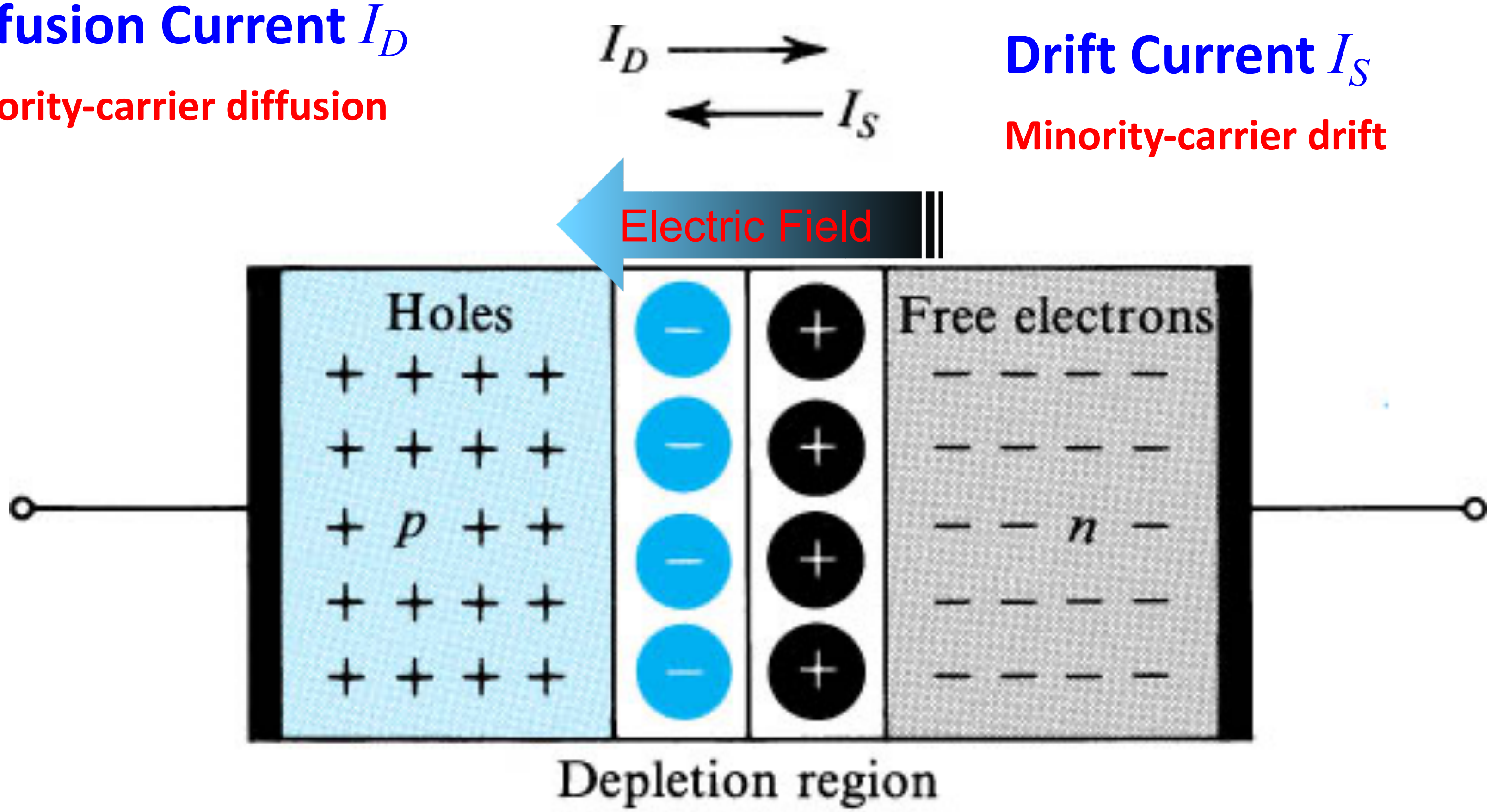
Figure 3.9 The *pn* junction with no applied voltage

Diffusion Current I_D

Majority-carrier diffusion

Drift Current I_S

Minority-carrier drift



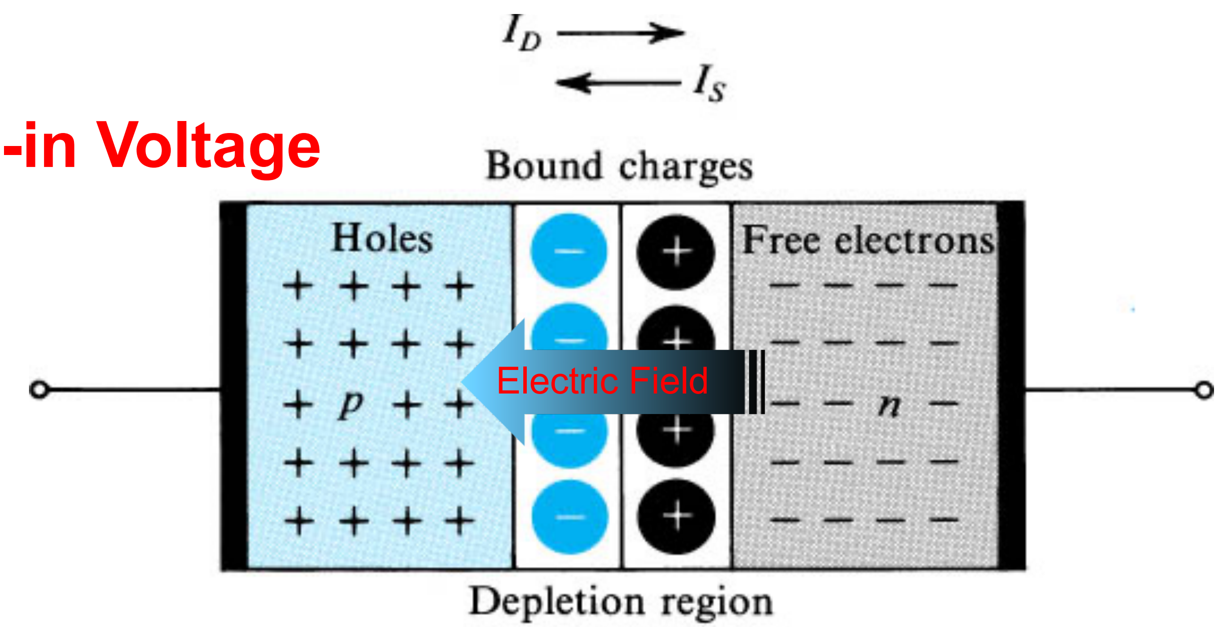
Depletion Region: depleted of free electrons

Figure 1.36

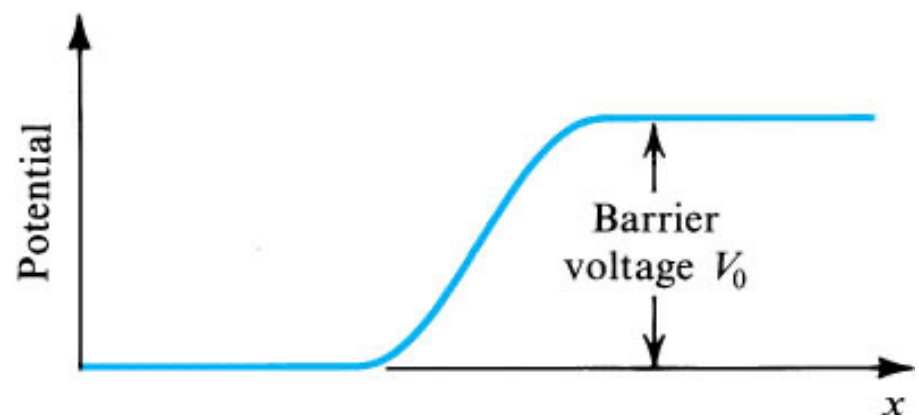
The Junction Built-in Voltage

$I_D = I_S$

Equilibrium



(a) The *pn* junction with no applied voltage (open-circuited terminals).



(b) The potential distribution along an axis perpendicular to the junction.

Note that the magnitude of drift current (I_S) is unaffected by level of diffusion and / or V_0. It will be, however, affected by temperature.

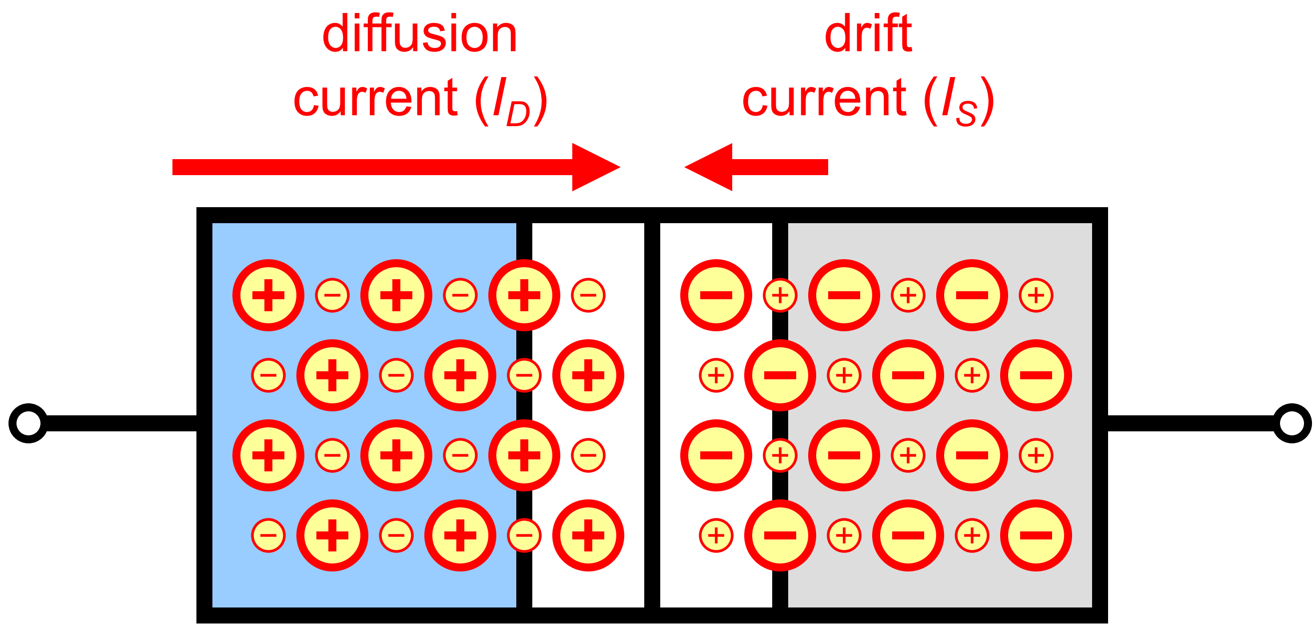


Figure: The *pn* junction with no applied voltage (open-circuited terminals).

3.5 The pn Junction with an Applied Voltage

Figure 3.13 The *pn* junction excited by a constant-current source supplying a current *I* in the **forward direction**. The **depletion layer narrows** and the **barrier voltage decreases** by *V* volts, which appears as an external voltage in the **forward direction**.

Forward bias

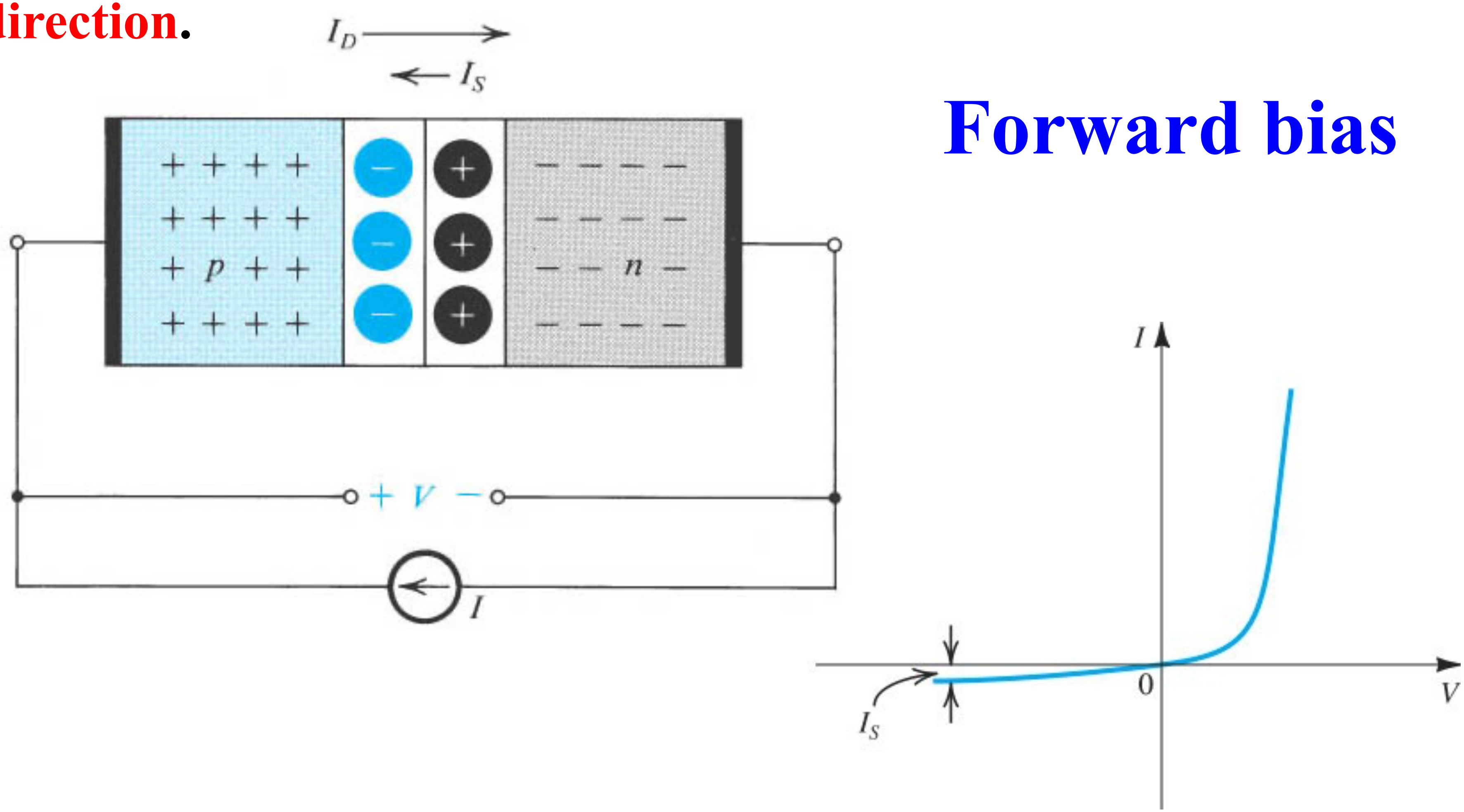
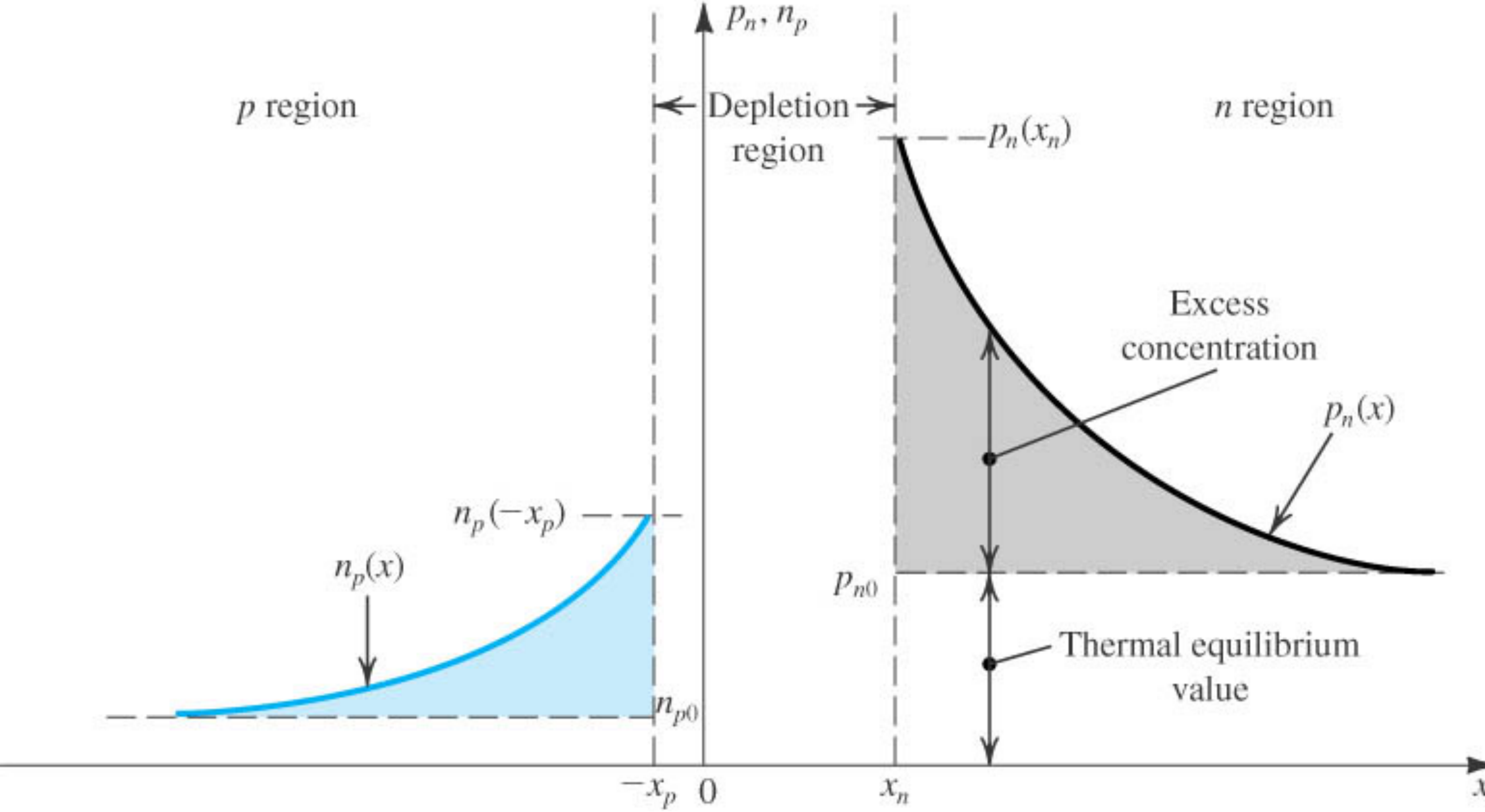
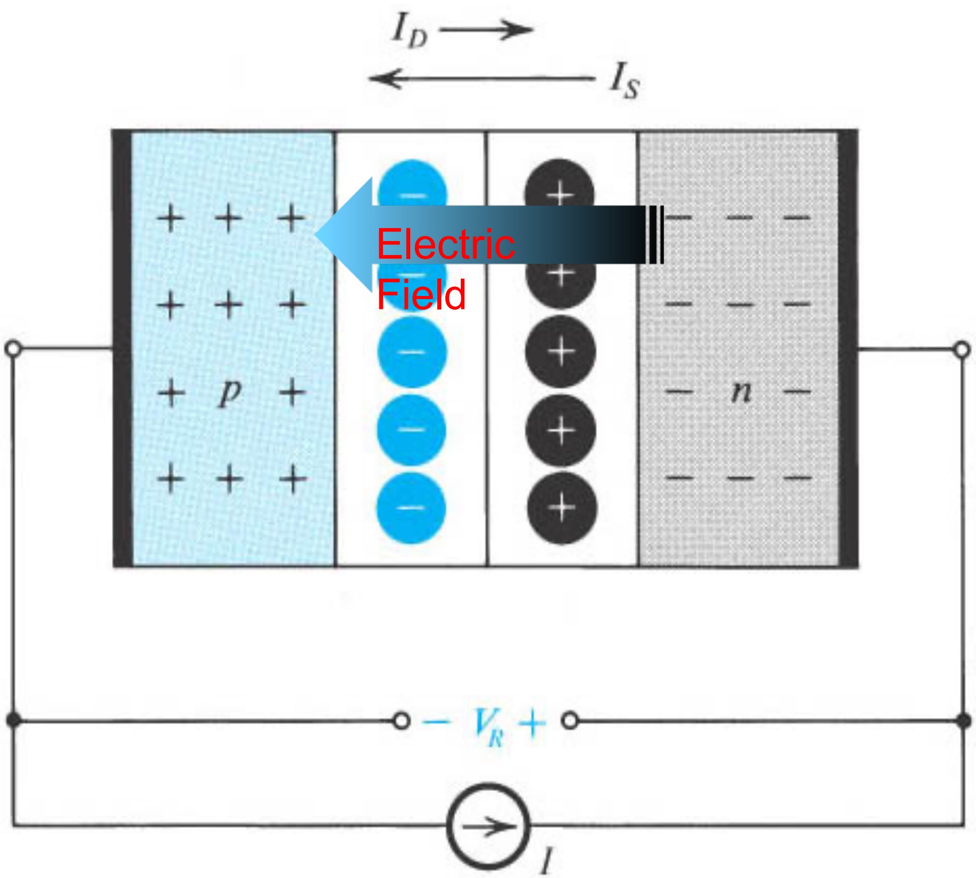


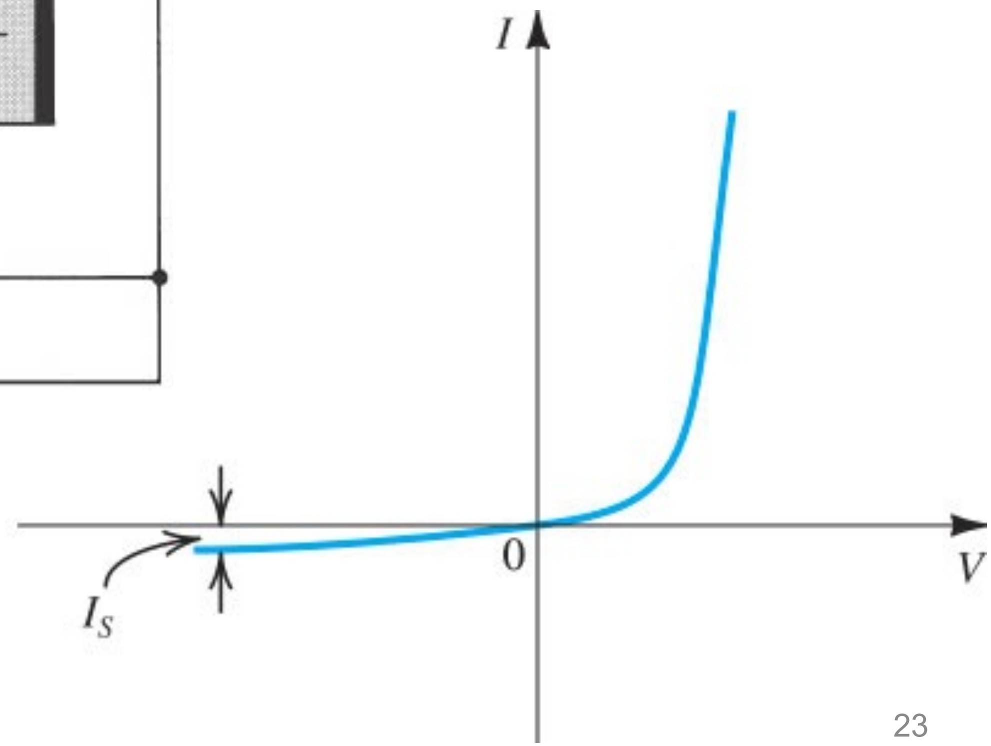
Figure 3.50 Minority-carrier distribution in a forward-biased *pn* junction. It is assumed that the *p* region is more heavily doped than the *n* region; $N_A >> N_D$.



The *pn* junction excited by a constant-current source I in the reverse direction. To avoid breakdown, I is kept smaller than I_S.

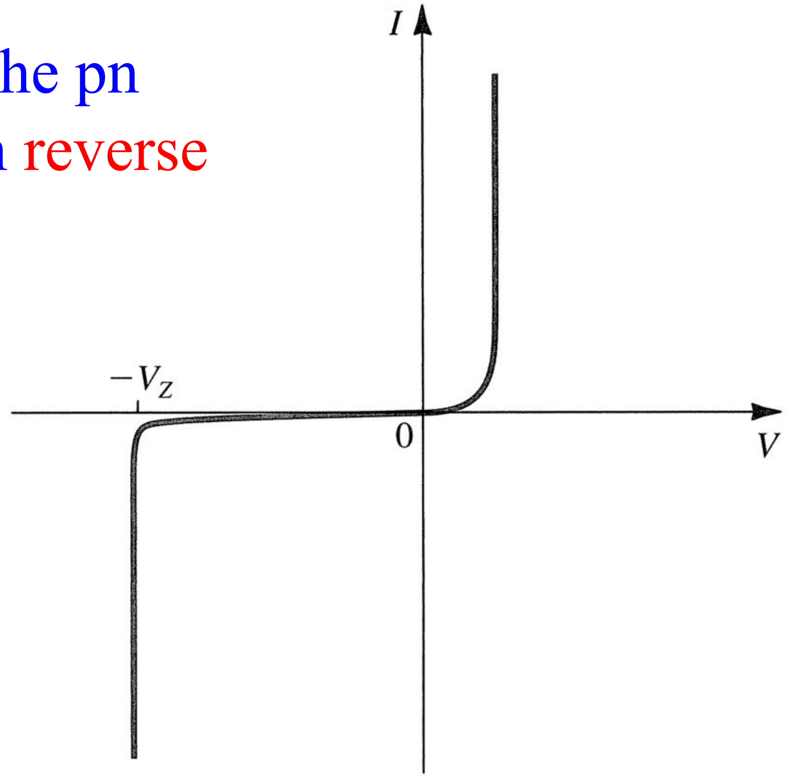


The depletion layer widens and the barrier voltage increases by V_R volts, which appears between the terminals as a reverse voltage.



Reverse bias

Figure 3.14 The I-V characteristic of the pn junction showing the rapid increase in reverse current in the breakdown region.



Reverse breakdown

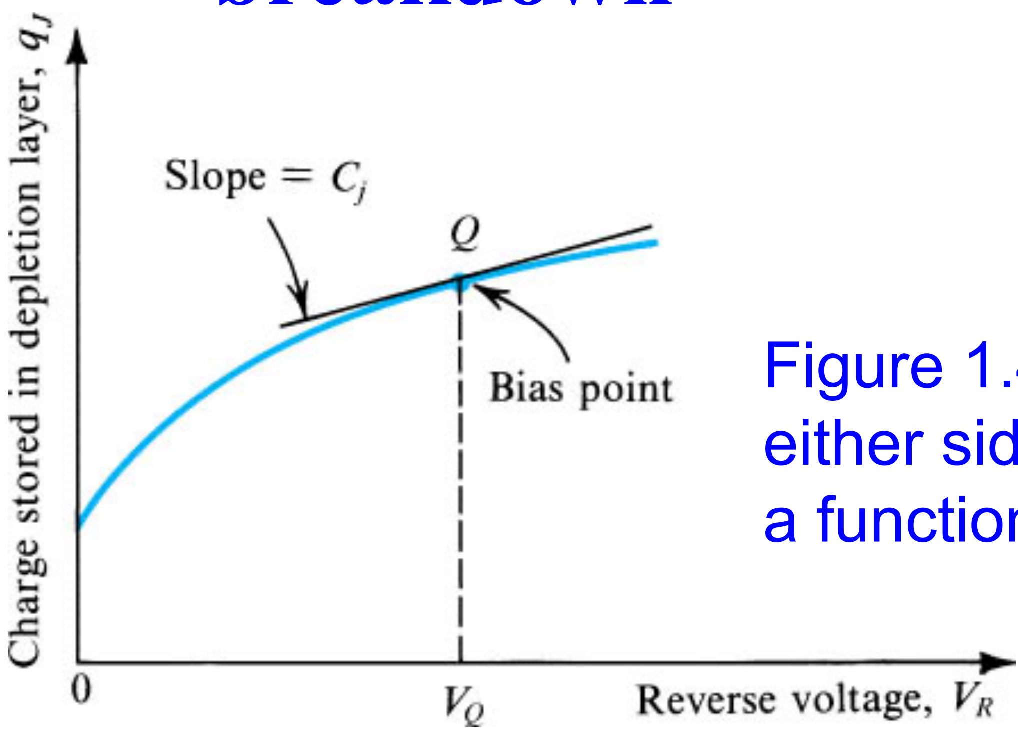
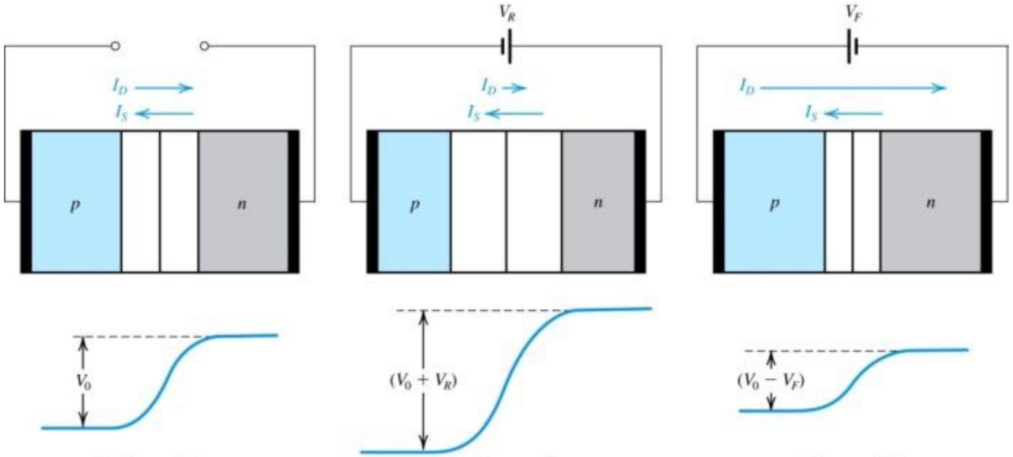


Figure 1.42 The charge stored on either side of the depletion layer as a function of the reverse voltage V_R

Qualitative Description of Junction Operation

- Figure to right shows *pn*-junction under three conditions:
  - open-circuit
    - barrier voltage V_0 exists.
  - reverse bias
    - dc voltage V_R is applied.
  - forward bias
    - dc voltage V_F is applied.



(a) Open-circuit (Equilibrium)
(b) Reverse Bias
(c) Forward Bias

The *pn* junction in:
(a) equilibrium;
(b) reverse bias;
(c) forward bias.

1) no voltage applied

2) voltage differential across depletion zone is V_0

3) $I_D = I_S$

1) negative voltage applied

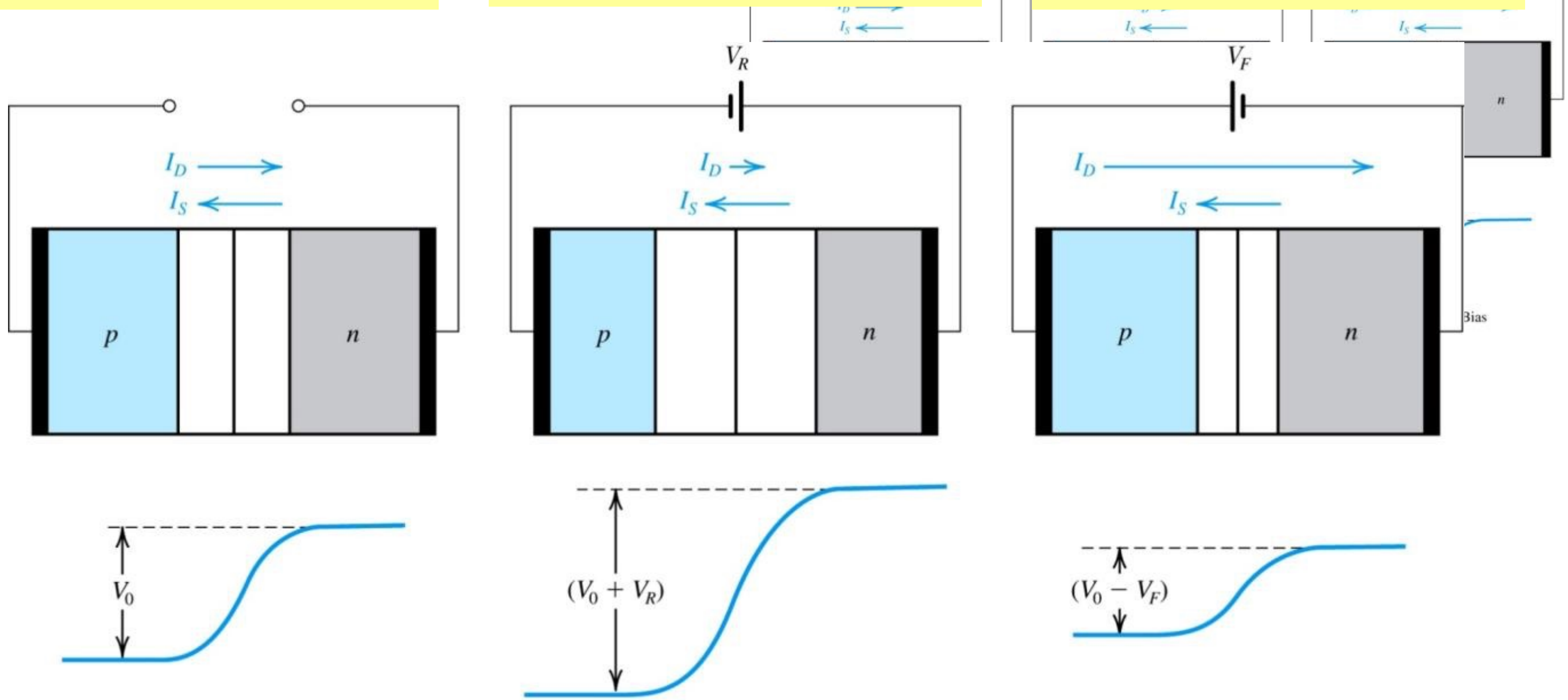
2) voltage differential across depletion zone is $V_0 + V_R$

3) $I_D < I_S$

1) positive voltage applied

2) voltage differential across depletion zone is $V_0 - V_F$

3) $I_D > I_S$



(a) Open-circuit (Equilibrium)

(b) Reverse Bias

(c) Forward Bias

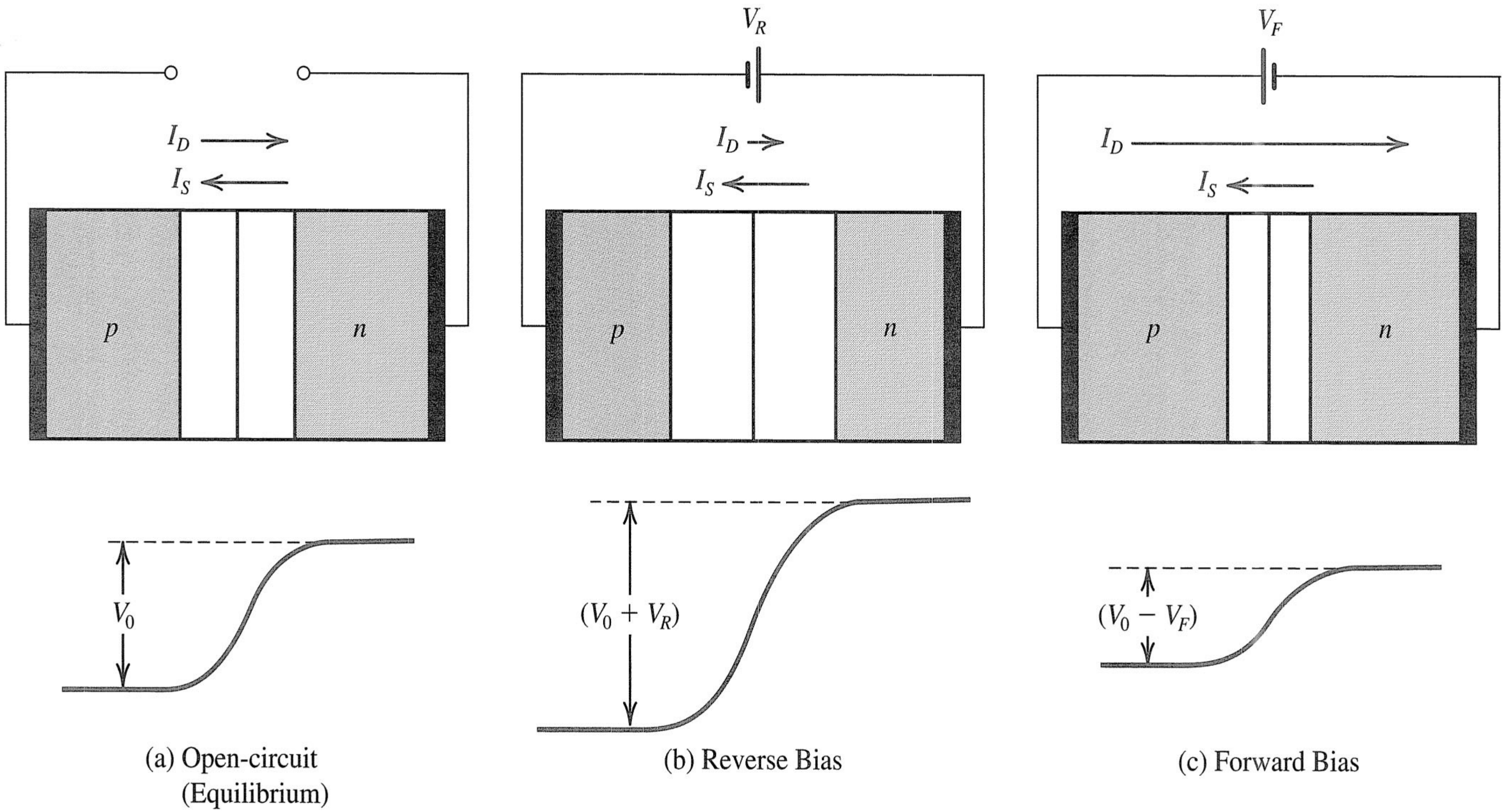


Figure 1.38 The *pn* junction in: **(a)** equilibrium; **(b)** reverse bias; **(c)** forward bias.