

# Digital System Design Lab

## Lab 15 A Guessing Game

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## 1. Objectives

- To become familiar with Verilog control
- To learn how to build pseudo-random combination with LFSR

## 2. Theorem

A Linear Feedback Shift Register (LFSR) is a type of shift register used in computing, where the input bit is a linear function of its previous state. The most commonly used linear function of single bits is exclusive-or (XOR). As a result, an LFSR is often a shift register whose input bit is driven by the XOR of some bits of the overall shift register value.

The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the stream of values produced by the register is completely determined by its current (or previous) state.

LFSRs have a wide range of applications, including generating pseudo-random numbers, pseudo-noise sequences, fast digital counters, and whitening sequences. They can be implemented in both hardware and software.

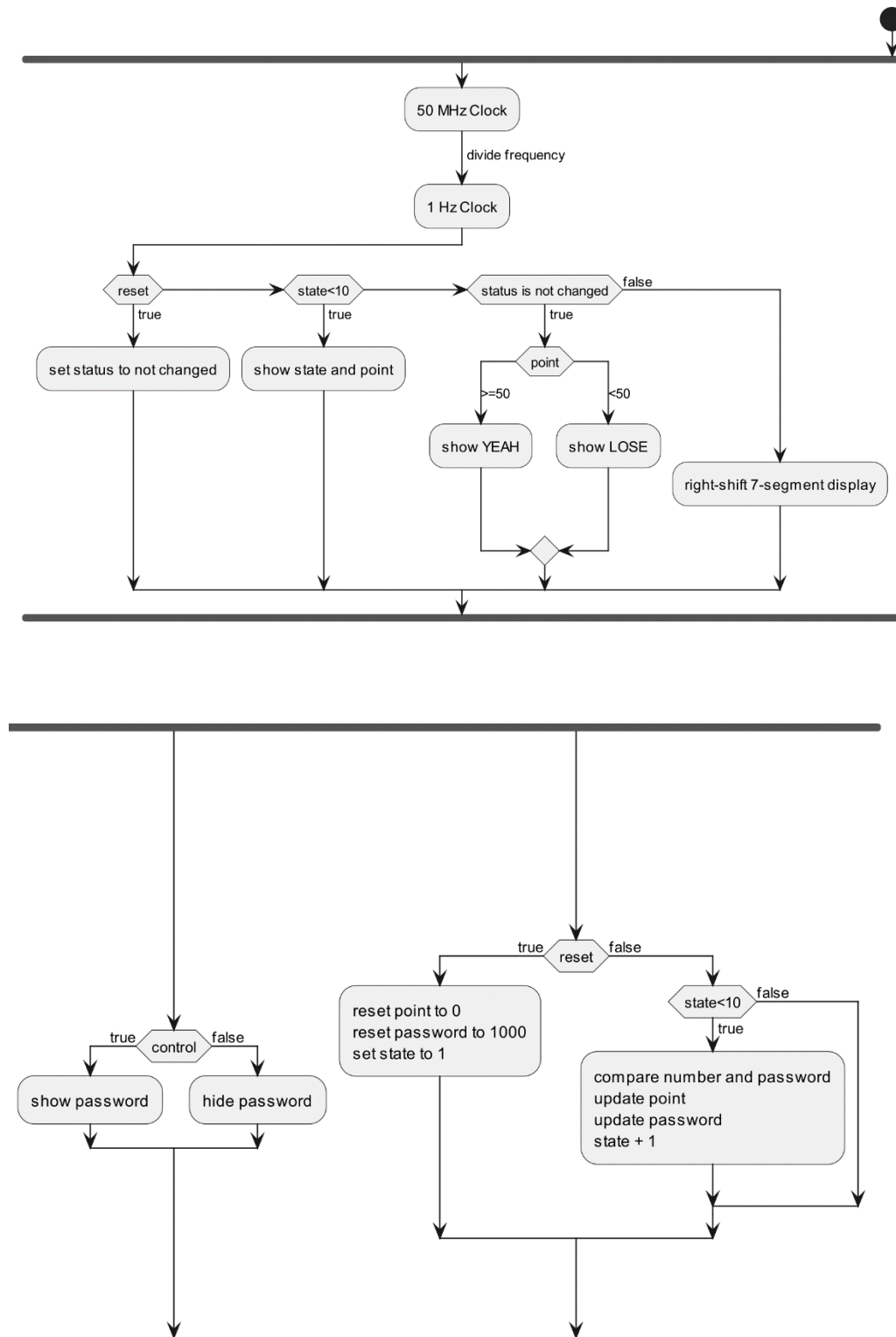
The bit positions that affect the next state are called the taps. In a maximum-length LFSR, it produces an m-sequence (i.e., it cycles through all possible  $2^m - 1$  states within the shift register except the state where all bits are zero), unless it contains all zeros, in which case it will never change.

It's worth noting that the mathematics of a cyclic redundancy check, used to provide a quick check against transmission errors, are closely related to those of an LFSR.

In summary, LFSRs are a powerful tool in digital systems for their ability to generate sequences that appear random and have very long cycles, making them useful in a variety of applications.

### 3. Experimental Results

#### (1) Flow Chart



## (2) Code

```
module step_4(clock, reset, control, number, led, HEX3, HEX2, HEX1,
HEX0, clock_50M);
    input clock, reset, control, clock_50M;
    input signed[3:0] number;
    output reg[3:0] led;
    output reg[0:6] HEX3, HEX2, HEX1, HEX0;

    reg [7:0] point=0, temp_point=0;
    reg Q=1'b0, last_Q=1'b0;
    reg change=1'b0;
    reg signed[3:0] password;
    integer count=0, state=1;

    initial begin
        password = 4'b1000;
    end

    function [0:6] converted_led;
        input [3:0] number;

        begin
            case (number)
                0: converted_led = 7'b0000001; // 0
                1: converted_led = 7'b1001111; // 1
                2: converted_led = 7'b0010010; // 2
                3: converted_led = 7'b0000110; // 3
                4: converted_led = 7'b1001100; // 4
                5: converted_led = 7'b0100100; // 5
                6: converted_led = 7'b0100000; // 6
                7: converted_led = 7'b0001101; // 7
                8: converted_led = 7'b0000000; // 8
                9: converted_led = 7'b0000100; // 9
                10: converted_led = 7'b0001000;

            // A
            default: converted_led = 7'b1111111;

            // default
            endcase
        end
    endfunction

    // password
    always @(posedge clock or negedge reset) begin
        if (!reset) password <= 4'b1000;
        else password <= {password[1]^password[0],
password[3:1]};
    end

    // state
    always @(posedge clock or negedge reset) begin
        if (!reset) state = 1;
        else if (state+1<=10) state = state + 1;
    end

    // point
    always @(posedge clock or negedge reset) begin
        if (!reset) point <= 8'b00000000;
        else if (state<10) begin
            if (number==password) temp_point = 9;
            else if (number<password) temp_point = 4;
            else temp_point = 0;
        end
    end
endmodule
```



#### **4. Comments**

None

#### **5. Problems & Solutions**

None

#### **6. Feedback**

None