Design and Commissioning of the CTF3 Phase Feedforward System

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Abstract

The arrival time of the correction signal (drive voltage) and the beam at the two kickers must be precisely synchronised. The beam time of flight between the upstream phase monitors and the first kicker is 380 ns. In comparison, the total PFF system latency was estimated to be around 335 ns, with the largest contribution being the 175 ns signal transit time in the cables between the amplifiers and kickers. [TODO: Latency breakdown table?] The DAC output of the FONT5a board can be delayed in steps of 2.8 ns (the ADC clock frequency) to align the correction with the beam.

The required output delay has been verified by observing the amplifier monitoring signals and beam based measurements.

ACKNOWLEDGMENTS

We wish to acknowledge Alessandro Zolla and Giancarlo Sensolini (INFN Frascati) for their work on the mechanical design of the phase monitors and kickers, Alexandra Andersson, Luca Timeo and Stephane Rey (CERN) for their work on the phase monitor electronics, and everyone involved in the operation of CTF3 for their help and support in realising the PFF system.

[1] M. Aicheler *et al.*, "A multi-TeV linear collider based on CLIC technology: CLIC conceptual design report," CERN-2012-007 (2012).

[2] A. Gerbershagen *et al.*, Phys. Rev. AB **18**, 041003 (2015).

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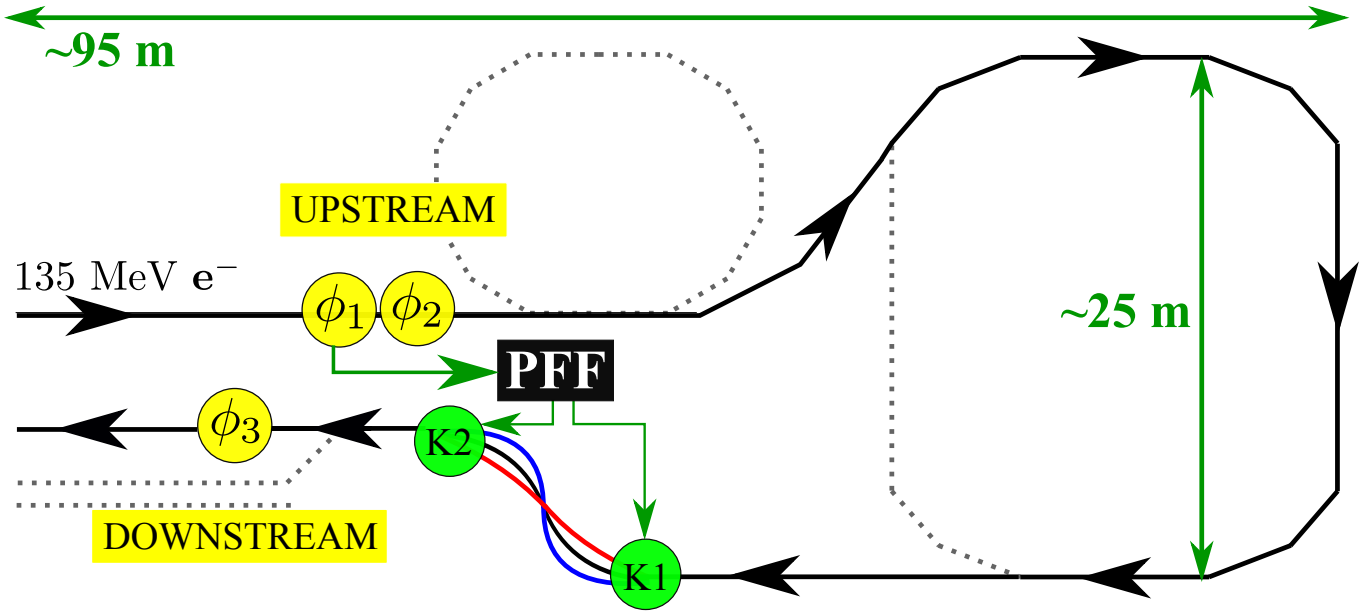

FIG. 1. Schematic of the PFF prototype at CTF3, showing the phase monitors (ϕ_1 , ϕ_2 and ϕ_3) and kickers (K1 and K2). The black box PFF represents the calculation and output of the correction, including the phase monitor electronics, feedforward controller and kicker amplifiers. Dashed lines indicate beam lines that are not used during PFF operation. Bunches arriving early at the upstream monitor (ϕ_1) are directed on to longer trajectories in the correction chicane (blue), and bunches arriving late on to shorter trajectories (red).

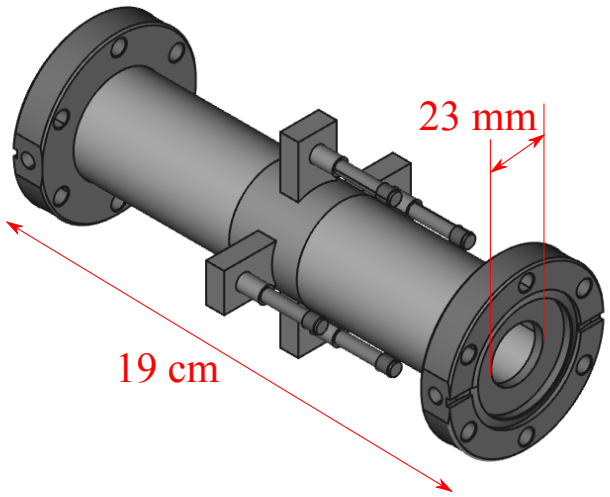

FIG. 2.

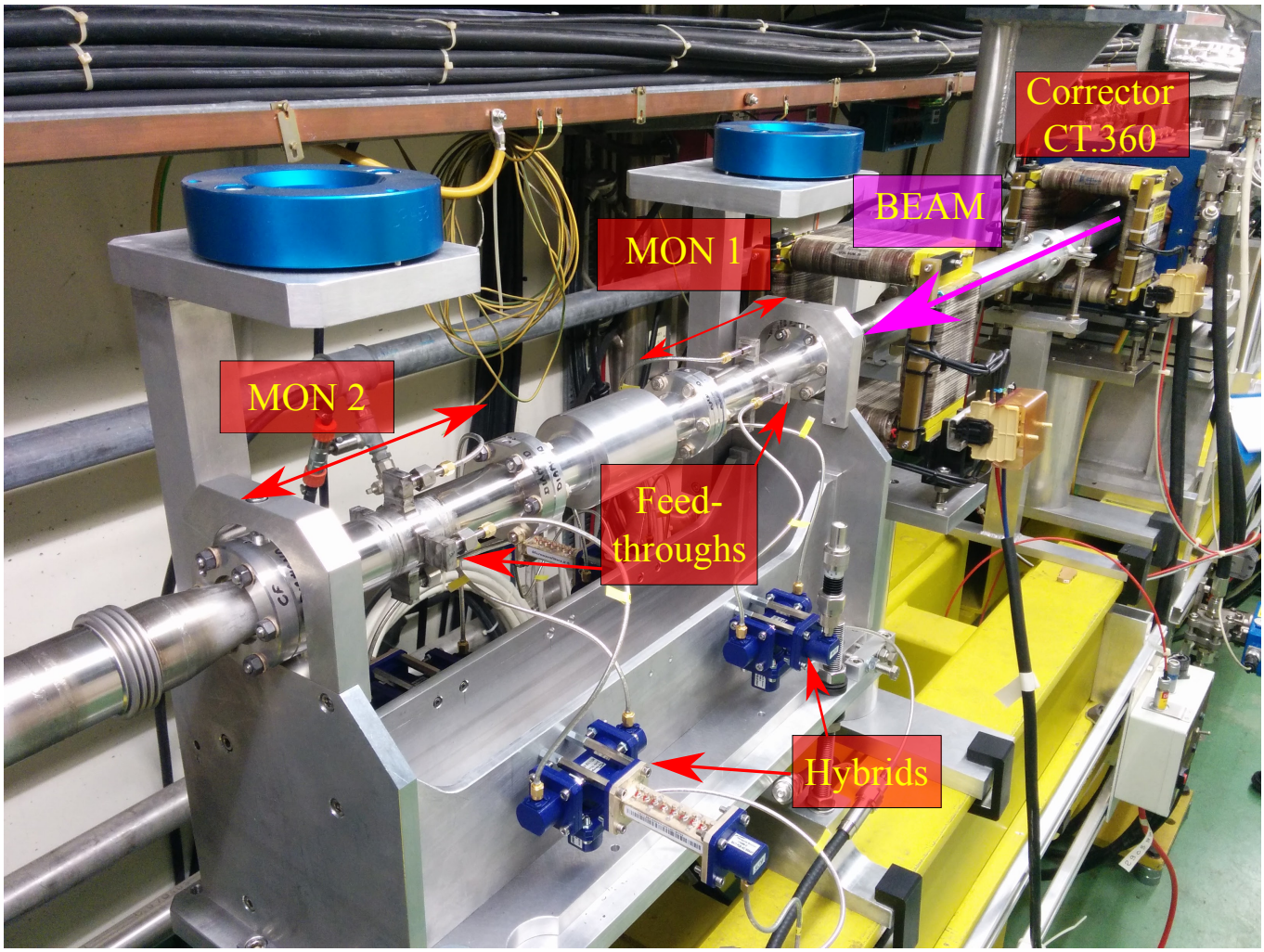
Corrector
CT.360
BEAM
MON 1
MON 2
Feed-
throughs
Hybrids

FIG. 3.

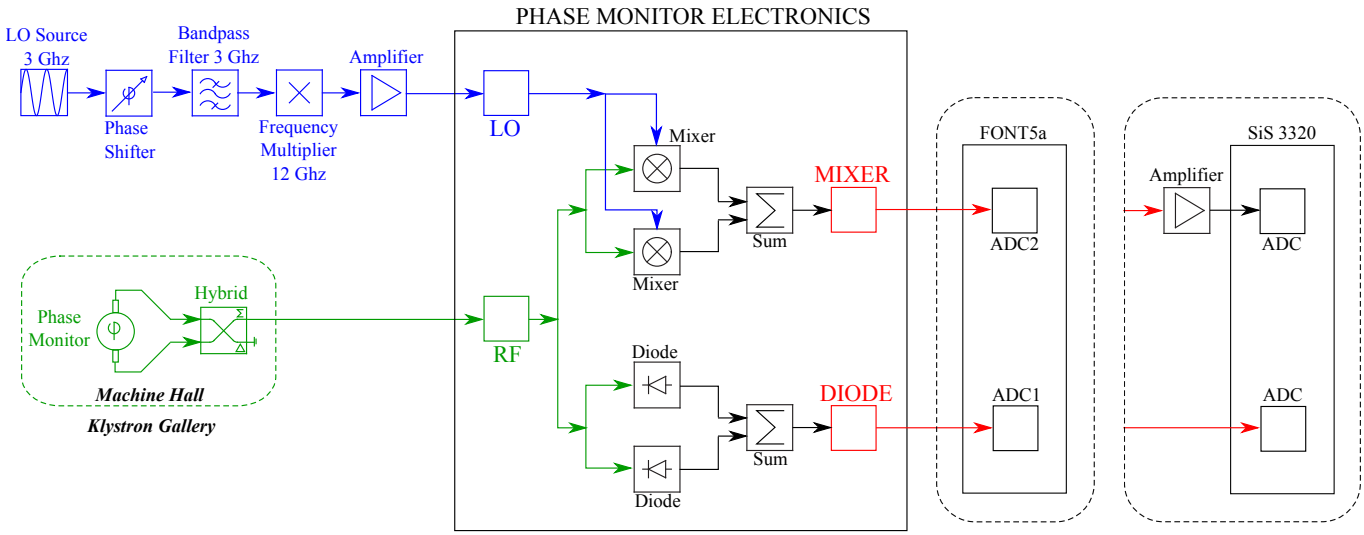
PHASE MONITOR ELECTRONICS
LO Source
3 Ghz
Phase
Shifter
Bandpass
Filter 3 Ghz
Frequency
Multiplier
12 Ghz
Amplifier
LO
Mixer
Mixer
Sum
MIXER
RF
Diode
Diode
Sum
DIODE
Phase
Monitor
Hybrid
Machine Hall
Klystron Gallery
FONT5a
ADC2
ADC1
SiS 3320
Amplifier
ADC
ADC

FIG. 4.

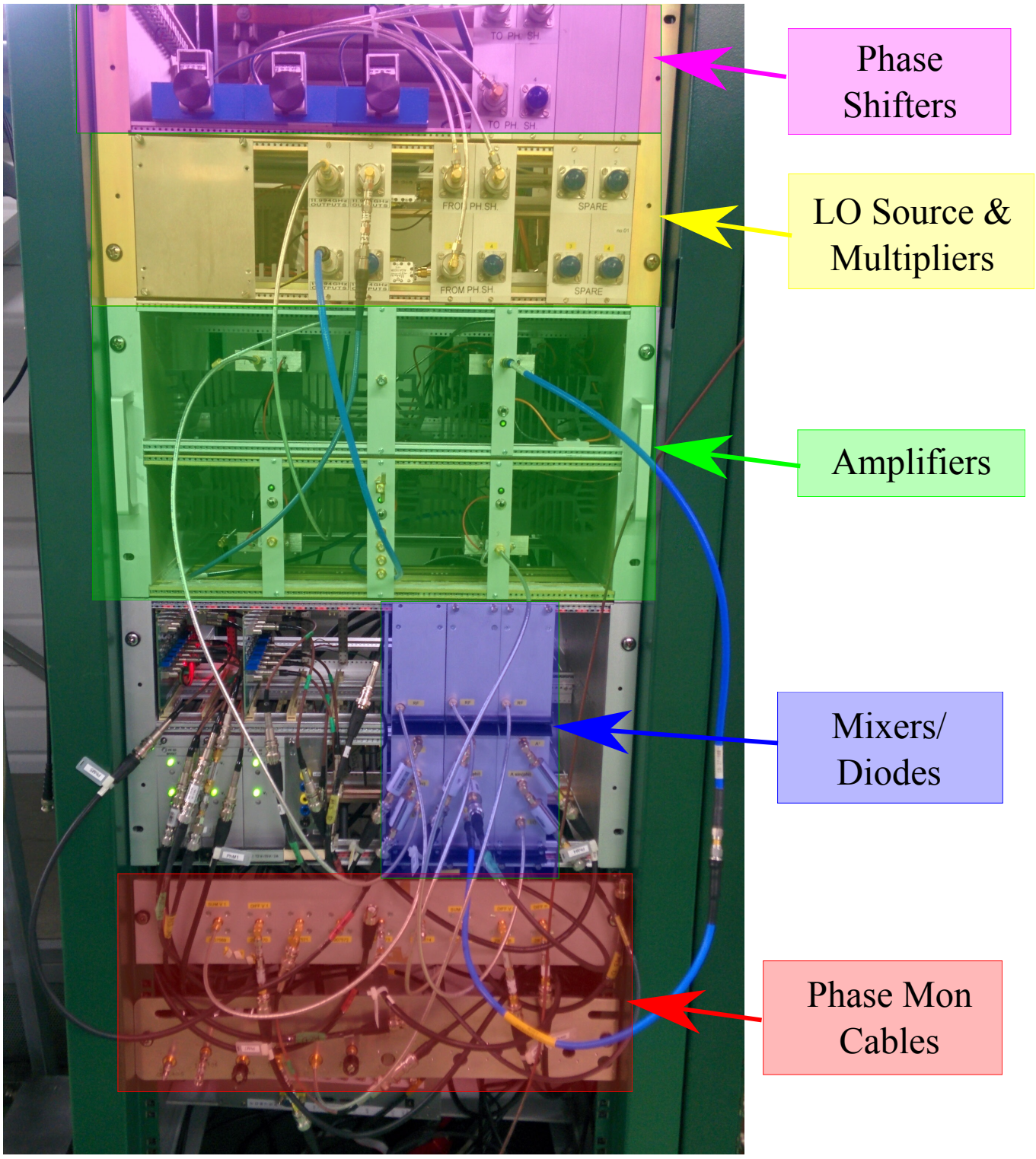
Phase Shifters
LO Source & Multipliers
Amplifiers
Mixers/ Diodes
Phase Mon Cables

FIG. 5.

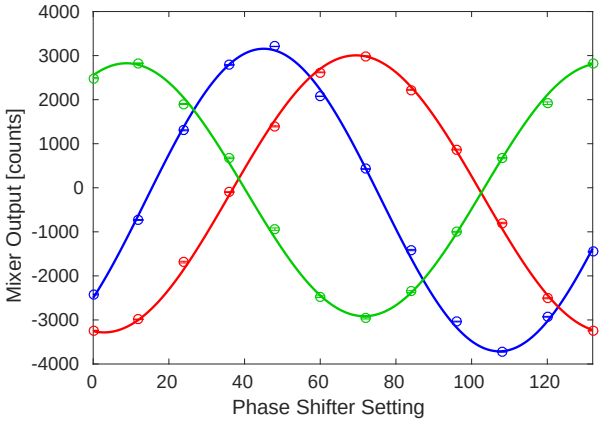

FIG. 6.

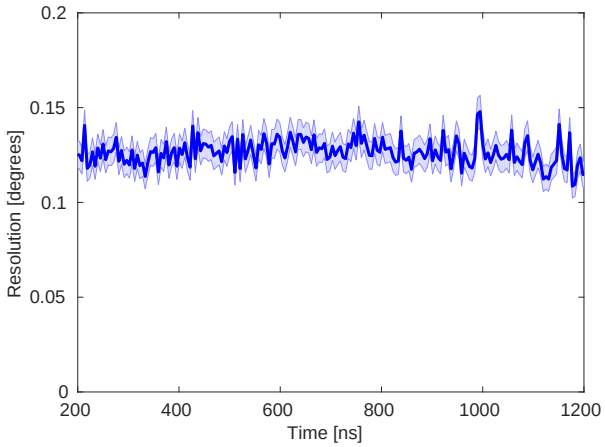

FIG. 7.

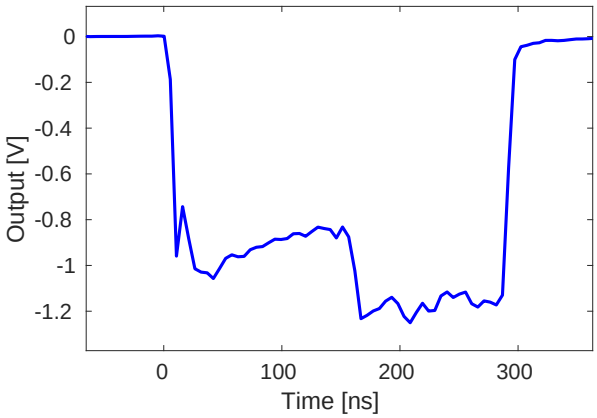

FIG. 8.

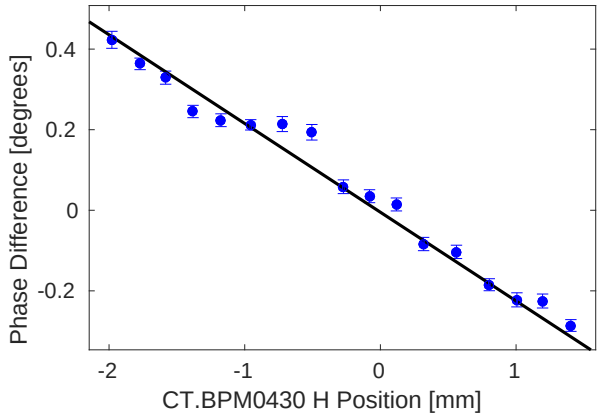

FIG. 9.

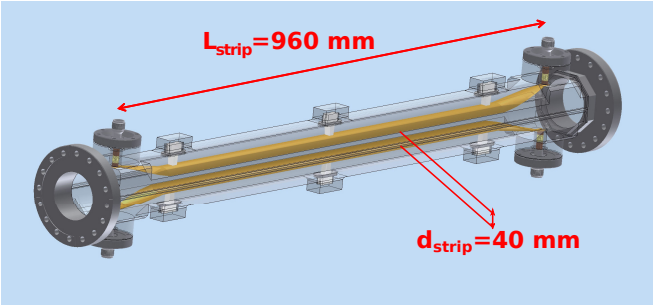

FIG. 10.

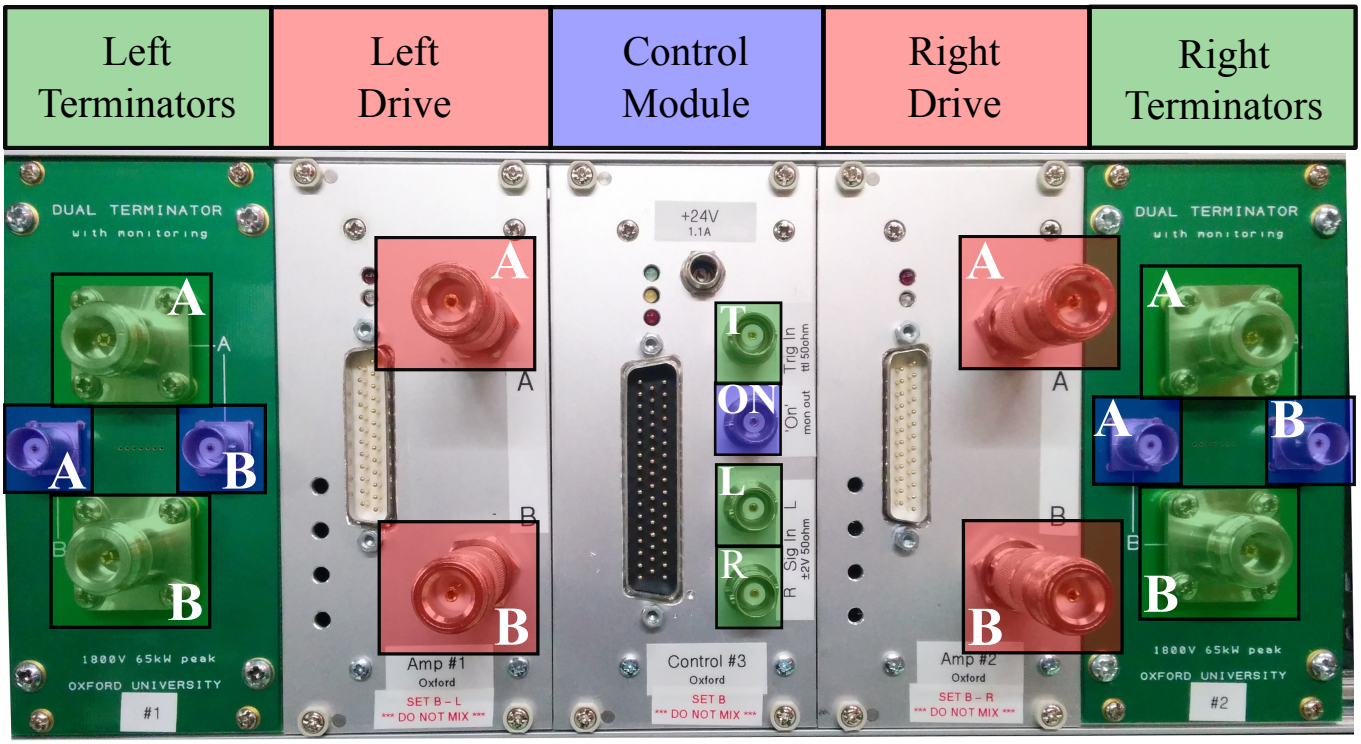

FIG. 11.

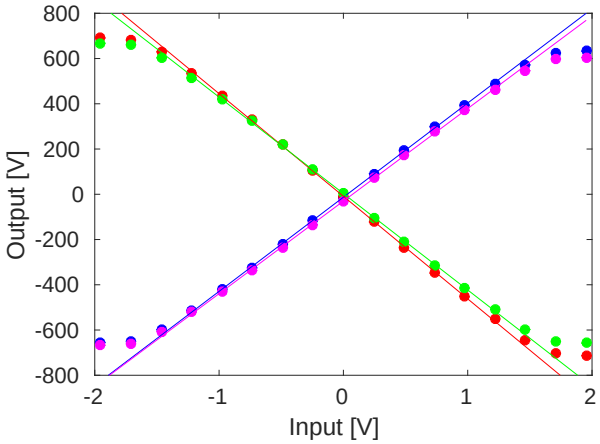

FIG. 12.

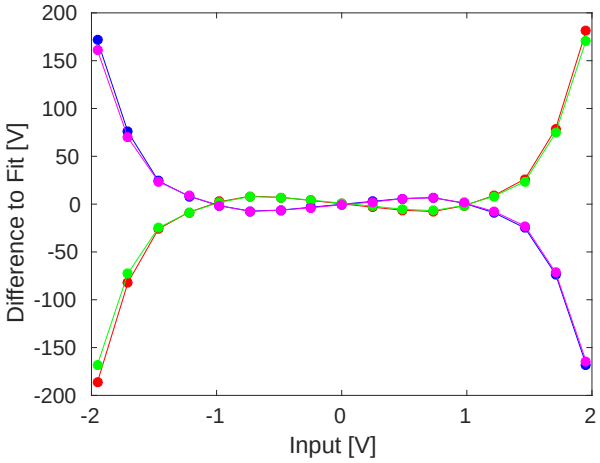

FIG. 13.

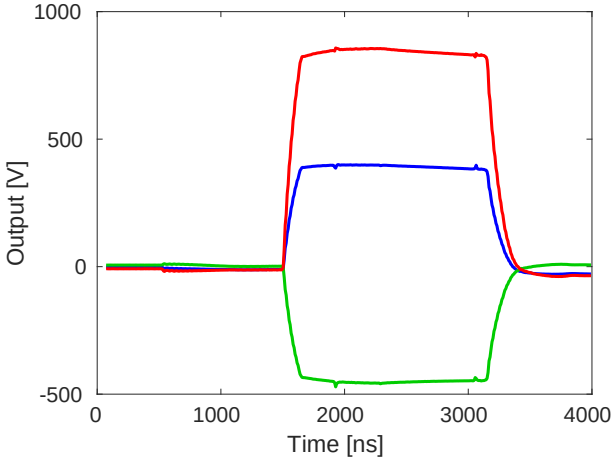

FIG. 14.

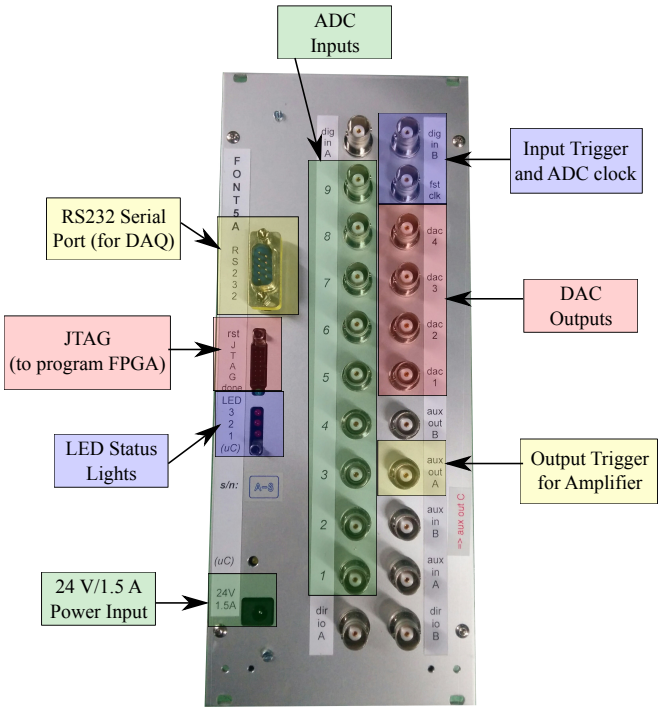
ADC Inputs
Input Trigger and ADC clock
RS232 Serial Port (for DAQ)
DAC Outputs
JTAG (to program FPGA)
LED Status Lights
Output Trigger for Amplifier
24 V/1.5 A Power Input

FIG. 15.

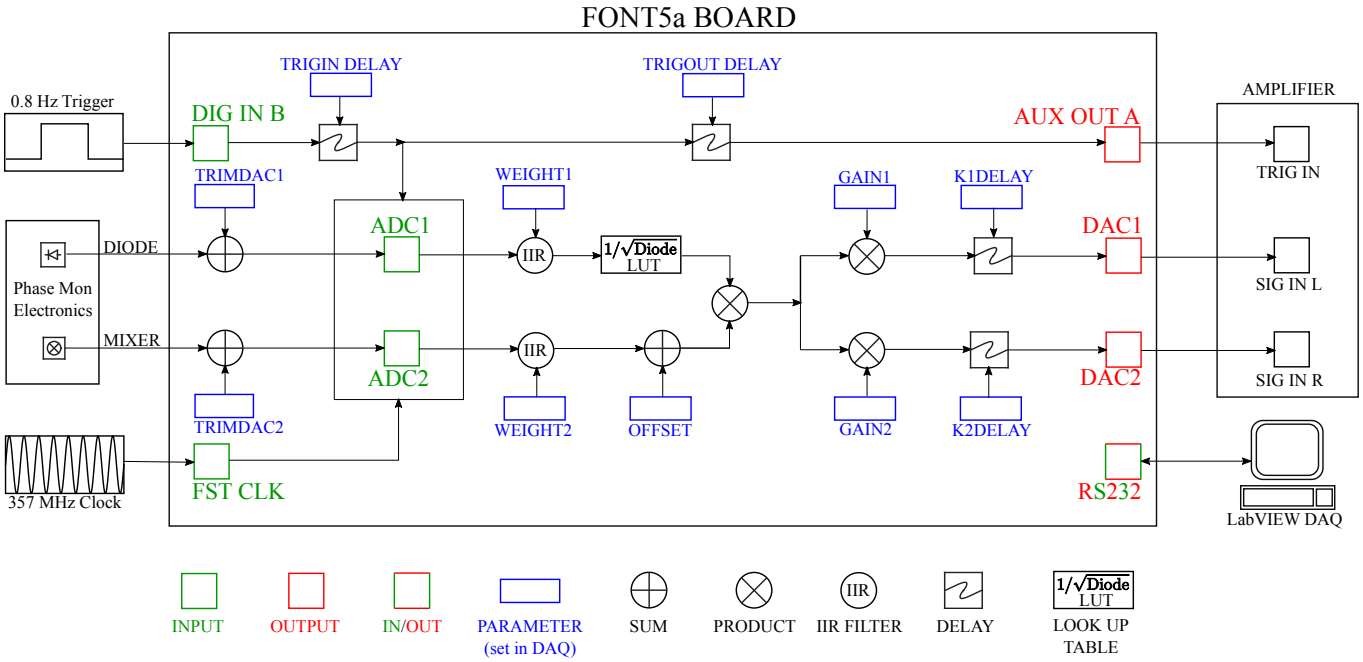
FONT5a BOARD
0.8 Hz Trigger
DIG IN B
TRIGIN DELAY
TRIGOUT DELAY
AUX OUT A
AMPLIFIER
TRIG IN
TRIMDAC1
WEIGHT1
GAIN1
K1DELAY
ADC1
DAC1
DIODE
Phase Mon Electronics
IIR
1/√Diode LUT
SIG IN L
MIXER
ADC2
DAC2
SIG IN R
TRIMDAC2
WEIGHT2
OFFSET
GAIN2
K2DELAY
357 MHz Clock
FST CLK
RS232
LabVIEW DAQ
INPUT
OUTPUT
IN/OUT
PARAMETER (set in DAQ)
SUM
PRODUCT
IIR FILTER
DELAY
LOOK UP TABLE

FIG. 16.

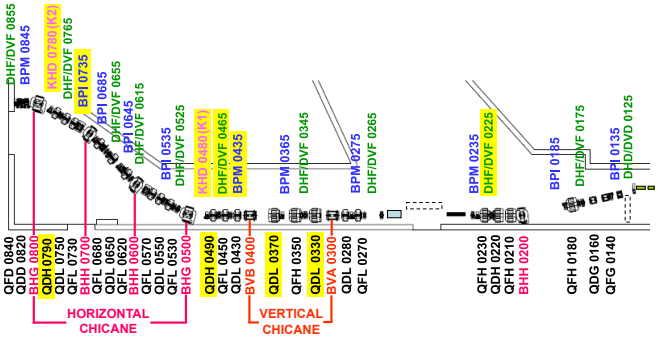

FIG. 17.

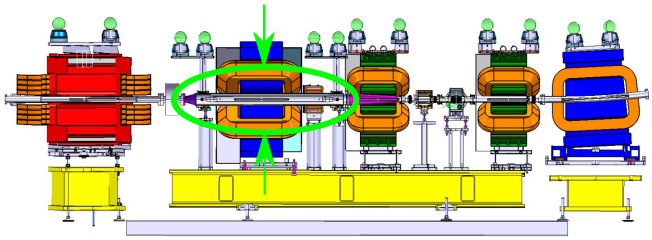

FIG. 18.

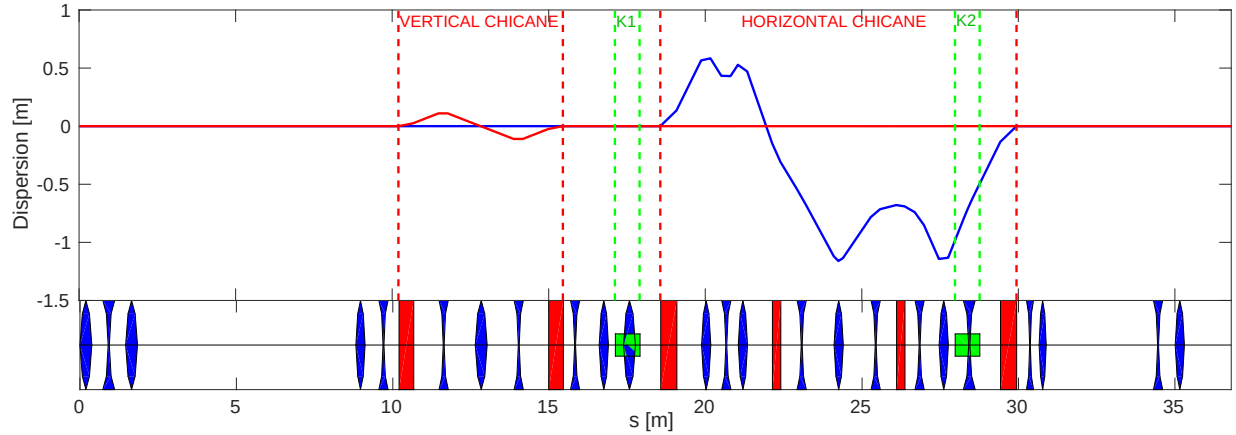

FIG. 19.

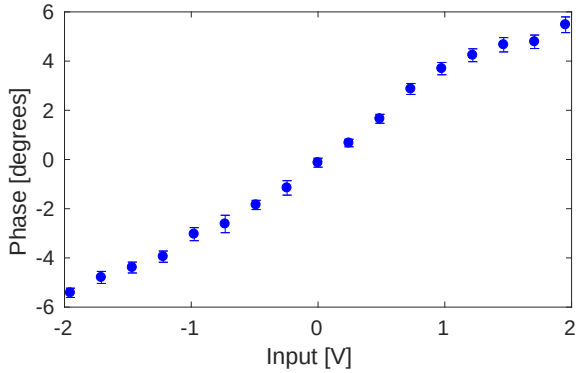

FIG. 20.

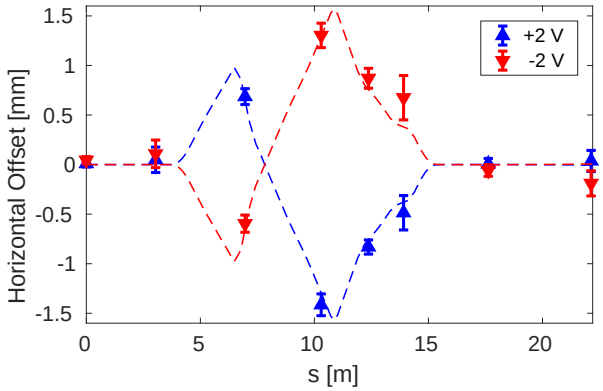

FIG. 21.

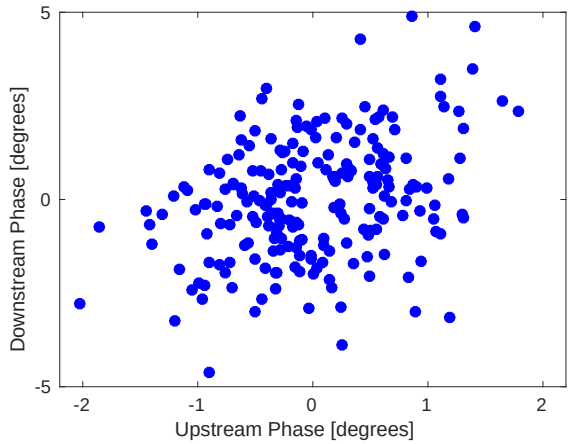

FIG. 22.

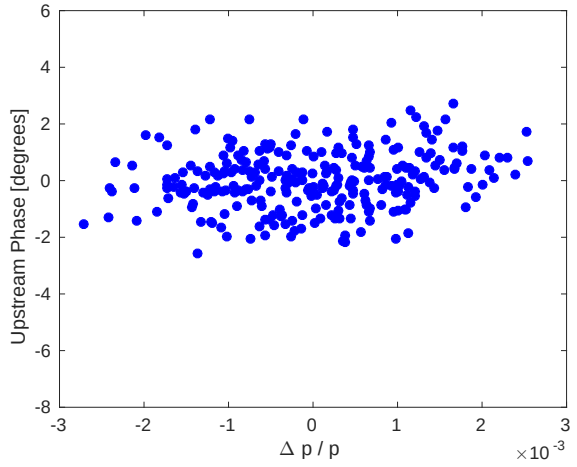

FIG. 23.

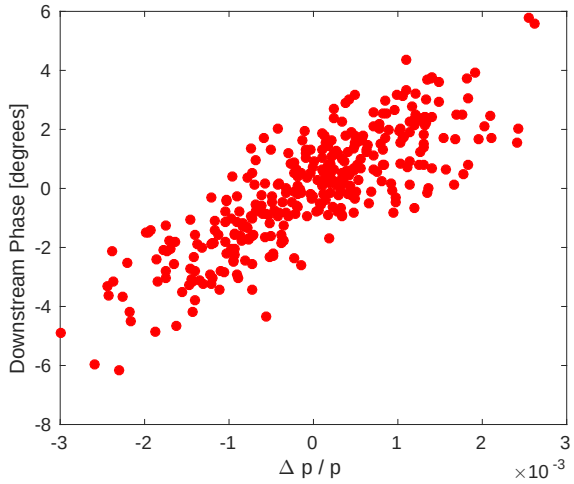

FIG. 24.

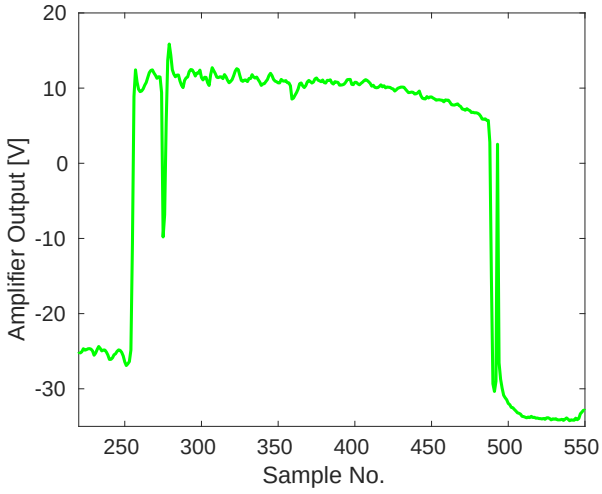

FIG. 25.

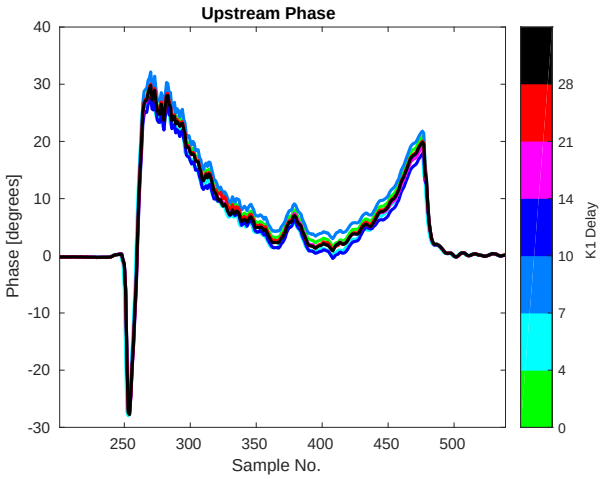

FIG. 26.

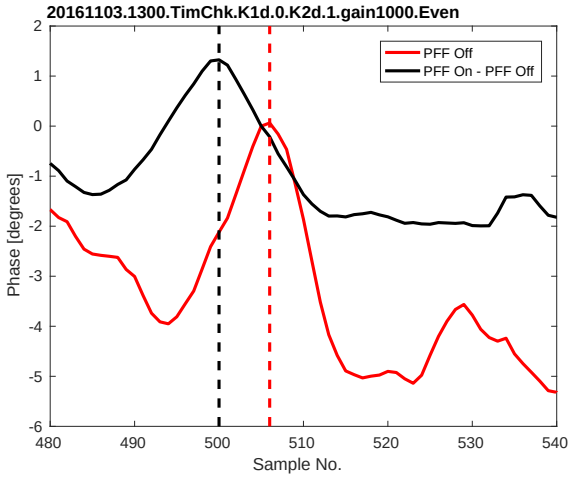

FIG. 27.

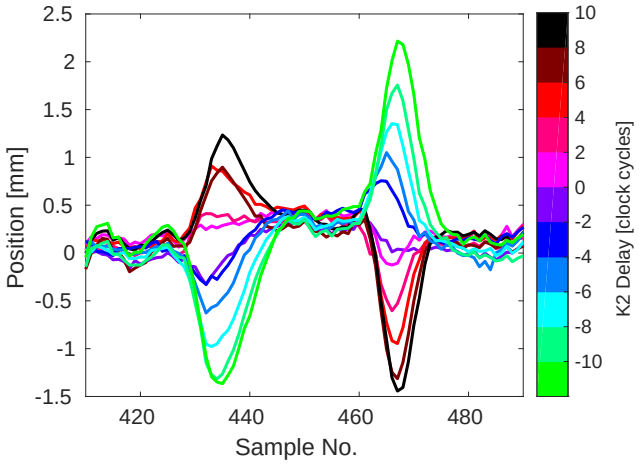

FIG. 28.

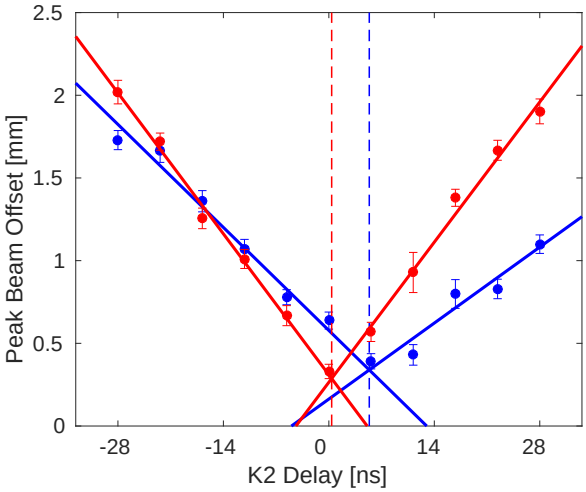

FIG. 29.