A Zero-Voltage Switched, Three-Phase Isolated PWM Buck Rectifier

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Abstract— **A novel three-phase, single-stage, isolated PWM rectifier is proposed, which is capable of achieving unity power factor, and low harmonic distortion of input currents, and in the same time realizing zero-voltage switching for all power semiconductor devices. Operation of the proposed circuit is thoroughly analyzed. Design equations and trade-offs are provided. The performance of the proposed circuit is demonstrated through a 2 kW, 100 kHz, digital signal processor controlled prototype. The conversion efficiency is around 93%.**

I. Introduction

INCREASING emphasis on power quality has placed a stronger demand on the performance of ac-dc converters as the front end power processing unit of many electronic systems. The requirements often include the following:

1) unity input displacement factor;
2) very low total harmonic distortion of the input current;
3) tight output voltage regulation;
4) transformer isolation between source and load; and
5) high efficiency and high power density.

These requirements are especially critical in high-power applications, when three-phase ac-dc converters are usually employed.

Several types of three-phase ac-dc converters have been proposed to date which satisfy one or more of the above requirements. All of them use some form of high-frequency pulse-width-modulation (PWM) controlled switching rectifier in order to minimize the size and weight of reactive filtering components. The first three requirements are easily met using the conventional six-step PWM technique (or input current space vector modulation) on a buck type bridge rectifier. The modulation technique was originally developed in [2] and can also be found in [3] and [11]. The technique provides maximum achievable output DC voltage without any low frequency harmonics, thus minimizing both the input and output filter requirements. Electrical isolation can be efficiently accomplished if the conversion process is divided in two stages: three-phase to high-frequency single-phase cyclo-conversion and high-frequency ac to dc rectification. A small and efficient high-frequency transformer can then be placed between the two stages, as shown in [9] and [10]. For an improved power density, higher switching frequency is desirable. However, the increase of switching frequency is accompanied by reduction of efficiency due to the increased switching losses. These losses can be significantly reduced or eliminated if the recently developed zero-voltage-switching (ZVS) technique for the ZVS full-bridge (FB) phase-shifted PWM dc-dc converters [4]–[8] can be implemented in the three-phase rectifier circuit.

In this paper, a novel ZVS PWM three-phase ac-dc converter, is described. It is topologically equivalent to the converter described in [9], [10], but the new circuit is capable of implementing ZVS by utilizing the parasitic capacitances of the switches and the transformer leakage inductance. The implementation of ZVS also enables utilization of MOSFET parasitic body diodes, instead of additional fast recovery diodes, thus allowing for very effective implementation.

The presence of leakage inductance has significant effects on the steady-state characteristics of the converter. The choices of transformer turns ratio, the leakage inductance, and the primary duty cycle are shown to be complex functions of input and output voltages, load current, switching frequency, ZVS range, and harmonic distortion of input currents [7], [8]. The paper presents the analysis of the converter and provides design equations for determining transformer turns ratio, leakage inductance, and switching frequency for a given set of design specifications. The operation of the converter and the results of the analysis are illustrated using a 2 kW, 100 kHz, microprocessor controlled prototype.

II. Principle of Operation

Fig. 1(a) shows the circuit diagram of the proposed converter. The converter can be divided into several functional blocks. The cycloconverter bridge (q_{11} to q_{23}) is used to synthesize the high-frequency ac voltage v_p from the three-phase input voltages. The four-quadrant switches are implemented as shown in Fig. 1(b), where p denotes the two-quadrant part of a switch q_{ij} in Fig. 1(a) which conducts current when i_p is positive, while n denotes the switch part which conducts current when i_p is negative. The unity input power factor is obtained by using a modified six-step PWM technique, so that the voltage v_p contains no dc component. Additional control is implemented to assure that ZVS is achieved on all bridge switches. The high-frequency ac signal is transferred through the high-frequency transformer to provide input/output isolation. The secondary ac signal is rectified and filtered to obtain the desired output dc voltage.

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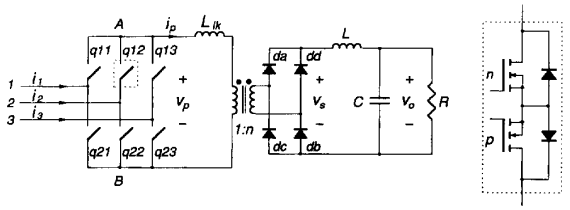

(a) (b)

Fig. 1. ZVS three-phase PWM rectifier: (a) proposed rectifier topology, (b) realization of four-quadrant switches $q_{11} - q_{23}$.

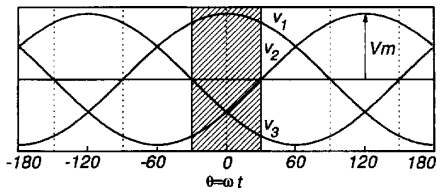

Fig. 2. Input phase voltages.

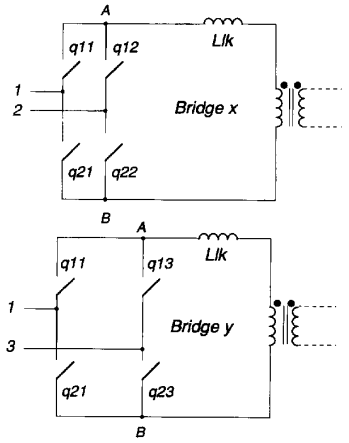

Fig. 3. Subtopologies similar to the ZVS-FB-PWM converter.

Within any 60° interval between two successive zero crossings of input phase voltages, shown in Fig. 2, there are two line voltages that do not change sign. For example, in the 60° shaded area in Fig. 2, the line voltages $v_{12} = v_1 - v_2$, and $v_{13} = v_1 - v_3$ are positive, and they both attain their maximum in this interval. Since the switching frequency of the converter is much higher than the line frequency, the two line voltages can be treated as slowly varying dc voltages. Therefore, within any 60° interval, the proposed converter is analyzed as two full-bridge (FB) converter subtopologies operating alternatively within the switching cycle. The two subtopologies for the interval $-30° \leq \theta \leq 30°$ are shown in Fig. 3. Fig. 4 shows the circuit principal waveforms within the 60° interval, with excessively increased switching period T_c so that PWM details can be observed. Different parts of the waveforms in Fig. 4 are shaded according to the subtopology that is used to generate them. At the beginning of every switching cycle subtopology y is used. Switches q_{11} and q_{23} are turned on creating a positive voltage pulse across points A and B and a current pulse flowing from phase 1 into phase 3. In order to keep the transformer flux balanced, a negative voltage pulse of same duration is next generated across points A and B by turning on switches q_{13} and q_{21}. The two pulses are separated by a zero-volt interval whose duration is chosen (for purpose of transformer flux balancing) so that the distance between adjacent pulses is even throughout the switching cycle. In the remaining part of the switching cycle, the subtopology x is used to create another two voltage pulses across the points A and B and two current pulses flowing from phase 1 into phase 2. Assuming that the converter output current is constant, the phase currents are synthesized from current pulses of constant magnitude. If the average phase currents, ($\bar{i}_1$, $\bar{i}_2$, $\bar{i}_3$), are to be sinusoidal and in phase with the phase voltages, the duration of the current pulses created by subtopology x has to be proportional to the phase voltage v_2, while the duration of the current pulses generated by subtopology y has to be proportional to v_3, [3]. If these conditions are satisfied, the current $\bar{i}_1$ is also sinusoidal and in phase with v_1 due to the three-phase system symmetry and due to the fact that $i_1 = -i_2 - i_3$.

The above described modulation strategy can be summarized as follows. If the input phase voltages are given by

$$v_1(\theta) = V_m \cos(\theta)$$
$$v_2(\theta) = V_m \cos(\theta - 2\pi/3)$$
$$v_3(\theta) = V_m \cos(\theta + 2\pi/3), \tag{1}$$

the duty cycles d_x and d_y of the input current pulses generated by subtopologies x and y, respectively, within the chosen 60° interval are

$$d_x(\theta) = -D_m(v_2(\theta)/V_m)$$
$$d_y(\theta) = -D_m(v_3(\theta)/V_m) \tag{2}$$

where $0 \leq D_m < 1$ is the modulation index. From Figs. 1 and 4, the output voltage, V_0, is

$$V_0 = n[d_x(\theta)v_{12}(\theta) + d_y(\theta)v_{13}(\theta)] \tag{3}$$

where n is the transformer turns ratio $n = N_{\text{sec}}/N_{prim}$. By substituting (1) and (2) into (3), after elementary trigonometric transformations, it follows that the output voltage is constant, and given by

$$V_0 = \tfrac{3}{2} n D_m V_m. \tag{4}$$

The above derivation was conducted for $-30° \leq \theta < 30°$. However, the same operation is maintained for all 60° intervals in Fig. 2, with the input phases 1–3 interchanging their roles, as is standard in the six-step PWM [2], [3]. Due to this fact, all analyses in this paper are restricted to $-30° \leq \theta \leq 30°$.

Because within every 60° interval the three-phase converter is operated as a set of two full bridge dc-dc converters, ZVS can can be implemented in the same way as in the ZVS-FB-PWM dc-dc converter, [4]–[8]. For example in subtopology x during the 60° interval, the antiparallel diodes of the switches

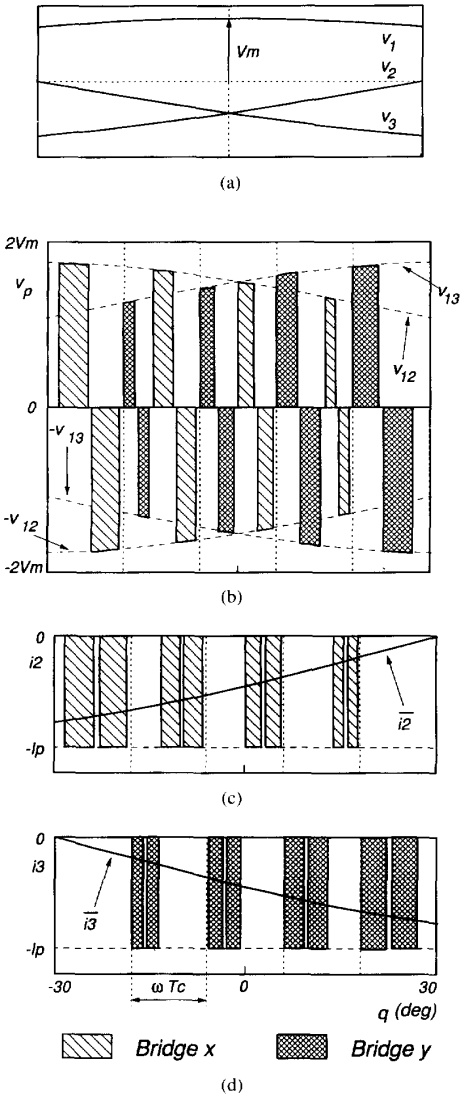

Fig. 4. Modified six-step PWM waveforms: (a) phase voltages, (b) primary voltage, and (c) phase currents i_2 and i_3.

q_{11n}, q_{22n}, q_{12p}, and q_{21p} are forward biased because $v_1 > v_2$, and therefore these switches can be kept on all the time. In this case the subtopology can be redrawn as shown in Fig. 5. This circuit can be operated in ZVS mode when the switches have 50% duty cycle and the gate pulses for one vertical leg are phase shifted with respect to the gate pulses of the other leg, [4]–[8].

The complete operation of the three-phase circuit during a high-frequency switching period is illustarted in Figs. 6 and 7. Fig. 5 shows the transformer primary voltage, v_p, and current, i_p, the rectified secondary voltage, v_s, and the current of phase 1, i_1. The gate drive signals for all twelve two-quadrant switches are shown in in Fig. 7 with the same time scale. Fig. 7(a) illustrates the operation of the saubtopology y, while Fig. 7(b) illustrates the operation of the subtopology x (the

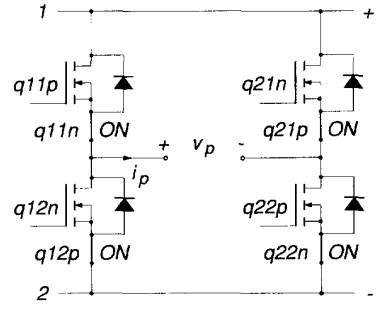

Fig. 5. Subtopology x redrawn as a full-bridge dc-dc converter.

gate signals for q_{11p} and q_{21n} are repeated for clarity). It is seen from Figs. 6 and 7 that the sircuit waveforms and the gate signals of the subtopology y during the interval t_1 to t_7, and of the subtopology x during the interval t_7 to t_{13}, are identical as in the ZVS-FB-PWM dc-dc converter. Since the operation of the ZVS-FB-PWM converter is well known, [4]–[8], a detailed switching cycle description is not presented in this paper.

It follows from the above discussion that only six out of twelve two-quadrant switches in the converter operate in any given 60° interval. The other six switches should be turned on during the entire interval. However, in a 30° subinterval one of the input phase voltages has a value that lies between the other two (Fig. 2) so that the switches in the leg connected to this input phase have to be turned off when the subtopology corresponding to this phase is not used. For $0 \leq \theta \leq 30°$, the voltage v_2 is between v_1 and v_3 and consequently the switches q_{12p} and q_{22n} can be kept on during the whole interval except when the switches q_{13} and q_{23}, respectively, are on, as shown in Fig. 7(c). This is to prevent a short circuit between phases 2 and 3 through the antiparallel diodes of q_{12n} or q_{22p}. During this interval, switches q_{12p} and q_{22n} are not switched under zero-voltage conditions. However, the resulting switching losses are very low for two reasons. First, these switches are never switching the full line-to-line voltage, but only the difference between v_2 and v_3 which varies from 0 to $(\sqrt{3}V_m)/2$. Second, each switch is operated without ZVS only during one 30° interval, and the total switching loses are proportional to $1/(12T_c)$ rather than to $1/T_c$.

III. Steady-State Analysis

As known from the operation of the ZVS-FB-PWM converter, and as seen in Fig. 6, the duty cycles of the transformer primary voltage pulses are always longer than the duty cycles of the corresponding secondary voltage pulses, due to the presence of the isolation transformer and its leakage inductance. The implications of this difference, together with other effects relevant to the circuit design are analyzed in this section, and the results of the analysis are used as a basis for design procedure presented in the next section.

The analysis performed in this paper is based on the assumption that the input phase voltages are sinusoidal and balanced, as given by (1). It is also assumed (unless otherwise stated) that the forward voltage drop across the diodes and the

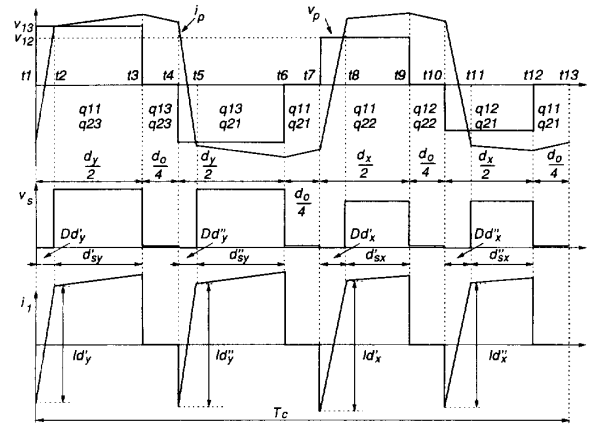

Fig. 6. Circuit waveforms: Primary voltage (top), rectified secondary voltage (middle), and current of phase 1 (bottom).

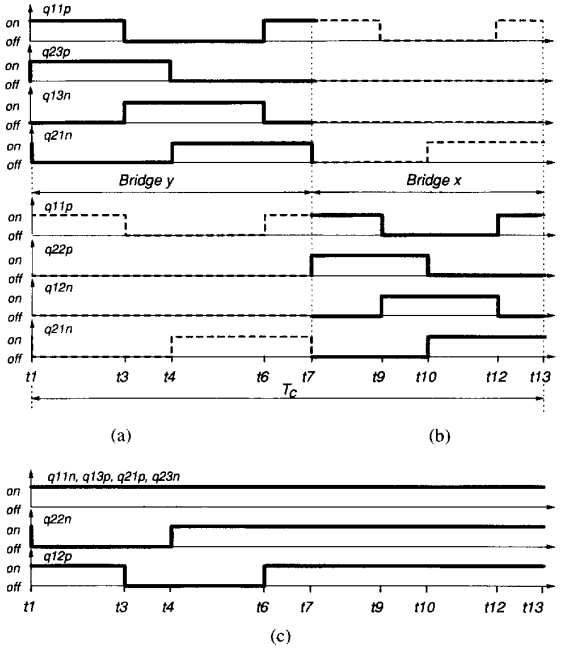

Fig. 7. Switch gate drive waveforms during switching period in Fig. 6: (a) subtopology y gate signals, (b) subtopology x signals, and (c) remaining gate signals.

MOSFET's is zero, and that the rectifier diode capacitances are equal to zero. In addition, the analysis is performed with the assumption that the output voltage V_0 is constant.

A. Duty Cycle Analysis

Referring to Fig. 6, the duty cycle of the primary voltage v_p is defined as

$$d(\theta) = d_x(\theta) + d_y(\theta) \tag{5}$$

where $d_x(\theta)$ and $d_y(\theta)$ correspond to the sum of duty cycles of the two voltage pulses created by subtopologies x and y, respectively. The four primary voltage pulses are arranged as two pairs of pulses with duty cycles $d_x(\theta)/2$ and $d_y(\theta)/2$ separated by four zero-volt intervals of equal duration marked in Fig. 6 as $d_0/4$. Similarly, the duty cycle of the rectified secondary voltage is defined as

$$d_s(\theta) = d_{sx}(\theta) + d_{sy}(\theta) \tag{6}$$

where $d_{sx}(\theta)$, and $d_{sy}(\theta)$ are defined as

$$\begin{aligned} d_{sx}(\theta) &= d'_{sx}(\theta) + d''_{sx}(\theta) \\ d_{sy}(\theta) &= d'_{sy}(\theta) + d''_{sy}(\theta). \end{aligned} \tag{7}$$

The total loss of duty cycle is then defined as

$$\Delta d(\theta) = \Delta d_x(\theta) + \Delta d_y(\theta) = d(\theta) - d_s(\theta) \tag{8}$$

where

$$\begin{aligned} \Delta d_x(\theta) &= \Delta d'_x(\theta) + \Delta''_x(\theta) \\ \Delta d_y(\theta) &= \Delta d'_y(\theta) + \Delta''_y(\theta). \end{aligned} \tag{9}$$

Because the primary and secondary duty cycles are not the same, the output voltage is not given by (3), but instead by

$$V_0 = n[d_{sx}(\theta) \cdot v_{12}(\theta) + d_{sy} \cdot v_{13}(\theta)]. \tag{10}$$

If it is desired that the average output voltage does not contain any low frequency harmonics, i.e., that it is given by (4), then the secondary duty cycles (and not the primary ones as in (2)), should be made proportional to the input phase voltages:

$$\begin{aligned} d_{sx}(\theta) &= -D_m(v_2(\theta)/V_m) \\ d_{sy}(\theta) &= -D_m(v_3(\theta)/V_m). \end{aligned} \tag{11}$$

This will cause additional distortion of the input currents due to the presence of small triangular parts t_1 to t_2, t_4 to t_5, etc. Worst case input current analysis shows that the input current fundamental is phase shifted with respect to phase voltage by less than 2.5°, and that the total harmonic distortion (THD) is less than 2% due to this effect.

B. Filter Inductor Current Ripple

In order to design the output filter inductor, it is necessary to know at which phase angle θ of the input voltage does the filter current ripple reach its maximum. The output filter current ripple is analyzed by evaluating (1), (7), and (11) at $\theta = 0$ and $\theta = \pi/6$. Fig. 8 shows the secondary voltage and the corresponding output filter inductor current ripple for $\theta = 0$ and $\theta = \pi/6$, respectively. At $\theta = 0$, v_s consists of four equal-amplitude voltage pulses evenly distributed within T_c (since $v_{12} = v_{13}$ at θ =0). The duty cycle of each pulse is $D_m/4$ and its amplitude is V_0/D_m, which is typically only 10–20% above the output voltage. In this case the filter inductor ripple is minimal. At $\theta = \pi/6$, v_s consists only of two pulses, each having a duty cycle of $(\sqrt{3}D_m)/4$, and amplitude of $(2V_0)/(\sqrt{3}D_m)$. The duty cycle of the other pair of pulses is zero (since $v_2 = 0$ at $\theta = \pi/6$), and three of the zero intervals merge into one after the second pulse, as shown in Fig 8(b).

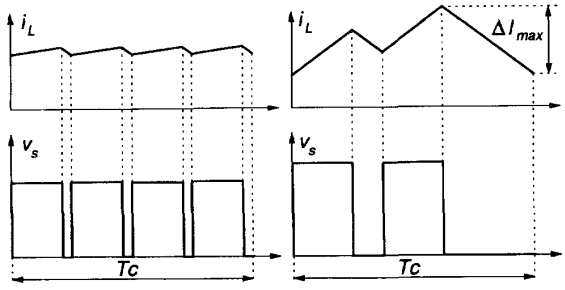

Fig. 8. Output filter inductor current ripple: (a) $\theta = 0$, (b) $\theta = \pi/6$.

Assuming that the loss of duty cycle Δd is relatively small, the maximum filter inductor current ripple is calculated from Fig. 8(b) as

$$\Delta I_{\max} = \frac{3}{4}\left(1 - \frac{\sqrt{3}}{2} D_m\right) T_c \frac{V_0}{L}. \tag{12}$$

C. Loss of Duty Cycle

Selection of the transformer turns ratio, n, and the modulation index, D_m, is directly related to the loss of duty cycle, which depends on the choice of the switching frequency, leakage inductance, and the ZVS range. This interdependence is evaluated next.

From (6), (8), and (11), the primary duty cycle is given by

$$d(\theta) = \Delta d(\theta) - D_m \left[\frac{v_2(\theta)}{V_m} + \frac{v_3(\theta)}{V_m}\right] \tag{13}$$

where $\Delta d(\theta)$ can be estimated from Fig. 6, by using definitions (8) and (9), and Fig. 1, from

$$\Delta d_x(\theta) = \frac{(I'_{dx}(\theta) + I''_{dx}(\theta))L_{lk}}{v_{12}(\theta)T_c}$$
$$\Delta d_y(\theta) = \frac{(I'_{dy}(\theta) + I''_{dy}(\theta))L_{lk}}{v_{13}(\theta)T_c}. \tag{14}$$

In order to satisfy the constraint $d(\theta) \leq 1$, it is necessary to find the angle θ at which $d(\theta)$ attains its maximum. It is shown in the Appendix A that $d(\theta)$ is maximum for $\theta = 0$ if $\Delta d(0) \leq 0.25$. In practice, the loss of duty cycle $\Delta d(0)$ should be limited to around 0.1. Therefore, in all practical designs, the choice of maximum duty cycle has to be made at $\theta = 0$. Assuming full utilization of duty cycle, it follows from (13) that

$$d(0) = D_m + \Delta d(0) = 1. \tag{15}$$

From Fig. 6 and (11), at $\theta = 0$,

$$I'_{dx}(\theta) = I''_{dx}(\theta) = I'_{dy}(\theta) = I''_{dy}(\theta) = n(2I_L - \Delta I) \tag{16}$$

where $I_L = V_0/R$ is the load current. The filter inductor current ripple is estimated from Fig. 8(a) by taking into account (15) as

$$\Delta I = \Delta d(0) \frac{V_0}{L} \frac{T_c}{4}. \tag{17}$$

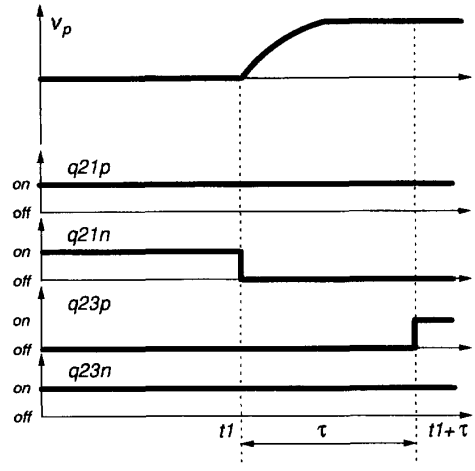

Fig. 9. Detail of primary voltage and gate drive signals at t_1.

Since $v_{12}(0) = v_{13}(0) = 3V_m/2$, it follows from (14)–(17) and (4) that the loss of duty cycle is given by

$$\Delta d(0) = \frac{8D_m \dfrac{n^2 L_{lk}}{RT_c}}{1 + D_m \dfrac{n^2 L_{lk}}{L}}. \tag{18}$$

Using (18) and (15), the designer can choose $\Delta D(0)$, which will finally lead to the choice of L_{lk}, T_c, and the ZVS range.

D. ZVS Range and Required Dead Times

Conditions for ZVS are not the same for all switching transitions. Referring to Fig. 6, at the leading edge transitions of v_p (t_1, t_4, t_7, and t_{10}), the energy stored in the leakage inductance is utilized to charge the parasitic capacitances of the nodes A or B in Fig. 1. However, at the trailing edge transitions of v_p (t_3, t_6, t_9, and t_{12}), the leakage inductance is in series with the reflected output filter inductor. The combined energy stored in both the leakage inductance and the output filter inductor is utilized to charge the capacitances of the nodes A or B. Since the energy stored in the output filter inductor is significantly larger than the energy stored in the leakage inductance, ZVS condition can be easily achieved at the trailing edges.

When the converter operates with light load, the ZVS property is lost because the energy stored in L_{lk} becomes smaller than the energy required to charge the parasitic capacitances of nodes A or B to the input line voltage. Since the energy in the capacitances is proportional to the square of the input line voltage, the worst case for achieving ZVS will occur when the input line voltage is the highest, i.e., $v_p = \sqrt{3}V_m$, which occurs at $\theta = \pi/6$. The energy needed to charge the capacitance of nodes A or B at $\theta = \pi/6$ is

$$E_c = \frac{1}{2}(\sqrt{3}V_m)^2 C_{eq} \tag{19}$$

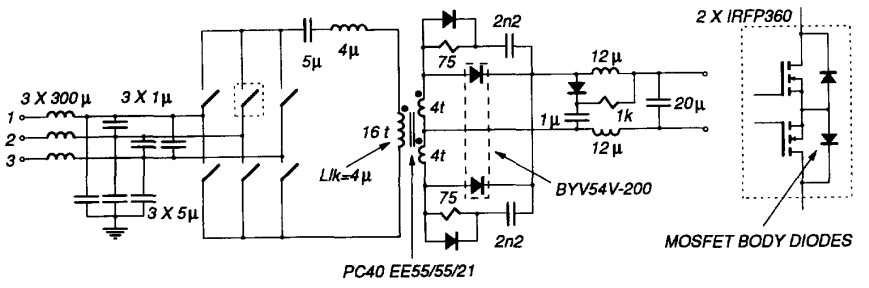

Fig. 10. Circuit diagram of the 2 kW prototype.

where C_{eq} is

$$C_{eq} = \frac{8+2\sqrt{2}}{3} C_M + C_T. \tag{20}$$

as shown in Appendix B. In (20), C_M is the output capacitance of the two-quadrant switch (MOSFET) at $\sqrt{3}V_m$, and C_T is the parasitic capacitance of the transformer.

The minimum energy stored in the leakage inductance required for ZVS is

$$E_l = \frac{1}{2} L_{lk} I_{cr}^2. \tag{21}$$

Equating E_c and E_l, and solving for L_{lk}, gives

$$L_{lk} = \frac{(\sqrt{3}V_m)^2}{I_{cr}^2} C_{eq}. \tag{22}$$

The current I_{cr} is the primary current at the end of the off-time, (e.g., at time t_{13} in Fig. 6). The minimum I_{cr} occurs at $\theta = \pi/6$ and from Fig. 8(b) is given by

$$|I_{cr}| = n\left(I_L - \frac{1}{2}\Delta I_{\max}\right) \tag{23}$$

where $\Delta I_{\max}$ is given by (12). The maximum input voltage amplitude and the minimum load current at which ZVS is lost (ZVS range) are related through (22) and (23) with L_{lk}, and $\Delta I_{\max}$. In the design of the converter, L_{lk} and T_c (which from (12) determines $\Delta I_{\max}$) have to be adjusted to achieve the desired ZVS range.

In order to achieve ZVS, it is necessary to provide some deadtime between turning one switch off and turning the other on. This is illustrated in Fig. 9 showing the voltage v_p and the gate-drive signals of the related switches around time t_1. After q_{21n} is turned off, the current in the leakage inductance is charging the equivalent capacitance of node B, until the voltage between point B and phase 3 becomes zero, and the antiparallel diode of the switch q_{23p} starts conducting. Only after this time delay, τ, q_{23p} should be turned on.

The optimum dead time is equal to one fourth of the resonant period between L_{lk} and C_{eq}, and can be estimated as

$$\tau = \frac{\pi}{2}\sqrt{L_{lk}C_{eq}}. \tag{24}$$

In practice, the dead time needs to be adjusted experimentally due to wide variation of the equivalent capacitance, and the approximation (24) gives only a fairly good initial estimate of τ.

IV. Prototype Design Example

Due to the complicated relationship between T_c, L_{lk}, and Δd shown in the previous analysis, the design of the converter has to be performed in several iterations. The design is illustrated on the example prototype built for the following specifications:

- maximum output power: 2 kW,
- output voltage: $V_0 = 50$ V, and
- input rms line voltage: 3×208 V.

From these specifications, $V_m = 170$ V, and $I_L^{\max} = 40$ A.

A. Power Stage Design and Implementation

1) Switching Frequency: The schematic diagram of the designed 2 kW power stage is shown in Fig. 10. The carrier period T_c is 20 μs. As shown in Fig. 6, in every carrier period there are four voltage pulses of v_p. Therefore, the switching frequency is $1/(T_c/2) = 100$ kHz. This switching frequency has been determined by the maximum speed of the microprocessor system used to control the converter.

2) Transformer Turns Ratio: A possible starting point of the design is to assume the value of D_m at low line. An initial choice for D_m is 0.8. This leaves ample room for $\Delta d(0)$ and for duty cycle overshoots during transients. With this value of D_m, the first iteration for the transformer turns ratio n can be calculated from (4).

3) Output Filter: The output filter resonant frequency is chosen at 7 kHz, to provide adequate attenuation of output voltage switching frequency ripple. Assuming a maximal output filter inductor current ripple, the output filter inductor can be calculated using (12). It is important to keep the current ripple relatively small, because as seen from (22) and (23), high ripple reduces the ZVS range of the converter. The output filter inductor was chosen to give a maximum of 20% ripple at full load, i.e., $\Delta I_{\max} = 8$ A.

4) Output Rectifier: In designing the output rectifier, more careful consideration has to be given to the problem of snubbing the voltage across the rectifiers. The parasitic capacitances of the rectifier diodes form a resonant circuit with the leakage inductance of the transformer. This resonant circuit causes high-frequency ringing across the rectifiers as a response to step changes of secondary voltage. If not snubbed or clamped, the initial voltage spike across the rectifiers can be several times larger than the steady-state voltage, and therefore has to

be removed. This problem also exists in the ZVS-FB-PWM dc-dc converter, and can be mitigated using either an RC snubber, a passive clamp circuit, or an active clamp circuit [6]–[8]. In the three-phase rectifier circuit the active clamp cannot be used because pulses of v_s vary in magnitude. In this design, both a passive clamp circuit and RC snubbers were used. The clamp circuit limits the first voltage spike across the rectifiers, and transmits a part of the energy to the output. The RC snubbers across the rectifiers damp the remaining oscillations. In this design, 200 V, 50 A rectifier diodes were used. Such high voltage rating is required because a center-tapped-secondary transformer has been used. The total power dissipated in the clamp and the snubbers does not exceed 5 W.

5) Power Switches: For this design, 400 V, 25 A MOSFET's were selected. The on-resistance of the selected MOSFET's is 0.2 Ω, and the output capacitance C_M is 160 pF.

6) Leakage Inductance: In this design step the capacitance of the transformer C_T is assumed, and the value of leakage inductance is calculated. This can be done in two ways. One can choose $\Delta d(0)$, and calculate the leakage inductance from (18). Another way is to choose ZVS range, calculate I_{cr} from (23), and finally calculate L_{lk} from (22). When the converter is designed to provide a wide ZVS range, the loss of duty cycle $\Delta d(0)$ is relatively large. which has to be compensated by increase in the transformer turns ratio, n. This increases the current in the primary, and leads to reduction in efficiency. On the other hand, if the ZVS range is narrow, and the ZVS property is lost with relatively high currents in the primary, the parasitic inductances and capacitances in the primary circuit can cause ringing of voltage across the switches and increase switching losses. In this design the ZVS voltage range is retained to 40% of full load. With $I_L = 16$ A and $\Delta I_{\max} = 8$ A, (23) gives $I_{cr} = 3$ A. Assuming the transformer capacitance of $C_T = 200$ pF, the required leakage inductance is $L_{lk} = 8$ μH. This value of L_{lk} causes loss of duty cycle $\Delta d(0) = 0.11$ at full load. Since the leakage inductance of the designed transformed was only 4 μH, a small external inductor of 4 μH was added in series with the transformer primary.

This completes the first design iteration. The obtained circuit parameters can be checked against different design criteria (for example if $D_m + \Delta D(0) \leq 1$, etc.). If the results of the first iteration are not satisfactory, the assumed values of the circuit parameters have to be corrected, and the design has to be repeated until satisfactory results are obtained.

A series dc blocking capacitor of 5 μF has been placed in series with transformer to prevent any dc current from building up in the transformer primary. A single-stage input filter with corner frequency of 10 kHz has been placed in front of the converter.

B. Control Implementation

To reduce the controller complexity and cost, and to improve the controller reliability and performance, the controller prototype has been implemented using a digital signal processor. The detailed description of the controller implementation is provided in [12].

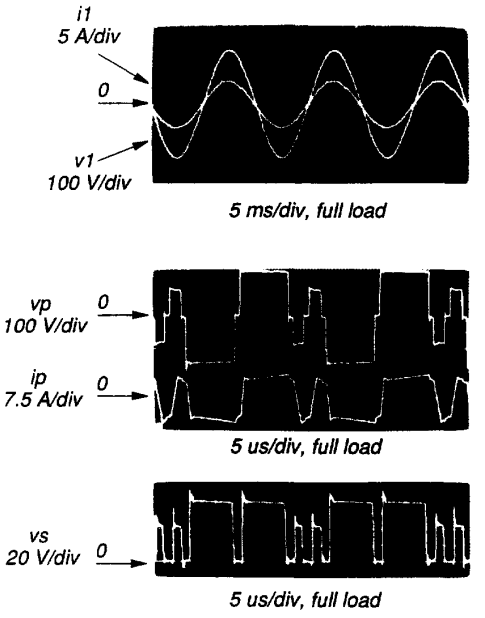

Fig. 11. Experimental circuit waveforms at 2 kW.

V. Experimental Measurements

Operation and performance of the proposed converter is illustrated by the following exeperimental results. Fig. 11 shows the waveforms obtained from the prototype operating at full load. Fig. 11(a) shows one input phase voltage and the corresponding current in front of the input filter. The current is undistorted, and in phase with the voltage. Fig. 11(b) shows the expanded view of the primary voltage v_p, and primary current i_p. Both primary voltage and currents are very clean, illustrating the ability of the circuit to absorb the parasitic capacitances of the switches and the leakage inductance of the transformer, thus making the high-frequency operation possible. Fig. 11(c) shows the corresponding rectified secondary voltage. The action of the clamping circuit and RC snubbers is apparent in the leading edges of v_s. Fig. 12 shows the primary voltage and current waveforms at the operating point where the ZVS property is lost. The waveforms are still very clean because the ZVS property is lost only partially, and because the primary current is less than half of the full load current. The abrupt drop of current that coincides with the trailing edges of v_p is caused by the discharging of the snubber capacitors across the rectifier diodes.

The efficiency measurement for different values of load current is shown in Fig. 13. The efficiency curve peaks between 40–50% of the full load current. The position of the peak coincides with the point at which the ZVS property is lost. At that operating point the conduction losses and the switching losses are small. As the load current is increased, the conduction losses rise, and the efficiency is reduced. At low load currents, the switching losses become larger, and residual losses are more significant, so that the efficiency rapidly drops below $I_L = 5$ A.

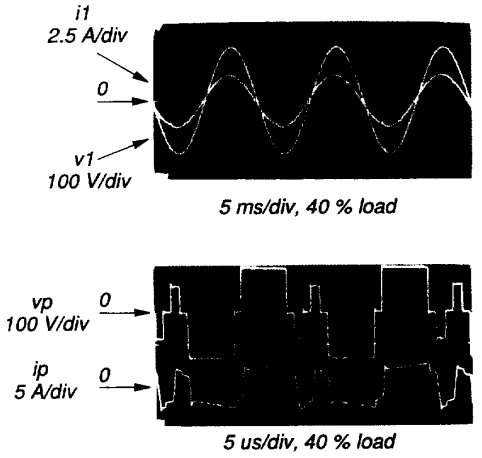

Fig. 12. Experimental circuit waveforms at 800 W.

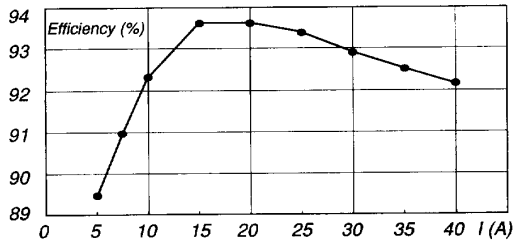

Fig. 13. Prototype efficiency as a function of load current.

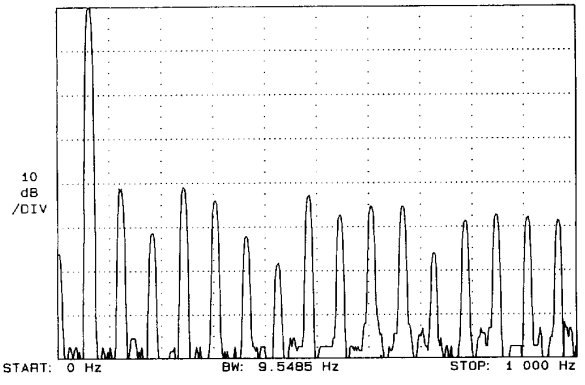

Fig. 14. Input current spectrum.

Fig. 14 shows the measured spectrum of the input current obtained from the prototype. The total harmonic distortion of the current, calculated from this measurement, is less than 2%. A part of the distortion is caused by the distortion of the input phase voltages which are used as references for the synthesis of input currents.

VI. Conclusion

The novel single-stage three-phase PWM rectifier presented in this paper offers the following distinct features:

- ZVS for all power semiconductor switches;
- tight output voltage regulation with fast transient response;
- unity input power factor;
- no low-frequency harmonics on either input or output; and
- transformer isolation.

In conventional approach, the above discussed features can only be accomplished using a two-stage conversion process consisting of a force-commutated, three-phase PWM rectifier (FCR) followed by a dc-dc converter. The first stage provides rectification and power factor correction, while the second stage provides transformer isolation and tight output voltage regulation. While a number of schemes have been proposed for the dc-dc converter, no soft-switching scheme has yet been proposed for the FCR. The proposed ZVS three-phase rectifier offers several significant advantages over this standard configuration.

The overall efficiency and size of the proposed ZVS rectifier is superior to that of the standard configuration. In the ZVS rectifier, the total conduction losses are reduced due to the fact that the current flows through two switches and four diodes, while in the standard configuration, the current always flows through four switches and four diodes. In the ZVS rectifier, soft switching conditions are provided for all devices. This eliminates the switching losses, significantly reduces the EMI problems, and eliminates the need for use of snubber circuits typically employed in the FCR.

The total number of semiconductor components is smaller in the proposed ZVS rectifier than in the standard configuration. Twelve active switches and four fast rectifier diodes are required for the implementation of the ZVS rectifier. In the standard configuration, ten active switches and ten fast diodes are required. In addition to this, there is no intermediate filter in the ZVS rectifier.

Being a buck-type converter, the ZVS rectifier presented in this paper is a good candidate for medium-power, high input voltage applications. In higher power applications IGBT's can be used instead of MOSFET's. In such a case, due to the ZVS conditions provided by the rectifier, lossless capacitive snubbers can be used to reduce the turn-off losses of the IGBT's. The loss of ZVS property at light load conditions is inherent to the proposed circuit. However, this does not represent a problem, because the ZVS property is lost only partially at light loads. Furthermore, at light loads, the conduction losses in the devices are very small, so that the additional switching losses will not pose any thermal problems.

VII. Appendix

A. Derivation of Maximum $d(\theta)$

In this derivation it is assumed that the output current ripple is small compared to the load current, which is a realistic assumption at full load where the loss of duty cycle is maximal.

From Fig. 6

$$I'_{dx}(\theta) + I''_{dx}(\theta) \simeq I'_{dy}(\theta) + I''_{dy}(\theta) \simeq 4nI_L. \qquad (25)$$

From (13) and (14):

$$\Delta d_x(\theta) \simeq \frac{4nI_L L_{lk}}{v_{12}(\theta)T_c}, \quad \Delta d_y(\theta) \simeq \frac{4nI_L L_{lk}}{v_{13}(\theta)T_c}. \tag{26}$$

Using (1), (6), (8), (11), and (26), it follows that

$$d(\theta) = -D_m\left[\cos\left(\theta - \frac{2\pi}{3}\right) + \cos\left(\theta + \frac{2\pi}{3}\right)\right] + \\ + \frac{\sqrt{3}}{4}\Delta d(0)\left[\frac{1}{\cos\left(\theta + \frac{\pi}{6}\right)} + \frac{1}{\cos\left(\theta - \frac{\pi}{6}\right)}\right] \tag{27}$$

where

$$\Delta d(0) = \frac{16nI_L L_{lk}}{3V_m T_c} \tag{28}$$

$d(\theta)$has a maximum for $\theta = 0$ if its derivative is negative for $0 \leq \theta < \pi/6$. If that is the case, we can write

$$d(0) = D_m + \Delta d(0) = 1 \tag{29}$$

and require

$$\frac{d}{d\theta} d(\theta) \leq 0. \tag{30}$$

Solving (29) and (30) for $\Delta d(0)$ gives

$$\Delta d(0) \leq f(\theta). \tag{31}$$

It is easily checked that $f(\theta) \geq 0.25$ for $0 \leq \theta < \pi/\ 6$. So, for $\Delta d(0) \leq 0.25$, $d(\theta)$ has a maximum at $\theta = 0$.

B. Derivation of Equivalent Capacitance C_{eq}

The energy needed to charge the capacitance of nodes A or B at $\theta = \pi/6$ is

$$E_c = \frac{4}{3}\sqrt{3}V_m)^2 C_M + \frac{4}{3}\left(\frac{\sqrt{3}}{2}V_m\right)^2 \cdot \sqrt{2}C_M \\ + \frac{1}{2}(\sqrt{3}V_m)^2 C_T \tag{32}$$

To explain how each term in (32) is derived, we examine the transition time t_1 in Fig. 6, taking place at $\theta = \pi/\ 6$. Just before t_1, the primary current is circulating through the switches q_{11}, and q_{21}. At time t_1, q_{21n} opens, and q_{23p} closes. The first term of (32) is the energy required to charge the capacitances of q_{21n}, and q_{23p}. The variation of voltage across each of these switches is $\sqrt{3}V_m$. The term 4/3 comes from the square-root dependance of the output capacitance of the MOSFET on the drain-to-source voltage [6]. The second term of (32) comes from the switch capacitances of q_{22}. At time t_1, the voltage between point B, and phase 2 changes from $\sqrt{3}V_m/2$ to $-\sqrt{3}V_m/2$. Due to the presence of the antiparallel diodes across each MOSFET, the variation of voltage across each of the two MOSFET's in q_{22} is $\sqrt{3}V_m/2$, and the output capacitance of each MOSFET is modified accordingly. The last term of (32) is the energy required to charge the parasitic capacitance of the transformer. The equations (19) and (20) are easily derived by regrouping terms in (32).

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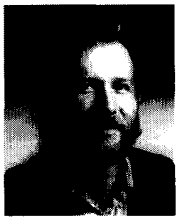

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