WBG DEVICES-BASED MATRIX CONVERTER FOR 3-PHASE AC TO DC CONVERSION IN INDUSTRIAL COMPUTING APPLICATIONS

An Undergraduate Research Scholars Thesis

by

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We, Jack Alagood, Kyle Bedrich, and Ian Farrar, certify that all research compliance requirements related to this Undergraduate Research Scholars thesis have been addressed with our Faculty Research Advisor prior to the collection of any data used in this final thesis submission.

This project did not require approval from the Texas A&M University Research Compliance & Biosafety office.

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ABSTRACT

WBG Devices-Based Matrix Converter for 3-Phase AC to DC Conversion in Industrial Computing Applications

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A devices-based 3x1 matrix converter is proposed for high voltage (HV) power delivery to industrial-scale computing operations such as AI model training, cloud computing, and crypto mining. The system described in this report aims to reduce the energy burden of these loads by improving power distribution efficiency. The project can be split into three key parts: a primary side matrix converter, secondary side transformer, and an external controls scheme.

The device begins with a matrix converter, which accepts a low frequency three-phase AC signal and outputs a high frequency one-phase AC signal. The matrix converter is controlled by a digital signal processor (DSP) connected to the gate drivers. A high frequency (HF) transformer then transitions the signal to DC and outputs 48 V.

The matrix converter consists of three wide-bandgap (WBG) bidirectional switches with gallium nitride (GaN) FETs. Using GaN technology provides greater power density over silicon carbide components, as does using a matrix converter over traditional rectifiers due to the lack of

DC-link capacitors. The experimental results of this report are from providing the matrix converter with 230 V.

A high frequency step down transformer transfers power from the 3x1 matrix converter on the primary side to the secondary side. The secondary side is composed of WBG, silicon carbide (SiC) semiconductors operating as switches in a rectifier. An inductor-capacitor (LC) filter reduces ripple in the rectified output.

The controls subsystem contains the logic and hardware necessary to switch the gate drivers for the GaN FETs. It relies on PowerSim to create the logic circuit, consisting of PLLs, sine wave generators, pulse-width-modulation (PWM) signal generators, and digital logic. For control I/O, a TI F28397D controlCARD handles the switching algorithm and outputs the PWM signal to the gate drivers.

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All other work conducted for the thesis was completed by the student independently.

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NOMENCLATURE

3x1	Three-to-one
AC	Alternating Current
ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
DC	Direct Current
DSP	Digital Signal Processor
FET	Field Effect Transistor
GaN	Gallium Nitride
GPIO	General-Purpose Input/Output
HF	High Frequency
HIL	Hardware-In-The-Loop
HPRC	High Performance Research Computing
HV	High Voltage
I/O	Input/Output
LC	Inductor-Capacitor
LV	Low Voltage
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
RC	Resistor-Capacitor
RMS	Root Mean Squared

SiC	Silicon Carbide
THD	Total Harmonic Distortion
TI	Texas Instruments
V	Voltage
WBG	Wide Bandgap
ZVS	Zero-Voltage Switching

1. INTRODUCTION

With today's remarkable demand for computing power, data storage, and artificial intelligence, there's no question our aging energy infrastructure is in dire need of upgrades. Fortunately, the necessary technology to develop said upgrades exists and is becoming more commercially viable with every passing day. Matrix converters, though not quite cutting edge, are a modern method for achieving high efficiency AC to DC power conversion while improving power density and overall functionality [1]. More recently however, research into gallium nitride (GaN) FETs shows they are capable of surpassing silicon carbide as the premiere semiconductor material in areas such as industrial computing.

1.1 Problem Statement

The emergence of cloud computing and data centers in the field of information technology has sprouted a new demand for energy that's expected to grow. To meet these demands, power engineers are responding with innovative energy delivery methods that promise to raise the ceiling on power conversion efficiency [2]. The aim of this research is to apply a 3x1 matrix converter topology for a more efficient step-down conversion from 3-phase AC power to DC, thereby reducing losses during the conversion process and making better use of power supplies. More efficient energy conversion creates an opportunity to lower carbon emissions and consider large-scale computing projects that otherwise would draw excess power.

1.2 Preexisting Research

Matrix converter-based topographies have been around for some time, yet the extent of their application continues to evolve. In the realm of electric vehicles, demand for faster DC charging is pushing automotive designers toward matrix converters due to their lack of

electrolytic capacitors [1]. Moreover, bidirectional power flow allows for using EVs as power sources instead of just loads [3]. In high power telecommunications, matrix converters promise to reduce the total harmonic distortion (THD) present in typical telecom-rectifier schemes in addition to simplifying the number of power conversion stages [4].

1.3 Scope and Limitations

The scope of this project is to provide proof of concept and to see whether or not GaN FETs can outperform their more established SiC counterparts. As such, the objective is not to create a ready to implement device, but to create a functioning matrix converter that doesn't consider the thermal limitations that would result from prolonged operation. To properly test a device similar to what is outlined in this paper, regulating temperature with heat sinks and a cooling system is necessary.

2. METHODS

The proposed topology is divided according to three subsystems: primary (3x1 matrix converter plus input LC filter), secondary (HF transformer, rectifier, and output LC filter), and controls to operate the FET switches on the primary and secondary sides.

2.1 3x1 Matrix Converter

The primary (front-end) subsystem refers to the 3x1 matrix converter responsible for converting a low frequency three-phase AC signal to a high frequency one-phase AC signal, as well as its I/O filters and voltage sensors. Schematics and footprints for this subsystem were modeled in Altium Designer.

2.1.1 Subsystem Description

The matrix converter is equipped with six digitally controlled bidirectional switches (two per phase), each of which are paired with an RC snubber to suppress potential voltage spikes. LC filters are placed before and after the switching array to limit the bandgap.

Each of the six switches contains two GaN FETs whose gate terminals share a gate driver circuit. The gate driver switches the FETs to their ON or OFF state according to the PWM control signal. When operating within the voltage limits of the FETs (230-650 V), the result is a consolidation of phases, from three to one, along with an increase in the signal frequency.

To verify the matrix converter is functioning as intended, voltage sensors monitor the positive and negative output voltages to be sent to the controls interface via an isolated amplifier with integrated DC/DC conversion. This also acts as a precaution to avoid damaging the more sensitive circuit components in the primary and secondary subsystems.

2.1.2 Subsystem Design and Validation

Primary subsystem validation requires (1) running simulations with various inputs to test edge cases, (2) confirming the controls subsystem is being provided with the necessary parameters (i.e. I/O voltages), (3) verifying the connection between the gate drivers and controls, and (4) testing the physical board. These are given in further detail below.

Validation begins by testing the board design in power electronic systems simulation software, such as PLECS. Power from the grid is provided by an ideal source, and voltage and current meters determine whether the expected behavior is observed. In the case that the circuit does not function as intended, component parameters can be altered and tested once more. Also, the input power signal should be modeled with fluctuations and/or voltage spikes to verify the system integrity.

With a working simulation (and all line currents well-within part limitations), we then make sure the controls hardware (TI controlCARD) is receiving the voltage sensor outputs. This is best accomplished through intentional debugging while referencing the relevant manuals. To avoid damaging equipment, refer to experienced faculty for directions.

Once the controls hardware is up and running and the state of the matrix converter is being actively monitored, we move to the final and most comprehensive validation step: testing the board. The PCB has built-in test points for recording voltages, so as each portion of the product is soldered, use a multimeter or oscilloscope for measurement, and compare those values to simulation. It’s best to assemble and test the board sequentially so as to identify and resolve issues the moment they arise.

2.2 High Frequency Transformer

The high frequency transformer facilitates the transfer of power between the matrix converter and rectifier while stepping the voltage down from 240 V_{RMS} line to line to 90 V_{RMS}.

2.2.1 Subsystem Description

Isolated power transfer from the primary to secondary side of the matrix converter is facilitated using a high frequency transformer. The high frequency transformer contains a ferrite core due to its ability to operate at higher frequencies and relatively high permeability facilitating efficient transfer of energy.

The transformer feeds the stepped down voltage into an AC-DC rectifier. Like the primary side, the secondary side uses WBG semiconductors as switches in the rectifier. An inductor and capacitor filter follows the rectifier to produce a more stable output and to minimize ripple.

Litz wire minimizes copper losses in the transformer coil windings. Selection of Litz wire configuration is discussed in section 2.2.2.

2.2.2 Subsystem Design and Validation

The high frequency transformer is designed in Ansys Maxwell, an electromagnetics simulation and modeling software. Core models are designed parametrically, allowing for the simple and quick adjustment of core dimensions by changing variable values. The “E” core shape was chosen for easier winding and lower core losses.

Due to the lengthy runtime and computationally expensive simulation process in Ansys Maxwell, the HPRC provided by Texas A&M University simulates different core model dimensions and windings. The transient simulation type in ANSYS Maxwell provides information on magnetic flux density in the core to determine if saturation is occurring. The

simulation also provides information on the losses occurring when the transformer is in operation. When deciding values for the mesh size and simulation time step, mesh size was simply adjusted decreased to the point where any further change would result in diminishing improvements in simulation results.

We run two simulations for each core model: one with a square voltage excitation applied to the primary winding and one with a sinusoidal current excitation applied to the primary winding. The square voltage wave was selected due to the switching behavior resulting in sudden shifts from positive to negative input voltages. The sinusoid wave shape was selected for the current excitation due to the resulting spike in voltage from sudden changes in current in the inductive elements of the transformer. The magnitudes of the excitations are set to the desired max rating for the matrix converter to ensure that the system can handle the maximum rated load. The frequencies of the excitations are set to 100 kHz to match the switching frequency set by the controls.

The core model with the best performance and efficiency as evaluated according to the above criteria was selected for the proposed design. On the primary transformer coil, one thousand 0.05 mm diameter Litz wire strands carry a rated current of 12 A, and on the secondary coil we have one hundred 0.20 mm diameter Litz wire strands handling a rated current of 20 A. These wires were chosen according to their current rating, strand size, and availability, as we are trying to avoid ordering custom designs. Litz wire reduces the copper losses resulting from the skin depth effect taking place at higher frequencies of AC current flowing through a wire. The maximum strand size is obtained by the following equation for skin depth where ρ is the resistivity of copper at room temperature (20 °C) and f is the frequency of operation (100 kHz).

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0}} \tag{1}$$

Different rules of thumb determine the desired strand size from calculated skin depth; in this paper, the strand diameter is limited to the calculated skin depth of 0.2 mm. The Litz wire material is simulated with Ansys Maxwell's built-in Litz wire model in the custom material build tool. Strand size, count, and the material properties of copper were used as inputs.

For simulation purposes, the windings are wound in a circular spiral pattern around the core's center leg. The primary coil is wound from one end of the leg until its end, then the secondary winding from where primary winding ends to the other end of the core's center leg. This was deemed sufficient for simulation to validate the design select a core type.

When the coils are wound around the real transformer, they are interleaved to reduce proximity effect losses, leakage inductance, and interwinding capacitance. These effects are ignored during simulation because they likely would not change the final core selection when all cores are limited in performance in the same manner and interleaving the windings would significantly increase the complexity of the model.

2.3 Controls Scheme

The controls include the logic, circuitry, and hardware parts managing the gate drivers of the matrix converter on the primary side of the board. The subsystem is crucial in controlling the operation of the matrix converter to ensure correct and efficient power conversion. It includes hardware and embedded control logic necessary to transform a 3-phase input signal into a stable AC output signal to facilitate smooth and reliable power transfer.

The primary objective of the control system design is to deliver a specified voltage level and reduce electrical noise and distortion. To accomplish this, the subsystem includes an open-

loop feedback circuit utilizing pulse-width modulation (PWM) techniques and logic circuitry that tell the gate drivers precisely when to turn on and off. The control system is also designed to ensure maximum efficiency, improve power factor correction, and offer safe operation in varying load conditions. The controls subsystem is fully responsible for the performance of the power conversion process.

Another main objective of the control system design is to thoroughly test and validate the proper operation of the system before its integration into the overall system. It is extremely important to ensure all components of the system operate as they should and lower the possibility of failure or malfunction when implemented within the final system. By finding and resolving issues sooner in the development phase, we can prevent errors in the subsystem and simplify and accelerate troubleshooting.

In order to achieve this level of dependability, we designed a comprehensive testing regimen specifically for the control subsystem. It entails rigorous testing on multiple levels: software validation through simulation and code verification, hardware testing to confirm all physical components function correctly, and hardware-in-the-loop (HIL) simulations to simulate real-time behavior under realistic operating conditions. These tests allow us to fine-tune the system, optimize its efficiency, and confirm its stability before moving to full integration. With the help of this structured process of testing, we verify that the control subsystem would perform as desired, avoiding potential unwanted issues and ensuring smooth functionality when implemented within the framework of the overall system.

2.3.1 Subsystem Description

The control subsystem governs all hardware and software elements involved in switching gate drivers for the matrix converter to influencing correct power conversion on the primary side

of the system. The controls subsystem has the central role to play in assisting the efficient and reliable operation of the matrix converter under conditions of varying loads. The entire system is regulated by a Texas Instruments C2000 microcontroller, chosen for its good performance and real-time control capabilities. The TI Delfino F28379D controlCARD interfaces with the hardware, providing the required I/O to control the matrix converter.

The controlCARD is the core hardware platform, offering a wide range of analog and digital I/O functions. These include analog-to-digital converter (ADC) inputs to monitor voltage and current sensor signals and general-purpose input/output (GPIO) pins to deliver digital switching signals for driving gates. The ADC inputs are needed for continuous monitoring of system performance, and the digital outputs enable precise control of the switching states of the converter.

In case a stable output voltage is desired, the control system contains an open loop feedback circuit and sensors to detect the input voltage, output voltage and other electrical parameters. Based on sensor data of the input voltage, the system dynamically alters the switching patterns in order to operate correctly at a setpoint using a PLL logic circuit. Furthermore, the sensors accomplish zero-voltage switching (ZVS), a technique for minimizing switching losses and improving overall efficiency by having switches turn on only when voltage levels are approximately zero.

While the proposed design uses the TI controlCARD for control and signal processing, a future version might prefer a custom PCB to host the control electronics. The custom PCB would integrate the microcontroller, power electronics, and the signal conditioning circuits needed in an integrated and optimized design with increased reliability and performance of the control system.

The control subsystem consists of both logic and hardware components that work together to regulate the switching of the matrix converter, enabling the conversion of a 3-phase input to a stable AC output signal. The logic is entered into the software and is responsible for executing a switching algorithm that precisely controls the converter's operation. This algorithm is designed in PowerSim, a specialized power electronics simulation software that allows for detailed modeling and validation of the control logic before generating the necessary embedded code for the TI Delfino F28379D controlCARD.

To create the signal in real life, we implement a TI F28379D controlCARD in conjunction with an expansion board with a built-in ADC, DAC, and GPIO. The control logic input is sent to the ADC, and the switching signal for the gate drivers is output from the GPIO pins.

2.3.2 Subsystem Design and Validation

Validation of the subsystem is an important development step since it ensures that each subsystem will function as required once it has been incorporated into the entire system. It is a step that is required to verify the performance, reliability, and stability of the subsystem before full implementation. The process of control subsystem validation is divided into three distinct phases: software validation, hardware validation, and combined logic and hardware validation, which is conducted with the assistance of hardware-in-the-loop (HIL) testing. All three phases are essential to the guarantee of correct operation of the control subsystem in real conditions.

Software validation is the first step in the process, in which the control logic is designed and tested alongside the power circuitry within a simulation framework. It involves implementing control algorithms, setting up system parameters, and modeling the desired system

performance. The primary purpose of this step is to simulate how the control logic interacts with the power electronics such that the designed algorithms will respond as intended.

To achieve everything described, we employ PowerSim as the primary verification software. With the control logic coded, the simulated system is observed under various conditions. The obvious issues, including phase misalignments and invalid output, were identified and corrected before moving ahead with the hardware realization. This phase of development is critical because it offers quick iteration and debugging in a risk-free environment prior to physical hardware testing.

Following software validation, the next step is hardware validation, which seeks to confirm that the control logic can be compiled, uploaded, and executed on the target hardware platform without any issues. This process verifies if the microcontroller can execute the control logic in real time and manage signal inputs and outputs at the desired frequency.

For hardware validation, the TI F28379D controlCARD is known for its processing capability and support for control applications. The methodology begins by generating code via PowerSim's code generation facility, which is capable of seamless integration with TI controlCARDs. This facility allows for automatic conversion of the validated software model to executable code to catch errors in manual code. Once the code has been generated, it is subsequently imported into TI Code Composer Studio, then compiled and uploaded onto the controlCARD. The uploaded code is then subjected to testing on the actual hardware.

The last step of the validation process is the logic + hardware validation, wherein both the control logic and hardware are combined into a real-time test environment. Hardware-in-the-loop (HIL) testing is conducted in this step to simulate real-world conditions with real hardware

components. This is a critical step to ensure that the complete subsystem functions properly before integrating it with the rest of the subsystems in the complete system.

For HIL testing, we have a Typhoon HIL 602+ box along with Typhoon HIL Control Center software. This setup enables a high-fidelity simulation of the system where the best circuit topology is created, and actual switching logic is implemented. Under the use of the HIL system, communication in real time among the control algorithms and hardware components is kept within real-world operating conditions so that the control subsystem performs as expected.

HIL configuration allowed exhaustive testing of multiple scenarios, including transient response, faults, and varying load profiles, allowing the engineers to identify and rectify any potential errors before deployment. This process significantly reduces the chance of failures at the last stage of integration.

2.4 Secondary Side Rectifier

The secondary side rectifier is composed of four wide bandgap silicon carbide MOSFETs being operated by the control system defined earlier. Following the rectifier is an LC filter to minimize voltage ripple effects.

2.4.1 Subsystem Description

The rectifier uses silicon carbide instead of gallium nitride MOSFETs since it receives a lower voltage than the matrix converter due to the step-down transformer, so there is no need for the gallium nitride to handle the higher voltages as in the matrix converter side of the circuit. The LC filter aids in creating a more precise DC output in the final stage of the topology.

2.4.2 Subsystem Design and Validation

The output rectifier is designed to accept the transformer's high frequency step-down AC voltage and convert it to 48 volts DC. Much like the matrix converter, this is validated through

simulating the power in and recording the power out, then comparing real values once the prior subsystems have been installed on the physical board.

2.5 System Integration and Testing

2.5.1 Integration

After each subsystem is complete and tested in isolation, the transformer coils will be soldered to the primary side and secondary side PCBs to facilitate power transfer between the two stages. The microcontroller unit will receive the sensor outputs and provide the control pulse width modulation signals via header pins on both PCBs.

2.5.2 Overall System Testing

The completely integrated system must be validated after assembly and after each subsystem passed the testing procedure outlined in its respective section above. The rated primary voltage of 230 V_{RMS} line to line is applied to the input of the matrix converter. Oscilloscopes and multimeters validate expected signals and voltage and current levels throughout the circuit. Measured points of interest include output of gate drivers, PWM signals, primary and secondary windings of the transformer, and DC output.

The input and output voltages and currents are measured to determine the input and output powers (**Equation 2**). Efficiency is then found from the calculated power in and power out values.

$$P = IV \tag{2}$$

The heat being produced by the system is also observed. As the aim of this paper is proof of concept, the device aims to only operate for a limited period of time and thus heat generation is not a practical concern beyond its relation to loss and efficiency. The monitoring of temperature prevents damage to the device while collecting under test to collect data.

3. RESULTS

3.1 3x1 Matrix Converter

3.1.1 Initial Planning

Shortly after the project's proposal, the elephant in the room for designing the matrix converter was a complete lack of knowledge of PCB design as well as Altium Designer. In retrospect, an attempt to create the final product right out of the gate would have likely ended in failure; we needed at least an elementary understanding of PCB design standard practices and the Altium interface to create something cohesive. After discussing with our faculty advisor Dr. Prasad Enjeti and his graduate assistant Peng-Hao Huang, it was decided that our team would spend the first portion of the project timeline making a single-phase prototype converter, then adapt it to be three-phase once most of its issues were resolved. As a result of this plan, a majority of issues were addressed prior to making the final product.

3.1.2 Single-phase Prototype

Like the matrix converter, the single-phase converter was given no limitations on size or weight beyond industry standards, which were quite lax, thus initial drawings for the prototype could take any form, so long as the following PCB best design practices were maintained:

1. Minimum part dimensions set at 1206 (for easier soldering)
2. Low and high voltage systems must be far enough apart to prevent risk of shorting
3. Where copper pours are not appropriate, HV traces must be very thick (~50 mils)
4. Traces should be as short as possible
5. Decoupling capacitors should be placed adjacent to their respective power supply

Following these guidelines, we came to the following layout (**Figure 1**). High voltage components are contained in a central area surrounded by low voltage traces and pours that reach around to connect the voltage sensors back to their designated pins.

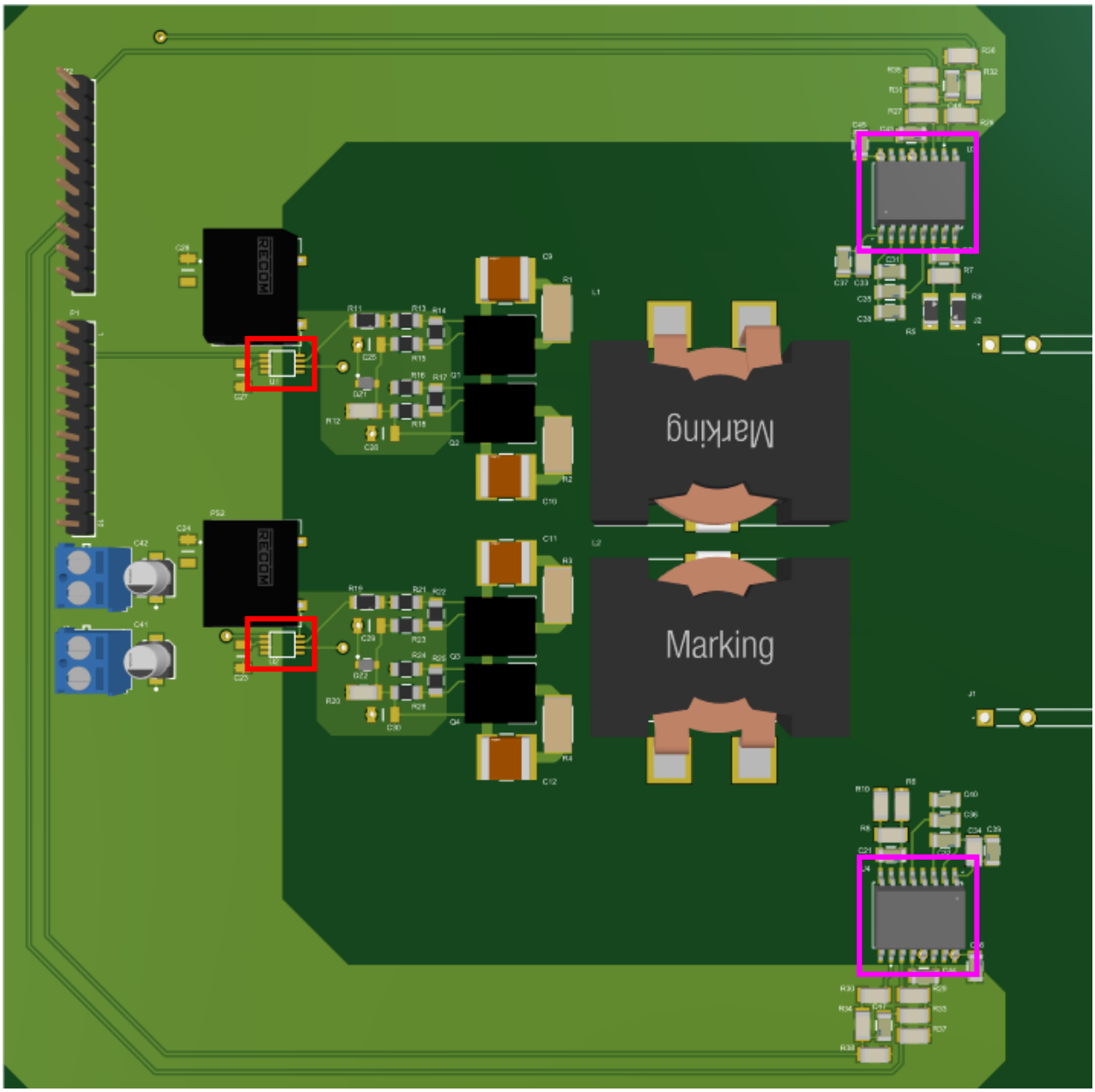

Figure 1: Single-phase converter PCB prototype. Low and high voltage elements are connected by gate drivers (red) and voltage sensors (pink).

Note that in comparison to the end product, this prototype is incomplete. Several changes such as bringing the two switches closer to one another, resizing the traces to the left of the GaN FETs, and adjusting the position and orientation of the LC filters to better align with the RC snubbers are needed. The smaller details were also ignored for the time being.

3.1.3 Three-phase Product

3.1.3.1 General Layout

The 3x1 matrix converter would ultimately take on a different layout than its predecessor. Rather than surrounding HV components with LV, we have LV components north of the board and HV to the south (**Figure 2**). This allows for easier access to HV inputs and outputs and ensures most connections stay relatively straight.

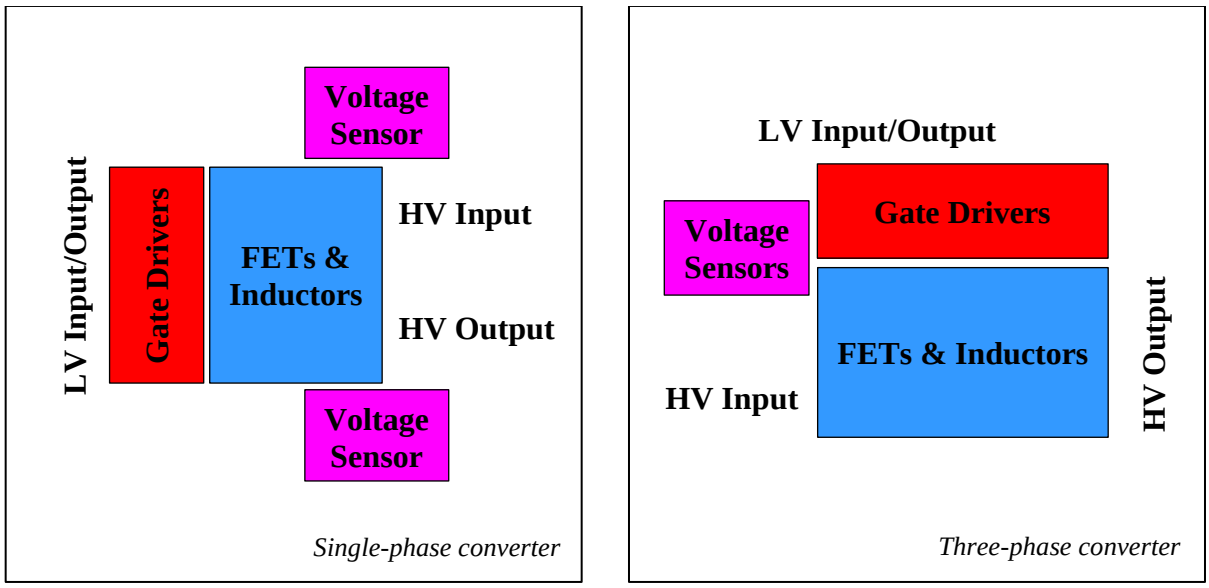

Figure 2: Single- and three-phase converter PCB layouts (not to scale).

Whereas the prototype PCB only uses a top and bottom layer, the three-phase board requires six: one layer per phase, two for input/output signals, and one layer for separation. From top to bottom, the netlists with copper pours per layer are:

1. **A**, **A_src**, and **GND**

2. **B**, **B_src**, and **GND**
3. **C**, **C_src**, and **VEE**
4. **+5 V** (aka **EN**)
5. **+12 V** and **Vmc_P**
6. **GND** and **Vmc_N**

Netlists **A_src**, **B_src**, and **C_src** are the per phase input powers from a 230 V transmission line (note that additional protections would need to be put in place prior to making this connection). Signals **Vmc_P** and **Vmc_N** are the positive and negative matrix converter outputs, respectively; they are to be the inputs for the HF transformer described in section 3.2. Layer 4 separates the inputs from the outputs, and PCB stands allow for vertical stacking.

3.1.3.2 Power Flow

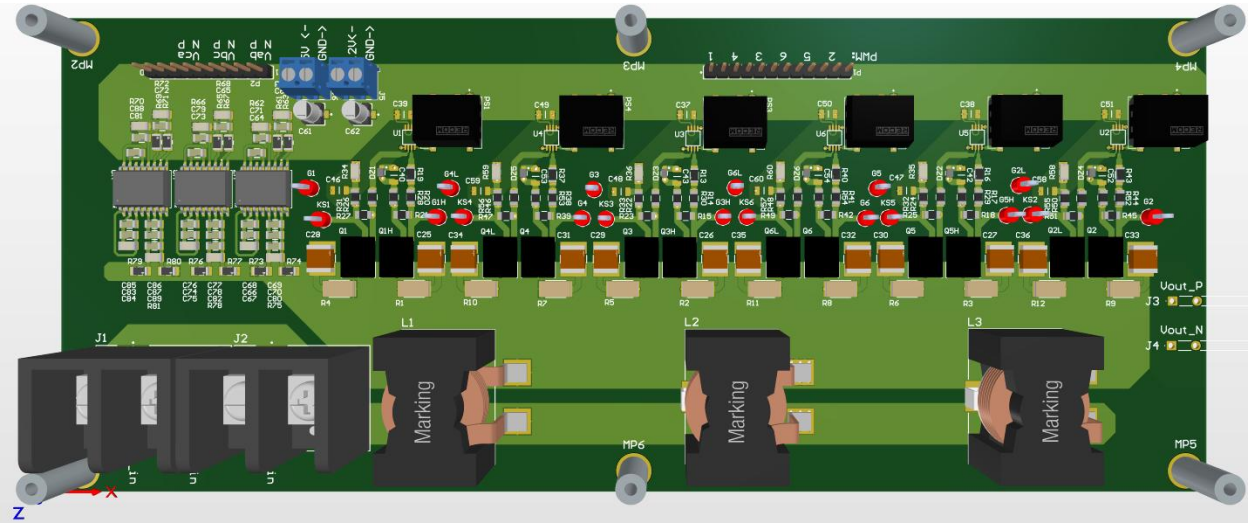

Figure 3: 3-phase matrix converter PCB (top view).

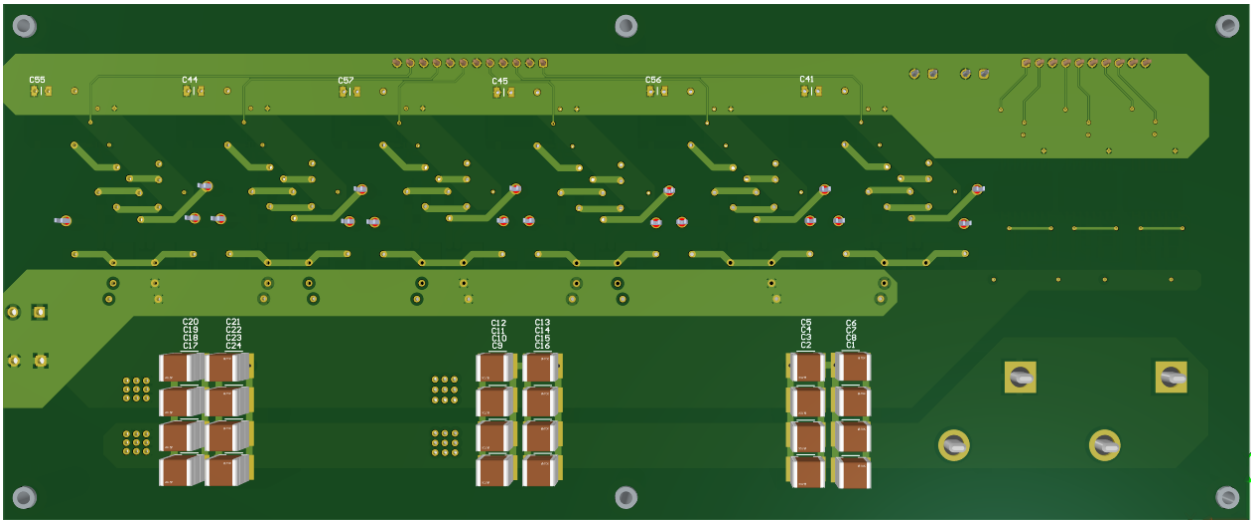

Figure 4: 3-phase matrix converter PCB (bottom view).

To summarize the power flow through the board, we begin at the north edge where there are six pins dedicated to the PWM signals sent from the controls described in section 3.3. Each **PWM** pin is juxtaposed with **GND** pins to avoid shorting and is arranged closest to its corresponding gate driver. The gate drivers are ordered 1-4-3-6-5-2 left to right because this arrangement minimizes the length of connections within netlists **A**, **B**, **C**, **Vmc_P**, and **Vmc_N**. The gate drivers can operate with 3.3 V or 5 V, but we selected 5 V as no other components require 3.3 V. To the right of each gate driver is a RECOM® power supply labeled that accepts 12 V.

Each gate driver's output is fed through a series of resistors and capacitors before reaching the gate and Kelvin source terminals of two GaN FETs. These signals are designated test points. One FET is attached to a filtered input phase voltage **A** (drivers 1 and 4), **B** (3 and 6), or **C** (5 and 2) at its drain. The other's drain is connected to either **Vmc_P** or **Vmc_N** and is designated an "H" for high or "L" for low (**Figure 5**).

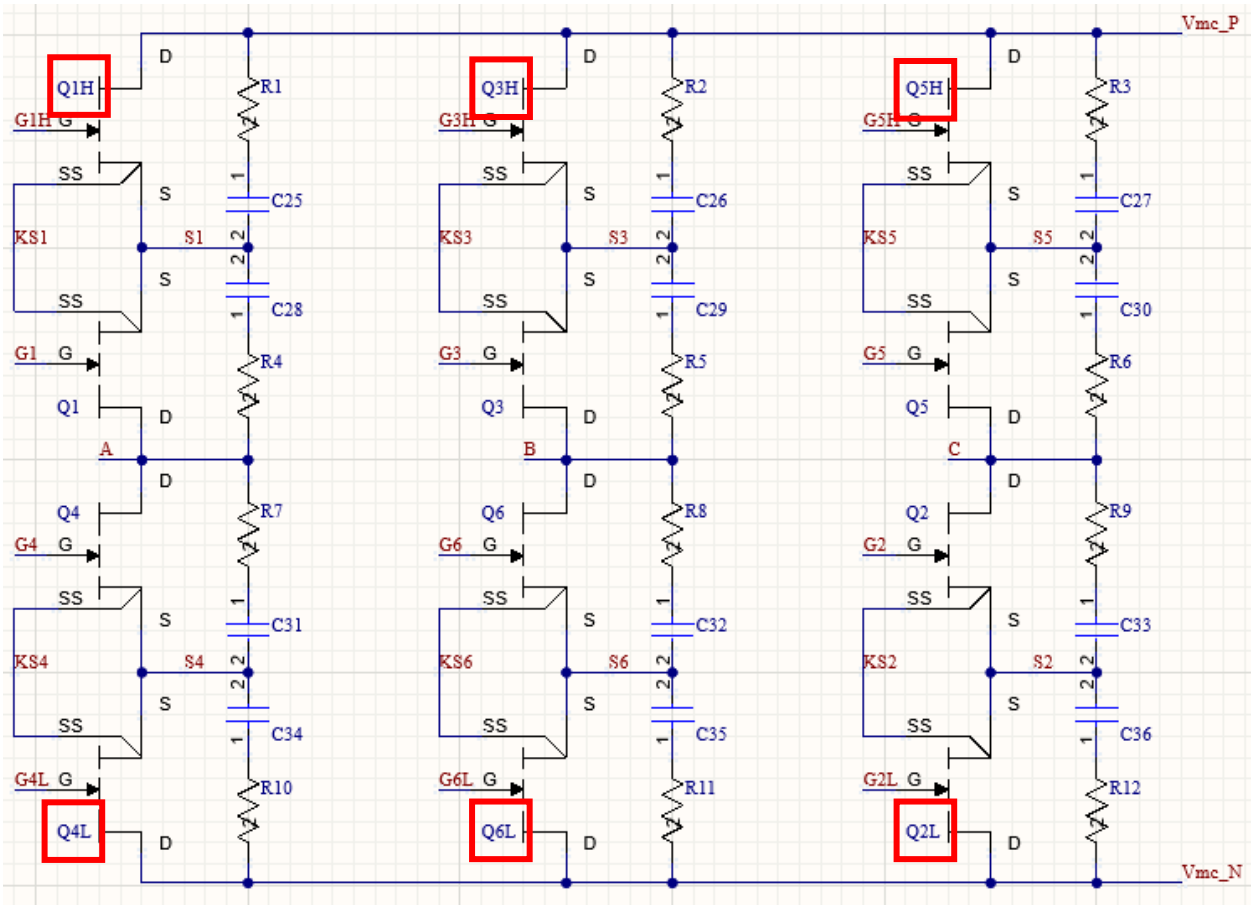

Figure 5: 3-phase matrix converter schematic. High and low GaN FETs are identified in red.

It is at this point that by the switching algorithm from the controls scheme, the PWM signals and gate drivers should have successfully gated the FETs to transform our 3-phase AC input to a single-phase high frequency AC output. **Vmc_P** and **Vmc_N** are sent to the output tabs “Vout_P” and “Vout_N” found on the right side of the board. The remaining outputs all come from the voltage sensors; signals **A**, **B**, and **C** enter resistors R73 through R81 on the south side of the sensors, and the voltages between phases are input as **Vab**, **Vbc**, and **Vca**. The voltage sensors then output a much lower but proportional voltage that’s safe to be read by lab equipment. These voltages, **SENab**, **SENbc**, and **SENac** can be measured at pin header “P2”, placed near the board’s northwest corner.

3.2 High Frequency Transformer

3.2.1 Simulation

A transformer simulation model was created to quickly simulate different geometries and transformer designs. Although the simulation model was not completed in time to influence the purchasing of the actual core used, simulations were conducted to evaluate how well different cores may have performed and how different design parameters affect transformer behavior and performance.

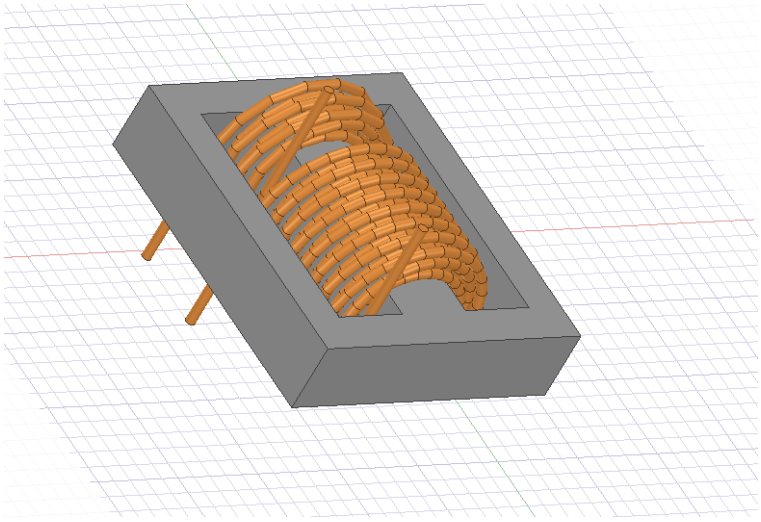

Figure 6: Transformer undergoing testing isolated from rest of system. Input voltage is applied to the primary coil, and a resistive load closes the secondary coil.

First, the step-down voltage of the transformer for different configurations was simulated and observed (**Figures 7** and **8**). We demonstrate how the step down holds around 3 to 8 as frequency increases, verifying the transformer's ability to facilitate power transfer across a wide frequency range. Note that for the following tests, the transformer is supplied with a 340 V peak square wave and is connected to a 5 Ω secondary side load.

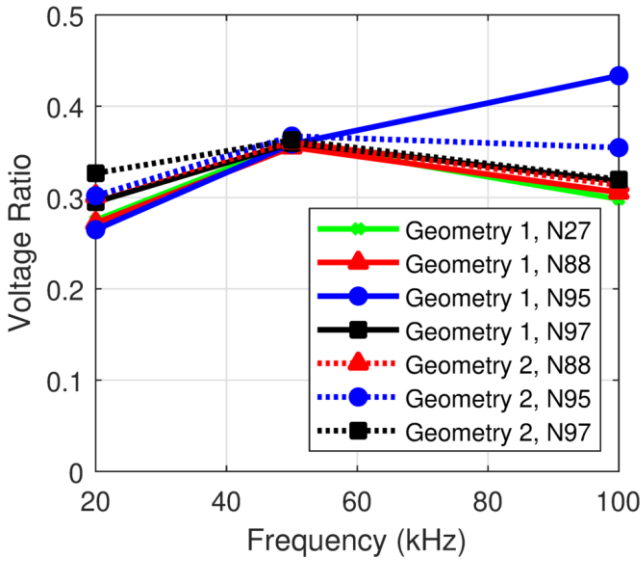

Figure 7: Secondary to primary voltage ratio for 340 V peak square wave voltage excitation.

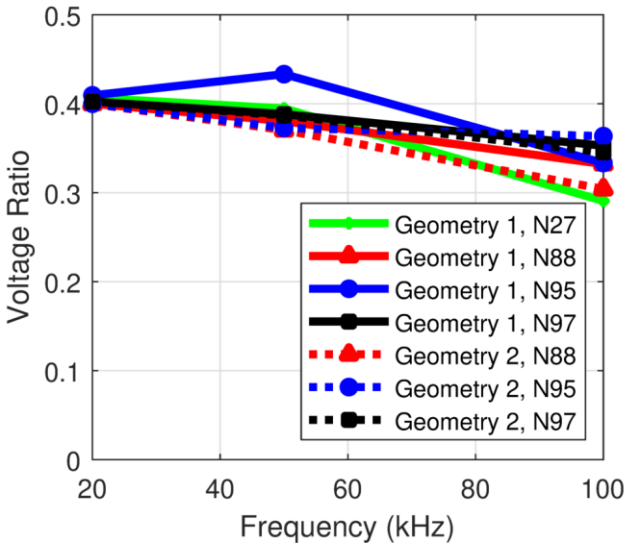

Figure 8: Secondary to primary voltage ratio for 7 A peak sinusoidal current excitations.

The expected ratio is 3:8, or 0.375. In both setups, the voltage ratios seem to hold around this expected value.

Next, we evaluated the core magnetization at different frequencies for the 340 peak input voltage to check for saturation. This was done at 20 kHz, 50 kHz, and 100 kHz. At each

frequency, the number of layers of windings was changed to create multiples of the turn ratio (**Figures 9**, **10**, and **11**).

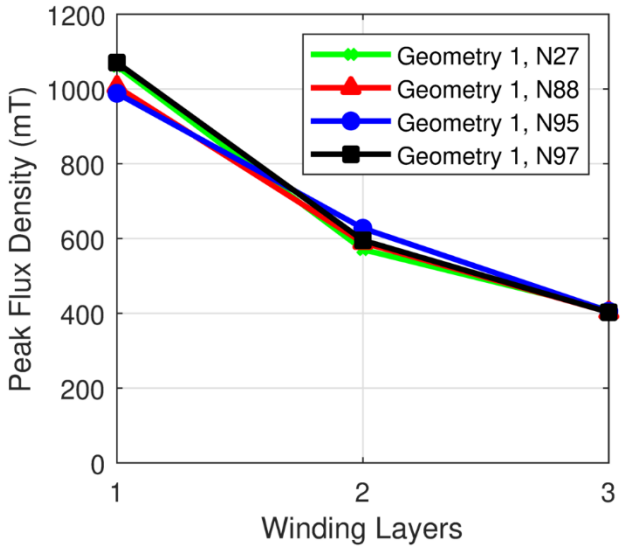

Figure 9: Core peak flux density at 20 kHz.

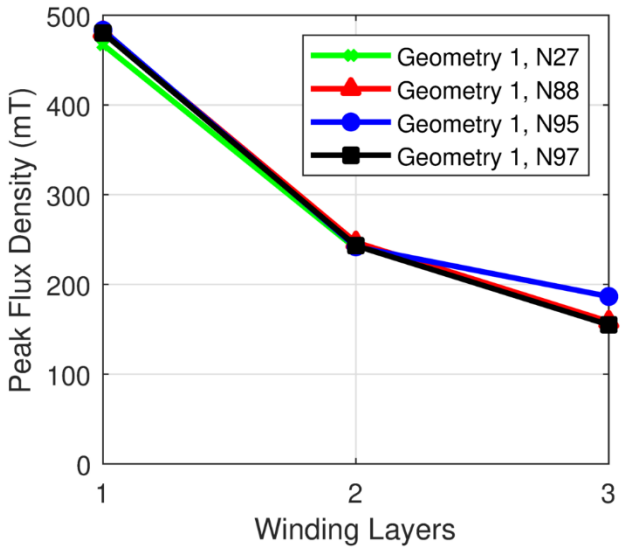

Figure 10: Core peak flux density at 50 kHz.

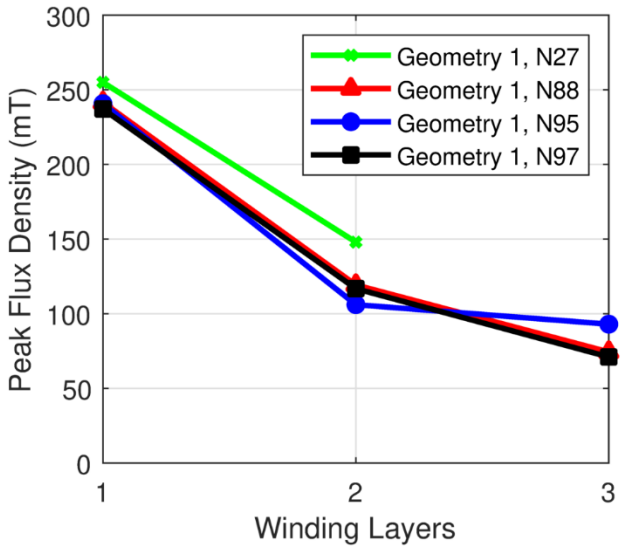

Figure 11: Core peak flux density at 100 kHz.

From the previous charts, we observe that as the number of turns and frequency increase, the peak flux density decreases. The next observation regarding simulated transformer behavior regards losses as the number of winding turns change (**Figures 12**, **13**, and **14**).

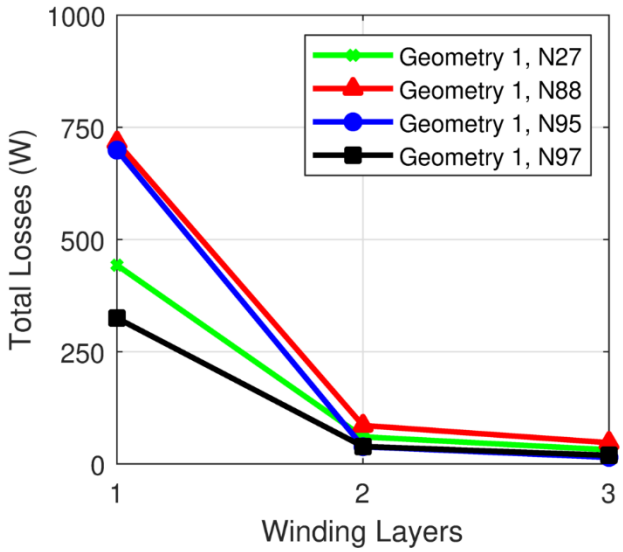

Figure 12: Total losses at 20 kHz.

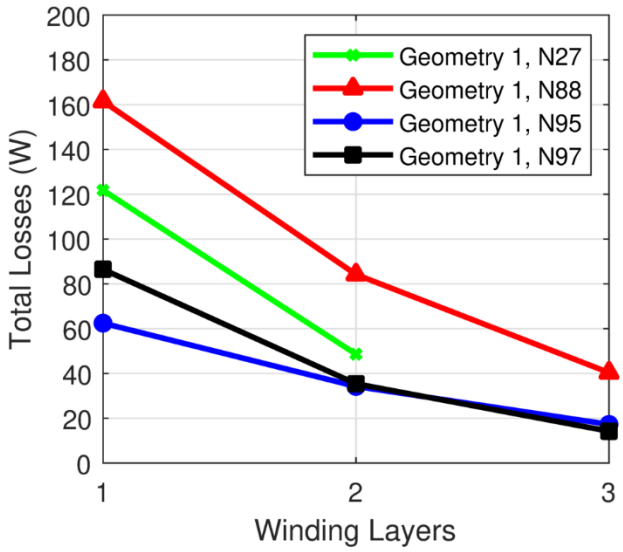

Figure 13: Total losses at 50 kHz.

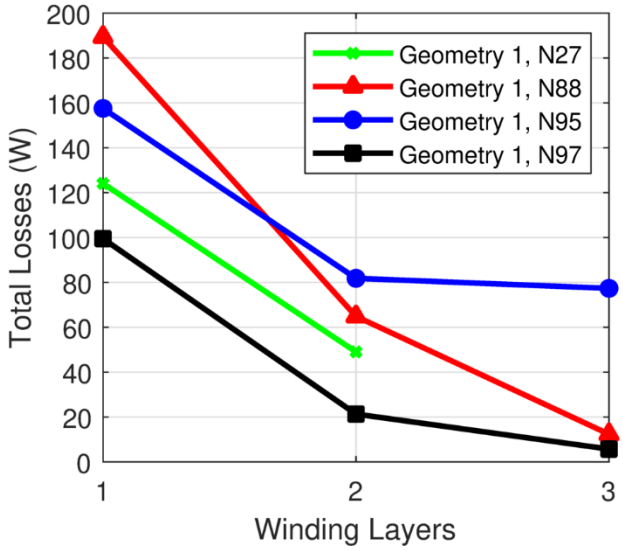

Figure 14: Total losses at 100 kHz.

Increasing turns can help reduce core losses, but it also adds conductive losses as the length of winding wire increases. These plots reveal that some transformer configurations may achieve their minimum losses by around 3 layers of primary windings, while others seem to still have room for decreasing losses with additional layers. Due to model geometry, the maximum

number of winding layers that could fit in the winding window without clipping was 3. The significantly higher losses in Figure 12 with one layer of winding can be attributed to losses associated with core saturation as the lower frequency and lower number of turns increase flux density.

To evaluate the efficiency, the output power was calculated using the secondary winding's current and voltage. This output power and total losses were used to calculate efficiency (**Figures 15**, **16**, and **17**). A similar marked decrease in performance occurs at 20 kHz and one layer of winding.

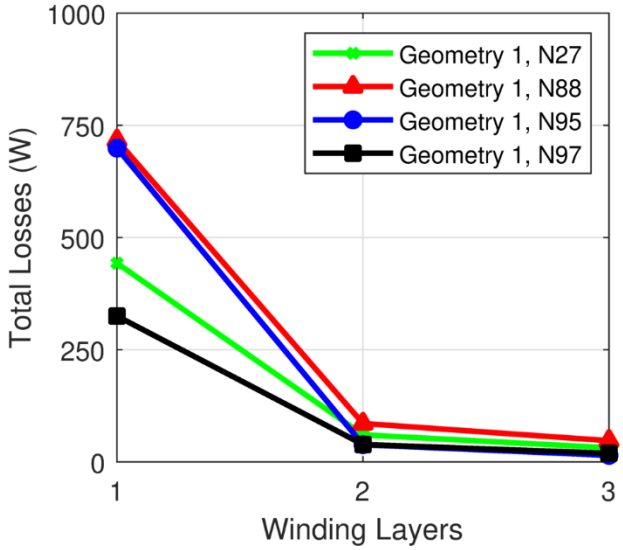

Figure 15: Efficiency at 20 kHz.

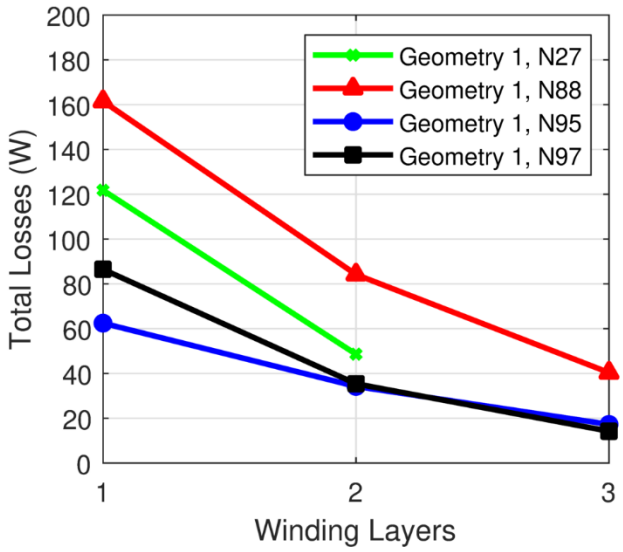

Figure 16: Efficiency at 50 kHz.

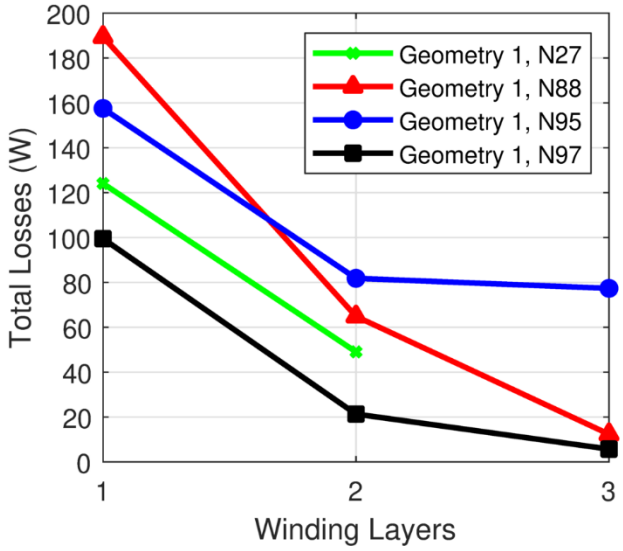

Figure 17: Efficiency at 100 kHz.

3.2.2 Real Testing Results

Due to time constraints, transformer core selection was conducted without simulation results as the simulation process and model were still being refined at the required time of purchasing parts. To identify the purchased core, ferrite cores available off the shelf from vendors such as Digikey and Mouser were first identified. Next, the peak flux density was calculated at different amounts of turns for each core (**Equation 3**).

$$B_{max} = \frac{V_{rms}}{kNA_e f} \tag{3}$$

N is the number of turns on the primary winding, A_e is the effective cross-sectional area of the core, f is the frequency of operation, and k is a constant depending on the voltage waveform. For simplicity, the switching signal was assumed to be a simple sinusoid, and k was subsequently set to 4.44. If a core would not saturate with a reasonable number of turns according to the saturation flux provided by the datasheet, then the core would be kept as a candidate. Cores readily available to be purchased but not fulfilling this requirement were removed from contention. After this elimination, two core shapes remained, each with the same material options available. The core shape with the larger effective cross-sectional area, winding window, and volume (TDK's E100/60/28 core) was selected. The larger volume and area allow for greater power transfer without saturating. The larger winding area ensures that there would not be difficulty in achieving the desired number of turns around the core. The material for this shape was then selected using the datasheet provided core loss plots as a function of frequency, temperature, and flux density. The material that seemed to minimize losses at the desired operating conditions was TDK's N95 ferrite material.

Additionally, the Litz wire identified in section 2.2.2 was not able to be purchased and delivered within the time constraints, so an alternative was identified for availability. The

primary was wound using 14 AWG Litz wire made of 260 strands of 38 AWG wire. The secondary was wound using Litz wire made of 600 strands of 38 AWG wire.

The coil former associated with the selected core shape for the winding and bonding of the two E cores was not available for purchase, so guides for core alignment and a bobbin for the windings were modelled in SolidWorks and 3D printed in PLA. Trigger clamps were utilized to press the two cores together.

The high frequency input PCB to the primary winding has not been completed, so the transformer was tested using a similar pre-existing PCB operating at 10 kHz and 10 V_{RMS}. The testing setup is shown below (**Figure 18**).

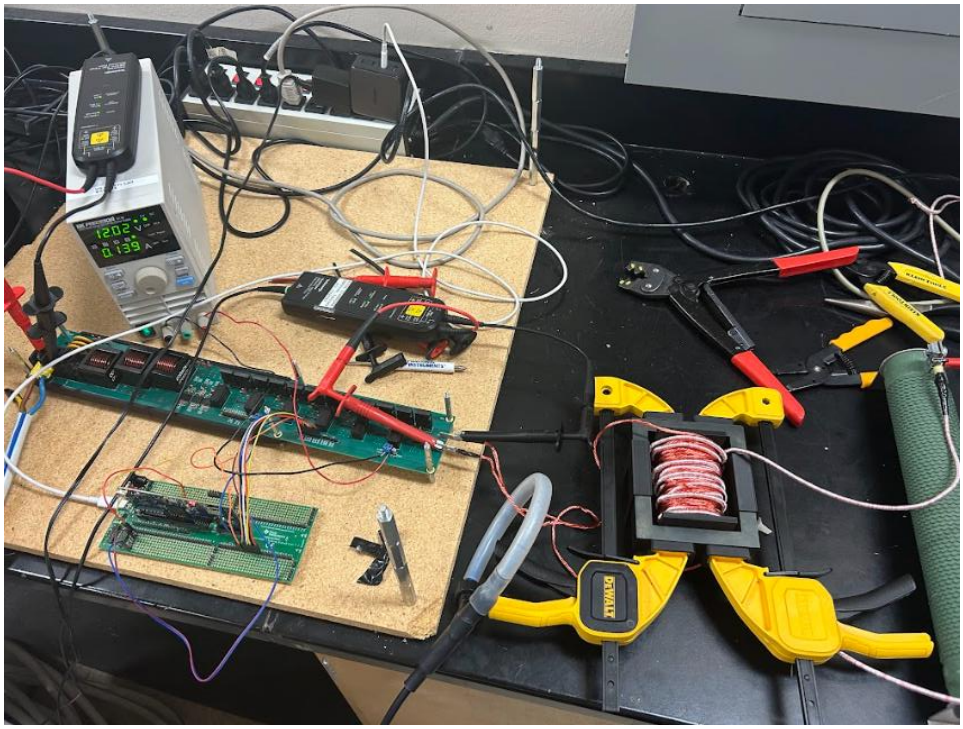

Figure 18: Transformer testing setup.

Input/output voltage and current were measured using an oscilloscope; these are given below (**Figures 19** and **20**).

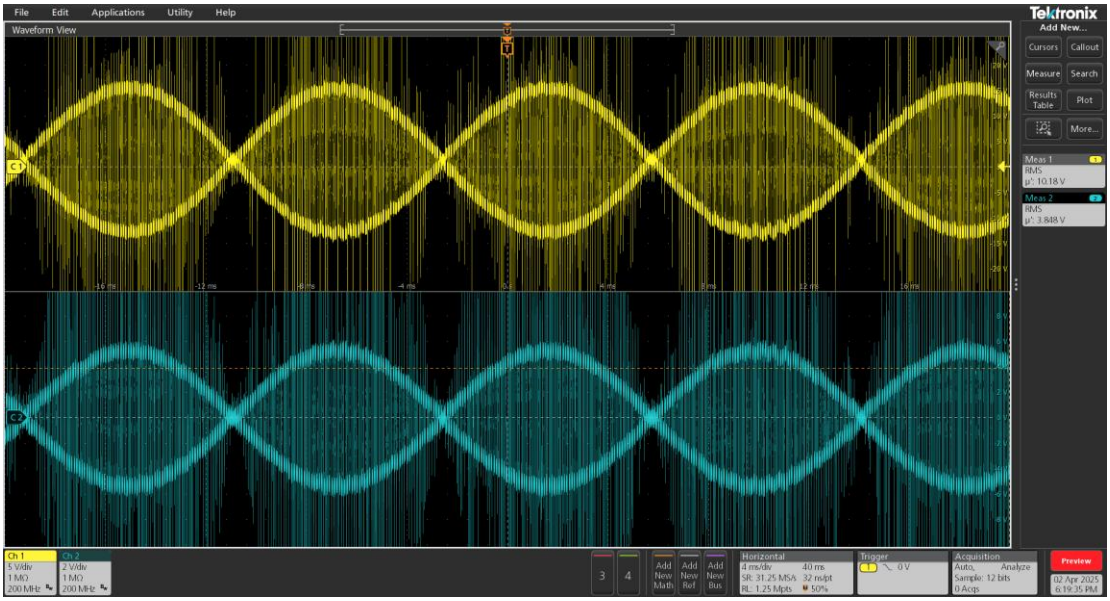

Figure 19: Input (yellow) and output (blue) voltages.

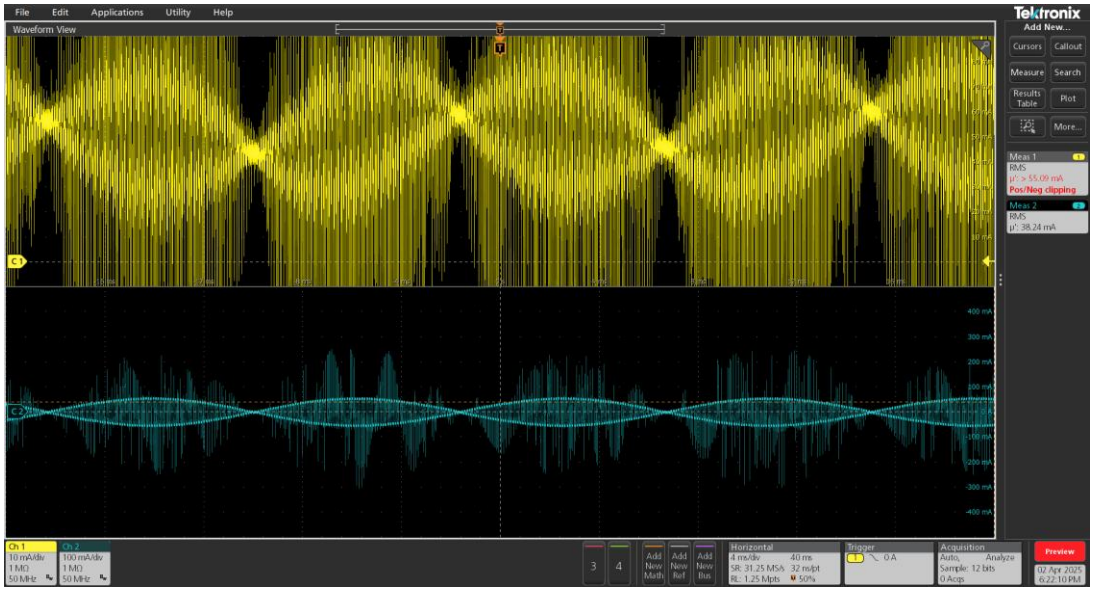

Figure 20: Input (yellow) and output (blue) currents.

The signal generation providing the input signal currently produces overshoot seen in the spikes in measurement. Otherwise, the input and output voltages were clean AC signals. The measured output current was also a clean AC signal, but input current had a DC component. The source of the DC signal is being investigated. The input power was calculated twice, once with

the measured current value, and once with an estimated value eliminating the DC component. Measured, estimated, and calculated values of interest are provided below.

Table 1: Measured voltage values.

Input Voltage (V RMS)	Output Voltage (V RMS)
10.18	3.848

Table 2: Measured and estimated currents.

Input Current (mA RMS)	Estimated AC Input Current (mA RMS)	Output Current (mA RMS)
55.09	15.91	38.24

Table 3: Input and output powers.

Input Power (mW)	Input Power with Only the Estimated AC Input Current (mW)	Output Power (mW)
560.82	161.96	147.15

The estimated AC input current was determined by identifying the peak-to-peak value of the current packets and ignoring the spikes (roughly 45 mA peak-to-peak) and then converting from peak-to-peak to RMS via the conversion for a sinusoid by dividing the peak-to-peak value by 2.828. As the calculated powers show, the efficiency of the transformer is drastically decreased by the DC current offset.

The step-down functionality of the transformer behaved as expected. The desired ratio was 8:3, or 2.67. The ratio for the input and output voltages comes to 2.64, and by the estimated AC input current, the current ratio comes out as 2.40.

3.3 Controls Scheme

The control logic and testing simulation was created in PSIM. PSIM allows us to test the functionality of the control logic on a simulated circuit so that when it is implemented with the other systems it will function properly.

3.3.1 Controls Scheme Layout

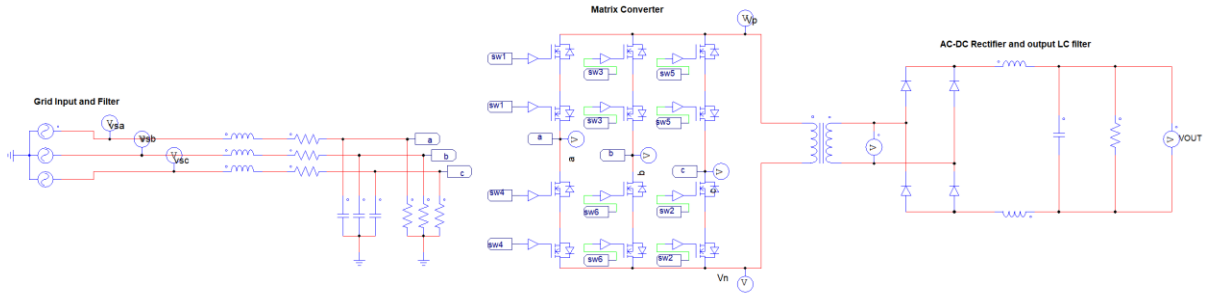

Figure 21: Testing circuit for the controls scheme in PSIM.

The above PSIM model shows the testing circuit for the controls scheme in PSIM. This is also a visual representation of the circuit layout to be built. The 3-phase AC grid input passes through an LC input filter and the 3x1 matrix converter reduces it to a single-phase AC signal. That signal is then passed through the transformer which steps down the voltage, and a rectifier converts the AC signal to DC and outputs through a second LC filter, with a resistive load at the end to represent load on the circuit.

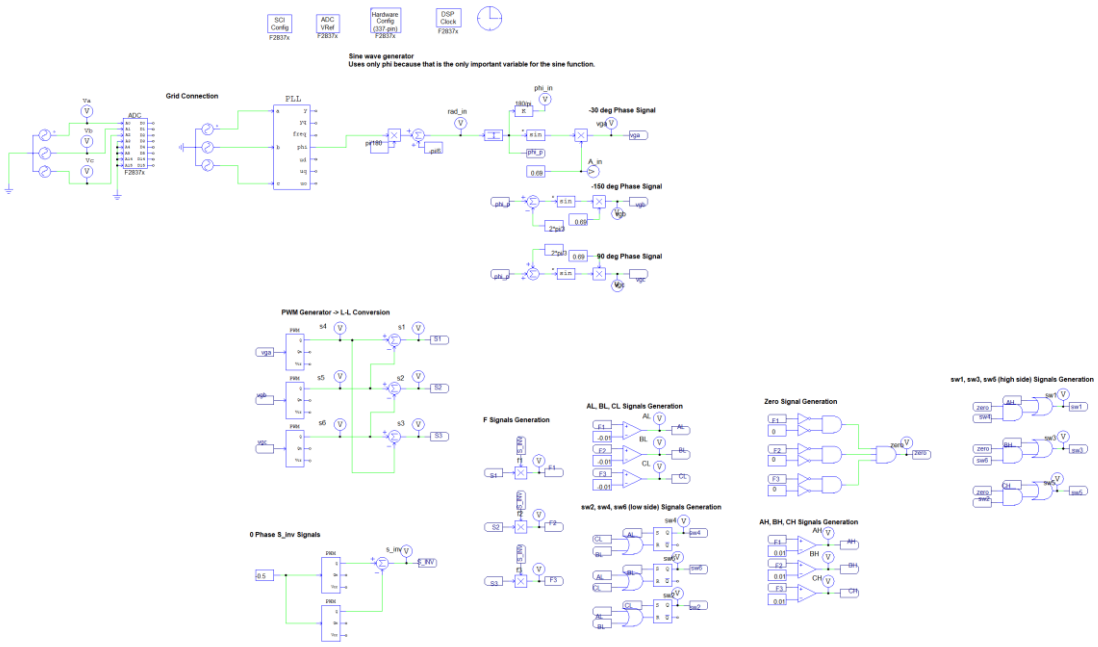

Figure 22: Controls scheme.

The input 3-phase AC signal determines the switching for the matrix converter. The PLL takes the input 3-phase AC signal to determine the phase angle. It then produces three 120-degree phase-shifted sine waves matching the original input but at a lower amplitude. The sine waves are fed into carrier PWM generators with a half duty cycle, then they are summed in a 3-phase line-to-line conversion. Lastly, a sequence of operators including comparators, logic gates, and an SR flip flop produces the switching signals (**Figure 22**).

3.3.2 Controls Scheme Testing

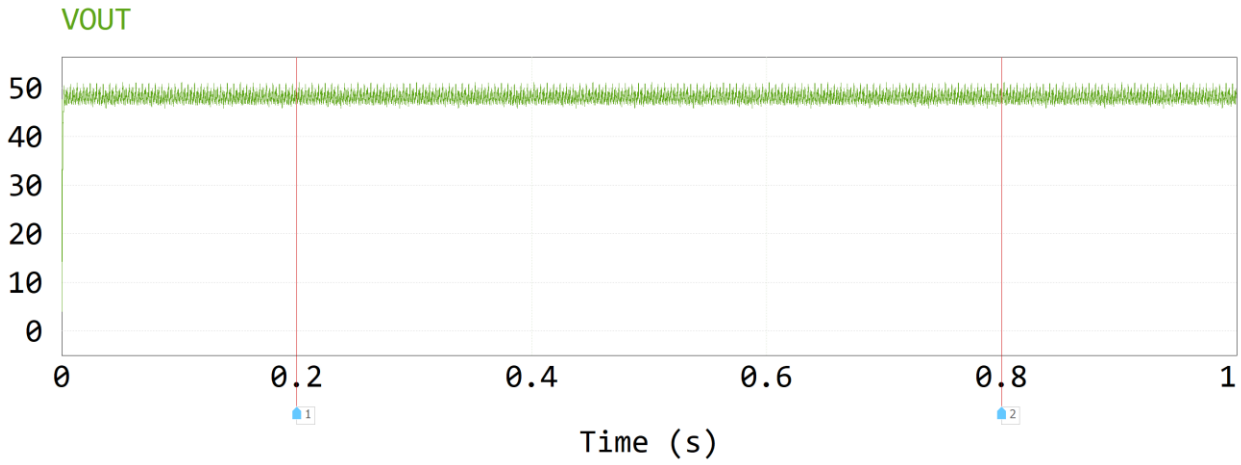

Figure 23: Output voltage of the testing control system and circuit in PSIM.

The goal of this subsystem is to switch the matrix converter so the circuit outputs a constant 48 V voltage with less than 2.5 V of standard deviation. Using PSIM, the controls scheme was tested for one second at 0.5 microsecond intervals, resulting in two million data points. The result was an average of 48.24 V with a 1.007 V standard deviation, which is sufficient for any DC power source to handle (**Figure 23**). From testing, a startup time of 1.697 milliseconds is needed for the control system to begin outputting 48 V.

3.3.3 Controls Scheme Hardware Implementation

The controls scheme is implemented in hardware using the TI F28379D Launchpad XL. To program the card in TI Code Composer Studio, we use similar logic to what was given in section 3.3.1 but with the programming language C.

Hardware-in-the-loop testing for the controls system uses physical hardware and a real-time simulation of the dedicated testing circuit. This testing is to be performed on the Typhoon HIL 602+ using Typhoon HIL Control Center software before the controls scheme is implemented with other subsystems.

4. CONCLUSION

4.1 3x1 Matrix Converter

The converter presented is capable of turning a three-phase AC input at 230 V into a high frequency sinusoidal voltage according to the modulation techniques provided (ignoring the effects of heat buildup), and the HV components are rated for 20.8 A. The board dimensions measure 9.39” long and 3.88” wide, with a total thickness of 32.9 mil. Trace widths range from 10 to 50 mil but are as wide as is appropriate (the only 10 mil traces are for the gate drivers).

As for desired changes, the inductor pads connect to their respective copper pour using via arrays, and this may also be necessary at the source terminal of each GaN FET. Furthermore, these FETs are rated for 30 A when it would be more cost-effective to find a similar component at a lower rating, say 10 A. Having a gate driver with larger pads would allow for easier soldering, and since they are one of the more expensive PCB components, the increased footprint is worth reducing the chances of making a mistake. Some traces, such as those for the Kelvin source, are slightly misaligned due to the presence of a “Keep-Out” layer on several component footprints and should be redone. The copper pours may need slight adjustments; for example, the space between different pours could be increased/decreased depending on design rules and preferred board size.

4.2 High Frequency Transformer

The step-down functionality of the transformer is behaving as expected, but a DC offset to the input current is present. Transformer efficiency struggles due to this offset. The source of this inefficiency is a subject of future investigation.

A parameterized transformer model was developed to rapidly simulate different transformer designs. Simulations on possible alternative transformer designs than what was implemented were conducted to identify potential room for improvement. The streamlined simulation process, interfacing a parameterized model with the Texas A&M HPRC Center, allowed for the mass launch of 252 simulations, with 222 completing. The remaining 30 failed due to Finite Element Analysis issues resulting from more complex and computationally intensive models.

4.3 Controls Scheme

The controls system can successfully take the 3-phase AC signal and create a switching algorithm that successfully converts a 3-phase AC signal to a single-phase AC signal. The controls system is created so the output voltage is 48.24 V with a 1.007 V standard deviation, as simulated in PSIM.

The controls system is implemented onto the TI F28379D Launchpad XL board using TI Code Composer Studio to create the controls scheme in C. It is then evaluated using HIL testing with the Typhoon HIL 602+ board.

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