Dwight Look College of
ENGINEERING
TEXAS A&M UNIVERSITY

Project name: WBG Devices-Based Matrix Converter

Team members: Jack Alagood, Kyle Bedrich, Ian Farrar

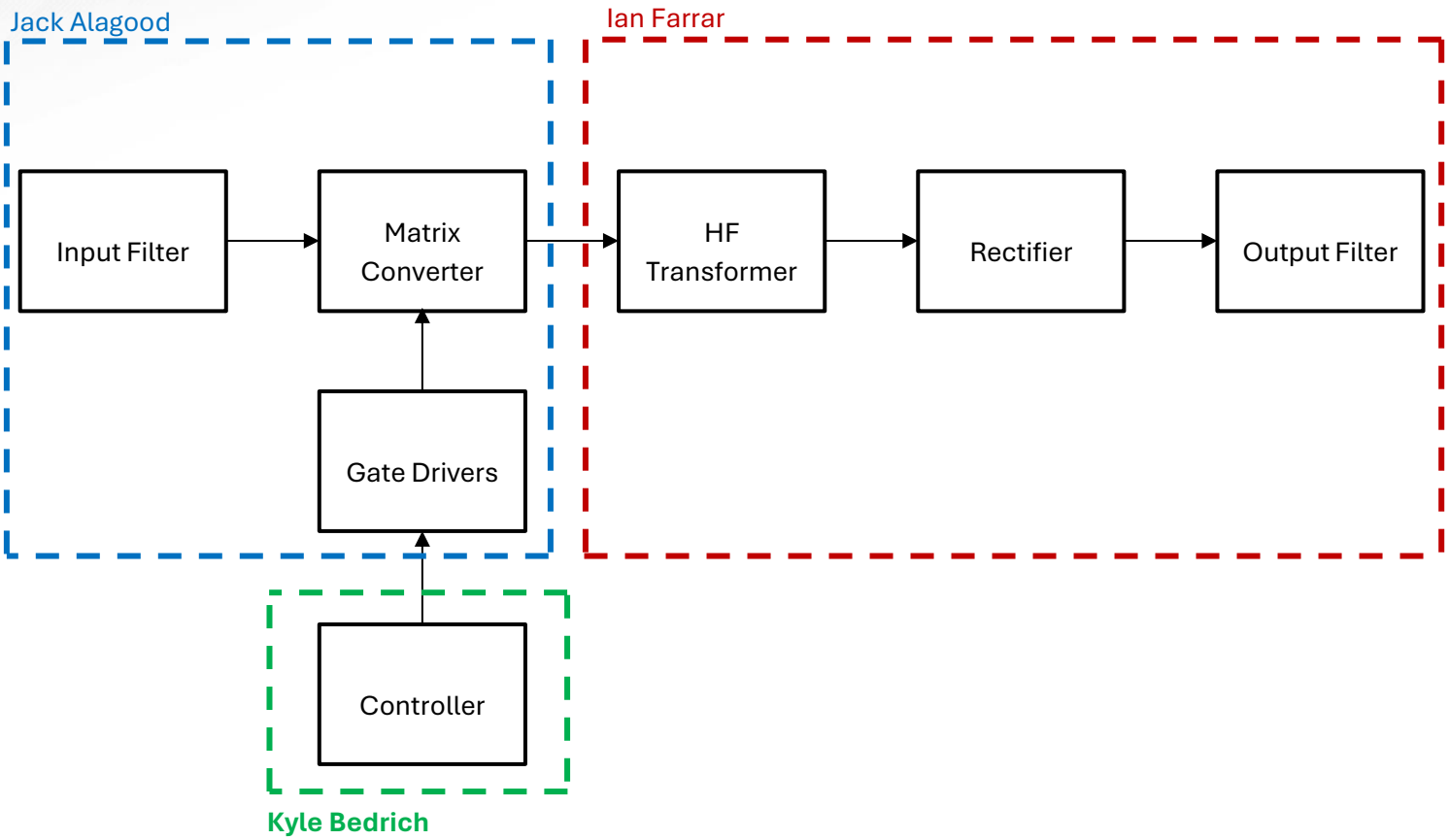
Problem Statement

- The rise of energy-intensive computing (AI model training, cloud computing, data centers, etc.) creates a need to optimize power delivery to these loads
- Though many solutions have been presented, there remains room for improvement in efficiency and cost

Proposed Solution

- GaN technology promises greater power density than SiC
- Matrix converters offer bi-directional power flow, adjustable input power factor, and greater power density due to less storage elements

System Diagram

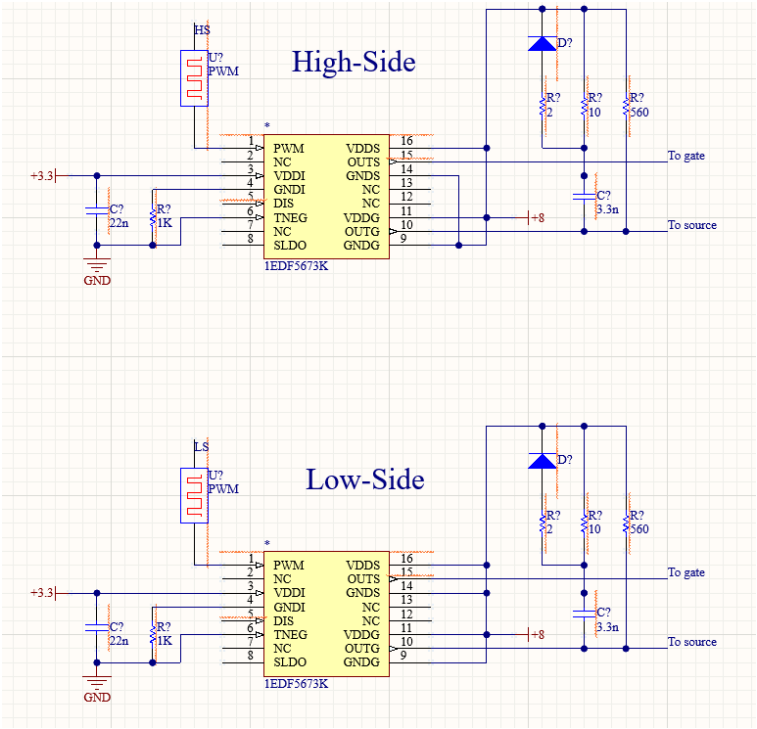


Task Partition

- Jack: “Design voltage sensor and gate driver”
- Kyle: “Design, validate, and test control system”
- Ian: “Design transformer and secondary side rectifier”

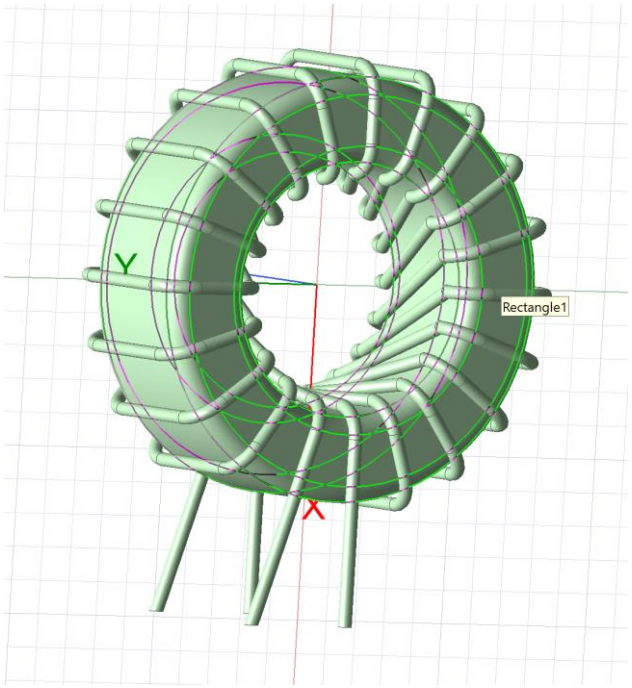
Primary Side Components

- Develop supporting hardware for matrix converter (input filter, voltage sensor, gate driver, etc.)
- Fine tune circuit components to control power factor, dead time, and parasitic inductance



Secondary Side Components

- Transformer steps voltage down from primary to secondary side
- Active rectifier converts AC input to DC output
- Created a transformer model in Ansys to understand Ansys development tools
- Researched high frequency transformer design process
- Researched viability of off the shelf components



Controls

- Gained understanding of 3-1 matrix converter control system
- Ported PLECS control system to PSIM, currently in validation
- Ready for TI C2000 code generation

Execution Plan

	8/19/2024	8/26/2024	9/2/2024	9/9/2024	9/16/2024	9/23/2024	9/30/2024	10/7/2024
URS Program Application								
Analyze Prior Studies								
Acquire Software Licenses								
Concept of Operations Report								
Research								
Functional System Requirements								
Interface Control Document								
Validation Plan								
Design and Simulation								
Midterm Presentation								
Prototyping								
Finish Prototyping								
Testing								
	10/14/2024	**10/21/2024**	**10/28/2024**	**11/4/2024**	**11/11/2024**	**11/18/2024**	**11/25/2024**	**12/2/2024**
Status Update Presentation								
Final Presentation								
Final Demo								

Validation Plan

Task	Deadline	Status	
URS Program Application	9/3/2024		Complete
Analyze Prior Studies	9/5/2024		Complete
Acquire Software Licenses	9/5/2024		Complete
Concept of Operations Report	9/15/2024		Complete
Research	9/19/2024		Complete
Functional System Requirements	9/26/2024		Complete
Interface Control Document	9/26/2024		Complete
Validation Plan	9/26/2024		Complete
Design and Simulation	10/3/2024		In Progress
Midterm Presentation	10/4/2024		Complete
Prototyping	-		
Finish Prototyping	-		
Testing	-		
Status Update Presentation	10/23/2024		
Final Presentation	11/20/2024		
Final Demo	11/26/2024		

Legend	
	Complete
	In Progress
	Overdue
	Not Started