PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	PCI Express Capability Structure Expansion
DATE:	21 March 2005, updated 3 November 2005
AFFECTED DOCUMENT:	PCI Express Base Specification Revision 1.1
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Part I

1 Summary of the Functional Changes

Extends the Device, Link and Slot register groups in the PCI Express Capability Structure by adding additional registers to the end of the capability structure. Changes the capability version to reflect the modified structure.

2 Benefits as a Result of the Changes

Additional register space is required for planned new capabilities.

3 Assessment of the Impact

Implementations implementing any future ECNs that use the added registers would be required to implement this new PCIe Capability Structure. If any part of the future ECNs using this register space is required (rather than optional) then this extended structure would, by extension, become required.

4 Analysis of the Hardware Implications

Additional register space required for new capabilities.

5 Analysis of the Software Implications

No impact to existing software. Provides register expansion space for future capabilities.

Part II

Detailed Description of the change

In Section 7.8, modify as shown:

PCI Express defines a capability structure in PCI 3.0 compatible configuration space (first 256 bytes) as shown in Figure 7-3 for identification of a PCI Express device and indicates support for new PCI Express features. The PCI Express Capability structure is required for PCI Express devices. The capability structure is a mechanism for enabling PCI software transparent features requiring support on legacy operating systems. In addition to identifying a PCI Express device, the PCI Express Capability structure is used to provide access to PCI Express specific Control/Status registers and related Power Management enhancements.

Figure 7-9 details allocation of register fields in the PCI Express Capability structure.

The PCI Express Capabilities, Device Capabilities, ~~and Device~~ Status and ~~/~~Control registers are required for all PCI Express devices. Device Capabilities 2, Status 2 and Control 2 registers are required for all PCI Express devices that implement capabilities requiring those registers. For devices that do not implement the Device Capabilities 2, Status 2, and Control 2 registers, these spaces must be hardwired to 0.

The Link Capabilities, ~~and Link~~ Status~~/~~ and Control registers are required for all Root Ports, Switch Ports, Bridges, and Endpoints that are not Root Complex Integrated Endpoints. For devices that do not implement the Link Capabilities, Status and Control registers, these spaces must be hardwired to 0. Link Capabilities 2, Status 2 and Control 2 registers are required for all Root Ports, Switch Ports, Bridges, and Endpoints (except for Root Complex Integrated Endpoints) that implement capabilities requiring those registers. For devices that do not implement the Link Capabilities 2, Status 2 and Control 2 registers, these spaces must be hardwired to 0.~~Endpoints are not required to implement registers other than those listed above and terminate the capability structure.~~

Slot Capabilities, Status and Control registers are required for Switch Downstream and Root Ports if a slot is implemented on the Port (indicated by the Slot Implemented bit in the PCI Express Capabilities Register). For devices that do not implement the Slot Capabilities, Status and Control registers, these spaces must be hardwired to 0. Slot Capabilities 2, Status 2 and Control 2 registers are required for Switch Downstream and Root Ports if a slot is implemented on the Port and the device implements capabilities requiring those registers. For devices that do not implement the Slot Capabilities 2, Status 2, and Control 2 registers, these spaces must be hardwired to 0.

Root Ports and Root Complex Event Collectors must implement the Root Capabilities, Status and ~~/Status~~Control registers. ~~in addition to PCI Express Capabilities, Device Capabilities and Device Status/Control registers~~ For devices that do not implement the Root Capabilities, Status and Control registers, these spaces must be hardwired to 0.

~~Root Control/Status registers are required for Root Ports. Root Ports must implement the entire PCI Express Capability structure..Slot Capabilities and Slot Status/Control registers are required for Switch Downstream and Root Ports if a slot is implemented on the Port~~

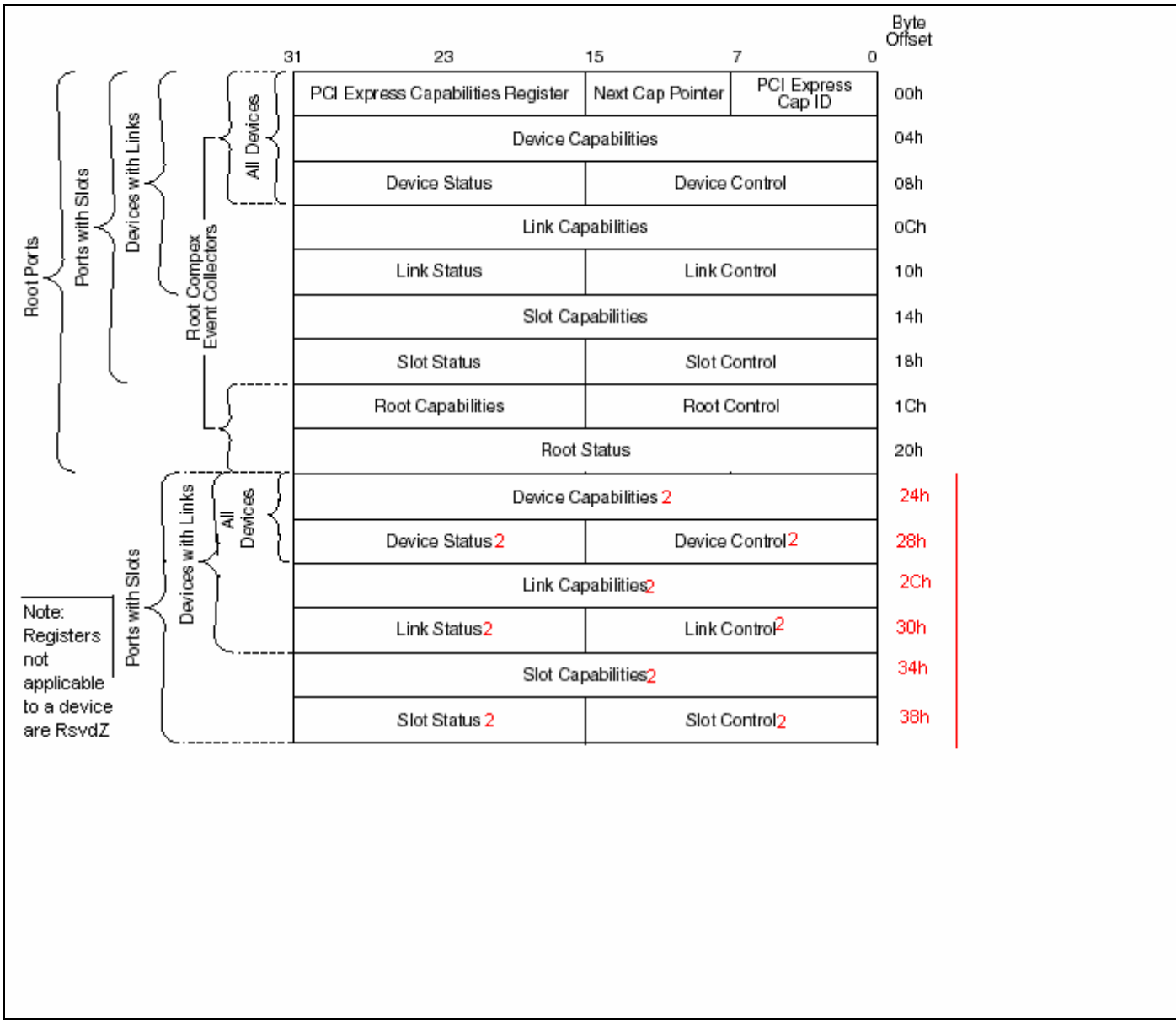

Figure 7-9: PCI Express Capability Structure

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In Section 7.8.2, PCI Express Capabilities Register (Offset 02h):

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Table 7-10: PCI Express Capabilities Register

Bit Location	Register Description	Attributes

Bit Location	Register Description	Attributes
3:0	**Capability Version** – Indicates PCI-SIG defined PCI Express capability structure version number. A version of the specification that changes the PCI Express capability structure in a way that is not otherwise identifiable (e.g., through a new capability field) is permitted to increment this field. All such changes to the PCI Express capability structure must be software-compatible. Software must check for Capability Version numbers that are greater than or equal to the highest number defined when the software is written, as devices reporting any such Capability Version numbers will contain a PCI Express capability structure that is compatible with that piece of software. Must be ~~1h~~ 2h for devices compli~~a~~int to ~~this specification~~the Express Capabilities Register Expansion ECN.	RO
...		

Add new sections as shown:

7.8.15 Device Capabilities 2 Register (Offset 24h)

This section is a placeholder – There are no capabilities that require this register.

7.8.16 Device Control 2 Register (Offset 28h)

This section is a placeholder – There are no capabilities that require this register.

7.8.17 Device Status 2 Register (Offset 2Ah)

This section is a placeholder – There are no capabilities that require this register.

7.8.18 Link Capabilities 2 Register (Offset 2Ch)

This section is a placeholder – There are no capabilities that require this register.

7.8.19 Link Control 2 Register (Offset 30h)

This section is a placeholder – There are no capabilities that require this register.

7.8.20 Link Status 2 Register (Offset 32h)

This section is a placeholder – There are no capabilities that require this register.

7.8.21 Slot Capabilities 2 Register (Offset 34h)

This section is a placeholder – There are no capabilities that require this register.

7.8.21 Slot Control 2 Register (Offset 38h)

This section is a placeholder – There are no capabilities that require this register.

7.8.22 Slot Status 2 Register (Offset 3Ah)

This section is a placeholder – There are no capabilities that require this register.