## Conclusion

The basic elements of several possible computers for use in linear, time-invariant, real-time control systems have been described. These computers offer significant savings in the number of vacuum tubes required and allow the computer pulse-repetition frequency to be lowered appreciably. These results point to the fact that, rather than adapting the general-purpose computer to specialized tasks, the engineer should design the computer for the specific job it is to perform.

## Acknowledgment

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# The MIT Magnetic-Core Memory*

WILLIAM N. PAPIAN†

## Introduction

ONE RECENT DEVELOPMENT which is significantly raising the reliability of today's high-speed automatic digital computer is the multico-ordinate magnetic-core memory. Two banks of 32 by 32 by 17 magnetic-core memory have been in full-time operation in the Whirlwind I Computer for some months. A description of the units and of the tests and operational data available on them will be preceded by a short review of operating principles of this type of memory.

## Operating Principles[1]

Each binary digit is stored in the magnetic field of a small, ring-shaped, ferromagnetic core. Two aspects of the core's rectangular flux-current characteristic are utilized:

a. The flux remanence of the core is utilized for the storage operation;[2]
b. The extreme nonlinearity of the flux-current characteristic is utilized to advantage in the selection operation.[3,4]

Fig. 1 shows the flux-current loop for a ferrite core. The remanent flux points are arbitrarily designated as ZERO and ONE. Note that the loop is sufficiently nonlinear so that the application of $I_m/2$ cannot switch the core, whereas the full $I_m$ can. Fig. 2 illustrates how this nonlinearity may be used to select one core out of many by the coincidence of two half-currents in a 2-co-ordinate scheme. The extension to three co-ordinates may be accomplished by stacking planes like those of Fig. 2 behind each other and connecting respective $x$ and $y$ co-ordinate lines in common to obtain a "volume" of cores as sketched in Fig. 3, following page.

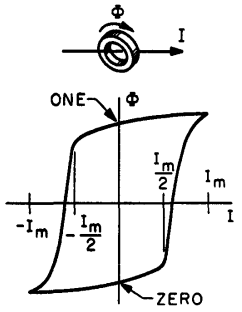


Fig. 1—Flux-current characteristic of ferrite toroid.

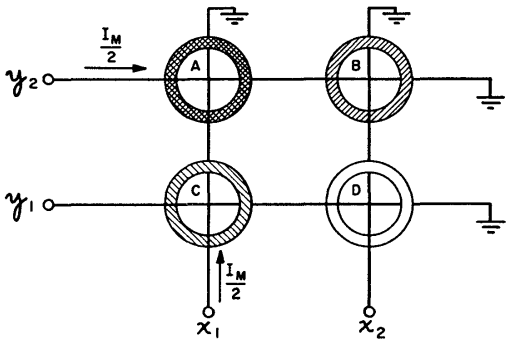


Fig. 2—Two-co ordinate array.

The application of a half current to the co-ordinate $x_l$ results in the half excitation of a "selection plane" through the volume. The same is true for the co-ordinate $y_m$, and the result is full-current excitation of the line of cores at the intersection of these two selection planes. The internal memory for a parallel type of machine might well resemble Fig. 3, and the selected line of cores might well represent the selected memory register, or word. A readout or sensing winding threaded through

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† Staff Member, Lincoln Laboratory, Massachusetts Institute of Technology, Cambridge, Mass.

[1] W. N. Papian, "A coincident-current magnetic memory cell for the storage of digital information," Proc. I.R.E., vol. 40, pp. 475–478; April, 1952. (Also "A Coincident-Current Magnetic Memory Unit," Master's thesis, E.E. Dept., Massachusetts Institute of Technology; August, 1950.)

[2] Harvard University Computation Laboratory, "Investigations for design of digital calculating machinery," *Progress Reports*, 2–6 (particularly No. 2); August, 1948–November, 1949.

[3] J. W. Forrester, "Digital information storage in three dimensions using magnetic cores," *Jour. Appl. Phys.*, vol. 22, pp. 44–48; January, 1951.

[4] Jan Rajchman, "Static magnetic matrix memory and switching circuits," *RCA Rev.*, vol. XIII, pp. 183–201; June, 1952.

every core in each $xy$ plane, or digit plane, would bring out the signal representing the stored digit. This part of the read operation is destructive, and the word must be rewritten.

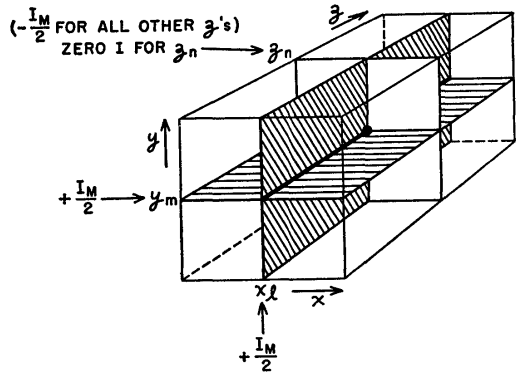


Fig. 3—Three-co-ordinate selection.

For the rewrite part of the cycle the selection technique remains the same, except that the half currents on the selection planes are now in the write polarity, which would result in the writing of ONE's into all the cores of the selected register; this writing is controllable for each $xy$, or digit, plane by the use of a digit-plane winding on which may be applied a half-current of an effective polarity opposite to the write currents. The presence of this "inhibit" current in any digit during the write operation leaves a ZERO; absence of the inhibit current leaves a ONE.

R. R. Everett of Massachusetts Institute of Technology has shown that these techniques may be extended into any number of co-ordinates but that the 2-co-ordinate read and 3-co-ordinate write system just described is one of the most desirable for the Whirlwind type of machine.

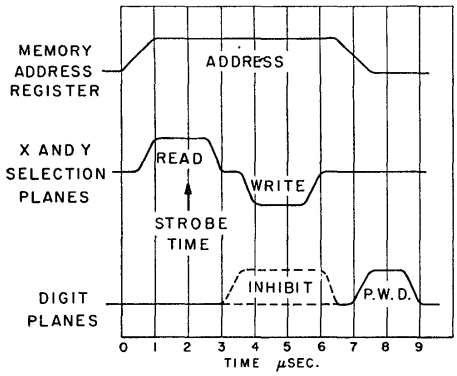


Fig. 4—Memory cycle.

## Description of Memory

The capacity of each memory bank is 1024 registers, with 16 digits (plus 1 parity digit) per register. The basic operating mode, or cycle, consists of setting the memory-address register to the new address and applying the read-current pulses, followed by the write currents for rewriting the information just removed. The information is stored in a memory-buffer register. The speed of the machine may be judged from the timing diagram (Fig. 4). Note that the read-rewrite time, or cycle time, is approximately 9 μsecs and that there are no restraints on how frequently this cycle may be applied to the memory. It is capable, therefore, of a basic repetition rate of over 100 kc. Note also that the information can be available to the machine approximately 2 μsecs from the beginning of the cycle.

### *Block Schematic*

Fig. 5 shows a block schematic of one bank of memory. Each half of the binary address in the Address Register is translated to a 1-out-of-32 selection by a crystal-diode Matrix and sets up a pair of "AND" gates for $x$ and a pair for $y$. The Read Flip-Flop forms a 1.5-μsec pulse and sends it to the two selected Read Drivers which supply the 0.45-ampere currents to two selection planes. The output signal voltages from each digit plane are amplified in the Sense Amplifiers and applied to "AND" gates which are strobed at the optimum time by a short (0.1 μsec) pulse. Pulses representing ONE's then go off to set the Buffer Register to the just-extracted number. At the end of the read currents the rewrite part of the cycle starts in the same manner, except that the write currents have to be safely overlapped by the inhibit currents at those digit planes where ZERO's are to be written. This is accomplished by having the "on" time of the Inhibit Flip-Flop overlap slightly that of the Write Flip-Flop. Short (1 μsec) currents may be applied to all digit planes after the rewrite; they are called Post-Write Disturb (PWD) currents and are used to improve the ONE-to-ZERO signal ratios under certain conditions. The PWD Flip-Flop forms this pulse and applies it to all 17 of the Digit-Plane Drivers through "OR" inputs.

### *The Cores*

The cores are made of General Ceramics material MF-1326B. The first bank contains their core size F-291 which has an outside diameter of 90 mils. A smaller core was used in the second bank; this is F-394, 80 mils in outside diameter. Single-turn switching currents are approximately 950 and 850 ma respectively, and single-turn output voltages (at optimum strobe time) are about 0.1 volt. Switching time, under these conditions, is approximately 1.2 μsecs.

One of the largest problems in the building of a memory of this type is the procurement of large numbers of uniform cores. Core selection was made on the basis of a series of pulse tests, approximately four per core, and resulted in a yield for the first bank of approximately 30 per cent of those shipped to us by the producer. (Yields have been improving materially since this first run.) The selection criterion was fundamentally that of an upper and lower limit on the voltage output from each core when the core was excited by a sequence of current pulses devised to resemble computer operation.

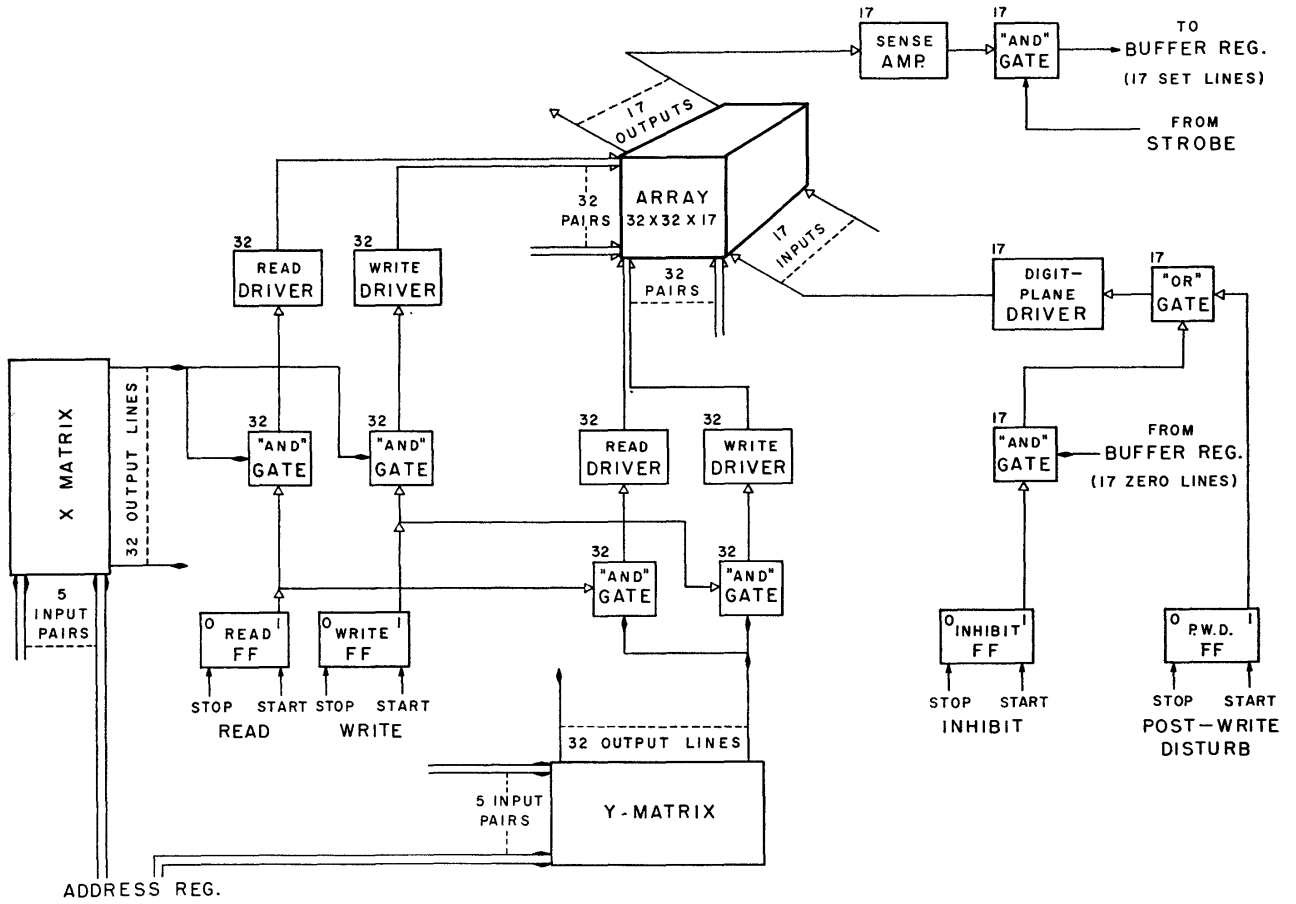


Fig. 5—Memory block schematic.

Fig. 6 shows typical output-voltage pulse shapes, the nominal limits within which cores were considered acceptable, and the strobe time at which these amplitudes were taken. The horizontal limit lines are at 90 and 120 mv, total pulse length is about 1.2 $\mu$secs, and the vertical line showing the strobe time is about 0.5 $\mu$sec from the start of the pulse.

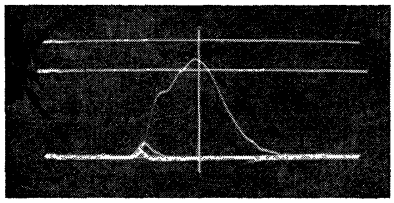

Fig. 6—Test-core outputs.

*Basic-Circuit Types*

The read and write currents for the selection planes of the memory are supplied directly from vacuum-tube plates. A single type-6080 vacuum tube, with its sections paralleled, is used to drive a given selection plane in the read direction. Another such tube drives the same plane in the write direction. The control grids of the 6080's are driven through 6BL7 amplifiers from the crystal-matrix output lines. The cathodes of all of the 6080 tubes in the $x$-read group are connected together, then through a large resistor to a negative-voltage supply. The cathodes of the three other groups of 6080's ($x$-write, $y$-read, $y$-write) are all connected in a similar manner. Each group of cathodes is normally held at a relatively high potential by a power amplifier and is allowed to drop at the proper time. Thus, each 6080 acts not only as a cathode follower but as the logical "AND" gate shown separately in the block schematic. The large amount of degeneration caused by the high common-cathode resistor compensates for nonuniformity and aging changes in the characteristics of the tubes. As a result, selection-plane currents remain within very close limits (plus or minus 4 or 5 per cent).

The digit-plane driver consists of a 6080 dual triode driven from two amplifier stages and incorporating sufficient negative feedback from the output to the input to keep the current amplitude within plus or minus 5 per cent over expected tube, component, and power-supply variations.

The output signal from the sensing, or read-out, winding is linearly amplified from the 100-mv level up to approximately a 30-volt level in a single-sided, ac coupled, wide-band feedback amplifier. The signal is then rectified and applied to the suppressor grid of a 7AK7 gate

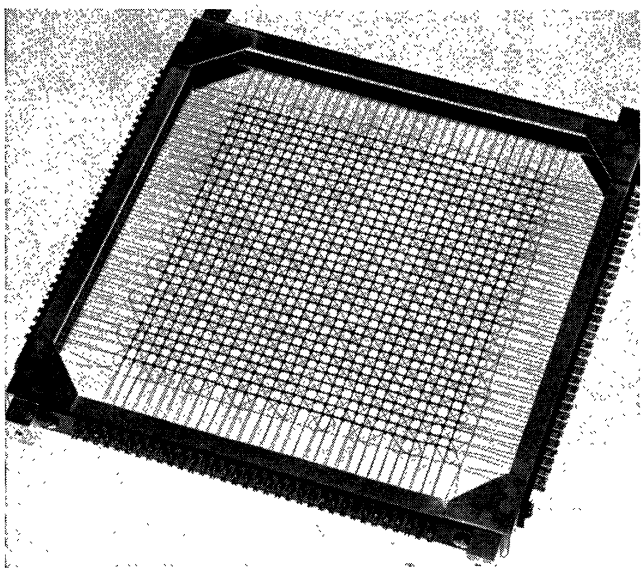

Fig. 7—32-by-32 plane.

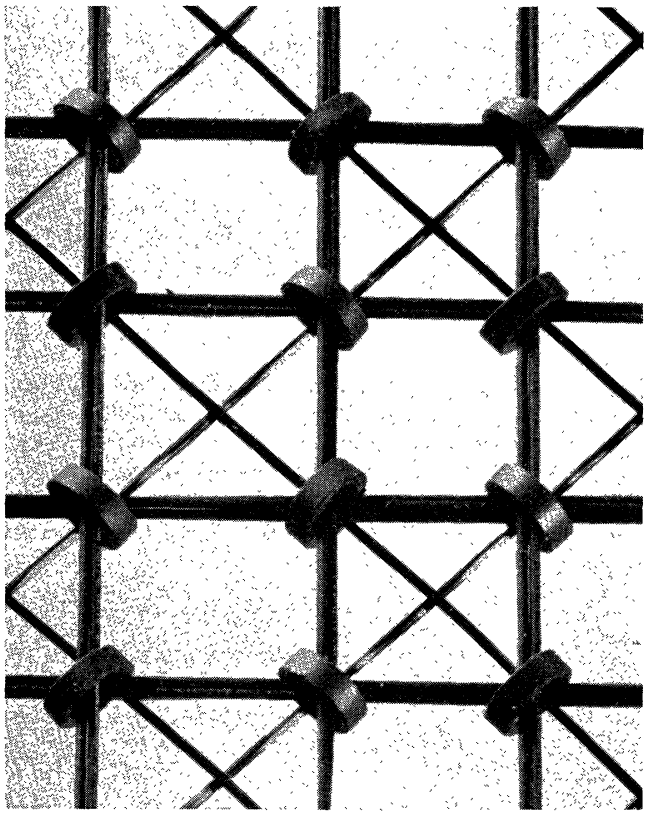

Fig. 8—Closeup of 32-by-32 plane.

tube on a bias level of about 30 volts. The control grid of the gate tube is pulsed with a 0.1-$\mu$sec pulse at the optimum moment so a "standard" Whirlwind pulse issues from the gate to indicate when a ONE is being read.

*Layout and Packaging*

A finished memory plane is shown in Fig. 7. The frame's outside dimensions are approximately 9.5 by 9.5 inches. All the windings consist of 32-gauge magnet wire with quadruple-Formex insulation. Fig. 8 shows the cores and wires in some detail. The $x$ and $y$ pairs run vertically and horizontally, the sense winding runs along the diagonals, and the digit-plane winding runs horizontally (but is obscured in the shadow around the $y$ pairs). Wiring time for one plane was about one man-week, including an intermediate test and final inspection. The intermediate test was performed when all the cores and $x$ and $y$ wires were in place but before the digit-plane and sense windings were installed; core replacement is relatively easy at this point. The test consisted of applying a sequence of current pulses to a given $x$ line and observing the response of each of the 32 cores on that line by manually stepping the observing-scope probe from one $y$ line to the next. This test was repeated for subsequent $x$ lines, until the 1024 cores were completed. Cores which displayed abnormally high or low outputs were marked for replacement. About 1 core per plane was replaced.

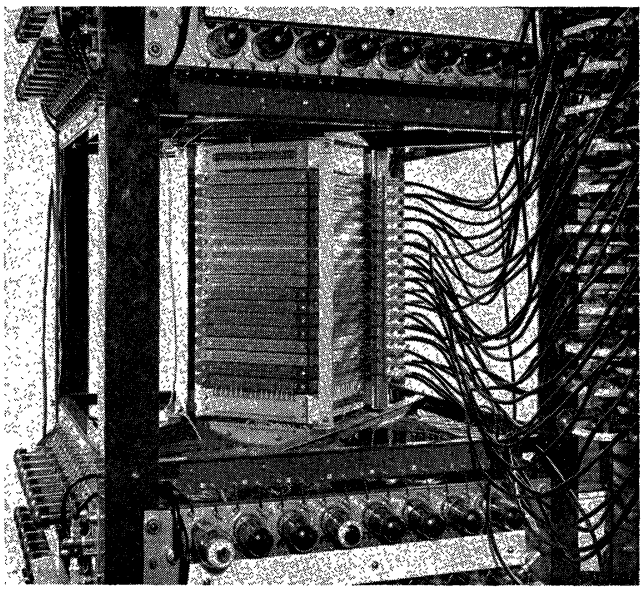

Fig. 9—Memory stack mounted in stall.

The 17 finished planes were mounted in a stack or array, as shown in Fig. 9. Plane-to-plane connections are made by means of the vertical busses soldered into the slotted lugs. Digit-plane and sense-winding connections were made from the same corner of each plane to a mounting board of connectors for coaxial connection to another rack. Selection-plane-driving connections fan out horizontally at the top and bottom of the array. It takes 3 to 4 hours to replace either the entire array or any single plane.

Fig. 9 includes a view of part of the four-posted stall, or rack, in which the array is mounted. Fig. 10 shows a front view of the Memory Test Computer; at the left of the picture may be seen the memory stall. The Whirlwind I core memory is shown in Fig. 11. Selection-plane-driver panels are mounted on the four faces of each stall with tubes pointing outward. Visible in each stall above

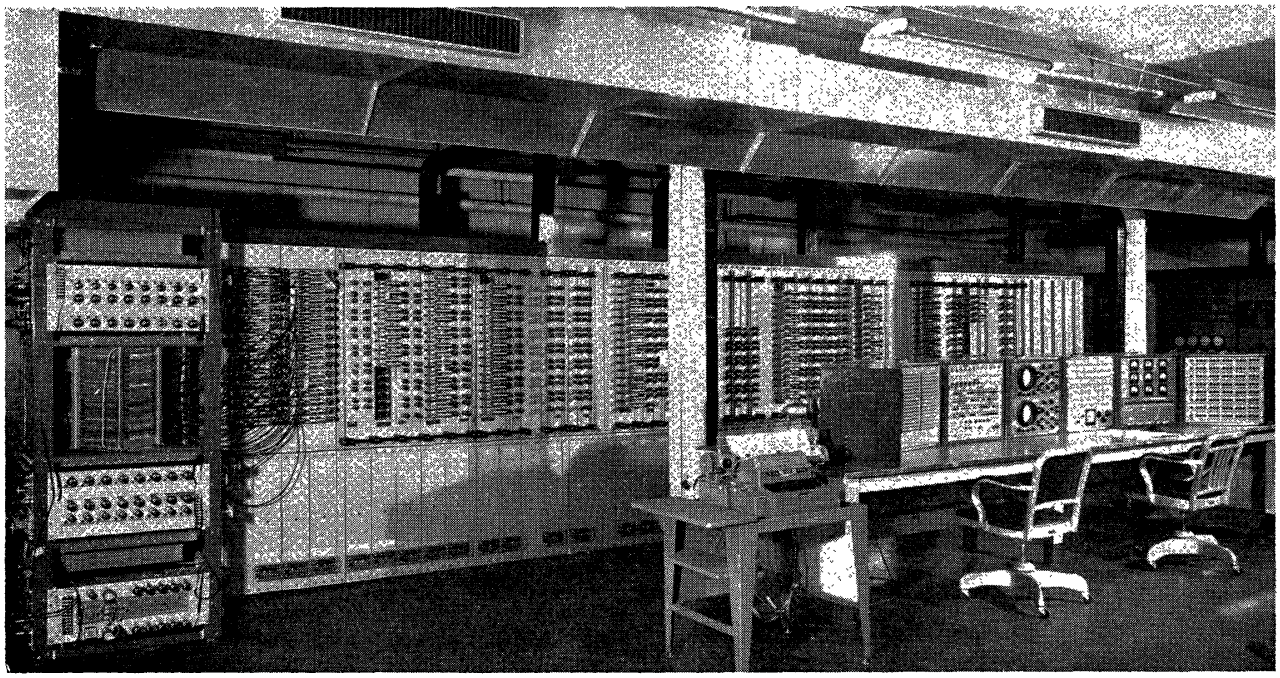

Fig. 10—Memory installation in MTC.

and below the selection-plane-driver panels are the two crystal-matrix switches. The general arrangement is such that temperature-sensitive components, such as cores and crystal diodes, are inside the stall, and large heat-dissipating components, such as tubes, are on the outside.

The sense amplifiers and digit-plane drivers are in plug-in chassis stacked in vertical racks next to the memory stalls.

## Tests and Performance

Ultimate judgment on the reliability of this particular core memory must rest on its performance over the next year or two. Tentative evaluation may be made, however, from observations of performance during the 4 months that one bank operated in the Memory Test Computer and the 3 months of 2-bank operation in Whirlwind. In addition, much may be determined from the results of tests made on the memory to ascertain its tolerance to variations in the parameters significant to its operation.

### *Parameter Variations*

Many conditions, or parameters, affect the operation of a core memory; driving currents ($x$, $y$, read, write, inhibit, and disturb), sense-amplifier gains, strobe time, ambient temperature, memory-information pattern, and repetition rate are good examples. These parameters are not all equally significant or equally easy to manipulate, and so some of them have, as yet, been examined in only a cursory manner. Because sense-amplifier gains have a simple, nearly linear, effect on operation they were adjusted and held at one setting during the tests. Ambient temperature is expected to be held within close

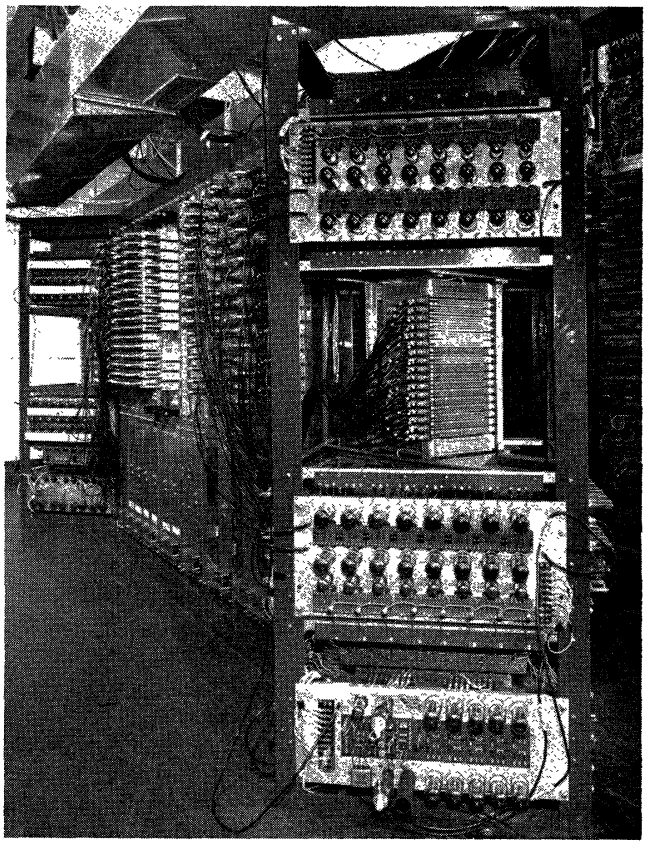

Fig. 11—Core memory in WWI.

tolerances in any operating machine, and a fair amount of information is available on the subject from the core-testing work; temperature was not controlled during the tests but recorded readings were kept. Memory-informa-

tion pattern and repetition rate were controllable to some degree by the program being run; a program which seemed to give the most adverse pattern and rate was designed and used during most of the testing.

The tests were made on the Memory Test Computer, a high-speed, 16-digit, parallel machine of the Whirlwind type. The machine has a parity-checking system which computes whether each 16-digit word to be stored contains an odd or an even number of ONE's, stores the result of this "parity count" in the 17th digit, recomputes the count when the word is read out, and rings an alarm if the result does not check with the contents of the 17th digit. Although major reliance was placed on parity checking for detecting memory malfunction, there was also some programmed identity checking used.

The bias bounds of the sense gates' suppressor grids were chosen as a very convenient measure of the quality of the memory output. The upper bound (least bias) is the point at which errors occur because the gate is mistaking the largest ZERO output for a ONE, at the lower bound (most bias) errors occur because the gate mistakes the smallest ONE output for a ZERO. The bias difference, in volts, is a direct measure of the voltage difference at strobe time between the smallest ONE and the largest ZERO.

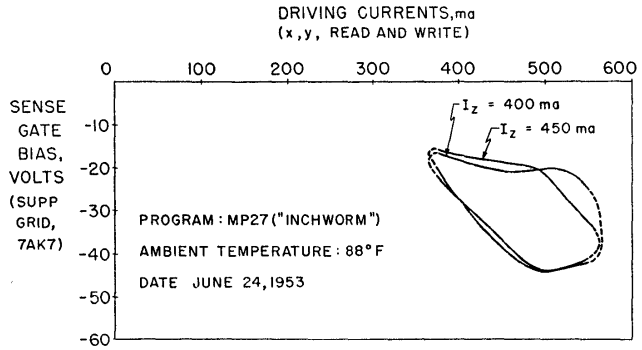


Fig. 12—Bias bounds versus drive currents.

Fig. 12 shows the bias bounds for all 17 sense gates as a function of the selection-plane driving-current amplitudes ($x$, $y$, read, and write). The program used was the so-called "inchworm" in which 16 words of instructions "bootstrap" themselves around the 1024 registers of the memory. The ambient temperature was recorded at approximately 88 degrees Fahrenheit, about 15 degrees higher than what is now believed to be optimum. Two curves are shown, one for digit-plane currents set at 400 ma and the other at 450 ma. The enclosed areas indicate how much the safe operating point of the memory bank may wander; recent circuit and adjustment improvements have enlarged these enclosed areas somewhat. Fig. 13 shows the bias bounds as a function of the timing of the strobe pulse. Time is measured from the instant the Read Flip-Flop is pulsed by the Start Read pulse. The three curves are for three values of selection-plane driving current, two extremes and one near optimum. A wide operating region is again indicated.

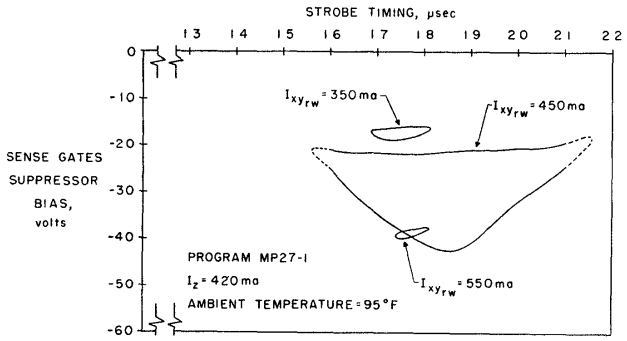


Fig. 13—Bias bounds versus strobe time.

*Computer Operation*

The first bank of memory has been in use in Whirlwind since mid-August, the second since September 5. There has been a steady improvement in their operation as the installation, which was an extremely hurried one, has been gradually cleaned up and made permanent and, also, as the process of debugging these relatively new equipments proceeded. The two banks have not quite been brought to an equal degree of reliability; this may be due, in part, to the fact that the cores in the first bank were not selected as carefully as those in the second so that output ONE/ZERO ratios are not as large. The demands on the Whirlwind computer are heavy, and only a few hours a month are available for further development work on its memory.

Parity alarms occurred, at first, about 3 or 4 times per week; at this writing (November 27) there has not been a parity alarm for four weeks. This comes to about 460 hours of useful operation or, assuming a 30-$\mu$sec average order time and 2 accesses per average order, it comes to slightly over 100 billion word accesses with each access parity checked and no error detected.

The exact nature of the errors which do occur is, as yet, not known. It is hoped that further work on the system will shed more light on the problem as well as reduce the error rate yet further.

## Conclusion

The test results and experience obtained thus far on the two 32 by 32 by 17 banks of magnetic-core memory now operating as the internal memory of the Whirlwind machine indicate high promise for this type of storage. Reasonable engineering extrapolations of the results are being used in present work on a 64 by 64 by 17 bank which is expected to be in operation in the Memory Test Computer by January 1954.