MAGNETIC CORE STORAGE

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TELEMETER MAGNETICS, INC.

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by

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INTRODUCTION

This book was written to provide a reference work for engineers concerned with the design and application of magnetic-core storage units. It summarizes the state of the storage art in 1959 and the developments in core storage and switching techniques during the period from 1952 to the present. It is not intended as a comprehensive text on magnetic core storage.

Characteristics of various types of magnetic cores are described. A section is devoted to storage techniques and another to switching techniques. Problems encountered in designing systems as well as component circuits of storage units are discussed. A section is devoted to the special problems of designing storage devices for operation in adverse environments. Several typical magnetic-core storage units are described, as are methods of testing and maintaining storage units. In existing core memories, information is destroyed during some part of the operating cycle. The non-destructive techniques being developed and other trends in magnetic core storage are discussed in a final section.

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Raymond Stuart-Williams

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Figure 13. Typical closely packed core matrix.

MAGNETIC CORE STORAGE

Magnetic core storage units driven by transistors are used in most computers to mechanize the random-access storage function. Initially these units were tube-driven, physically large, and costly, and required special air conditioning to maintain a constant temperature around the cores. They had the supreme advantage of high reliability, compared to all other available forms of random-access storage. Designers and users suffered the expense and inconvenience of the early units in order to obtain the high reliability.

Core storage units of recent design are generally smaller and less expensive than the early units. Greater reliability has been achieved with the newer core memories. Typical tube-driven core storage units with a capacity of about 200,000 bits were sold in production quantities at one to two dollars per bit. A present-day unit of this capacity will cost less than 25 cents per bit. The volume of an early unit might be over 300 cu ft, not including the air conditioning require and motor-generator. Recently manufactured units do not need either of the latter devices, and they range in volume from less than 60 cu ft down to as little as 1 cu ft. Power consumption has dropped by at least a factor of ten.

Early units were held at a temperature controlled within $\pm 10^{\circ}$F. Most of the present units operate from 0°C to 40 or 50°C, and some operate from -20°C to 100°C. The reliability of a typical early core storage unit is such that a mean error-free time of up to 1,000 hours can be obtained with 4 per cent maintenance. With present-day units, mean error-free times in excess of 1,000 hours can be obtained with only ½ per cent maintenance.

These changes in magnetic core storage have taken place over a period of four years, and the art is still progressing rapidly. Core storage units with capacities of less than one million bits are now more reliable and, in most cases, more economical than any other form of electronic storage.

During this four-year period, the importance of different aspects of the core storage art has shifted. Originally magnetic switches were of great importance but are now of minor value in most random-access storage units. Recently a

demand has developed for small special-purpose storage units, frequently classified as buffers. A major problem encountered in designing buffers is the need to reduce the transistor count to a minimum in order to achieve high economy and reliability. Special types of magnetic switch have been used to solve this problem. The magnetic switch has in fact almost completely superseded the transistor as a logical timing or decoding element in small storage units. Moreover, techniques have been developed whereby utilization of magnetic switches to perform logical and timing operations has been extended beyond the storage unit into the computer itself. This is not true magnetic core logic but is rather the introduction of logical properties into memory units.

The evolutionary process illustrated by the use of magnetic switches in buffers is continuously taking place, and new applications for obsolete techniques are being found every day. Therefore, all aspects of core storage, whether or not they are considered important at present, will be discussed. The number of different core storage systems is too great to be fully covered in a short description. Many new storage devices are being investigated, and development of existing devices and systems is continuing. For these reasons, fundamental concepts and principles will be expounded to a greater extent than is usual in a handbook. Actual data presented will be restricted to widely used techniques and components.

STORAGE CORES

CHARACTERISTICS OF STORAGE MATERIALS

The ideal storage material whould have the characteristics shown in Figure 1. Its hysteresis loop would be absolutely rectangular and its saturation characteristics completely flat. A major hysteresis loop and a series of minor loops of a good, commercially available material are shown in Figure 2. These loops, particularly the minor ones, are not too far from the desired rectangular form.

Figure 1. Hysteresis loop of an ideal storage material.

Figure 2. Major and minor loops of a practical storage material.

The minor loops are almost invariably employed in coincident-current storage applications. If the core is in one state of saturation and H is altered to tend to move the core to the other state of saturation, at first there is very little change in flux. A value H_k is finally achieved beyond which the permeability is high, and this region continues to a value H_t.

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When H is reduced to ZERO, the remanent flux density is equal and opposite to the original flux density. If H_k/H_t is greater than 0.5, the core is a useful storage element since there will be almost a trigger action in moving from one flux storage state to another. There is a range of values of H over which adequate storage loops are obtained. In a good storage material this range is high, allowing the designer to tolerate relatively large changes in driving current in the storage system. If the core is driven by means of a rectangular pulse which generates the value of H_t corresponding to the center of this range, the core will take a time T_s to switch from one state of storage to the other. This time is known as the characteristic switching time, or turnover time, of the material.

SWITCHING TIMES OF STORAGE MATERIALS

In any given storage material the switching time is related to the value of the coercivity (H_c) of the loop under consideration by the equation

$$T_S \ (H_C - H_O) = K \qquad (1)$$

where H_O and K are constants depending on the material. This equation does not hold when H_c becomes very nearly equal to H_o. It has been found experimentally that for mid-range values of H_c and T_s most storage materials fall near a curve represented by

$$T_S \ (H_C - 0.3) = 1 \qquad (2)$$

where T_s is in microseconds and H_c is in oersteds. This equation can be used to roughly predict the performance of as yet unknown materials, provided that T_s is less than 5 to 10 microseconds.

Equation (2) seems to present an ultimate limit to the rapidity of storage operations using conventional materials and methods. Recent work on special ferrites and thin metallic films has shown that this empirical equation is incorrect and that it is possible to make materials which will operate at very high speeds without requiring extremely large drive currents.

In the case of thin metallic films, the film is made to operate more rapidly than is indicated by the theoretical equation by

employing an internal magnetic stress in the material to assist in obtaining rapid switching action. Under these circumstances switching is achieved in a dipole manner instead of in the normal domain-wall-movement manner which is usually associated with ferromagnetic phenomena. A price is paid for this increase in speed in that the flux change that occurs during switching is reduced relatively rapidly as the speed is increased. At very high speeds, virtually no flux change occurs and the thin metallic film does not really switch in the normal ferromagnetic sense. Instead a slight angular change in the vector of magnetization occurs, which is exhibited externally in a manner similar to a flux change.

Special ferrites which operate more rapidly than the ferrites used in coincident-current storage applications attain a high speed both by having special properties and by being used in a special mode of operation. A typical BH loop used in this mode is shown in Figure 3. The broken loop is a relatively minor loop of the material. The partial loop shown in full, which is employed for storage applications, does not exhibit normal rectangular loop properties. Storage points are indicated by the numbers ZERO and ONE. To the left of the B axis the material is sufficiently rectangular so that coincident-current techniques can be used to determine whether a ZERO or ONE is stored. However, to the right of the B axis no rectangular properties are exhibited and a special mode of operation is required. In this mode, a large pulse is used to destroy all information in the selected cores and, at the same time, read the contents of these cores. (A complete description of this partial-flux mode of operation will be given later.) It is possible to design special materials for this

Figure 3. BH loop for partial-flux mode of operation.

type of operation which will operate approximately ten times as fast for the same drive as would a normal coincident-current storage material.

TYPES OF STORAGE MATERIALS

Thick Metal Tapes. Typical materials in this category are Deltamax and Orthonol. They have a very high saturation flux density, high Curie point, and low coercive force. They have extremely rectangular characteristics, which are lost when the metals are rolled into thin films. Metal tapes of this type begin to be unusable in storage and switching applications when their thickness is below 0.001 in. They are useful in applications where slow operation is desired and where relatively high power must be transmitted. At high rates of operation, eddy current losses become very large.

Thin Metal Tapes. Typical materials in this category are 4-79 Molybdenum-Permalloy and HI-MU-80. These materials have half the saturation flux density of the thick metal tapes, a high Curie point, and low coercive force. They are not particularly rectangular in tapes thicker than 0.001 in. Their rectangularity and coercive force increase as the material is rolled into thin tapes. The 0.00025- and 0.000125-in. tapes have excellent properties. Cores wound with thin tapes have been used in special storage systems, but their chief applications are as switches, shift registers, and core logic. The characteristic switching time depends on tape thickness; in the very thin tapes this time can be as low as a few microseconds. It is difficult to maintain high uniformity in rolling thin tapes. Components must therefore be designed using the maker's specifications and tolerances and not by means of measurements or tests on a small sample batch.

Thin Films. Thin metallic films are usually deposited by electrolytic or vacuum evaporation techniques, whereas thin tapes are almost always rolled from a block of the metal. Although thin films have extremely desirable qualities, they present considerable difficulty in controlling the uniformity of the separate storage elements. The present investigations into thin films are aimed at finding a thin metallic element which will exhibit relatively little dynamic loss and at establishing techniques to improve the electrical properties by utilizing magnetic or mechanical stress in the material. To

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solve this latter problem, four major approaches are being investigated. The first is to use very thin, flat disks of material deposited in a magnetic field so that they exhibit a built-in magnetic stress. These disks are deposited, usually in vacuum, a large number at a time on a glass plate. Printed windings laid over the top of the disks provide a means of access to them. The "twistor" provides another method of approaching the problem. In this approach, the material is plated or deposited on a wire and is then subjected to a mechanical torsional strain in order to set up a helical field pattern. Access to this type of storage device is by means of windings wrapped around the wire and by the use of the wire itself. A third approach is to deposit the material on small rods so that it is formed into a bar magnet, the effective thickness of which is very small compared to its length. And, finally, an attempt is being made to construct thin metallic cores, which are analogs of the conventional ferrite core, by depositing a thin layer of metallic material as a continuous path around a small toroid. At present, insufficient equipment has been built utilizing any of the four techniques described above to be able to predict which, if any, of them will achieve wide usage.

Ferrites (Ferrospinels). Cores of these materials are made by several manufacturers under different trade names. Most of them are magnesium-manganese or copper-manganese ferrite bodies. In manufacture, the oxides or other salts of the metals are mixed in the correct quantities and then undergo a series of grinding, milling, and firing cycles. The product at this stage is a uniform free-flowing powder. Cores are pressed individually from this powder under considerable pressure and then subjected to a lengthy firing process under controlled atmospheric conditions and at a maximum temperature which may be in excess of 2500°F. The cores, ceramic in nature, are vitrified throughout and consequently are very hard and brittle. They are reasonably good insulators and exhibit high permitivity, but are relatively weak magnetically. The maximum flux density is low, as is the Curie point. The coercive force is usually rather high. Since cores are insulators, they may be molded in fairly large sections without altering their loss characteristics. In a tape core a large amount of the cross-section area is taken up with inter-tape insulation and a bobbin. In a ferrite core the entire cross-section area is useful material; this compensates, to some extent, for the low flux density.

Magnesium-maganese ferrites are exceedingly stable. Extensive tests indicate no change in their properties with life. If correctly packaged, they do not appear to be subject to subsequent mechanical or electrical failure. The experience with well packaged ferrite cores indicates that the probability of failure is in excess of one part in 10^{10} and probably is one part in 10^{12} core hours. The copper-maganese ferrites, though fairly stable, have the undesirable characteristic that at high temperatures their properties can change. In all cores of this type that have been tested, a temperature of 100°C appears high enough for a slow change to commence. However, in all normal equipments the copper-manganese ferrites can be considered highly reliable. Most commercial ferrite cores will operate reliably up to about 70°C. Special cores which will operate in a coincident-current mode at temperatures in excess of 100°C are also available commercially. Experimental cores have been produced which can be operated at temperatures higher than 200°C.

All ferrite cores have relatively large temperature coefficients, which are predictable, stable, and uniform. Each parameter of the core's operating characteristics has a different temperature coefficient. The parameter of major importance is the drive current required to maintain the operating characteristics constant over a range of temperature. In most magnesium-manganese ferrite cores this temperature coefficient is approximately ½ per cent per degree Centigrade. The drive current must be reduced as temperature is increased by this amount, or conversely must be increased by this amount as temperature is reduced. It is possible either to temperature-compensate the whole system so that drive currents are optimum at the operation temperature, or alternatively to operate the cores at all times at the highest expected temperature.

An important property of a ferrite core is the effective tolerance available over a range of drive current and temperature. This tolerance is usually expressed as the percentage ratio of H_k to H_t. For example, a core is said to have a 65 per cent knee. This implies that a tolerance of 15 per cent is allowable on the half-current fed to the core in the coincident-current mode without expecting deterioration of the operating properties of the core. A typical core which operates over a wide temperature range will have a knee of 75 per cent at 25°C and will still be in excess of 65 per cent at 70°C. This indicates that the core could be operated without

temperature compensation over a wide range of temperatures. However, adequate temperature compensation of the system will tend to center the core at the optimum operating current, allowing the driving elements to deteriorate considerably with age without affecting performance of the equipment.

Because ferrites can be molded by mass production methods into small-size cores with a high degree of uniformity, they are almost always adopted in storage applications. They also find some use in switch cores and in shift register and logical applications. Ferrites are not suitable for large switch cores; since they are insulators, it would be difficult to remove heat from the cores. Cores have been made in a range of materials having characteristic switching times from 0.1 to 15 microseconds, but commerically available materials have switching times from 0.2 to 5 microseconds.

Table 1 lists the properties of two typical ferrite materials which are in common use today.

Table 1. Properties of Two Typical Ferrite Materials

	One-Microsecond Material	Four-Microsecond Material
Switching Time (Microseconds)	1.00	4.00
Coercive Force (Oersted) H_c	1.25	0.55
H_k (Approximate)	1.125	0.51
H_t (Approximate)	1.54	0.92
Saturated Flux Density	1740.00	2100.00
Remanent Flux Density (B_r) (Gauss)	1600.00	2000.00
B_r/B_s	0.92	0.95
Curie Temperature (°F)	450.00	360.00
Temperature Coefficinet (Per cent of H_c per °F)	0.14	0.17 to 0.2

CORE GEOMETRY

It is well known that in a long, open-ended bar magnet some portion of the flux tends to return down the magnet. This flux has a demagnetizing effect on the magnet which tends to reduce the rectangular properties of the material. In thin films where, almost universally, open-ended storage elements are employed, the ratio of thickness of the magnet to length is always extremely small. In ferrite or metallic toroids, this ratio is usually relatively large. It is not practicable to cut and rejoin either metal or ferrite cores; for the resulting gap, however small, will reduce the B_r/B_s ratio and increase the coercive force. Since even small cracks or chips will alter the properties of cores, the toroids must be complete and undamaged.

Several typical toroids are shown in Figure 4. The current required to drive the toroid is a function of the mean diameter; consequently, the tendency is to use the smallest possible core. Practical limitations determine the minimum wire size for a given toroid. The number of wires which can

CORE	D_2	D_1	d
A	.050	.030	.015
B	.080	.050	.025
C	.100	.070	.030
D	.180	.090	.045

Figure 4. Typical toroids.

be inserted through the center of the toroid will be proportional to $(D_1)^2$ if the core is threaded at right angles to its plane. In practice, the plane of a core is normally at 45 degrees to the direction of the wire threading; therefore, the actual effective aperture is considerably smaller than the maximum available aperture shown in Figure 4. Aperture size is also affected by the thickness of the core. For this reason, cores should be as thin as is feasible in order to permit easy passage of wire through the aperture. The ampere-turns required to drive the toroid will be proportional to $D_1 + D_2$. The voltage drop per turn will be proportional to $d(D_1 - D_2)$. If minimum current to drive the toroid is desired, a large diameter should be used. As the diameter of a toroid is increased, the number of turns which can be wound through the window rises more rapidly than the number of ampere-turns which are required to drive the toroid. For a fixed wire size and given geometry, the driving current is inversely proportional to the diameter of the toroid. The voltage drop increases rapidly as the number of turns is increased; therefore, multiple-turn windings are employed only in small storage units. Most switches are treated as small matrices employing large cores and multiple-turn windings.

The core is not a perfect thin-walled toroid. As the value of H is reduced in moving from D_1 to D_2, a new storage loop is adopted which is narrower and has less flux change than the original loop. Consequently, the over-all storage loops of the core is the sum of a number of loops which have different values of coercive force and of flux density. Consider a toroid consisting of three co-axial rings. Let the BH loops of these rings be L_1, L_2, L_3, as shown in Figure 5(a). The over-all BH loop of the system will be that of Figure 5(b). If an infinite number of rings, each of which is perfectly rectangular, is taken, the over-all loop will be a parallelogram. The rectangular characteristics of the core are degraded as the ratio of D_1/D_2 is reduced. Manufacturing considerations limit the wall thickness. A D_1/D_2 ratio of 0.7 is about the maximum value which will give adequate yield. For a high yield of the most economical cores, $D_1 - D_2$ should not be reduced below 0.03 in. Fortunately most ferrite materials used in storage applications have very good rectangular characteristics. This makes it possible to use relatively inferior core geometry and still attain good operation. However, if as nearly ideal as possible characteristics are required, a thin-walled toroid should be chosen.

Ferrite cores which have been adopted as relatively standard cores are listed in Table 2.

Figure 5. Effects of wall thickness on toroid characteristics. (a) Loops of three co-axial rings. (b) over-all system loop.

Table 2.   Standard Cores

D_2	D_1	d	D_1/D_2	$\frac{1}{2}(D_2+D_1)$	No. of wires wound through window
0.100	0.070	0.030	0.700	0.085	5 to 15
0.080	0.050	0.025	0.625	0.065	4 to 11
0.060	0.038	0.018	0.633	0.049	4 to 8
0.050	0.030	0.015	0.600	0.040	4 to 6
*0.030	0.020	0.006	0.666	0.025	3 to 5

*   Still in developmental stage.

TYPICAL FERRITE CORES

Manufacturers of ferrite cores specify core material and geometry in order that components of definable electrical and mechanical properties may be supplied. A number of typical commercially available cores are described below. Considerably more data about these cores can be obtained from the manufacturer.*

Core No. 1. The size of this core is 0.080 in. (outside diameter), 0.050 in. (inside diameter), 0.025 in. (thickness). Its switching time is less than 1.25 microseconds. The drive pulse required is normally 0.82 ampere-turns. At 25°C the core is usually driven with this amount of full current by means of a pulse which is 1.5 microseconds long, and has a rise time of 0.2 microsecond and a fall time of 0.3 microsecond. The switching time (P_S) is 1.25 microseconds. The amplitude of a ONE signal (dV_1) is 125 millivolts; and the amplitude of a ZERO (dV_Z) is 10 millivolts. Peaking time (t_p) is 0.65 microsecond. The signal-noise ratio at peaking time is at least 50 to 1. This indicates that the ZERO or noise signals decay rapidly as the amplitude of the ONE signal builds up. At peaking time the amplitude of noise or ZERO signal is less than 2.5 millivolts.

Typical test conditions and output signals obtained under these conditions are shown in Tables 3 and 4.

Table 3. Test Conditions

Temperature		25 ± 1°C
Drive pulse I_R or I_W	=	740 ma ± 1%
Drive pulse I_{PR} or I_{PW}	=	470 ma ± 1%
Pulse rate	=	56 kc ± 1%
Pulse duration	=	9 usec
Pulse rise time (10% ... 90%)	=	0.20 ± 0.02 usec
Pulse overshoot		1% rise or droop max

* Telemeter Magnetics, Inc.

Table 4. Output Signals (Under Test Conditions)

Disturbed ONE dV_1	=	90 mv min
Peaking time t_p of dV_1	=	0.65 $\pm$ 0.05 usec
Switching time t_s of dV_1	=	1.40 usec max
Peak disturbed ZERO dV_z	=	25 mv max
Amplitude of dV_z at t_p	=	0.5 mv max

Sample cores are also tested over a range of temperature to determine temperature-drive relationship. Results are summarized in Table 5.

Table 5. Temperature - Drive Relationship

Temperature	0°C	25°C	40°C
$I_R = I_W$	900 ma	820 ma	775 ma
$I_{PR} = I_{PW}$	550 ma	510 ma	460 ma
dV_1 min	125 mv	125 mv	125 mv
dV_z max	30 mv	30 mv	30 mv

Core No. 2.   The size of this core is 0.080, 0.050, 0.025. It is intended for use in low-speed memories where economy of current drive is important. The core normally switches in less than 4 microseconds when driven with a full current of 364 milliamperes. At 25°C the drive pulse is usually 6 microseconds long with about 1 microsecond rise and fall time. Under these conditions the switching time is 3.8 microseconds. dV_1 is 35 millivolts, dV_z is 4.5 millivolts, peaking time is 2 microseconds, and the signal-noise ratio is in excess of 100. Typical test conditions and the output signals obtained under these conditions are shown in Tables 6 and 7.

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Table 6. Test Conditions

Temperature	$25 \pm 1^\circ C$
Drive pulse I_R or I_W $\quad=$	330 ma $\pm$ 1%
Drive pulse I_{PR} or I_{PW} $\quad=$	200 ma $\pm$ 1%
Pulse rate $\quad=$	56 kc $\pm$ 1%
Pulse duration $\quad=$	9 usec
Pulse rise time (10%...90%) $\quad=$	0.6 $\pm$ 0.05 usec
Pulse overshoot	1% rise or droop max

Table 7. Output Signals (Under Test Conditions)

Disturbed ONE dV_1 $\quad=$	20 mv min
Peaking time t_P of dV_1 $\quad=$	2.0 $\pm$ 0.2 usec
Switching time t_S of dV_1 $\quad=$	4.0 usec max
Peak disturbed ZERO dV_Z $\quad=$	7.0 mv max
Amplitude of dV_Z at t_p $\quad=$	0.5 mv max

Results of tests performed over a range of temperature to determine temperature-drive relationship are summarized in Table 8.

Table 8. Temperature - Drive Relationship

Temperature	$0^\circ C$	$25^\circ C$	$40^\circ C$
$I_R = I_W$	400 ma	360 ma	345 ma
$I_{PR} = I_{PW}$	240 ma	215 ma	200 ma
dV_1 min	30 mv	30 mv	30 mv
dV_Z max	7 mv	7 mv	7 mv

Core No. 3. This core is one of the small-size (0.050, 0.030, 0.015) variety. Switching time is 1 microsecond when pulsed with a full current of 500 milliamperes. At 25°C the core is driven with a pulse of 500 milliampere-turns full current and a width of 1.5 microseconds. It switches in less than 1 microsecond and peaks at about 0.5 microsecond. dV_1 is 75 millivolts, dV_z is 5 millivolts, and signal-noise ratio is in excess of 100.

Typical test conditions and the output signals obtained under these conditions are shown in Tables 9 and 10.

Table 9. Test Conditions

Temperature		25 ± 1°C
Drive pulse I_R or I_W	=	450 ma ± 1%
Drive pulse I_{PR} or I_{PW}	=	285 ma ± 1%
Pulse rate	=	56 kc ± 1%
Pulse duration	=	5 usec min
Pulse rise time (10%...90%)	=	0.2 ± 0.05 usec
Pulse overshoot		1% max rise or droop

Table 10. Output Signals (Under Test Conditions)

Disturbed ONE dV_1	=	45 mv min
Peaking time t_p of dV_1	=	0.5 ± 0.05 usec
Switching time t_s of dV_1	=	1.25 usec max
Peak disturbed ZERO dV_z	=	10 mv max
Amplitude of dV_z at t_p	=	0.5 mv max

Typical temperature-drive relationship over a range of temperature appears in Table 11.

Table 11. Temperature - Drive Relationship

Temperature	0°C	25°C	40°C
$I_R = I_W$	565 ma	500 ma	480 ma
$I_{PR} = I_{PW}$	345 ma	310 ma	285 ma
dV_1 min	65 mv	65 mv	65 mv
dV_z max	8 mv	8 mv	8 mv

Figure 6. Output-drive curves for typical ferrite core.

Figure 6 shows the relationship of output and drive for Core No. 3. Similar curves can be plotted for most ferrite cores. It will be seen that at low values of drive current, the operation of the core is limited by a low value of the ONE signal. At high values of drive current, the disturb or ZERO signal (dV_z) rises rapidly while the ONE signal (dV_1) drops rapidly, and there is a marked deterioration in the operation of the core.

Core No. 4.   The dimensions of this core are 0.050, 0.030, 0.015. Its switching time is nearly 3 microseconds when pulsed with a full current of 234 milliamperes. In normal operation it is pulsed with either the full current or a half-current of 117 milliamperes, using a pulse with slow rise and fall times and a width of 3 microseconds. This core is particularly useful in transistor-driven applications, and does not require the use of particularly costly transistors. dV_1 is 15 millivolts, dV_z is 2.5 millivolts, peaking time is approximately 1.5 microseconds, and the signal-noise ratio is in excess of 100. Test conditions and output signals are shown in Tables 12 and 13.

Table 12.   Test Conditions

Temperature		$25 \pm 1^{\circ}C$
Drive pulse I_R or I_W	=	212 ma $\pm$ 1%
Drive pulse I_{PR} or I_{PW}	=	138 ma $\pm$ 1%
Pulse rate	=	56 kc $\pm$ 1%
Pulse duration	=	6 usec min
Pulse rise time (10%...90%)	=	0.6 $\pm$ 0.05 usec
Pulse overshoot		1% max rise or droop

Table 13. Output Signals (Under Test Conditions)

Disturbed ONE dV_1	=	10 mv min
Peaking time t_p of dV_1	=	1.6 ± 0.05 usec
Switching time t_s of dV_1	=	3.2 usec max
Peak disturbed ZERO dV_z	=	3.5 mv max
Amplitude of dV_z at t_p	=	0.5 mv max

Typical temperature - drive relationship for a range of temperatures is shown in Table 14.

Table 14. Temperature - Drive Relationship

Temperature	$0^\circ C$	$25^\circ C$	$40^\circ C$
$I_R = I_W$	255 ma	235 ma	217 ma
$I_{PR} = I_{PW}$	155 ma	148 ma	132 ma
dV_1 min	14 mv	14 mv	14 mv
dV_z max	4 mv	4 mv	4 mv

Core No. 5. This 50-mil core (0.050, 0.030, 0.015) is intended for applications where high environmental temperatures are encountered. The characteristics of this core are shown in Tables 15 through 19.

Table 15. Recommended Drive Conditions

	At $25^\circ C$	At $70^\circ C$
Drive pulse	430/215 ma turns	326/163 ma turns
Pulse width	2 usec	2 usec
Pulse rise time	0.2 usec	0.2 usec
Pulse fall time	0.3 usec min	0.3 usec

Table 16. Typical Output Signals

	At 25°C	At 70°C
Switching time t_s	1.0 usec	1.1 usec
Amplitude ONE dV_1	40 mv	40 mv
Amplitude ZERO dV_z	10 mv	8 mv
Peaking time t_p	0.5 usec	0.5 usec
Signal/noise ratio at t_p	100	100

Table 17. Test Conditions

Temperature	$25 \pm 1^{\circ}$C
Drive pulse I_R or I_W =	420 ma $\pm$ 1%
Drive pulse I_{PR} or I_{PW} =	264 ma $\pm$ 1%
Pulse rate =	10 kc $\pm$ 1%
Pulse duration =	5 usec
Pulse rise time (10%...90%)=	0.2 $\pm$ 0.05 usec
Pulse overshoot	1% max rise or droop

Table 18. Output Signals (Under Test Conditions)

Disturbed ONE dV_1	=	30 mv min
Peaking time t_p of dV_1	=	0.55 $\pm$ .05 usec
Switching time t_s of dV_1	=	1.2 usec max
Peak disturbed ZERO dV_z	=	10.5 mv max
Amplitude of dV_z at t_p	=	0.5 mv max

Table 19. Temperature - Drive Relationship

Temperature	25°C	55°C	80°C
$I_R = I_W$	435 ma	345 ma	296 ma
$I_{PR} = I_{PW}$	266 ma	211 ma	180 ma
dV_1 min	35 mv	35 mv	35 mv
dV_z max	10.5 mv	10.5 mv	10.5 mv

Core No. 6.   This is a 50-mil (dimensions, 0.050, 0.030, 0.015) designed for use in word-selection or linear-selection memory systems with high repetition rates. The rates are achieved by utilizing a small portion of the total flux, thereby min-imizing heat dissipation requirements. This core is pulsed with a large current I_R in order to read and with a long low-amplitude pulse I_W in order to write. If a ONE is to be written, a digit-drive pulse I_D is applied in addition to I_W. Recommended oper-ating conditions at 25°C and typical output signals are shown in Tables 20 and 21.

Table 20. Recommended Operating Conditions at 25°C

Current Pulses	Read (I_R)	Write (I_W)	Digit (I_D)
Amplitude	500 ma turns	170 ma turns	130 ma turns
Rise time (t_r)	0.1 usec	0.1 usec	0.1 usec
Fall time (t_f)	0.1 usec	0.1 usec	0.1 usec
Width at base (t_d)	0.3 usec	0.6 usec	0.6 usec

Table 21. Typical Output Signals

	Amplitude	Peaking time (t_p)	Switching time (t_s)
Read ONE (dV_1)	100 mv	0.1 usec	0.25 usec
Read ZERO (dV_z)	20 mv	---	---

TESTING STORAGE AND SWITCH CORES

Every core that is used in a storage unit must be tested thoroughly to ensure as near perfect operation as is possible in the matrices and switches. Ferrite cores are subjected to three series of tests: production sampling, core evaluation, and quality control tests.

Sampling tests are performed on a sample of cores in a production run to determine statistically whether all the characteristics of the batch are correct. The entire production run is then tested for critical operating parameters such as loop squareness, switching time, peaking time, and operating current range. Storage cores are tested on an automatic testing device which, in view of the large number of cores involved, is faster and more economical than hand testing. A standard core is used to maintain calibration of the tester, which is usually set to operate at a fixed ambient temperature. Each core is demagnetized before testing commences to remove any previous "history".

Of all the evaluating tests for storage cores, the most important is the determination of the operating current range. A core is tested for drive range by means of a long train of variable-amplitude pulses, and with various sensing amplifiers and automatic grading circuits. The core is first disturbed with a low value of current to determine whether it provides sufficient voltage output. It is then disturbed by a high value of current either as a long pulse or as a train of pulses in the direction which could cause demagnetization. Conditions of low turnover current and high disturbed current are those most likely to demagnetize the core. The amount of demagnetization compared to the signal produced on complete turnover is known as the "disturb sensitivity" of the core.

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For most storage systems, the high and low ends of the operating range are defined as +5 to +15 per cent of the optimum value, and the allowable disturb sensitivity is 0.3 or 0.4. Testing for disturbed signals is of particular value when cores with very large ONE/ZERO ratios are desired.

Switch cores, both ferrite and metal, are ordinarily tested by hand because only small quantities are used. A core is energized by current pulses which will switch it in a time somewhat shorter than the characteristic switching time. The area of the output pulse is examined to measure the flux output; and the shape of the pulse is examined to determine the coercive force and the behavior at the knee of the loop and in the region of decreasing permeability. The over-all loop is also checked with a BH tester. When the switch core is wound as a separate transformer, it is tested in an analog of the circuit in which it will operate. Testing of switch cores is generally complex because the principal parameters are indicated by the shape of the output pulses. Skilled human operators are more effective than machines in performing the necessary tests.

The final series of tests for both storage and switch cores are the quality control checks. Storage cores are tested automatically on the testing device and switch cores are tested semi-automatically. A double check of operating parameters is usually made on a sample of cores at this point to eliminate any defective batches which may have been accepted as the result of a malfunction of the automatic equipment.

Automatic testing equipment is expensive and, to justify its cost, must be capable of testing a group of cores over long intervals with substantially the same results. All the circuits in the equipment must be extremely precise because even a slight change in pulse shape can alter test results.

STORAGE TECHNIQUES

PRINCIPLES OF COINCIDENT-CURRENT SELECTION

A magnetic core is a non-linear element which will not change its state when a half-current (I/2) passes through it, but will change its state when a full current (I), consisting of two half-currents, is applied. This property of the core is the basis for the principle of coincident-current selection of a core from an array for storage or read-out of information. It is possible to select a specific core by energizing the horizontal X wire and the vertical Y wire through the core, each wire carrying a half-current. The cores on the X and Y co-ordinates which are linked by only a half-current will not change state, but the core at the intersection of the wires will receive the full current and will change its state. In practice, cores will tolerate more variation in current than the theoretical 2 to 1 ratio because the knee of a core is usually at 65 to 75 per cent of the I value. Currents which are not exactly equal may therefore be used in the X and Y wires, particularly for the purpose of improving the tolerance of the electronic part of the system.

Selection by triple coincidence is theoretically possible by using X, Y, and Z wires through the cores. A current of I/3 would be applied to each of the selected co-ordinate wires, and only the core at the intersection of the energized wires would change its state.

A simple coincident-current matrix is shown in Figure 7. Conventionally, if a current corresponding to $H_t/2$ is applied to two of the intersecting wires, the core at the intersection will be forced into the ZERO state. Similarly if $-H_t/2$ is applied, the opposite state of storage will be produced. If, for example, B and D are energized with a positive half-current, then core 3 will be forced into the ZERO state. If the core was already in the ZERO state before this action occurred, very little flux change would occur; but if the core was in the ONE state, a complete flux reversal would occur. If all the cores are linked by a sense winding such as EE, the flux change resulting from a core being forced from the ONE state to the ZERO state would induce a voltage in EE. This voltage could be detected by means of a suitable amplifier connected to the terminals EE. This is the basic method of reading employed in a coincident-current memory. In order to write, positive half-currents can be applied to the desired lines to set the selected core into the ZERO state, or negative half-
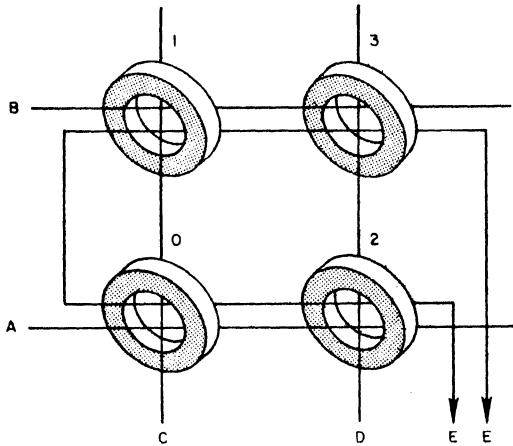
24

Figure 7. Core matrix for simple
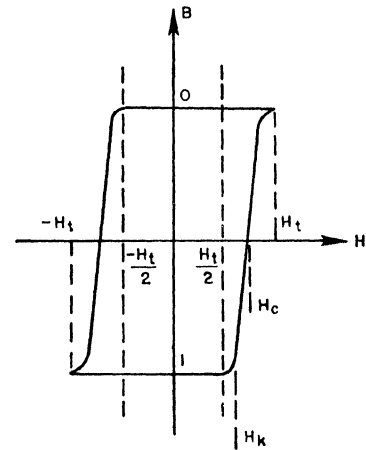coincident-current operation.

Figure 8. Hysteresis loop of
a core operated by coincident
current.

currents can be applied to set the core into the ONE state. In
most memories a writing action consists of first setting the core
into the ZERO state and, if it is desired to write a ONE, later
setting the core into the ONE state.

Coincident-current selection is illustrated in Figure 8 in
terms of a hysteresis loop. The half-currents correspond to $H_t/2$
or $-H_t/2$. Full currents correspond to either H_t or $-H_t$. In order
to obtain the best tolerance in the system, ideally the most
suitable core to employ is the one in which H_k exceeds $H_t/2$ by as
large a factor as possible. It should be noted that H_k and H_t
are special terms employed in coincident-current storage. The
normal parameter associated with magnetic materials, the coercive
force, is shown as H_c. Usually the values of H_c and H_k are very
close, while H_t is much larger than H_c. For this reason, H_c and
H_k are frequently confused in the literature and are often used
indiscriminately to replace each other.

In a coincident-current matrix, a sense winding links all the
cores. Undesired signals introduced by all the half-excited cores
induce a voltage in the sense winding. During a reading action
in an n^2 matrix, one core will receive a full excitation and $2(n-1)$
cores will receive a half-excitation. The other cores receive no

excitation. If the cores had perfectly flat saturation characteristics, the half-excited cores would provide no output. In practice the voltage induced in the sense winding by a half-excited core may be an appreciable fraction of the voltage induced by the selected core, the amount of voltage depending on the type of core and on the type of operation. The output due to half-excitation takes the form of a voltage pulse which lasts for a short period of time. The peak amplitude of this pulse may be as great as a third of the amplitude of the turnover signal. If the sense winding linked all cores in the matrix in the same polarity, a considerable voltage would be induced in this winding due to the disturbed cores. In a 10,000-core matrix, for example, the total voltage induced in the sense winding would be sixty times as large as the turnover or ONE signal. In order to overcome this problem, the sense winding is arranged to link the matrix cores in alternating polarities so that equal numbers of cores provide positive and negative disturbed signals with a consequent tendency toward cancellation. The disturbed signals can be made to cancel completely if the matrix is well designed, the cores are uniform, and the correct driving functions are performed.

Large-capacity storage units sometimes employ magnetic core switches or transformers to drive the matrices, which are usually operated in a parallel manner. Core switches and transformers must be restored after they have been set, and two pulse times must be allowed for any transformer or switch operation. The cycle which is employed under these circumstances consists of two parts. First, a reading operation is performed. If it is part of a reading cycle, the information is read from the selected core; or if the operation is part of a writing cycle, cores are turned over to the ZERO state. The switch or transformer cores are usually set during this read operation. Secondly, a write operation is performed during which the cores are usually set into the ONE state. The transformer or switch cores are usually reset during this write operation. Writing is used to generate information destroyed during reading or to insert new information into the storage device. An additional driver, known as the digit-plane or inhibit driver, is energized if a core is to remain in the ZERO state during the write part of the cycle. This driver provides a half-current to an inhibit winding in the storage matrix which prevents the ONE setting action inherent in a normal write operation.

The same cycle is used for both reading and writing operations. In reading, the second beat of the cycle is used to restore the information which was read. In a parallel storage system, a number of matrices corresponding to the number of bits in the stored word

are driven in cascade. Separate digit-plane drivers, provided for each matrix, are used during the second beat of the cycle to modify the information in the individual bits of the word. In some storage units, the two beats of the cycle must always occur; they are usually referred to as the "reading" and "writing" beats. In other units it is possible to separate the two beats. They are then referred to as the "unload" and "load" operations. If this latter mode of operation is used, and unload operation must be preceded by a load operation, and similarly a load operation must be preceded by an unload operation. The basic principles of operation of a core storage unit do not require that an unload operation must occur first and then immediately be followed by a load operation. In many devices considerable advantages may be obtained by allowing random access not only to the address in the unit but also to the part of the cycle that is required.

Triple Coincidence. Coincident-current operation has the advantage that the number of wires required to select a core is less than the number of cores which can be selected. In normal operation 2n wires will select n^2 cores. If a material is used in which the knee is greater than 67 per cent, then 3n wires would select n^3 cores. Triple coincidence may be achieved by a biasing technique without using a material that is any more rectangular than those normally used in double coincidence. Triple coincidence is not of great value in small matrices, but as the size increases it may become necessary to adopt triple coincidence.

There is a continuous demand for ever higher rates and ever larger capacity in storage units. In transistor-driven equipment, high rates can be achieved only by direct connection of the transistors to the storage arrays. The tendency is to greatly increase the number of transistor drivers as rate and capacity are increased. Under these circumstances, triple rather than double coincidence is the economical choice, considering the number of drivers required. (See Table 22.)

Materials are available which can be used in simple triple-coincidence applications. The signal-noise ratio achieved with these materials is poor, and there is an undesirable loss of tolerance in operating the system. Because of these disadvantages, triple-coincidence systems are rarely used. When such systems are considered essential for storage applications, the bias technique mentioned above is almost invariably adopted.

Table 22. Number of Drivers for Double-and Triple-Coincidence
Matrices

Number of Cores in Matrix	Number of Drivers	
	Double Coincidence	Triple Coincidence
64	16	12
4,096	128	48
262,144	1,024	192
1,000,000	2,000	300

OPERATION OF A NUMBER OF MATRICES IN PARALLEL

A form of three-dimensional operation can be achieved by operating a number of matrices in parallel. One set of drivers drives all the matrices in cascade, and an individual driver per matrix sets the information into that matrix. This system is not as efficient as a true triple-coincidence system, but it does have the advantages that a whole character or word can be operated on at once with a consequent increase in computing rates. Even in storage units which work in conjunction with serial machines, it is common practice to employ a parallel storage unit together with circuits which perform serial-parallel conversion. For example, a 262,144-bit store could employ one matrix using 48 drivers or sixty-four 4,096-bit matrices using a total of 88 drivers. The second arrangement would be 64 times as fast as the first, although the increase in the number of drivers is less than a factor of two.

Two basic methods have been adopted to control the insertion of information into the individual matrices in a parallel system: use of a digit-plane or inhibit winding, and use of a switch.

Control by a Digit-plane or Inhibit Winding. In this method, the outputs of the magnetic or transistor switches are taken through all the matrices in cascade. Both switches are operated at the same time and provide like outputs. The selected core in every parallel matrix is set to ZERO and the reading operation is performed. At the end of this operation the two selected switch cores are in the non-normal state of flux. These cores are then restored to their normal state, which tends to set all the selected matrix cores into the ONE state. A fourth winding is wound through each matrix, linking all of the cores in the same sense. An mmf equal and opposite

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FIRST CYCLE
READ OR WRITE "ONE"

SECOND CYCLE
READ OR WRITE "ZERO"

MMF DUE
TO X
WINDING

X_p X_n X_p X_n

MMF DUE
TO Y
WINDING

Y_p Y_n Y_p Y_n

MMF DUE
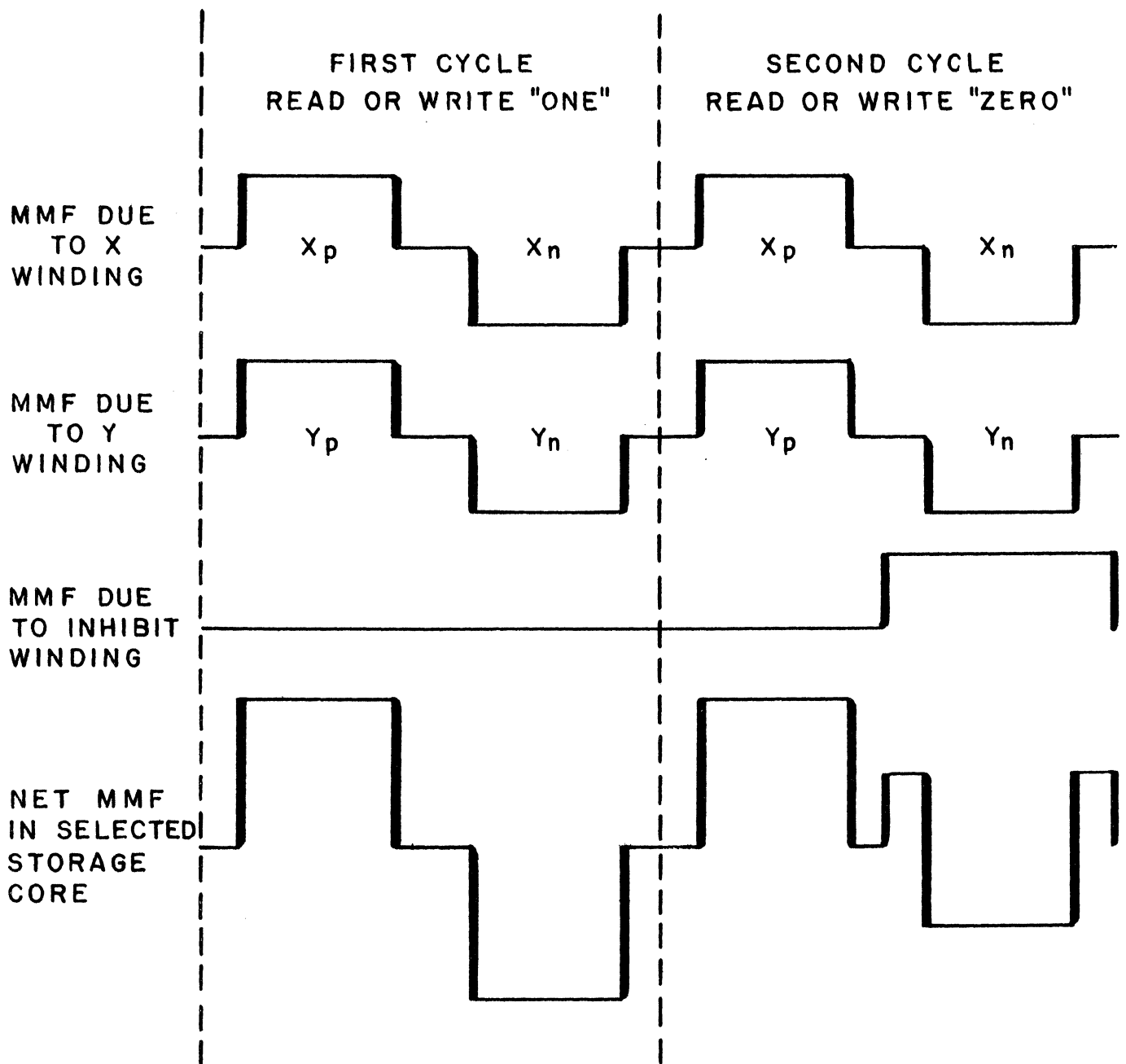TO INHIBIT
WINDING

NET MMF
IN SELECTED
STORAGE
CORE

Figure 9. Cycle when inhibit winding is used to operate matrices in parallel.

to that flowing in each of the selection lines can be applied by this fourth winding during the period when the switch cores are restored. When this mmf is applied, the selected core receives a net half-excitation and remains in the ZERO state. The fourth winding, known as a digit-plane or inhibit winding, is driven by a digit-plane driver. This makes it possible to control individual bits of the word independently, even though the major selection and drive process is performed by one set of drivers. This action is illustrated in Figure 9. In this diagram and in subsequent diagrams, a pulse is written subscript p if the mmf is tending to move the core into the ZERO state and subscript n if the mmf is tending to move the core into the ONE state. It should be noted that the introduction of the inhibit winding pulse causes considerable mmf change in all the cores linked with this pulse. They first move in a positive direction, then move negative, and finally move positive again. Because this action introduces considerable noise and ringing in the magnetic array, a pause is required after a digit-plane operation before the next reading operation can be commenced.

Control by a Switch. In this method, there is one X switch common to all of the parallel matrices and a separate Y switch for each matrix. One set of drivers links all the Y switches in cascade. The X and Y drivers, operating simultanously, set all the selected Y switch cores. The selected matrix cores are set to ZERO, and reading is performed. A restoration winding linking all the cores in each of the Y switches is driven by a digit-plane driver so that the Y switches can be reset independently. In order to insert a ONE into a particular matrix, the Y switch controlling that matrix is restored at the same time as the X switch. In order to insert a ZERO, the Y switch is restored at some time other than during the X switch restoration. This action is illustrated in Figure 10. In most storage units in which this type of operation is employed, it is the normal practice to restore all the Y switches corresponding to ZEROs first, and then to restore the X switch and the remaining Y switches.

BEHAVIOR OF MINOR LOOPS IN STORAGE CORES

In practice every operation performed on a storage core involves minor hysteresis loops. Only rarely is a core allowed to settle onto a portion of the major loop. For example, a core with a 1-microsecond switching time is usually driven with pulses which may be as short as 1½ or as long as 3 microseconds in duration. Such a core is still in process of settling at the end of a pulse
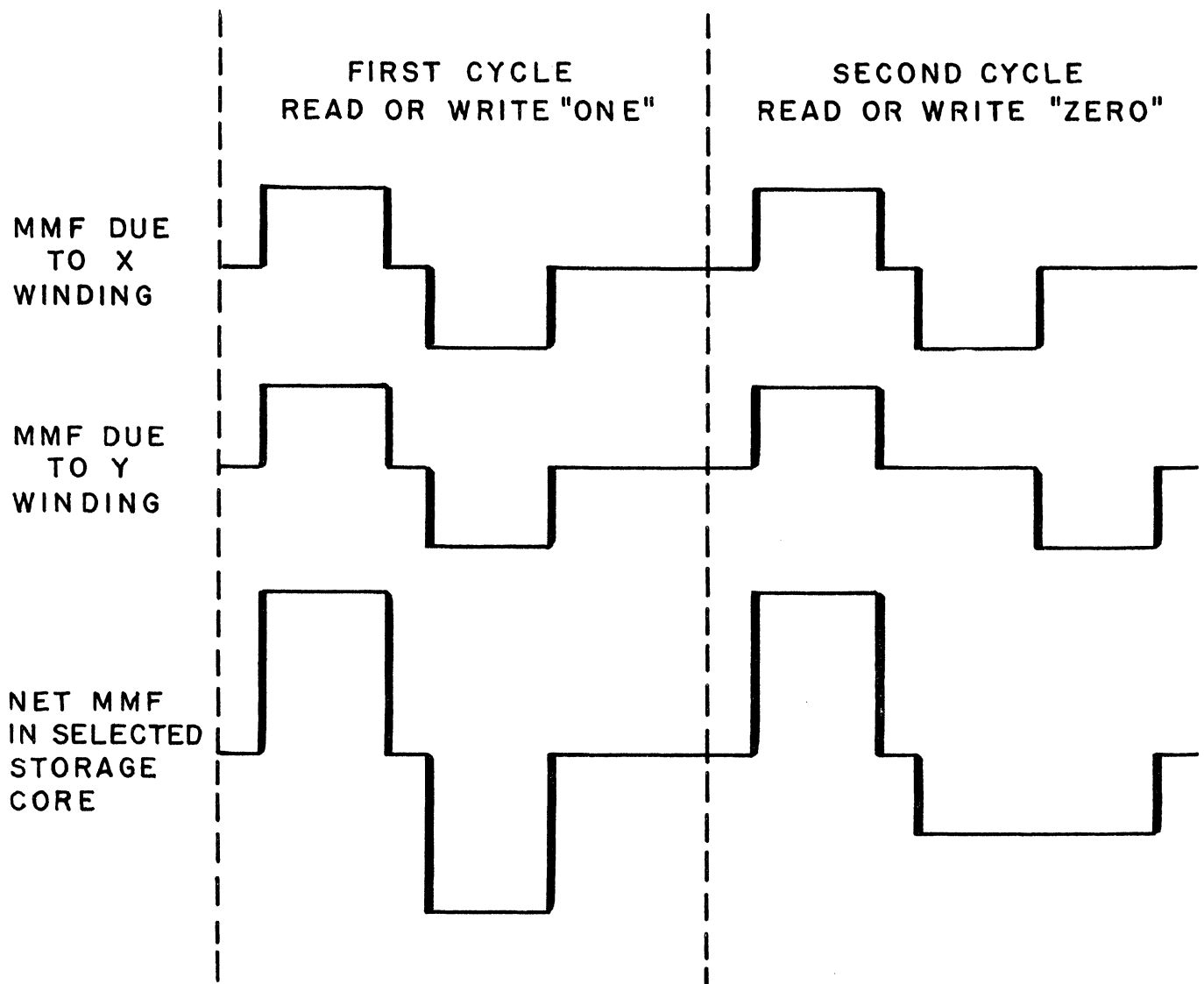
30

Figure 10. Cycle when switch control is used to operate matrices in parallel.

which is 40 microseconds long. Even though the applied current may be sufficient to force the core onto the major loop, ordinarily the pulses would not be of sufficient duration to allow the core to settle completely. Considerable attention should be paid

to the settling problem when extremely rectangular cores which have a high value of knee are used. With cores of this type, it is possible to vary the operating current over a wide range of values without apparently affecting the storage properties. However, the ultimate settling time constant of a core is strongly dependent on the drive current. In designing storage units which employ very rectangular cores, it is necessary to conduct adequate experiments over the complete operating current range to determine the settling characteristics of the cores.
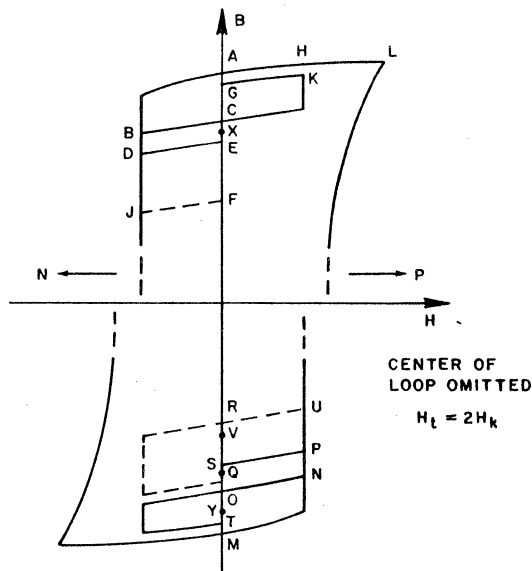

Figure 11. Idealized minor loops associated with storage operation.

In storage matrices the minor loops are extremely important. Figure 11 shows some typical but idealized minor loops associated with storage core operation. To illustrate the problem, the worst possible storage loop in which $H_t = 2H_k$ has been chosen. Point A is what is usually defined as the ZERO storage state. The ZERO state set during the first part of a cycle is followed by at least one half-excitation during the second part of a cycle. Therefore, the initial ZERO state is point C rather than the desired point A. If a series of n direction half-excitations are applied, the core will progress through loops such as CBDE until ultimately a point F is reached. At this point any further half-excitations will produce no more flux change, and the core will remain on the loop FJF. On the other hand, if subsequent half-excitations are in the p direction, the core will move through loops such as CKG until a final stable loop AHA is attained. During a reading action the core is driven to L and then returned to A. Very little output occurs if loop ALA is traversed. In many storage units the action at the ZERO state consists of a complex of p and n half-excitations, and the actual loops tend to fall in the ADEKH region.

To summarize these effects: any disturbances caused by a writing or storage operation tend to move the core to a point such as C, E, or F; whereas disturbances in the read direction tend to move the core towards point A which is the desired storage state.

The lower half of Figure 11 shows loops associated with the ONE state. In most storage cycles, point M is the original storage state. However, it is not so important for the core to remain at point M as it was to remain at point A, because demagnetization from M will result in a ONE signal of reduced amplitude while demagnetization from point A will result in a signal which is large instead of being of ZERO or low amplitude. Excursions via loops MNO, ONPQ, etc., up to point R are often permitted or even encouraged in the design. As in the case of the ZERO state, the actual loops in most storage units also include such loops as RS and OT.

The minor loops which are traversed in the ZERO and ONE states alter the amount of signal obtained when a selected core is read, but this is not as important as the effect on the signals produced by half-excited cores. The sense winding is arranged to link an equal number of half-excited cores in the positive and negative directions. Consider the case of the positive cores being at point A and the negative cores at point M when the reading operation is performed. Since the flux change AH is small and the flux change MN is large, there will be imperfect cancellation. Furthermore, there are great differences between loops AHA and MNO. AHA is a saturated loop of low permeability and involves little or no domain-wall movement. The voltage output from such a loop is a sharp peak which settles rapidly. Loop MNO traverses a region of high permeability involving domain-wall movement, and the voltage output is a rounded peak with a long settling time. There are differences in the flux output of the various loops and in the shape of the voltage pulse. If a large matrix is imperfectly driven, these differences can prevent the reading of the signal from a selected core. Two methods of solving the driving problem are described below.

Use of Saturated Loops. This approach is feasible when the matrix has a digit-plane winding. A selected core is initially set in state C for ZERO or state M for ONE. Subsequently, a non-selected core can be subjected to the types of disturbance listed in Table 23.

Table 23. Types of Disturbance Applied to Selected and Non-Selected Cores

Non-selected core is on	Selected core is set to	
	ONE state	ZERO state
Selected line	half-p, half-n action	half-p action
Non-selected line	no action	half-p action

The two possible types of excitation are a net half-p and a symmetrical half-p, half-n. Under normal conditions of operation there is an equal probability of writing a ZERO or a ONE into a matrix. During a ONE action $2(n-1)$ cores are disturbed in an n^2 matrix. During a ZERO action n^2-1 cores are disturbed. Therefore, the ratio of the probability of the half-p action to the probability of a half-p, half-n action is $\frac{n^2-1}{2(n-1)}$ or $\frac{n+1}{2}$.

In most matrices this factor becomes large, as can be seen in Table 24.

Table 24. Relationship of Number of Cores in Matrix to Half-p/Half-p, Half-n Actions

Number of cores in matrix	Number of half-p actions per half-p, half-n action (average)
64	4.5
4,096	32.5
262,144	256.5
1,000,000	500.5

The tendency is to favor the half-p excitations, which would move the cores onto loops such as AHA and RUR. Because these loops have similar characteristics, nearly complete cancellation is ob-

tained. The half-p, half-n type of disturbance tends to move the core from points A and R to points C and S. As a result of this, most cores in the matrix operate on non-domain-wall-movement loops, while the remaining cores operate on domain-wall-movement loops. This can lead to imperfect cancellation of the disturbed signals. In small matrices the resulting disturbance can be low enough to be ignored, but in large matrices this source of error can be dangerous. In order to correct the disturbance, all the digit-plane drivers can be operated for a short time after any storage cycle to produce what is known as a post-write disturb pulse.

A post-write disturb pulse moves a core which has been left at C or S up to points such as G or V which are not too far removed from the correct storage point. A few more applications of pulse will bring the loops to A and R. An important advantage of this type of cycle is that very little domain-wall movement occurs in the disturbed signals. Therefore, the disturbances decay rapdily and it is possible to employ gating to improve the signal-noise ratio. The use of a post-write disturb pulse has other advantages. It maintains all cores on a loop in which the disturbance due either to the operation of the digit-plane driver or to the operation of any of the address drivers is at a minimum, and thereby essentially reduces the inductance of the whole system to a minimum value. If it is desired to drive extremely large arrays, the introduction of a post-write disturb pulse can simplify the driving problem considerably. The disadvantage of a post-write disturb pulse is that it increases the cycle time and also introduces noise into the cycle in the same way that the normal digit-plane pulse does. For this reason, a post-write disturb pulse operation is usually avoided if possible.

Unequal Currents in the X, Y, and Z Lines. Another solution to the driving problem is to use unequal currents in the X, Y, and Z lines of a matrix. Use of this technique requires careful experimentation to achieve the correct balance of currents. The disadvantage of the technique is that it always reduces the working current tolerance of the core array; but if the cores have sufficiently high "knee", it is usually possible to maintain sufficient tolerance. Any one of a number of methods can be used to introduce this inbalance of current to a system. In practice, it is found that the performance of a memory can be improved both by increasing and by decreasing the value of the digit-plane current, although theoretically optimum results would be obtained by using a slightly high value of digit-

plane current. Performance can also be improved by employing different values of positive and negative current in the X and Y directions if the drivers can be set to different currents in these two directions. Empirical results indicate that there is always an optimum method of compensating any particular memory device. The method depends partly on the design of the device and partly on the usual mode of operation of the device. The correct method is determined by experimentation on the first model of each memory device that is produced.

LINEAR OR WORD SELECTION

An exaggerated form of the unequal-drive-current operation is the linear-or word-selection method of reading. The windings and cycles used in this method are illustrated in Figure 12. Coincident current is not employed for reading; instead, as many drivers

Figure 12. Windings and cycle waveforms for linear selection.

or a switch giving as many outputs as there are characters or words stored in the storage unit are used. Reading is accomplished by providing very large pulses to the read drive winding. The four turns of this winding indicate that the drive current is approximately twice as large as the current normally required for coincident-current operation. Under these conditions the core turns over very rapidly, and a very large read signal is emitted if the core is in the ONE state. If the core is in the ZERO state,

a non-domain-wall-movement type of disturbance is produced which is short in duration and very small in amplitude. Because the sense winding links only the disturbed cores, extremely high signal-noise ratios are obtained with this type of operation.

Two writing methods may be used with linear-selection cores. The first is illustrated in wave form in Figure 12 under Cycle Type A. In method A, the write drive current is half the required current to set the core to the ONE state. A digit-plane winding, wound in the same sense as the write drive winding, is also energized if a ONE is to be written. In the method shown as Cycle Type B, a write drive signal large enough to turn the core to the ONE state is applied at all times. The digit-plane winding, which opposes the write drive winding, is energized only when the core is to remain in the ZERO state.

Method B exaggerates the non-domain-wall-movement disturbances since both the read and the digit-plane signals tend to force the cores onto an asymmetric loop. The read signal is so large that the loop employed is more analogous to a switch-core loop than to the normal storage-core loop, and the half-n disturbance produced by the write line has little, if any, effect on the storage position of the core. Very small ZERO signals are therefore obtained. This particular method of operation is employed in those cycles where it is either desired to obtain very large read signals or where it is desired to operate cores on a shorter cycle than that normally defined by coincident-current operation. Method B has the additional advantage that the cores are extremely tolerant to current variation. All the drive and digit-plane signals may be varied through wide range without serious effects on the performance of the storage unit. Cores operated in this manner will tolerate a wider temperature range than is possible with normal coincident-current operation. They will also operate to a higher maximum temperature because the cycle permits the use of much less rectangular materials than are required for use in coincident-current operation.

Cores with normal rectangular loops may be operated by the methods described above with a considerable improvement in operation at the expense of additional electronic equipment. Special cores have been designed for use in the linear-selection mode. In these cores the hysteresis loop shown in Figure 3 has been greatly exaggerated. Cores are made very small in diameter and wafer thin to obtain a large surface-volume ratio and, consequently, maximum heat transfer. Use of a material with a low

maximum flux change reduces the heat generated within the core.

Electrically the core is designed to have very flat saturation characteristics. The knee on the left-hand side of the loop, if a normal rectangular-loop material is employed, is extremely abrupt and sharp. A knee value approaching 90 per cent is not difficult to obtain. Materials used are degraded considerably to reduce the knee down to the conventional 65 or 70 per cent. This allows much faster switching in the write portion of the cycle than can be obtained with conventional coincident-current material. On the right-hand side of the loop, where very small permeabilities are encountered even in rectangular-loop materials, it is important that minimum permeability be obtained. The core will then switch very rapidly when a large drive pulse is applied during reading and will still switch rapidly during coincident-current write operations.

It is essential to use Cycle A shown in Figure 12 with cores designed for the linear-selection mode because the core materials have such poor rectangular-loop properties that they will not tolerate the disturbances introduced by Cycle B. The properties of these cores are unique in that they can be driven with pulses having a very slow rise time. For example, a typical material will switch in 0.2 microsecond if a pulse is applied which rises in 0.2 microsecond and then falls at about the same rate so that the read pulse is completely triangular. The writing operation requires much lower currents and somewhat more rapid rise and fall times in order to obtain a pulse that is more nearly rectangular. With a rise time of about 0.1 microsecond in the write mode, the core switches in about 0.3 microsecond. With cores of this type, it is not difficult to obtain complete cycle times of less than 1 microsecond, although transistor limitations tend to enforce cycle times somewhat larger than this for most of the large memories. At present the limitation on this technique appears to be one of availability of transistors. It is confidently expected that cycle times of a small fraction of a microsecond can be achieved within the next few years as better transistors become available to designers of core storage units.

MATRICES AND SENSE WINDINGS

Matrices are usually assembled in a square or rectangular shape with the X and Y selection wires at right angles to each other. This is a matter of convenience rather than necessity, since a diamond-shaped matrix could easily be used. If rectangular matrices

are used, the first departure from the square is usually selected. For example, a 4,096-bit matrix can be driven by two 64-way switches, which in turn can be driven by 32 drivers. It can also be driven by one 32-way switch and one 128-way switch, which can be driven by 36 drivers. Matrices can be folded so that the cores are in two layers, making a compact package in which one set of wires enter and leave the matrix on the same side. This has some advantages in assembly and in the construction of some types of sense winding.

The X and Y wires are frequently made of copperweld, a wire of copper solidly welded around a steel center. This wire, more resistive and stronger than copper, simplifies assembly and produces a sturdy final product. The sense winding is always made of maximum diameter copper wire. It is important to keep the resistive impedance of the sense winding as low as possible in order to effect the maximum power transference from the selected core to the reading amplifier. The digit-plane winding can be made of either copper or copperweld. Matrix wires are always coated with a heavy grade of tough insulating material. Thin insulating coatings would be destroyed by abrasion from the cores during assembly. After a matrix has been tested and assembled, it must be covered with a light flexible cement to glue the wires and cores into a solid mat. If this precaution is not taken, the wires and cores will chafe with any subsequent vibration, and breakdown of the insulation will occur.

Design of Sense Windings and Elimination of Disturbances. The X, Y, and digit-plane windings are relatively simple to design. The configuration of the sense winding dominates the design of the matrix. Electrical disturbances introduced into the sense winding as a result of the selection of the X and Y wires must be taken into account in the final mechanical design. The three types of disturbance introduced are as follows:

(1) Disturbance due to the cores themselves. The solution of this problem has been discussed previously.

(2) The magnetic pick-up which occurs because the sense winding and the X and Y wires are inductively coupled loops. This problem is solved by reducing the effective area of the sensing loops to a minimum.

(3) Electrostatic pick-up. When a number of matrices are driven in cascade, the instantaneous voltage of the X

and Y wires may rise to 20 or more volts. Since the signal which is to be detected in the matrix is never more than 0.1 volts and since a 10 millivolt disturbance is undesirable, there must be considerable rejection between the X and Y wires and the reading amplifier to obtain adequate performance.

A correctly designed matrix minimizes the effect of all three types of disturbance.

Cancellation of disturbances is complicated by the fact that there is a considerable propagation time in the sense windings of large matrices. For example, the propagation time is usually between 0.1 and 0.25 microsecond in a 4,096-bit array. In very large matrices the sense winding must be broken up into a number of sections so that the propagation time does not become too long. If the storage cores are widely spaced in the matrix, the propagation time in the sense winding will be long. In addition, the inductance of the address wires and the digit wire will be large; and this, in a matrix of any reasonable size, will introduce difficulties in driving the cores. In a well designed matrix, about half the load presented to a driver is due to the air inductance of the winding and the other half, to the non-linear inductance of the cores. This approximation is based on the assumption that the cores in the matrix are as close together as possible. If the matrices are to be driven at a maximum rate, it is highly desirable to pack the cores so that they are almost touching. This particular point of minimum size in a matrix presents a considerable problem to the designer. He can improve the electrical design by using the maximum packing density, but at the same time he will inevitably increase the manufacturing cost of the matrix. In recent years improved manufacturing techniques have permitted designers to employ spacing between matrix wires which is nearly ideal. In most present-day matrices, the distance between adjacent wires is a little more than the outside diameter of the core that is used in the matrix. Figure 13 is a diagram of a recently designed matrix of maximum density.

Disturbance Due to Cores. Minor loop disturbances due to the selected X and Y wires have been discussed previously. Disturbances of a secondary order on a large number of other X and Y lines also arise because the switches are not perfect. The sense winding must be wound in such a manner that cancellation occurs repeatedly over very short sections of the winding.

Magnetic Pick-up. The sense winding must be wound so that its

net area is zero or nearly zero. This means that the input and output must be at the same point. Furthermore, any wire which has a component of direction parallel to the X or Y wires must have in close proximity to it a wire which travels in the opposite direction and which has the same components with regard to the X and Y wires. The process is somewhat analogous to the methods used in non-inductively winding high-quality wire-wound resistors and register cards.

Electrostatic Pick-up. This is one of the most troublesome of all types of disturbance. Because the capacitance between the sense winding and the X and Y wires is large, it is difficult to prevent the sense winding from moving with the X and Y wires. A correctly designed sense winding moves in such a fashion that no net voltage appears across the two sense winding output wires even though the whole sense winding may move through a considerable excursion. This must be true regardless of which X and Y wires are selected. Information is coupled out of the sense winding either by means of a difference amplifier or by a balanced transformer. Investigation has shown that most of the disturbance in a matrix is due to electrostatic pick-up. Improvements in the ONE/ZERO ratio by as much as 3 or 4 to 1 have been achieved by apparently minor alterations to the sense winding. The best solutions to this problem have been obtained by balancing the electrostatic pick-up in a symmetrical manner around the center of the winding. This balance must be maintained for all combinations of X and Y selections.

The principles of operation for two popular types of sense winding are described below.

Sense Winding - X and Y Pulses Are Simultaneous. Figure 14 is a diagram of a small sense winding of this type. The arrows on the X and Y lines show the manner in which these wires are driven with respect to each other to produce the same action. The signs against the cores show the polarity of the linkages of the sense winding. Moving from the center of the sense winding towards either A or B, the same pattern of polarities is encountered and the winding is symmetrical about the center. Consider that line X_0 is excited. Moving from C towards A, the excited linkages induce $-v_e$, $+v_e$ and cancellation occurs. Moving from C towards B, the same pattern is encountered. Consider that line Y_0 is excited. Moving from C to A or from C to B, the excited linkages induce $+v_e$, $-v_e$ and cancellation occurs. Complete analysis of the sense winding carried out by this
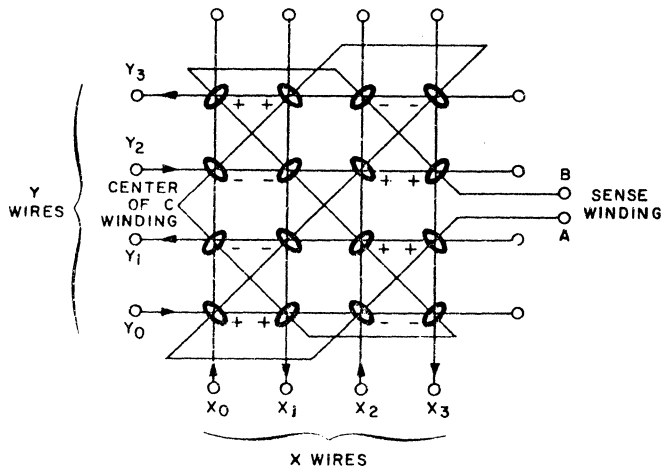
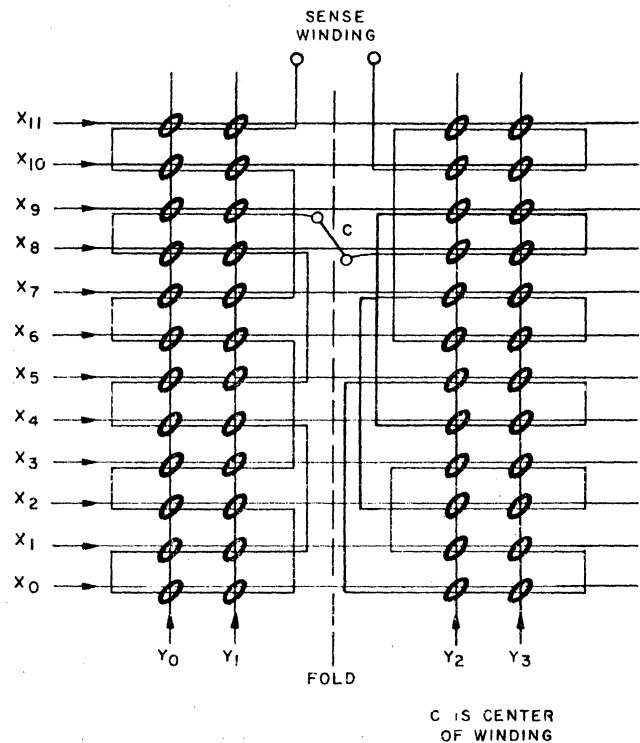Figure 14. Sense winding used when X and Y pulses are simultaneous.

Figure 15. Sense winding used when X pulse commences before Y pulse.

method will indicate that cancellation is always adequate.

Sense Winding - X Pulse Commences before Y Pulse. Sometimes a high ONE/ZERO ratio is required, and slightly slower operation may be permitted to achieve this improvement. In such cases the X pulse commences about 1 microsecond ahead of the Y pulse. The sense winding is designed to minimize the disturbance due to the Y pulse at the expense of increased disturbance due to the X pulse. The reading signal is gated and does not commence until just after the Y pulse has commenced. Use of this technique with a sense winding has made it possible to achieve ONE/ZERO ratios of 30/1 in large matrices.

Figure 15 is a diagram of a small winding shown as a flat plane. This winding is usually employed in folded rectangular matrices. Y disturbances in the winding are cancelled out every

time the sense winding links a Y line for the second time. X disturbances can be cancelled by bucking one half of the X line against the other half. There is a minimum of electrostatic pick-up with respect to the Y line and a maximum with respect to the X line. The winding has mechanical advantages in that the sense winding is parallel to the X line and is therefore easy to thread through the cores.

Characteristics of the Sense-Winding Output Signal. Figure 16 shows some characteristic waveforms from a single core. The disturb signals are cancelled in the sense winding, but each signal is delayed slightly with respect to the next. The result is that complete cancellation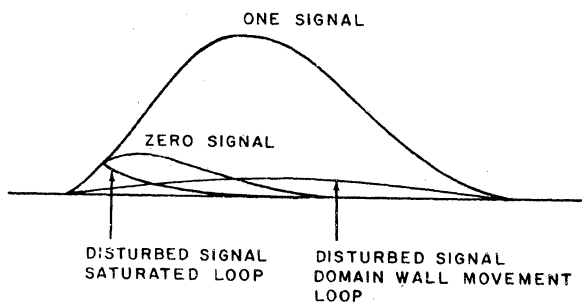 does not occur even with a very good sense winding. The same type of delayed action occurs in magnetic and electrostatic pick-up. The resulting output signal contains the following components:

Figure 16. Characteristic waveforms of output signals of a single core.

(1) A large voltage excursion of the whole winding due to electrostatic pick-up.

(2) A ONE or ZERO signal plus any uncancelled disturbed signals on an area basis.

(3) A burst of high frequency of amplitude much greater than the ONE signal due to lack of cancellation of disturbances in time.

Component (1) can be rejected by a difference amplifier or by a transformer or, in some cases, by both. Component (2) is the actual reading signal which must be utilized by the equipment component. Component (3) can be rejected by means of a simple low-pass filter. This filter is usually arranged to cut off at a frequency which is just high enough to allow reasonably small distortion of the ONE signal.

SWITCHES AND SWITCHING TECHNIQUES

PRINCIPLES OF MAGNETIC SWITCH OPERATION

When magnetic core switches are used to drive the selection wires of a coincident-current matrix, the switches are usually arranged as small matrices which, in turn, are driven by an anti-coincident form of drive rather than the coincident-current form. Consider the circuit shown in Figure 17 and the operating loop shown in Figure 18. A current producing mmf AD is applied to drive
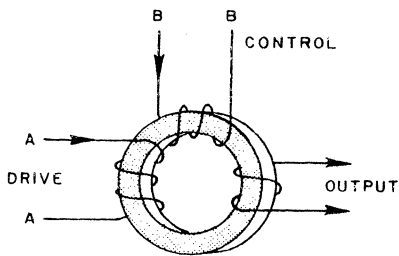

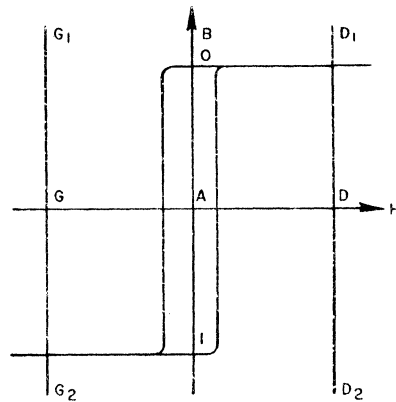Figure 17. Magnetic core switch circuit.

Figure 18. Operating loop for magnetic core switch.

winding AA. A control current producing mmf AG is applied to control winding BB. Let GA=AD and let the core be in the ONE state. If the control winding is energized before the drive winding, there will be very little flux change and virtually no output will appear. If only the drive winding is energized, there will be a large flux change and the mmf, which is included between the line D_1DD_2 and the hysteresis loop, will be available to the load at the output winding. The core is reset by reversing the current in the drive winding to produce mmf AG. An output which is of opposite polarity to the original output will be produced.

A matrix of switch cores may be wound so that one of m.n outputs is operated by the simultaneous driving of one of m wires and n - 1 of n wires. This principle can be extended to any number of coincidences. Table 25 indicates the number of drivers required

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for various matrix sizes when all the co-ordinates of the matrix
are driven by switches.

Table 25. Number of Drivers for Various Matrix Sizes

Number of Cores in the Matrix	Double Coincidence Matrix			Triple Coincidence Matrix		
	Number of Switches	Coincidence in Switch		Number of Switches	Coincidence in Switch	
		Double	Triple		Double	Triple
64	16	12	12	12	12	Not Possible
4,096	128	32	24	48	24	24
262,144	1,024	96	48	192	48	36
1,000,000	2,000	130	60	300	60	42

The following facts may be noted from this table:

(1) A double-coincidence matrix driven by triple-coin-
cidence switches requires the same number of drivers
as a triple-coincidence matrix driven by double-
coincidence switches.

(2) The triple-coincidence matrix driven by triple-coin-
cidence switches does not employ many less drivers
than a double-coincidence matrix driven by triple-
coincidence switches.

MAGNETIC CORE SWITCHES

Magnetic core switches provide a means of driving the large
number of selection wires associated with the storage matrices
from a reasonable number of electronic drivers. They replace
what would otherwise consist of two drivers per matrix line plus
a large tree of diode logic used for decoding purposes. In this
sense they represent the first use of cores as a logical element.
Switches have been designed to replace diode adders and to per-
form other logical functions; they are likely to find extensive
logical use when computers are designed around the use of magnetic
components.

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A simple switch and the cores associated with it act as a transformer. Consider, for example, a multiple-winding transformer which has a core of rectangular material. There are two primary windings and one secondary winding. A small signal may be applied to one of the primary windings and a control current to the other. When the control winding maintains the core in the saturated region of the operating loop, there will be virtually no output in the secondary winding. As the control current is altered, there will be no output due to the signal until a signal, control-current relationship has been established which allows the signal to operate beyond the knee of the curve into the high permeability region. There will be an output as the control current is changed because the saturation characteristics are not completely flat. To prevent this unwanted secondary signal, a switch core material having a ratio of remanent flux density (B_r) to saturated flux density (B_s) as close to unity as possible is most desirable. Materials having a B_r/B_s ratio of less than 0.9 are not usually desirable; the best materials have a ratio of at least 0.95. When the signal is in the region of very high permeability, the transformer is almost perfect in its characteristics; but when it is in the region of decreasing permeability, the transformer becomes more and more imperfect until the signal is again in the saturated region. In the best switch core materials the amount of total flux change in the region of decreasing permeability is small and the rate of change of permeability is very large. For a given flux output, the total area of the loop should be as small as possible to keep eddy current and other dynamic losses to a minimum. This is particularly important in switch cores because their average power transmission is relatively large.

Switches are normally driven by flat-topped current pulses. Switch cores in the normal state are in a saturated region such as state 1 in Figure 18. If the net ampere-turns applied to the switch core leave it at state 1 or take it towards G_2, the switch core will not produce an output. On the other hand, an output is produced if the net ampere-turns take the core beyond the knee of the curve towards D_2.

When the switch core is in the operating state, it acts as a current transformer in which the output current is equal to the current available between line D_1DD_2 and the hysteresis loop. The magnetizing ampere-turns vary between H_k and H_t as the switch operates. If H_i is the input ampere-turns and H_o is the output

ampere-turns, they can be expressed in terms of limits such that $H_i - H_t \lesssim H_o \lesssim H_i - H_k$.

In most cases it is desired to achieve a pulse of a given "flatness" from the output winding. As an example, let $H_t = 1.75$ H_k and let the output pulse droop by 5 per cent at the top. Let $H_i = nH_k$.

Then

$$nH_k - 1.75H_k \lesssim H_o \lesssim nH_k - H_k$$

$$(n-1.75)\ H_k \lesssim H_o \leq (n-1)\ H_k$$

But H_o at the lower limit is 0.95 times its value at the upper limit. Hence n = 16. To achieve this high value of n, the number of ampere-turns on both primary and secondary windings would be large and, as a direct corollary, the number of turns would be large. This would tend to produce a physically large and inductive switch which would be difficult to drive. Therefore, switches are often operated over only a part of the loop in order to keep the variation of magnetizing current to a minimum. In most core material $H_c = 1.1\ H_k$, and if the core is used over half its characteristic, then n = 3. Switches are rarely constructed with n greater than 6 and have been constructed of exceptionally good materials with n as low as 2.

A driver which is driving a magnetic switch has as its load one switch core which is acting as a transformer and a number of other switch cores which are in a saturated state. The driver must maintain constant-current conditions into this inductive load. Consider the effect of the saturated cores alone since in most cases the voltage drop due to the operating core is trivial. If i is the driver peak current, N is the number of primary turns, k is the factor which depends on the time of rise of the current, on the cross-section area of the switch core, and on the saturated permeability of the loop; and if there are m saturated switch cores, then the voltage drop (V) will be kiN^2m. For a given output the ampere-turns iN must be constant. Therefore, any attempt to reduce i is accompanied by a rapid increase in V. H_i is proportional to iN. H_k for a given core is fixed. Therefore, if it is desired to increase n, then iN must be increased. The following relationships govern the design of switches once a core size and material have been chosen.

$$V \propto \frac{1}{i} \quad \text{when "n" is constant}$$

$$V \propto N^2 \quad \text{when "i" and "n" are constant}$$

$$V \propto n^2 \quad \text{when "i" is constant}$$

Actually these equations do not imply the complete relationships. In order to keep the voltage drop in a switch low, the cores of minimum diameter are employed to keep the magnetizing current to a minimum. An increase in N in most cases represents an increase in the size of the core and a constant increase in the desired iN. Therefore, if the core size is also considered, the above relationships are altered. For normal switch sizes the following relationships are true on an empirical basis.

$$V \propto \frac{1}{i^x} \quad \text{when "n" is constant and } 1.5 < x < 2$$

$$V \propto N^3 \quad \text{when "i" and "n" are constant}$$

$$V \propto n^3 \quad \text{when "i" is constant}$$

Designing a switch involves a difficult compromise between adequate performance and reasonable driving voltage and current.

An ever-present problem in system design is how many coincidences may be utilized in a switch. The initial tendency is to choose the design which requires the least number of drivers. However, a reduction in the number of drivers necessitates a disproportionate increase in the size of the drivers and, consequently, system efficiency decreases.

Switch wiring diagrams can become so complex that it is necessary to employ special symbols to describe them. Figure 19 shows the basic symbols and defines their meaning. The output windings are frequently omitted in the diagrams because, except in unusual circumstances, every switch core provides one output.

Behavior of Minor Loops in Switch Cores. Figure 20 shows a typical action in a switch core. The core is initially at point A, which is on the major loop. It is then driven to point B by means of a drive pulse. The drive is removed, and the core settles to point C. A reverse drive is then applied which is removed at point D and the core settles to point E. In a normal switch there is a high probability that the core will receive subsequent reverse drive pulses which produce loops such as EFG and may ultimately settle to A, but the next action after the core is set at E may be

THE
MAGNETIC → CORE

OUTPUT WINDING
→ IF SHOWN

WINDING WHICH DOES
NOT LINK THE CORES

WINDING WHICH LINKS THE
CORE WITH ONE UNIT OF MMF
IN THE DRIVE DIRECTION

WINDING WHICH LINKS THE CORE
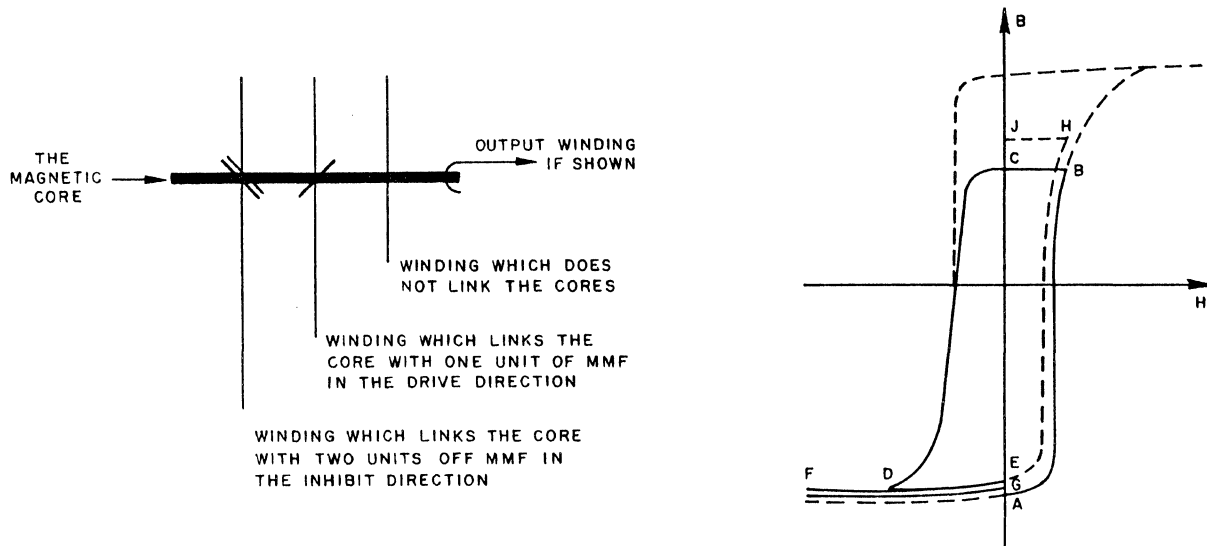WITH TWO UNITS OFF MMF IN
THE INHIBIT DIRECTION

Figure 19. Symbols used in switch
wiring diagrams.

Figure 20. Typical action of a
switch core on a hysteresis loop.

a drive action. During this action the core is on a minor loop
which is narrower than the original loop and a little more current
will be available to the load, resulting in a slightly higher flux
transference from the core to the load. The core will move to H
and, on release of the drive, to J. The flux CJ will be greater
than the flux AE. This action is cumulative, and the operating
loop will move until it is centered around the origin. In practice
the core receives a mixed sequence of forward and reverse drive
pulses; its behavior depends upon the immediate past history.
Because the core drifts from giving a relatively small output to a
relatively large output, extremely poor operation of the storage
matrices results. To overcome this, the reverse drive imposed
from C to D is usually maintained for a longer time than the drive
from A to B. The core will still move from the major loop, but by
only a small amount. The exact amount by which the duration of the
reverse drive pulse should exceed the duration of the drive pulse
is a matter of experiment since it is a function of material, load,
and drive characteristics. In some systems all the switch inhibit
drivers are operated during some portion of the cycle with the same
effect as the lengthened reset pulse.

An ideal method for minimizing loop drift is to ensure that the switch core is always driven from one point of saturation to another. Switches which employ operation from one state of saturation to another usually require auxiliary equipment for stabilizing either the voltage output from the switch or the current output from the switch or, in some cases, both.

Binary Switches. Binary switches are probably the most elegant of all switch designs. An eight-way version is shown in Figure 21. The switch decodes a binary number which is expressed as 2^q, 2^{q-1}, $--2^0$ into 2^{q+1} combinations. The switch is driven by q+1 pairs of drivers, in which one driver of the pair operates
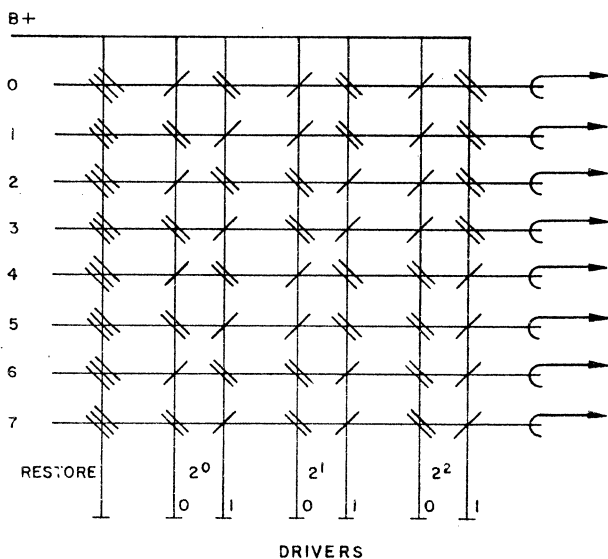

Figure 21. Eight-way binary switch.

Figure 22. Two-out-of-five code binary switch.

for a ZERO and the other for a ONE. A drive winding provides one unit of mmf and an inhibit winding q units. All activated drivers combine to provide the drive current. Restoration is effected by a separate restoration winding which provides q+1 units of mmf. The selected core has q+1 units of drive. Those cores whose address differs by one digit from the selected number have ZERO drive and those whose

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address differs by two digits have - (q+1) units. Therefore, only the selected core provides an output.

Each core is linked by a number of wires proportio.ial to (q+1).(q+2) and provides q+1 output. The number of turns per core and the load on each driver rise very rapidly as q is increased. The switch relies on coincidence of the driving currents at all points in the switch; but this is difficult to achieve because each driving line acts as a delay line in which the delay at any point in the line is a function of the number of turns up to that point. For these reasons, the switch is useful only in small sizes.

The binary switch has the unusual feature that all the activated drivers combine to provide the output. With certain types of redundant code this feature can lead to improved operation. An example is the two-out-of-five code switch illustrated in Figure 22. In this switch only those drivers corresponding to a ONE are driven. It is also possible to design single-ended binary switches, but these are less efficient than the push-pull version described above.

Switches which fully utilize the combinatorial advantages of cores are almost useless in storage units, but they provide the basis on which functions such as addition can be mechanized. In such applications there is no requirement that the switch should be efficient or that the output waveform should be well shaped. Quite large switches can be used to perform complicated functions.

Switches in which Only One Driver Contributes to the Output Current. Consider a core which has four primary windings and one secondary winding. Let all the primary windings be fed with equal numbers of ampere-turns. Let one winding, A, be in the drive direction and the other windings, B, C, and D, be in the inhibit direction. Then an output is obtained if A, and not (B or C or D). This operation is fundamental to all switches of this type. The only amplitude requirement is that the mmf fed to B, C, or D is never less than that fed to A. Because of this type of operation, these switches are often called anti-coincidence switches.

Figure 23 shows an eight-way binary switch of this type. If the same terms are used as were employed in the previous binary switch, then there are 2^{q+1} outputs as a result of 2(q+1) drivers. The 2^0 driver pair acts as the drivers; the others act as inhibitors. The drive to the selected core is one unit, to the next selected is zero, and to the remaining is negative. Restoration
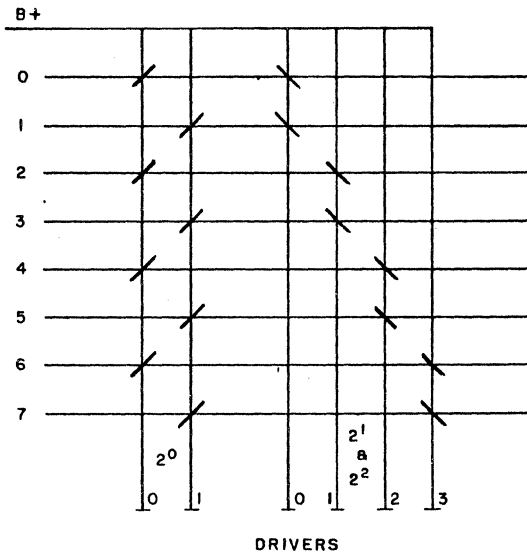
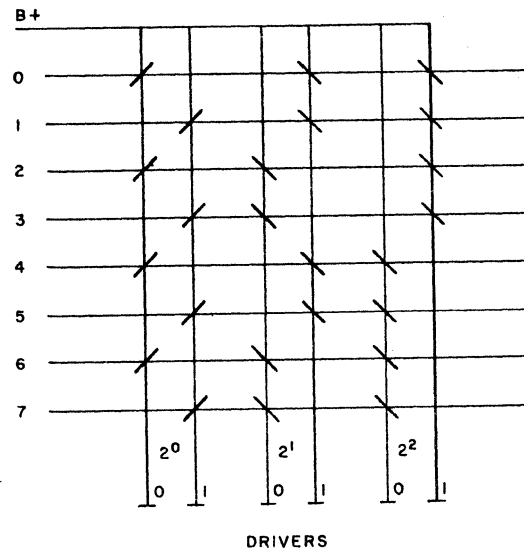Figure 23. Eight-way anti-coincident binary switch.

Figure 24. Eight-way triple-coincidence switch.

is effected by causing both drivers of one of the inhibit driver pairs to conduct. A separate restoration winding can be used if desired. The number of turns per core is proportional to $q+1$ and the output is one. In this respect, the switch utilizes wire no more efficiently than did the original binary switch.

There is no difficulty in achieving coincidence in a large switch of this type. In practice, double coincidence or, at most, triple coincidence is employed. An eight-way switch of this type is illustrated in Figure 24. In this case, the 2^1 and 2^2 bits are decoded; and the three drivers which are not selected, as a result of decoding, are allowed to conduct.

The number of wires per core increases with switch size. The number of ampere-turns driven by a driver increases as $\dfrac{q+1}{2}$, which

is an improvement on the pure binary switches. If there is triple concidence, then the ampere-turns driven by a driver increases as $\frac{2}{3}$ (q+t). As a generalization the driven ampere-turns for a n-way coincidence increase as $\frac{2^{n-1}}{2^n}$ (q+1). It can be seen in Table 26 that as n is increased the switch approaches the efficiency of the binary switch rather rapidly. Therefore, double coincidence is usually employed.

Table 26. Number of Drivers for Binary, Double-coincidence, and Triple-Coincidence Switch Operation

Number of Positions in the Switch	Number of Drivers for Binary	Number of Drivers of Relative Size 1 for Double Coincidence	Number of Drivers for Triple Coincidence	Relative Driver Size	Drivers Times Size
16	8	8	8	1	8
64	12	16	12	2	24
128	14	24	16	2	32
256	16	32	20	4	80
512	18	48	24	2	48
1,024	20	64	32	4	128

In order to obtain the relative driver size, the largest load in the triple-coincidence switch was compared to the largest load in the double-coincident switch. It should be noted that the number of drivers used for triple coincidence rises rather slowly with respect to the number of drivers for pure binary, while the number of drivers for double coincidence rises rapidly. In most cases the total power required is greater in triple-coincidence operation than in double-coincidence operation. Certain switches which are a cube, such as 512 or 1,000, are efficient under triple-coincidence conditions.

It is possible to construct and operate switches of this type on somewhat different principles. A winding links all cores of the

switch in the inhibit direction. This winding is dc driven by a precise, high-impedance, constant-current driver. Usually the winding has few turns and the current flowing in it is high. In an n-1 coincidence switch the ampere-turns provided by this winding to each core must be exactly n-1 times the ampere-turns provided by any selection driver. The selection windings link the switch in a conventional manner except that they are all in the drive direction. One driver is operated in each set to select the switch core. For example, in a double-coincidence 64-way switch there would be two sets of eight drivers and the dc constant-current driver. If A is the ampere-turns provided by any driver, then initially the drive to all the cores will be -A. The two selected drivers will provide a total of 2A. The resultant drive to the selected core is +A. The drive to the cores on the selected lines is zero and to all other cores is -A.

To operate the switch both selected drivers are energized simultaneously and then a reset pulse is applied to all the cores by removing both drivers together. The switch has the advantage that the logic required to control it is simple. It has the following disadvantages:

(1) The dc current flowing in the common winding must not change when the selection drivers are operated. If it does change, the winding acts as a shorted turn and removes mmf from the drive. Therefore, the constant-current source to this winding must be of high impedance. In addition, the voltage induced in the winding by the selection action must be small. If it is not, the capacitance associated with the winding will reduce the driving impedance. Therefore, the winding itself must be a low-impedance, high-current winding, driven from a high-impedance, low-capacitance source.

(2) The dc current flowing in the common winding provides the reset mmf. If A is the mmf applied to the core on set, then a value B, which is greater than A, must be applied on reset, because the switch core moves from H_k to H_c on set and from H_c to H_t on reset. Therefore, the dc current must be adjusted to the value B, and the drivers adjusted to a value of $\frac{1}{2}(A + B)$.

(3) The tolerance of the selection and bias currents must be small because the three currents are involved in any set action. In a normal switch, only one current is involved in a set action. The drivers employed to drive this switch must be much more precise than those that are required in a normal switch. In practice it is usually found that only one half or one third of the tolerance is permitted for drivers used in conjunction with switches of this type.

(4) Leading and trailing edges of the drive pulses must be controlled with care. The leading edge defines the set pulse, while the trailing edge defines the reset pulse. Therefore, the drivers must be specially designed to provide the correct pulse shape. In a normal switch the leading edge is controlled, but the trailing edge is simply allowed to fall smoothly without any particular control.

This switch has another distinct advantage apart from its logical simplicity. Because the switch cores are reset at all times except during an actual set action, the tendency towards an operating loop shift is small. This is particularly important during very fast cycles. A short reset action will occur at some time in every cycle, which tends to stabilize the operation of the switch.

Unidirectional Switches--Diodes in the Secondary Circuit. The magnetic switches described above produce bidirectional signals at the output, effect impedance matching, and introduce some combinatorial advantage. The last two features are always advantageous, but the production of bidirectional signals can be as much of a disadvantage as it is an advantage. If a bidirectional signal is produced from a normal switch, the cycle and mode of operation must be based on a two-beat principle, which may be an undesirable restriction. For this reason, there has been considerable interest in producing unidirectional switches.

One way of obtaining a unidirectional output is to drive the switch with a large current in order to obtain a pulse in the output winding and then to reset the switch very slowly so that essentially no current is obtained from the output winding. This mode of operation has been used successfully in a number of storage devices. In some devices the current produced at the secondary of the switch due to resetting the switch core has been maintained as significantly less than half of the switching current in the matrices. During reset a current flows in the matrices, but it is too small to affect the stored information. A considerable time is expended in resetting the switches in this type of operation; therefore, it is applicable only to memory units in which the cycle time is long.

A second method of using conventional switches to provide an effectively unidirectional output is to reduce the reset drive to a point where the current from the secondary during reset is about half the value of the current from the secondary during set. This mode of operation has been used successfully to implement the drive operation in linear-selection or word-selection memory devices.

Memory devices of this type frequently require about half the driving current during the write part of the cycle. This mode of switch operation will produce a large short pulse during the set operation and a long, small-amplitude pulse during reset.

Another way of obtaining unidirectional operation of a switch is to insert a diode in each secondary circuit. Under these conditions, current can flow from the switch core into the matrix in one direction only. The diode is highly reliable in this mode of operation. The voltages occuring in the secondary of the switch core can be very low and the diode does not require a large back resistance at any time in its life. The introduction of an electronic element will, of course, reduce the reliability of the magnetics; but it has been found that diodes used in this mode can be considered almost as reliable as the cores themselves.

A switch utilizing diodes in the secondaries has unique properties. Power will be transferred from the primary winding to the secondary winding when the diode is able to conduct; but if the primary current is in a direction such that the diode in the secondary cannot conduct, power cannot be transferred to the secondary winding, and all the power in the primary must be used in switching the core and overcoming losses in the core. Therefore, the introduction of the diode introduces properties beyond that of unidirectional operation of the switch. It is possible to set the core, using very low primary power and no power output from the secondary, and later to reset the core, transferring power from the primary to the secondary. The converse operation is also possible: power can be transferred from primary to secondary during the set operation, and later the core can be reset, using low primary power, without loss of speed. Unidirectional operation implies loss of time somewhere in the system because it is necessary either to set or to reset the core without output. In most systems using unidirectional operation, an overlapping type of cycle is adopted so that one core is being set or reset while another core is performing the opposite function. By this means time loss is limited to the small amount of time in setting the switch into an initial state or clearing it into a final state at the beginning and end of long major operations.

The basic operation of an element of a unidirectional switch is illustrated in Figure 25. A simple switch, shown in Figure 25(a), consists of a transformer using a non-linear core. A single drive winding has been shown, but ordinarily several windings are used in order to obtain combinatorial advantage. The basic element of the
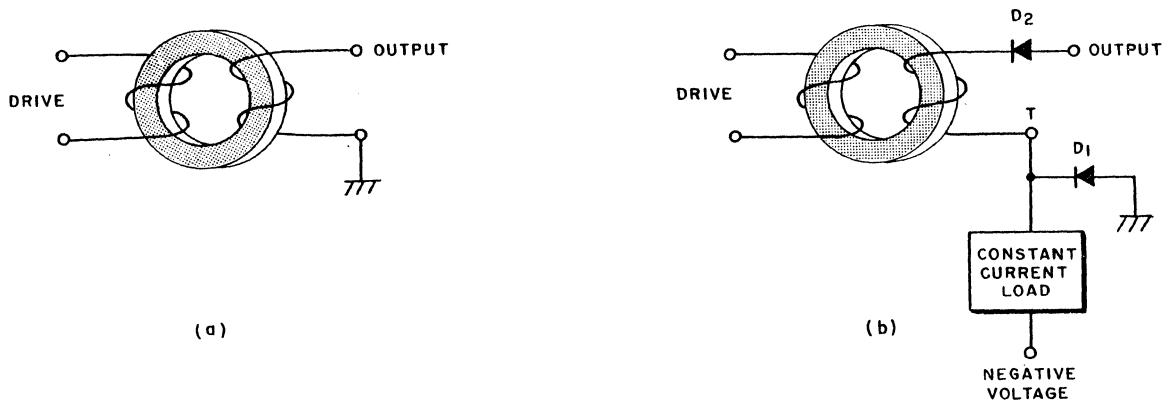
Figure 25. (a) Simple transformer switch core. (b) Basic element of a unidirectional switch.

unidirectional switch is shown in Figure 25 (b). This consists of the same transformer with the addition of a diode in the output circuit and, in series with the output circuit, a constant-current load. The output circuit is shown connected to a terminal T, because in switches of this type a constant-current load with an associated diode can be used in common to all elements of the system. Normally, current flows through the constant-current load through diode D_1 to ground. If a drive current is applied to the core to set it so that diode D_2 does not conduct, no current flows in the secondary circuit and a small amount of power is used in setting the switch core. If the core is now reset by applying a large current of the opposite polarity to the drive winding, diode D_2 can conduct. Current through this diode must be drawn from terminal T. It is usually drawn as the result of the secondary winding lifting terminal T above ground so that diode D_1 is cut off and the constant-current load is inserted as part of the load of the secondary of the switch core. This has the effect of defining the current that may flow in the secondary of this core precisely.

The addition of the diode to the secondary circuit has created a circuit in which unidirectional current flows at the output, in which very low power is required either to set or reset switch cores, and in which a constant-current load may

be inserted in the secondary so that the current flowing in the output circuit is regulated to a high degree. This last feature is important in designing core memories. A switch of this type allows the designer to attain large combinatorial advantages and, at the same time, to route extremely precise currents into the storage elements themselves.

The BH loops describing the operation of the core are shown in Figure 26. Loop (a), the conventional square loop used by a switch core, defines the operation of the circuit shown in Figure 25(a).
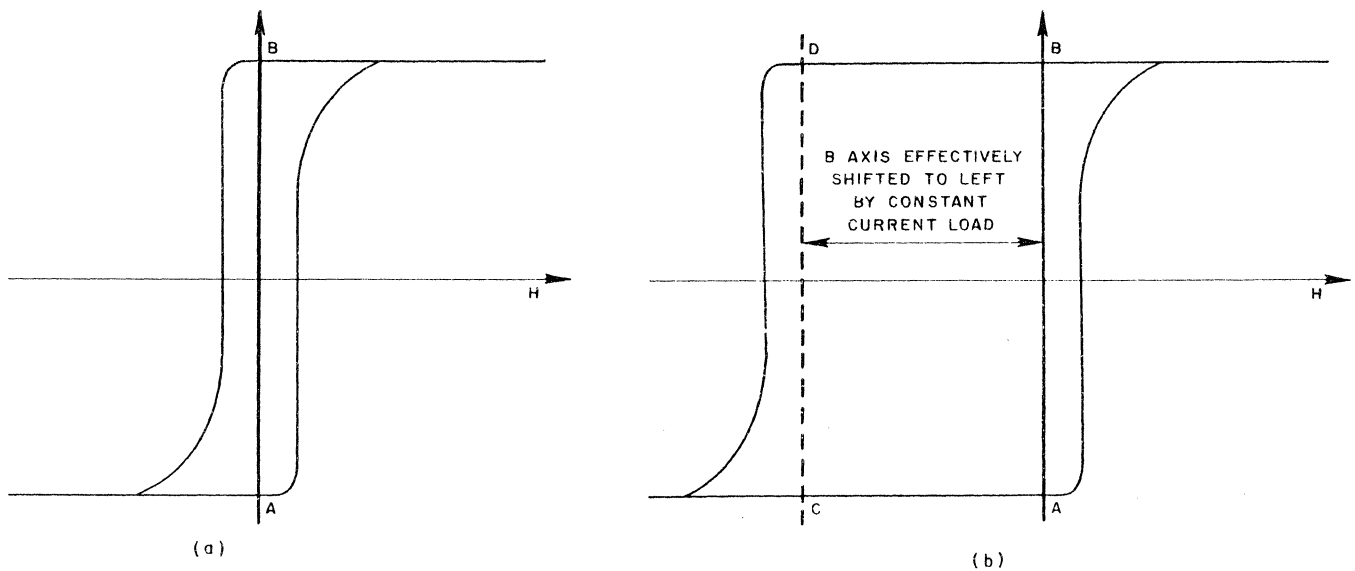

Figure 26. (a) Hysteresis loop of simple switch core shown in Figure 25 (a). (b) Effective loop used by switch shown in Figure 25 (b).

If the current corresponding to H is greater than is required to satisfy the loop, the excess current during either set or reset is transferred into the output winding. The loop used by the circuit in Figure 25 (b) is shown in Figure 26 (b). During the set action, in which the core moves from point A to point B, the current supplied by the primary circuit need be only enough to move the core through this excursion. It is not possible to transfer any excess current into the output circuit; and if excess primary current is provided, it will result in additional core losses and more rapid transition from A to B. During reset, however, the amount of current BD or AC must be provided before adequate current is available for switching the core. This current is defined by the constant-current load. The current provided to the primary will be distributed as BD into the secondary circuit, and any excess current above this amount will be used to switch the core and also to

overcome losses in the core. A small amount of excess primary current will produce a much faster switching action of the core.

Because the constant current in the secondary is unidirectional, the constant-current load may feed a large number of secondary output circuits, provided that only one of these circuits is selected at a time. Under these conditions, the current flowing in the matrix is independent of switch characteristics. An eight-way switch operated with such a current arrangement is shown in Figure 27. The switch is set by any of the conventional methods to store the address in the selected core. No power is transferred from the set winding to the output winding because the diodes block any flow of current. The current required to set the switch need be only sufficient to provide the customary tip ampere-turns. Therefore, the inductance of the windings may be very low, and comparatively low-powered circuits may be used for set drivers.

When it is required to produce an output from the switch, the single high-power reset driver is operated and the selected
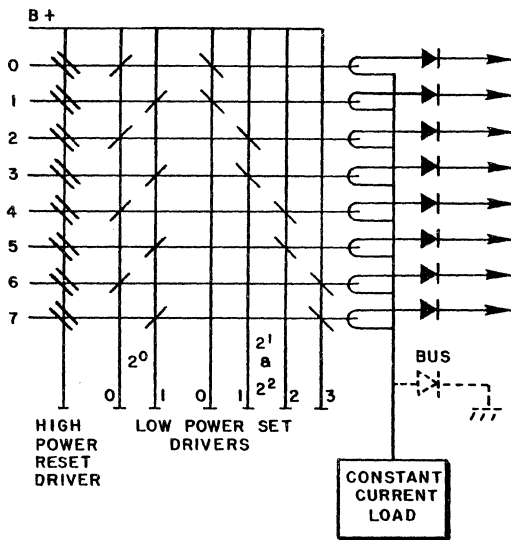
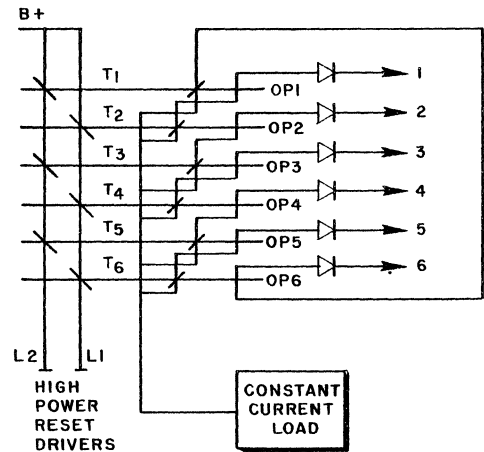

Figure 27. Eight-way unidirectional switch.

Figure 28. Switch in which output of a core sets next core in sequence.

core is restored to its normal state. The constant-current load may be either a pulsed or a dc source; if it is the latter, a diode may be connected to the bus as illustrated to carry the

current in the quiescent state. When the selected core is operated, the bus is depressed to cut off all the unselected diodes and current flows only in the selected line. It should be noted that the reset driver is really a constant-current load which absorbs power from the selected core. While the driver is supplying current to the output circuit, the core acts as a transformer. In large switches the extra diode on the bus is not required because the quiescent current is shared equally by all the output lines. The current in each line will be so small that it will introduce no adverse effects on the performance of the storage unit. Before deciding whether to use a diode, it is important to perform adequate end-of-life computations on the behavior of the diodes in the switch. It is possible for all the diodes to have deteriorated considerably in regard to forward resistance and for one of the diodes to have failed and been replaced by a new diode. This worst-case computation should be performed to ensure that a large proportion of the constant current is not being routed through one of the matrix lines.

The current relationships in the switch are rather complex because the cores are essentially current transformers feeding into a constant-current load. The mmf supplied by the reset winding must be equal to the output ampere-turns plus the magnetizing mmf plus an mmf absorbed as core losses. If either the driving current or the constant current alters, the new difference must be taken up almost entirely as an alteration of the core losses. In a highly efficient transformer, the losses are low and a small change in either of the currents may produce a large change in the losses. Losses are always associated with the switching time of the core. A small increase in driving current can decrease the switching time and increase the voltage output. The excess voltage is taken up by the bus, but the reduced length of the output pulse presents a serious problem. Consequently, the two drivers must be very precise and, if they change, must change together. There is an effective way of solving this problem in small switches. The reset driver lines are connected to the constant-current bus in place of the constant-current driver. The drive current is then equal to the matrix current, the difference between driver and output ampere-turns is fixed, and the switch is stable.

In Figure 26 (b) the current relationships illustrated are approximately to scale for a typical switch. Considerably more mmf is available at the output of the switch core than is needed either to set or to reset the core. The switch behaves to an extent as a magnetic amplifier and exhibits power gain. This makes it possible to set one switch core from another and still retain enough power

to do useful work in the storage arrays. A switch utilizing this principle is shown in Figure 28. Two reset drivers (L_1 and L_2) are operated alternately. Suppose core T_1 is set. The reset driver (L_2) is operated, and the core produces an output which drives the load and also sets core T_2. The other driver then operates to produce an output from core T_2 and set core T_3. The switch then acts as a counter and can be used to mechanize complex logic. The power gain in such a system is usually between six and ten.

In an actual sequential switch like that in Figure 28, lines L_1 and L_2 do not return directly to B+. Instead the drivers are driven from B-,and the lines ultimately return to ground. When line L_2 has passed through cores T_5, T_3, and T_1, it then is returned at the bus for output windings OP_1, OP_3, and OP_5. Similarly, line L_1 links cores T_2, T_4, and T_6, and then becomes the bus for output windings OP_2, OP_4, and OP_6. Ultimately these lines return to ground after they have passed through the matrices.

A more conventional diagram of a switch is Figure 29, which shows how the drive lines are brought around to become the buses for the output windings and, also, shows a clear winding. The clear winding links core T6 in the opposite direction to that employed in all the other cores and it also links T_6 with more mmf than is used for the other cores. In this particular switch, T_6 is considered to be the ZERO or initial value of the address which is being defined by the switch.

Figure 30 is an actual circuit diagram of a complete 28-way shifting switch, which is used to operate a storage unit at a 100 kc rate. The accented line starting at input 1 indicates the path followed by the current when the switch is operated immediately after a clear operation. This current passes down through the primary reset windings of all even-numbered transformers and is then steered by means of a switch action through the output circuit of transformer 28. The current continues through the set winding of transformer T_1 and is then routed from that position to X line 1 in the storage matrices. The next drive action will be used to energize input 2. The current in this case will pass through the primary reset winding of all the odd-numbered transformers, will return down the bus, and will be routed by the output winding of transformer T_1 through the set winding of transformer T_2 to X line 2. This action will continue as long as currents are applied to inputs 1 and 2 alternately.

Unidirectional Switches--Transistors in the Secondary Circuit.
Transistors capable of handling the same peak currents as diodes are now being used for switching purposes. It is possible to modify
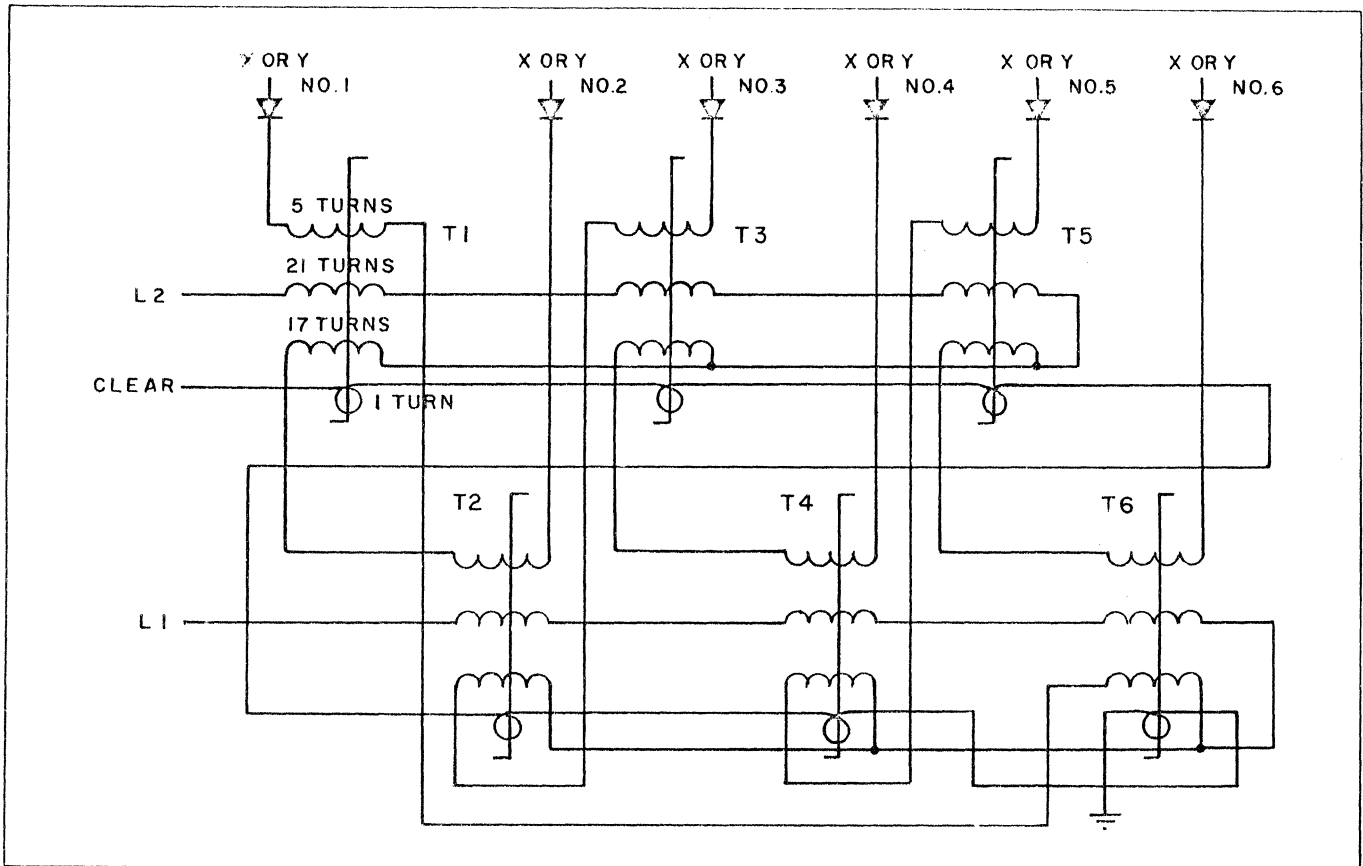
Figure 29. Conventional diagram of a sequential unidirectional switch.

unidirectional switches so that the base emitter portion of a transistor replaces the diode. Several advantages result because the output is taken from the collector circuit. First, the output from the collector is at much higher impedance than is available in the base emitter circuit. The transistor therefore acts as an impedance amplifier, providing a very high output impedance into the matrices. Secondly, the switch cores are providing only the power necessary to drive the base emitter circuit and not the power necessary to drive the matrices. Therefore very small cores of storage-core size may be used for the switching operation. This, in turn, increases the number of cores which may be driven by a single set of drivers. Large switches incorporating the base emitter portions of transistors can be manufactured. Since the output from the transis-
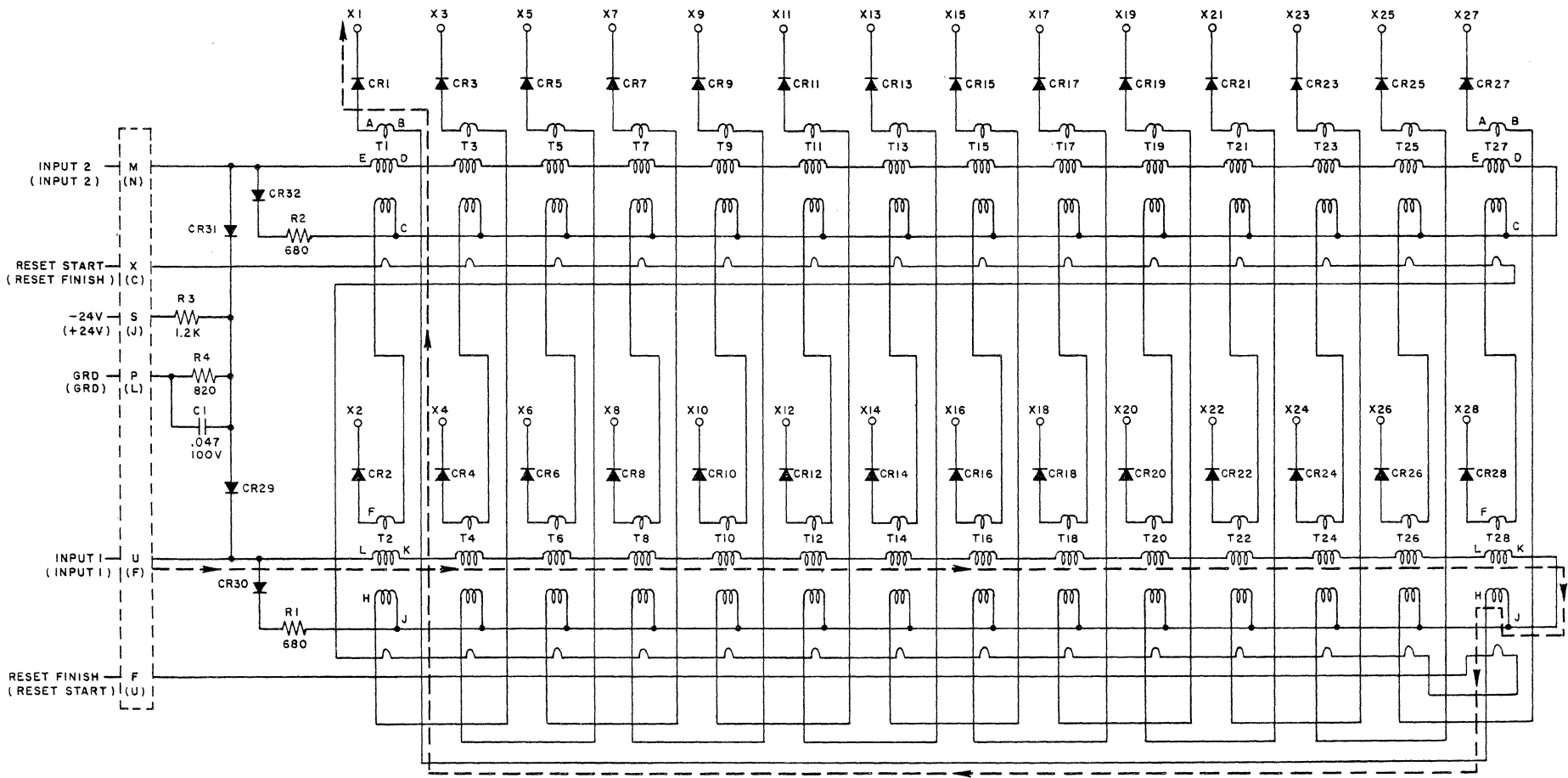
Figure 30. Twenty-eight-way shifting switch.

tors is not only at high impedance but can also tolerate very large voltage swings, it is possible for these large switches to drive large matrix arrays. Such switches are useful in the construction of large, sequentially addressed storage systems.

A transistor switch can be arranged to count either in a forward or a reverse direction by energizing the appropriate winding in the switch. Figure 31 is a diagram of such a switch. It is used to drive the 120 X lines in a memory system and to scan these X lines either in a forward or reverse direction as required. The reversible switch steers current to the 120 X lines of the storage array, selecting each line sequentially in either an ascending or descending order. It consists of 121 ferrite cores, each of which controls the operation of a transistor which, in turn, controls the flow of current through one of the 120 X lines. The emitter of the transistor associated with the 121st core is grounded. The function of this extra core is to start the reverse count if 120 words have been loaded. Each core is linked by six windings, five of them with six turns, and one with 12 turns. As shown in Figure 31, the five 6-turn windings include the clear windings, two drive windings, and the forward and reverse count windings. The 12-turn winding, which is connected between the emitter and base of the transistor, drives the transistor. Windings are arranged to saturate the transistor when the core is reset. At all other times, all transistors are cut off.

The clear winding linking all 121 cores is reverse-wound for core T_0. Core T_0 will be cleared to an initial ONE state while all others are reset to ZERO. A three-beat drive is used. After clearing, drive 0 will be the first line to be energized. The pulse through this line will reset T_0, driving Q_0 into conductance and allowing current to flow through X-0 and to set T_1. Drive 0 does not link T_1 and therefore does not oppose the setting of this core. Drive 1 is the next line to be energized. It will reset T_1, turning on Q_1 and permitting the current to flow through X-1 and both the "forward" count windings of T_2 and the "reverse" count windings of T_0. Drive 1 will oppose the setting of T_0 but will not oppose the setting of T_2. In this manner, the switch is set sequentially as long as the three drive lines are energized sequentially. The operation is the same for both loading and unloading. After it ends with the setting of T_{120} or sooner, the next pulse will always be "clear" to restore the initial operating conditions.

To reverse the action, the drive lines should be set in reverse numerical order. For example, if drive line 2 was the last to be energized, reversal will occur if drive line 1 is energized next instead of drive line 0. Once reversal has occurred, the reverse action will continue until a further reversal of drive sequence takes place. The first drive pulse after a reversal should be considered as an extra pulse. It is necessary to apply this extra
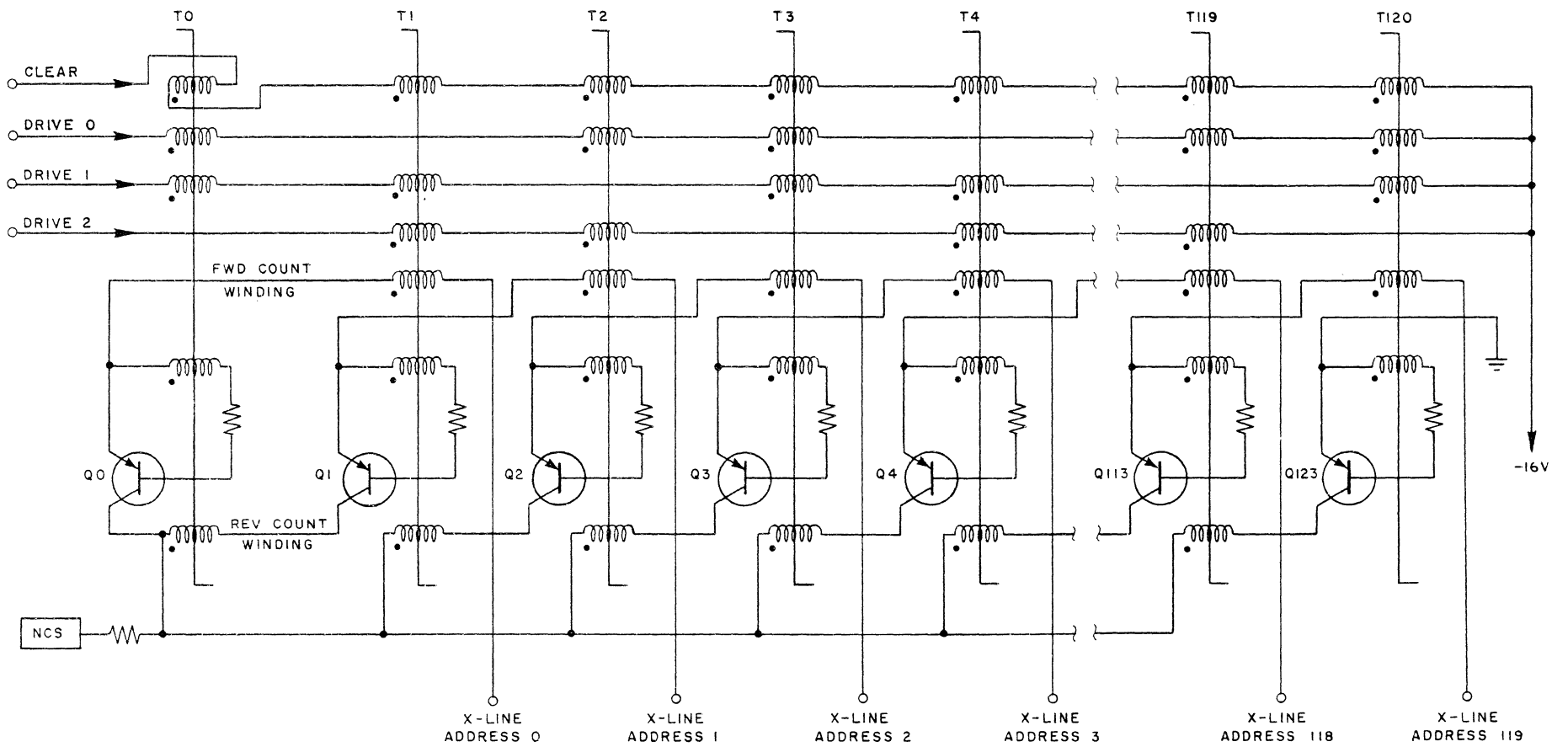
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Figure 31. Reversible transistor core switch.

pulse to return the core to the last used position before reversal
occurred. For example, if core 3 was the last used, it would have
been as a result of energizing drive line 0, and core 4 would also
have been set. The first pulse of the reversal process will be pro-
duced by driving on line 2, causing core 4 to reset and energizing
transistor Q_4. The next winding on drive line 2 (not shown) will
prevent core 5 from being set; therefore, the reverse count winding on
Q_4 will set core T_3, while the action of the forward count winding
will be inhibited by the current flowing in drive line 2. It should
be noted that during the reversal action, X line 4 will be energized.
The entire system must be designed so that this additional line will
become energized in the process of effecting a reversal.

Bidirectional Switches--Diodes in the Primary Circuit. There
are considerable advantages to employing diodes in the primary cir-
cuits of magnetic switches. First, they can add to the non-linearity
of the switch core or can provide all the non-linearity in the cir-
cuit. Secondly, they can be used to reduce the load presented by
the switch to the drivers. This is of considerable importance in
large storage units or in very-high-speed storage units. Unidirec-
tional switches with diodes in both the primary and secondary cir-
cuits are operated by a combination of the two techniques.

Figure 32 shows a typical small switch employing diodes in the
primary circuits of the transformers. In operation, first one of
the sinks, then one of the drivers is energized. If sink P and
driver A are energized together, current can flow through only one of
the primary windings of transformer T_1, and a pulse appears at the
output of this transformer in OP_1. Later driver A must be energized,
routing current to sink P through the other primary of transformer
T_1 to produce an output in OP_1. The two primaries of each trans-
former are wound in opposite directions so that one can set the core
while the other resets the core. If a diode is not included in the
secondary circuit, the switch acts like a conventional magnetic-core
switch in that it produces biphase outputs at its output terminals.

If the cores in this switch (Figure 32) are made of rectangular-
loop material, driver A may drive for as long as is necessary and may
then be turned off. No further action need proceed until it is de-
sired to produce a reverse output; then driver A'should be energized.
Since the current flow through the primary is selected entirely by
the diodes, with a switch of this type it is possible to separate
the load and unload actions in the cycle. For example, if a drive
such as AP is used to produce the read action, then a drive such as
A'P is used to produce a write action. If a switch is used in this
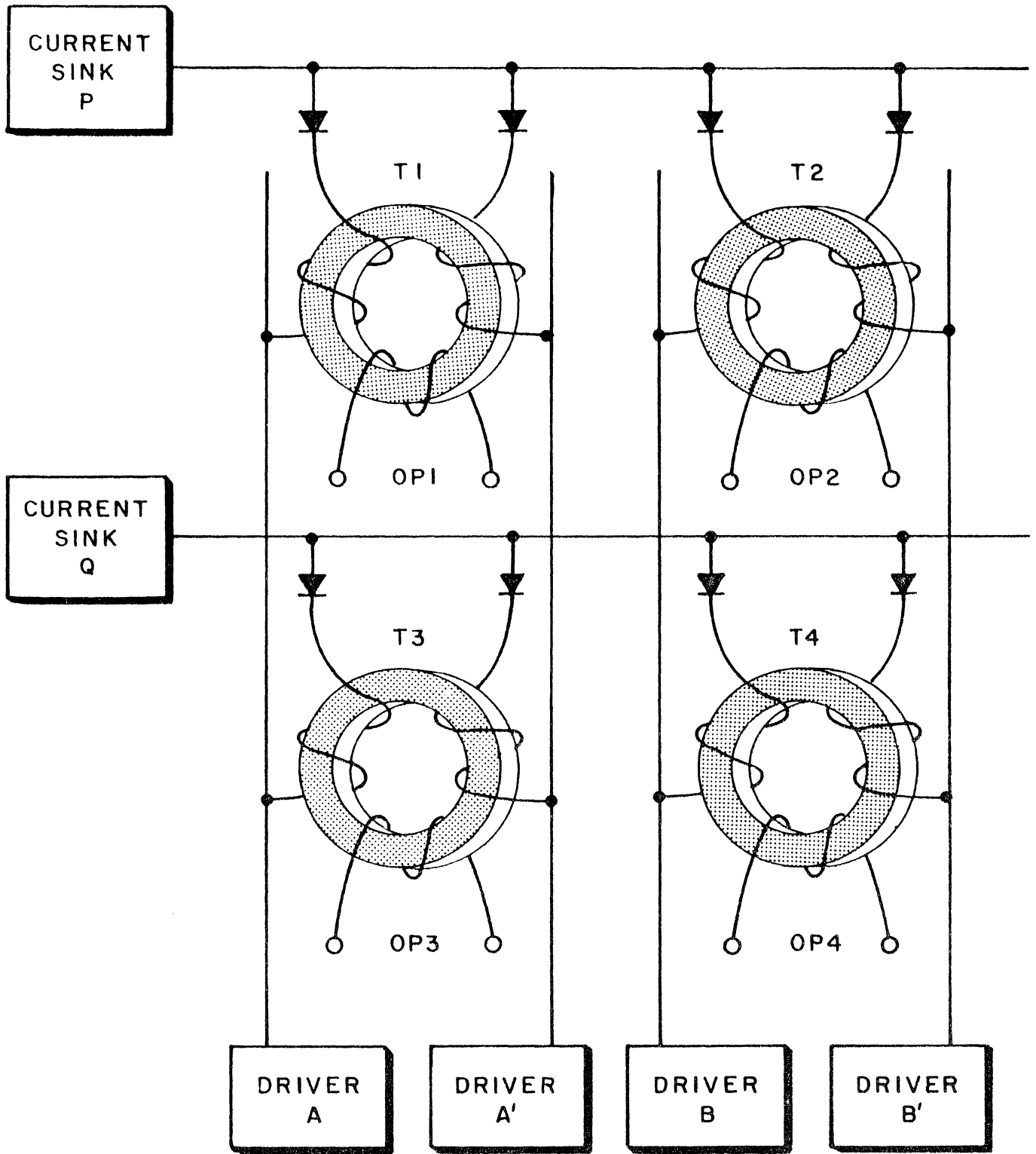manner, the operating technique must be such that an A'P action always

Figure 32. Small switch with diodes in the primary
circuits of the transformers.

occurs before a second AP action in an individual core.

Another way of mechanizing the switch is to replace all the A', B', etc. drivers and their associated windings with a single constant-current winding threading all switch cores. This winding must be capable of resetting any of the switches. The drive handled by the remaining drivers and the current sinks must then be double its previous value. A read action is initiated by a connection such as AP; but when driver A is no longer energized, a reverse output is obtained immediately from core T_1 under the action of the common bias winding. This type of switch has considerable advantages. It requires a small number of drivers, and its cycle time is short since a write action automatically follows a read action with maximum speed. Its disadvantages are the large size of the drivers and the necessity of controlling the trailing edge of the current from the drivers. This edge forms the rising edge of the write pulse from the output windings.

The cores in the switch need not be of square-loop materials. In fact, cores of linear material have lower coercive forces than square-loop cores. If linear-type cores are used, they act as transformers and the switching action is controlled entirely by the diodes. Extremely rapid operation is obtained with these switch cores, making them suitable for high-speed storage units.

The Secondary Circuit of a Switch Core. The load presented by a matrix has linear elements of resistance, capacitance, and inductance, as well as a non-linear element which contributes varying capacitance, inductance, and resistance values. The pure inductance is by far the greatest quantity, with the non-linear inductance, capacitance, and resistance following in that order. During switching, the switch core behaves as a relatively high impedance and sets up a current through the load. When the core is saturated, this current continues to flow because the secondary winding then becomes a small, relatively linear inductance. The natural time constant under these circumstances is very long; and usually it is necessary to add resistance in series with the load to shorten the saturated secondary-circuit time constant. Additional resistance can be provided by resistors at the end of the winding or can be distributed by using a resistive wire for the matrix windings.

The instantaneous voltage across the load during the operation of the switch depends on the number of storage cores which are moved from one state to another by coincident-current action. For example, in a system driving a 40-bit parallel word any number from zero to

forty cores can turn over. In the 1-microsecond materials this can
represent a change of 4 volts. The entire secondary voltage may be
no higher than 15 volts and would probably be no higher than 40 volts.
This represents a change of 10 to 25 per cent in the instantaneous
value of the load. If all the cores turn over, the switch core must
provide more flux to the load than if none of them turn over. Dur-
ing a reading cycle the same amount of flux is required during both
the set and the reset actions. During a write cycle, however, a word
of all ZEROs may be changed to a word of all ONEs, and there is a
considerable flux variation between set and reset. Ordinarily no flux
can be transferred through a transformer, and the flux absorbed by
the load must be exactly equal to the flux change in the transformer.

In the above-mentioned example, a small amount of flux is re-
quired during the setting action, and only this amount is available
on reset. Unless special measures are taken, it would be impossible
to alter the state of the storage cores. One such measure is to
add to the load a resistance which acts as a flux-dissipating device.
The resistance allows the transformer to move through a relatively
fixed flux change while the duration of the secondary reset pulse
varies slightly to compensate for load variations. The correct
value of resistance must be found by experiment. Generally it is
higher than the value required for correct damping in the secondary.
In order to obtain reliable operation, the voltage drop in the resis-
tance should be about ten times the amount by which the load voltage
can change with alteration of information content. Some storage
units have been operated successfully when this figure is as low as
five, but unless particular care is taken in the design to control
the operating currents, marginal operation can be expected.

DIODE AND TRANSISTOR SWITCHES

Figure 33 shows a typical arrangement for diode decoding. The dia-
gram indicates current flow in one direction only in the matrix
lines and in one set of matrix lines only. In a typical system
there will be 64 such diodes, eight drivers, and eight sinks; and
in a complete 4,096-word memory system there will be four sets of
drivers, diodes, and sinks, or a total of 32 drivers, 32 sinks, and
256 diodes. Superficially, diode decoding switching does not appear
to be very efficient since a large number of components is employed
and the combinatorial advantage is no greater than can be achieved
with magnetic switches. However, the impedance match between tran-
sistors and cores is so good that a medium-capacity memory can be
driven efficiently from a single set of transistor drivers and
sinks. If a magnetic core switch is interposed between the drivers
and the matrix, the loss introduced by the core switches is usually
sufficient to necessitate increasing the number of transistors in

the drivers and sinks.

The technique of decoding with diodes directly into matrices can frequently introduce a considerable cost reduction in large systems. Where very high speed switching is required, this is one of the few feasible methods. To date no magnetic switch has been designed to operate at the high speed necessary to drive the fastest available storage cores. In linear- or word-selection memories the complete selection is performed by diode switching. In a 1,024-word memory, for example, there would be 32 drivers, 32 sinks, and 1,024 diodes for each direction of current flow in the matrix. Low-speed linear-selection storage devices can be built with magnetic core switches, but they are usually less economical than coincident-current devices operated by core or diode switching.

Operation of the diode decoding scheme in Figure 33 is as follows: If driver A and sink Q are selected, the current flows from the current stabilizer through driver A and through the diodes on lines 0 and 1.
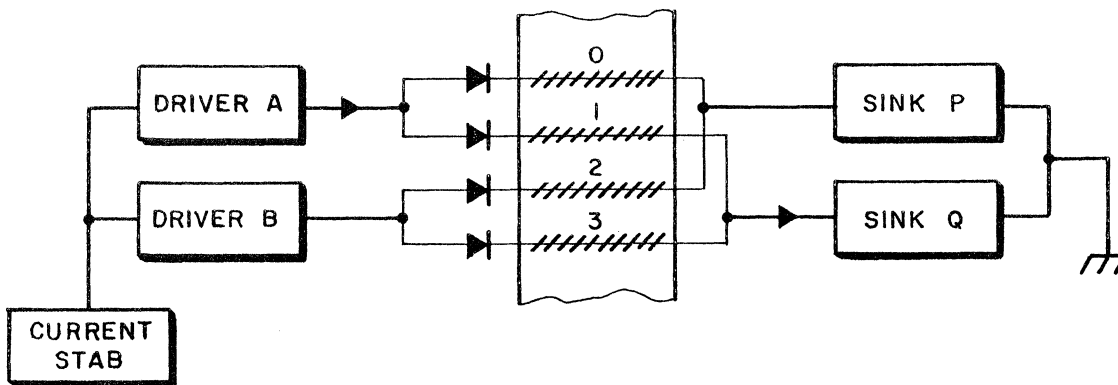
Figure 33. Diode decoding switching arrangement.

These lines behave as short time constant delay networks, and initially the currents divide equally down lines 0 and 1. However, the current flowing in line 0 encounters an open circuit at the end of that line, with reference to sink P, and flows up line 2 towards the diode. The current in line 1 encounters a short circuit because

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sink Q is conducting; it therefore flows into sink Q. Meanwhile the current which is flowing in line 2 finally encounters an open-circuit at the diode on line 2 and is reflected back down line 2 and then up line 0 to establish an open-circuit condition at the input end of line 0. Four complete propagation times through the matrix are required to establish the correct current in line 1. In practice, the lines do not encounter perfect open-circuit or short-circuit terminations at their ends. A total of six to eight propagation times should be allowed to completely establish the current in the selected lines. An alternate method is to bias the matrices so that an open circuit is encountered at the input end of every line. Then if sink Q is energized in advance of driver A or B, only the diode on line 1 will conduct when driver A conducts, and the current conditions are quickly established with respect to driver A.

Transistor Switches. It is also feasible to switch directly into matrices by transistors instead of diodes. This has already been discussed to some extent in the description of a transistor core switch. A typical transistor switching scheme is shown in Figure 34. The transformers shown can be elements of a switch or can be linear transformers driven from low-level decoding logic ahead of the drivers. The positive and negative current stabilizers feed a large number of these transistor switches. The advantage of driving by transistors is that large voltage swings can be tolerated at the output circuit. Transistor driving is therefore suitable for large memory systems, particularly when high-speed operation is desired. Transistors may also be used as power amplifiers in a large magnetic switch with low output power. By this means, it is possible to obtain the combinatorial advantages of a magnetic switch with the impedance-matching advantages of transistors.
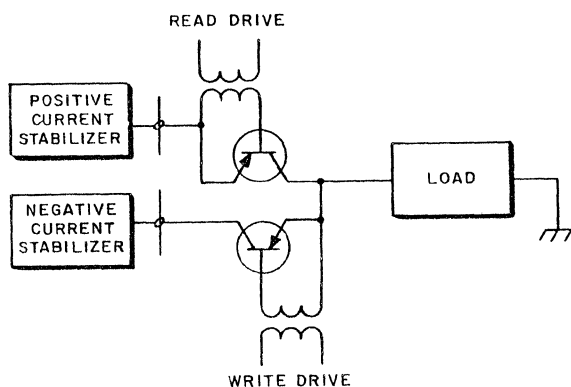
Figure 34. Transistor switching scheme.

STORAGE UNITS AND SYSTEM DESIGN

COINCIDENT-CURRENT STORAGE UNITS

Figure 35 shows a general block schematic of a coincident-current storage unit. The units at the top of the diagram perform the necessary timing and control, and produce partially decoded address waveforms. These units employ conventional computing-type circuits which provide the X and Y drives to the matrix storage unit. Some of the blocks, such as the memory register, are omitted in certain storage systems, but they will be found to exist in some form in the computer.

There is at least one reading amplifier for each parallel bit stored, and in very large units several amplifiers per bit are used to reduce the length of each sense winding. The reading amplifier, a suitable push-pull, stable amplifier, must offer high rejection to in-phase signals. It must have good low-pass characteristics and must not be paralyzed by noise spikes which are somewhat larger than the amplitude of the desired signal. The final component is a gated discriminator which emits either ZERO or ONE signals under the control of a strobe pulse. If the delay in propagation through the matrices is large, several strobe pulses are employed so that each reading waveform is strobed at the optimum time.

The parallel output from the reading amplifiers sets the memory register which, in turn, transmits the information to the computer. The memory register, which controls the re-write action during a read cycle, is loaded from the computer to control the write action. The writing or digit-plane drivers are precise pulsed current drivers which cause the information to be inserted into the matrices.

In serial machines it is common practice to employ a parallel storage unit, which is often more economical than an all-serial unit. Serial-to-parallel and parallel-to-serial converters are inserted in the incoming and outgoing lines. In some serial machines two storage units are used, each storing one half of the word. These units are then employed in an interlaced fashion so that one unit is writing, or re-writing, the last half of the word at the last address, while the other unit is reading the first half of the word at the present address. This arrangement leads to rapid serial operation.
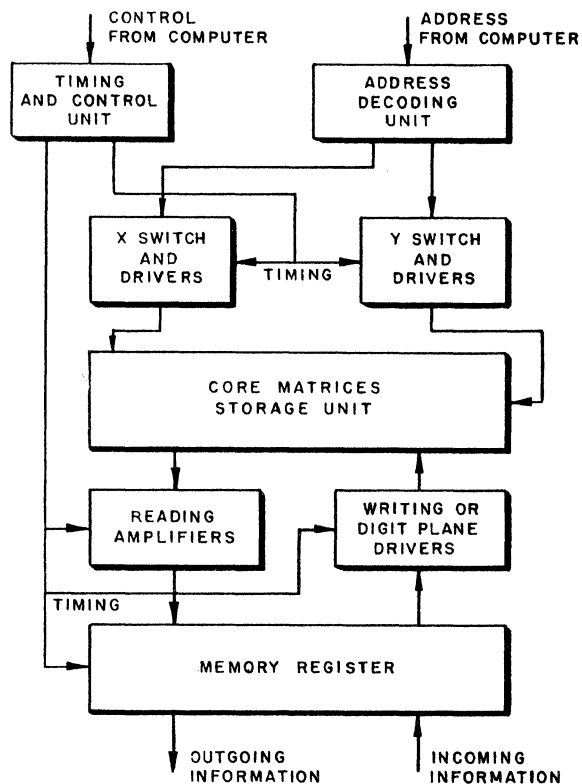
Figure 35. Block schematic of a
coincident-current storage unit.

Figure 36. Part of the driver
system of an early storage device.

METHODS OF DRIVING COINCIDENT-CURRENT STORAGE SYSTEMS

Progress in the design of coincident-current magnetic-core
storage systems has always depended on the availability of new
storage materials and new tubes or transistors for driving purposes.
The investigation of transistor drive had scarcely been started in
1955, but by the end of 1956 every storage unit which was in design
used transistor drive entirely or for the major portion of the unit.
This rapid transition from tube to transistor drive was due to the
superiority of transistors in matching magnetic core impedances.

Direct Drive. All the original magnetic core storage systems
used direct vacuum-tube drive because switch and storage materials

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were so poor at the time that they could not be combined into an operating system. A schematic of part of the driver system in an early storage device is shown in Figure 36. It is still typical of circuits that are frequently used in evaluating the performance of matrices. A direct-driven circuit, such as that shown in Figure 34, is used nowadays with transistors replacing the tube drivers in Figure 36 and with only one wire in each direction in the matrix. In the system shown in Figure 36, two X and two Y wires are used for each core in order to utilize the high impedance from the plate circuit for driving into the magnetics. Later systems used a single X or Y wire which was driven by one driver plate and one driver cathode. One matrix has been shown in the diagram, but in practice a number of matrices are usually employed in cascade. In the example shown, the impedance match is very poor because the tubes are capable of delivering much higher voltages than are ever required by the matrices.

Consider a storage unit which is designed to store 4,096 words of 40 bits each. Let us assume that the system is driven by 64 drivers in each of the X and Y directions. Also let us assume that the current flowing in the X or Y wires is 200 milliamperes and that the voltage induced in a selected core is about 30 millivolts and the voltage induced in an unselected core is about 3 millivolts. It is difficult to determine the exact value for the cores which are energized with only a half-current. The first time that a core is disturbed, a large disturb signal will be produced. The amplitude of the disturb signal will decrease with each subsequent disturbance until it reaches a minimum value. In designing a core storage unit, it is not correct to use either the maximum or minimum value in estimating the average load on the lines. The full potential operating range of the equipment should be examined in order to choose a correct average value. The number of cores in operation on the X and Y lines is symmetrical. The selected X or Y wire links 63 half-selected cores in each matrix and one selected core. The selected core may or may not switch, depending on whether it is storing a ZERO or a ONE. For the complete system, each X or Y wire links 2,520 half-selected cores and 40 selected cores. The minimum voltage drop due to the cores themselves, if the word that is read contains all ZEROs, will be 7.68 volts. To this must be added the voltage drop due to the resistance of the wire and to the two inductances of the windings. Generally, the sum of these two factors is about equal to the voltage drop introduced by the cores. Therefore, it will be assumed that the normal voltage drop through the matrices, if none of the selected cores switches, is a little over 15 volts, say 15.25 volts. If all the selected cores switch, an additional 1.25 volts

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will be required. In designing the system it should be assumed
that the minimum instantaneous voltage drop is about 15 volts and
the maximum is about 16½ volts. This voltage at a current of 200
milliamperes can be delivered by transistors, although the value
of the voltage is perhaps a little high for reliable operation. It
does indicate that the match between the transistors and the cores
is extremely good. In a tube-driven system this voltage would
represent an extremely poor match.

Transformer Drive. Linear transformers may be inserted be-
tween the drivers and the cores to effect an impedance match. It
then becomes necessary either to add resistance in series with
the matrix wires or to use resistance wires for winding the mat-
rices. (The use of this resistance was described under the para-
graph headed The Secondary Circuit of a Switch Core.) The amount
of resistance required in the secondary circuit of a linear
transformer is not so great as that needed in a switch core but
some resistance is required to compensate for the varying flux
absorbed by the matrices as the information content changes. In
addition, since the transformer itself introduces loss and induc-
tance, about twice as much peak power must be supplied to the
primary of the transformer as is supplied in a direct-driven
system. For this reason, transformer drive is chiefly of value
in small-capacity storage units.

Transformer drive is frequently used in conjunction with
diodes to form a diode transformer switch. Such a switch effects
an impedance match and introduces some combinatorial advantage,
which reduces the required number of drivers. Transformer coup-
ling between the drivers and the storage matrices has been used
successfully in transistor-driven equipment. In very large
systems, transformer coupling is used to step down a current in-
to the matrices when the transistors cannot develop enough
voltage to drive the storage matrices. In small systems, transformer
coupling is used to step up the current to the storage matrices.
The matrices require more current than can be delivered by transistor
drivers.

Switch Drive. Direct- and transformer-driven systems are
simple to design and are particularly desirable for memory units
which will not be reproduced in large quantities. If quantity
production is to be considered, savings in equipment and cost can
be effected by using switch-driven systems. Although they are
more difficult to design and test than direct-driven systems, the
switch-driven systems are more economical to produce and usually

more reliable. Most magnetic-core storage units in wide use today
employ a switch of some type in the drive circuits. If a unit is
designed for small-quantity production, usually a rather simple
switch is employed. Only in high-quantity production devices are
the more complicated types of switch used.

Random-access Switches. In random-access applications, the
choice of a simple type of switch is dictated not only by the econ-
omical advantages in design cost and over-all system operation,
but also by the fact that complex switches are rather inefficient.
A typical simple switch-driven system using an anti-coincident
switch is shown in Figure 37. The broken lines in the switch matrix
indicate the wires that are energized. In this instance, line 1
in the vertical direction and lines 1, 2, and 3 in the horizontal
direction are energized. The current in the horizontal direction
inhibits the switch, while the current in the vertical direction
drives the switch. Only core 1 is driven and not inhibited; there-
fore, only this core produces an output. The connections between
the output circuits of the switch cores 0 through 15 and the com-
pensating resistors numbered 0 through 15 are not shown in order
to simplify the diagram.

There are many kinds of double-coincident switch in use today.
They all have similar properties and utilize about the same number
of drivers for a given size of switch. The choice of one form of
switch or another is usually made on economic rather than on tech-
nical grounds. The cost savings introduced by a specific switch
cannot be stated in any general form. Various types of switch
must be sketched out in a fairly complete design to decide which
is the most economical for a particular system. Generally, a switch-
driven system will use only about 20 per cent of the components in
the driver circuits that would be required in a direct-driven
system. On a similar scale, a transformer-driven system will use
somewhere between 50 and 60 per cent of the components that would
be used in a direct-driven system. These figures can be misleading
because the switch may be a costly item to manufacture.

Mixed systems in which one axis of the storage planes is switch-
driven and the other axis is direct-driven or transformer-driven
are occasionally fabricated. They are particularly effective when
it is necessary to obtain accurate control of the current in one
direction, usually in the axis which is direct- or transformer-driven.

Special-purpose Switch Systems. Sometimes storage units are
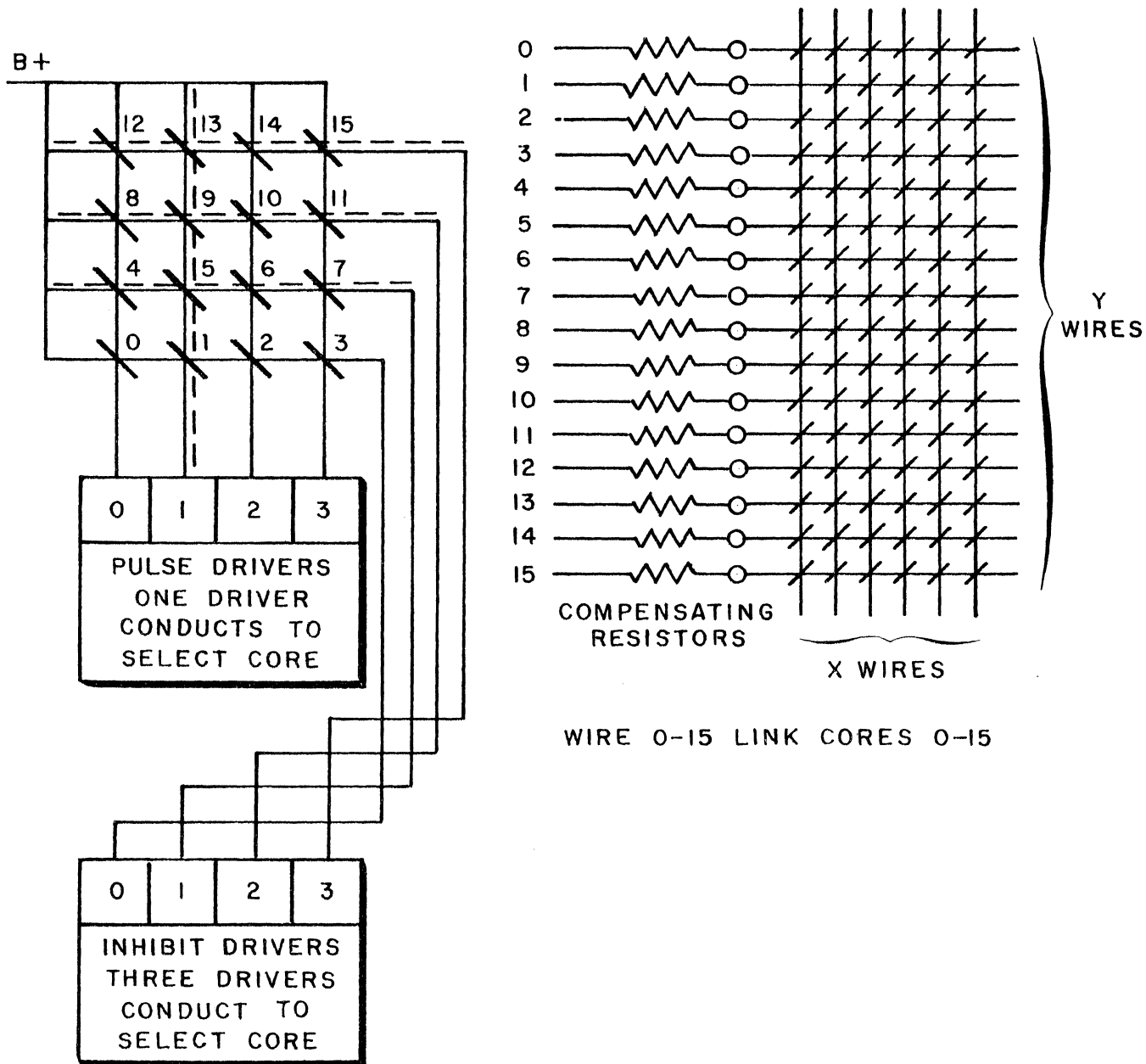required which refer to each address in a sequential manner rather

Figure 37. System driven by an anti-coincident switch.

than in a selective manner. A unit of this type permits the designer to achieve an increase in circuit economy. The switches illustrated in Figures 26 through 30, 33, and 34 are useful in this respect, because they act both as counters and as switches. They remove the necessity for address circuits and, in addition, require very few drivers to operate them. Two switches of this type may be used in the X and Y directions as long as the number of outputs from one switch is mutually prime with respect to the number of outputs from the other switch. This requirement can be mechanized in a simple fashion if one of the switches has three drivers instead of the two illustrated in Figure 26. Both switches will count together, and ultimately every core in the matrices will be scanned as indicated in Table 27.

Table 27. Scanning Pattern in a Special-Purpose Switch System

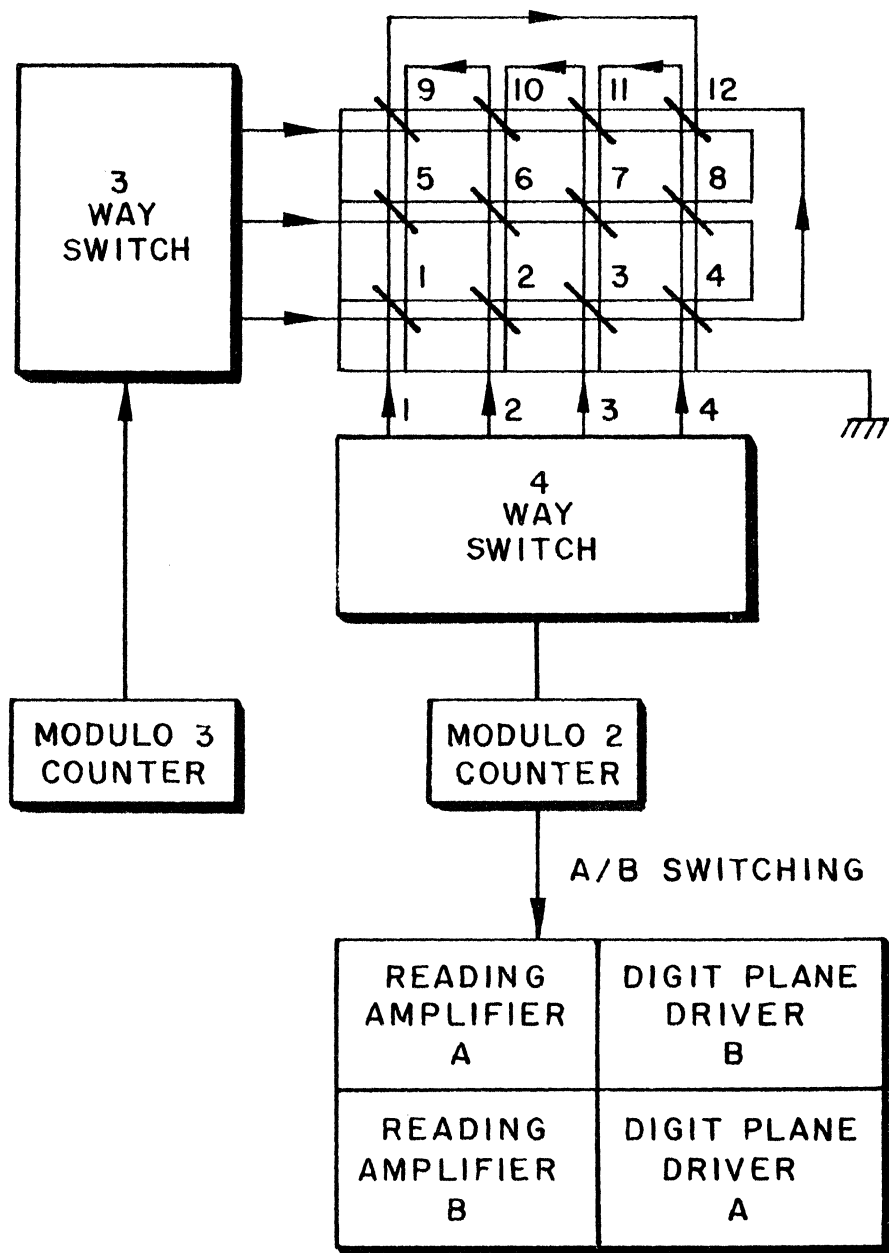| X Switch Driver	X Switch Position	Y Switch Driver	Y Switch Position	Core which is Scanned
1	1	1	1	1
2	2	2	2	6
1	3	3	3	11
2	4	1	1	4
1	1	2	2	5
2	2	3	3	10
1	3	1	1	3
2	4	2	2	8
1	1	3	3	9
2	2	1	1	2
1	3	2	2	7
2	4	3	3	12

In most storage systems of this type, it is not important to retain the information once it has been read. Then it is convenient to employ two sets of switches, one of which operates during a write operation and the other during read. Because each switch remembers the address of the next operation, it is possible to write in a block of information, read out some of it, write in some more, and so on. In this type of operation only one beat is required either to write or to read since every reading operation clears the storage cell to ZERO in readiness for a write operation.

The information may be regenerated, and the operation of the storage unit may be speeded up, by employing a special matrix configuration in conjunction with the shifting switches. A system of this type is illustrated in Figure 38. The matrix wires are taken through a row or column of cores and are then returned in the opposite polarity through the previous row or column. Wires in the first row or column are taken back through the last row or column. If, for example, core 6 is being set to the ZERO state, or read, then core 1 which was the last core set to ZERO is in process of being set into the ONE state. Two reading amplifiers and two digit-plane drivers and their associated windings are used alternately. The operating sequence is shown in Table 28.

Table 28. Operating Sequence in a Special-Purpose Switch System

4-Way Switch Output	Reading Amplifier in Use	Digit-Plane Driver in Use	Core Read	Core Write
Odd	A	A	1	12
Even	B	B	6	1
Odd	A	A	11	6
Even	B	B	4	11 and so on.

The system reads and writes simultaneously and, therefore, operates twice as fast as a conventional selective system. It is economical with respect to components, but the complexity of the matrix windings limits its application to small storage units.

SENSE WINDING 'A' LINKS ODD CORES AND SENSE WINDING 'B' LINKS EVEN CORES.

DIGIT PLANE WINDING 'A' LINKS EVEN CORES AND 'B' LINKS ODD CORES.

Figure 38. Special-purpose switch system for sequential operation.

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The diode decoding scheme illustrated in Figure 33 is also used to achieve additional decoding associated with the storage unit itself. Diode decoding may be used in conjunction with a direct-driven system or to place two magnetic switches in cascade. Essentially the system is arranged so that one switch produces a positive voltage while the other produces a negative voltage. The selected diode is the only one that can conduct as a result of the positive and negative operations of the two switches in cascade. In order to operate a system in this manner, there must be close control of the dc bias which is used as part of the selection operation and of the outputs of the switches. To achieve adequate control of the voltages, switches employed in cascade are usually unidirectional steering switches in which the prime current is drawn from a current stabilizer of some type.

Diode decoding in conjunction with magnetic switches has been used successfully in sequentially accessed linear- or word-selection memories. In a memory of this type the current through the diode is allowed to charge a shunt inductance at the same time as a large pulse of current is routed down the matrix wire to perform the read operation. When the drive switch has ceased to operate, the current flowing in this inductance causes a current reversal in the matrix wires which is low in amplitude and long in duration compared to the original current pulse applied by the switches. Such a current-generating technique is adaptable in either a random-access or a sequential-access unit in which only one set of unidirectional switches is used to initiate the read operation. The write operation follows automatically as a result of the overswing of current due to the inductances.

CIRCUITS PECULIAR TO CORE STORAGE UNITS

In most core storage units, standard circuits are used for flip-flops, gates, delay elements, timing elements, and for all the usual logical functions. In those units designed to achieve high reliability, special types of core logic replace the conventional transistor-diode logical circuits. There are two types of circuit which are truly peculiar to the magnetic-core storage unit. The first are the driver circuits which insert addresses and information into the memory, and the second are the reading or sense circuits which detect the output from the magnetic-core array.

The electronic circuits associated with a storage unit must be extremely reliable because errors introduced in the memory are a severe handicap to the user of digital equipment. All circuits,

whether or not associated with the memory, are toleranced carefully
to achieve a high probability of long life. Components are de-
rated and toleranced to operate at a much higher temperature than
would be expected within the equipment. They are rigorously in-
spected and tested before assembly, and a sample number are tested
to destruction. Power supplies are regulated to reduce the effects
of line variation, and circuits are toleranced to withstand large
variations in power.

Circuits described below are typical of those in high-quality
equipment.

Current Stabilizer. The current stabilizer is an important
element in many driver circuits. It delivers a constant regulated
current at a high impedance which may be steered by means of tran-
sistor switches into the magnetic portion of a storage unit. A
typical current stabilizer is shown in Figure 39. This circuit is
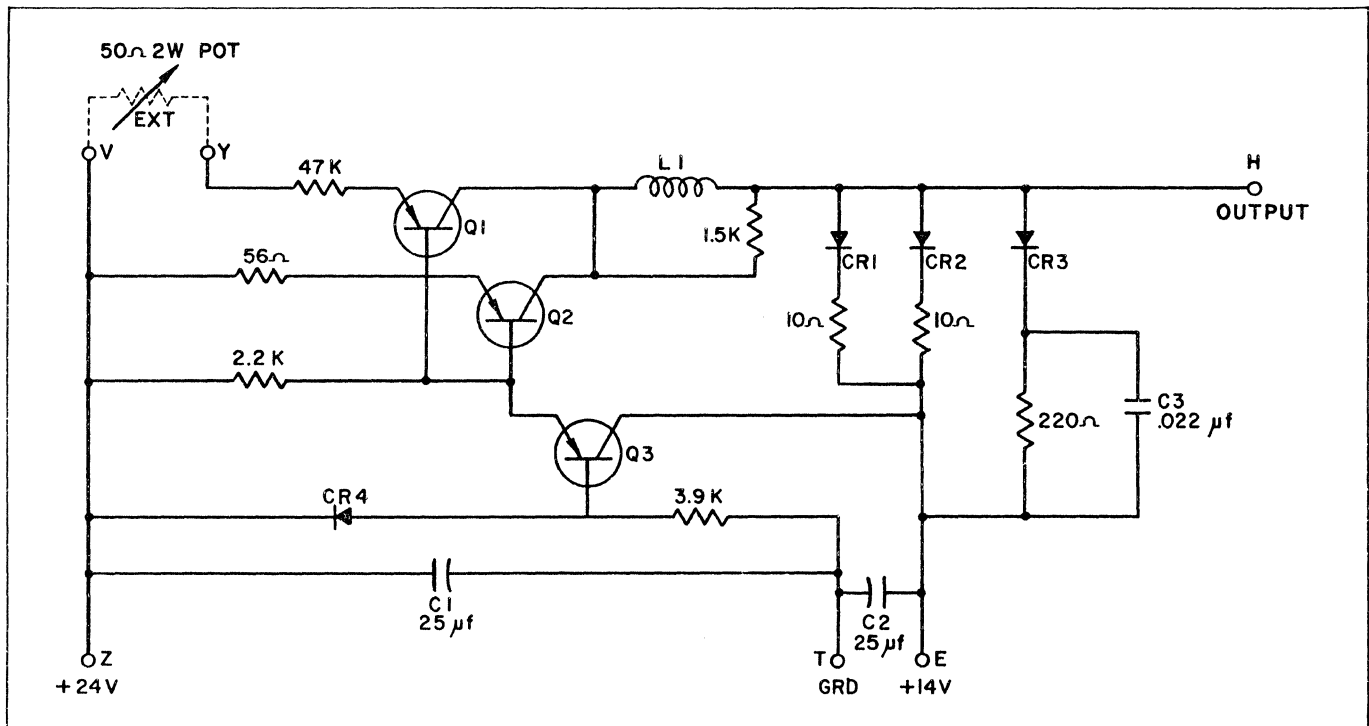designed to produce a constant current regardless of the operating

Figure 39. Current stabilizer.

temperature. Other circuits are temperature compensated to vary their current output and compensate for the changing characteristics of the switch core effected by variations in temperature. This circuit maintains current at a constant value regardless of load voltage excursions ranging from zero volts (ground) to close to +14 volts. The magnitude of the current may be adjusted with an externally mounted potentiometer to 185 milliamperes. The diode CR_4 acts as the regulating element and may be considered a constant battery of +6 volts placed across the emitter base section of Q_1 and Q_2. The L_1 in the collector circuit is a surge-limiting element.

Transistor Switch. Transistor switch circuits are used in routing current from a current stabilizer to a magnetic portion of a storage unit. A typical circuit is illustrated in Figure 40. Transistor Q_3 serves as a unidirectional switch with both of its terminals floating so that the switch may be connected between a variety of power sources and loads within capabilities of the circuit.
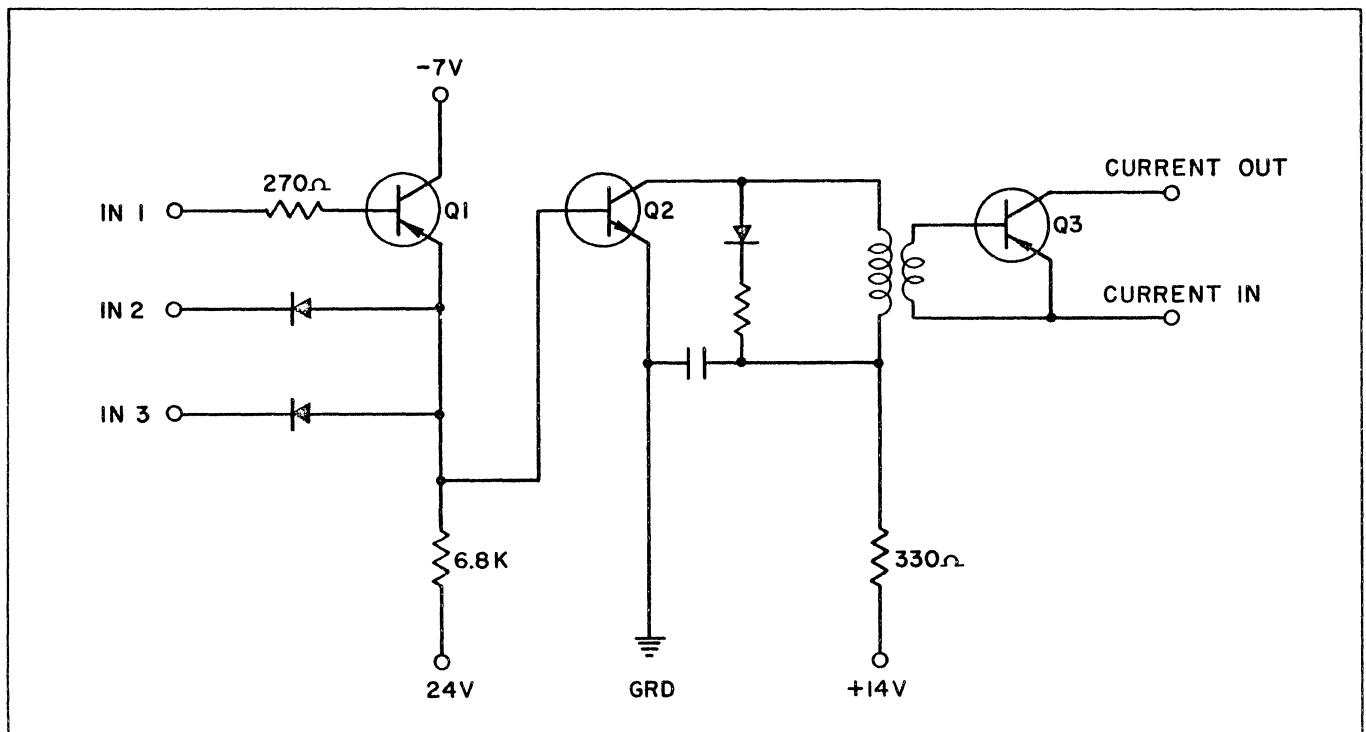

Figure 40. Transistor switch circuit.

The power source may be of either polarity and of either the constant-voltage or constant-current type.

The versatility of the circuit is due to transformer coupling of the enabling pulse to the base of Q_3. The transformer is also the source of two limitations of the circuit: (1) the maximum duration of switch closure is 10 microseconds, and (2) the recovery time is 10 microseconds.

Transistor Q_1 and the diodes at the inputs to the circuit form an AND gate whose nominal operating voltage levels are ± 5 volts. Transistor Q_2 serves as an amplifier between the gate and the switch (Q_3). If any one (or more) of the input levels is -5 volts, the switch will be open. When all input levels are +5 volts, the output of the gate will rise and cause Q_2 to conduct, which in turn energizes Q_3 to conduction.

Because of its time limitations, the switch must be turned off within 10 microseconds and must not be re-energized for another 10 microseconds. This timing is usually accomplished with pulses of a suitable duration and a duty cycle applied to the base of Q_1. The maximum current permitted to flow through a closed switch is 200 milliamperes. The rise time of current to 200 milliamperes through a resistor load is not more than 1 microsecond.

The above circuit is used in small storage units. Transistor switch circuits used in large storage units operate in a similar manner, but are designed to handle much larger currents and voltages.

Digit Driver. Digit-driver circuits are used to insert information into the storage matrices. They are also used for inhibit purposes when driving switches and as sinks when driving diode core switches or in applications requiring diode decoding in association with storage matrices.

A typical digit-driver circuit, shown in Figure 41, functions as a switch. One of its two terminals is connected to ground; the other (output) may be connected to a negative supply through a suitable load. The switch is closed when both the information input and the $\overline{LU}$ input are at -5 volts, and open when either input is at +5 volts. The specific function of the circuit is to hold a selected core in the ZERO state by energizing the inhibit winding passing through the matrix cores whenever the information input is a ZERO (-5 volts).
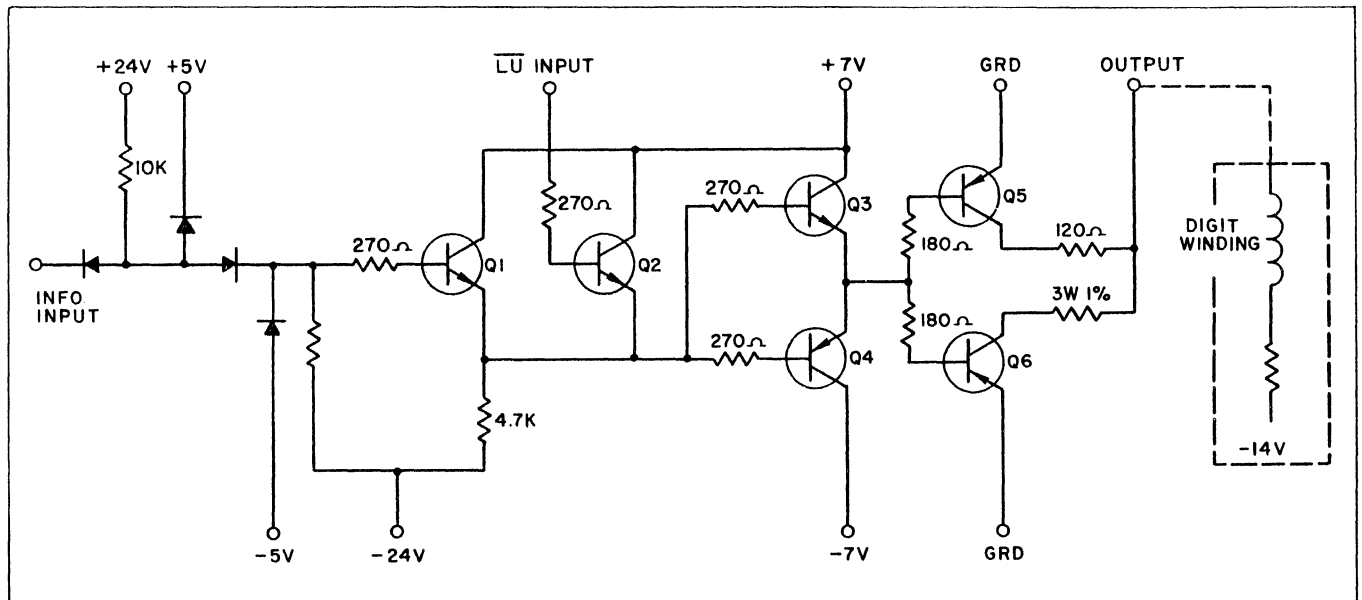
Figure 41. Digit driver circuit.

The circuit has an input stage, consisting of transistors Q_1 and Q_2 plus four clamping diodes; a difference amplifier, Q_3 and Q_4; and a transistor switch, Q_5 and Q_6, that forms the output stage. The information input is clamped to ± 5 volts; the $\overline{LU}$ input is at +5 volts during UNLOAD and -5 volts during LOAD. The emitter followers, Q_1 and Q_2, form a negative AND gate for these inputs. When both inputs are at -5 volts, Q_1 and Q_2 will conduct very little and drive the transistor switch out of conduction through the emitter follower Q_3.

The output circuit consists of current-limiting resistances in series with a digit winding and the switch. It is energized by a -14 volt supply. A maximum of 15 volts is permitted across the switch when it is open, and a maximum current of 200 milliamperes is permitted to flow through a closed switch. The rise and fall times of the currents through a resistive load are not more than 1 microsecond.

The digit-driver circuit described above is designed for applications where the current is kept constant with temperature. If it is desired to compensate for temperature change, instead of using -14 volts in the collect circuit of Q_5 and Q_6 a special power

.supply is used in which the change of voltage with temperature is proportional to the change of current that is required in the cores.

Read Amplifier. The output signal from the sense winding of the core matrix consists of two types of signal. The first is a large in-phase excursion of the sense winding due to electrostatic coupling between this winding and the X and Y wires in the matrix. Both ends of the sense winding go through this excursion together if the sense amplifier and sense winding are correctly designed. A second signal, between the two output wires, is the desired read signal. The ratio between the undesired electrostatically induced in-phase signal and the desired magnetically induced out-of-phase signal is never less than a hundred to one, and in large memories is frequently as high as a thousand to one. In order to detect the desired signal, the read amplifier must be a well balanced and well designed difference amplifier.

A typical read-amplifier circuit used in very small storage devices is shown in Figure 42. This circuit accepts bidirectional
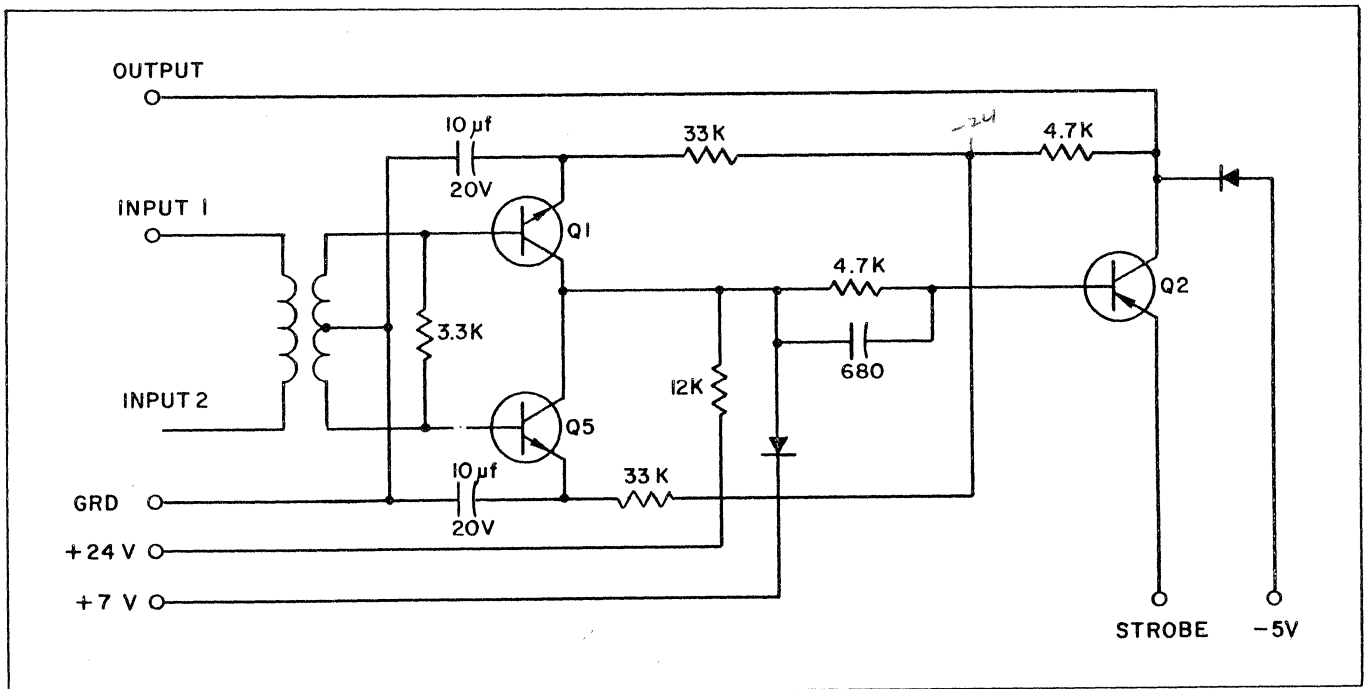

Figure 42. Read-amplifier circuit for small storage unit.

turnover signals from a magnetic matrix core. A signal is first am-
plified and then sampled at its peak amplitude with a strobe pulse.
The circuit consists of an input pulse transformer, a highly sen-
sitive input amplifier, and a transistor gate. Both ends of the
matrix sense winding are connected to the primary of the input
transformer. Depending on its polarity, the input signal is ampli-
fied by either Q_1 or Q_3 and is applied to the base of the transistor
gate Q_2. The strobe pulse is inserted into the emitter of the
transistor gate Q_2.

To provide proper detection, the turnover signal from the sense
winding must have a peak amplitude of 20 millivolts or more, and the
duration of the signal at 5 millivolts must be 3 microseconds or
more. Following detection of such a signal, the output pulse will
be a replica of the strobe, rising from its normal level of -5 volts
to +5 volts in not more than 1 microsecond, remaining at this level
for not less than 1 microsecond, and falling to the original -5 volt
level in less than 1 microsecond. It remains at the -5 volt level
when no turnover signal is detected.

A more sophisticated read-amplifier circuit which is used in
large storage units is shown in Figure 43. The input signal is
applied to the primary of transformer T_1. The secondary windings
of T_1 provide a balanced push-pull input to transistors Q_1 and Q_2.
The positive-going edge of the pulse input provides a voltage at
the base of Q_1, that is positive with respect to the voltage at the
base of Q_2. Under these conditions, Q_1 reduces conduction and Q_2
increases conduction. The collector output voltage of Q_1 drops and
the collector output voltage of Q_2 rises, resulting in a negative
voltage at the base of transistor Q_3 with respect to the voltage
applied to the base of transistor Q_4. Transistors Q_3 and Q_4 com-
prise a differential amplifier circuit with cross coupling accom-
plished by capacitors C_1 and C_2. The resultant increase in
conduction through Q_3 provides a positive voltage at the junction
of resistors R_{13} and R_{15}. This rise in voltage is fed back to the
emitter of Q_1 through capacitors C_3 and C_4 to stabilize operation.
The positive voltage at the collector of Q_3 is also applied through
capacitor C_9 to the junction of diodes CR_1 and CR_3. Decreased
conduction through Q_4 produces a negative voltage at the junction
of resistors R_{14} and R_{16}. This drop in voltage is fed back through
capacitors C_5 and C_6 to the emitter of Q_2 to stabilize operation.
The negative voltage at the collector of Q_4 is also applied through
capacitor C_{10} to the junction of diodes CR_2 and CR_4. Capacitors
C_7 and C_8 in the collector circuits of Q_3 and Q_4 maintain a sharp
pulse edge on the collector feedback voltage. The voltage at the
junction of CR_1 and CR_3 is positive with respect to the voltage at
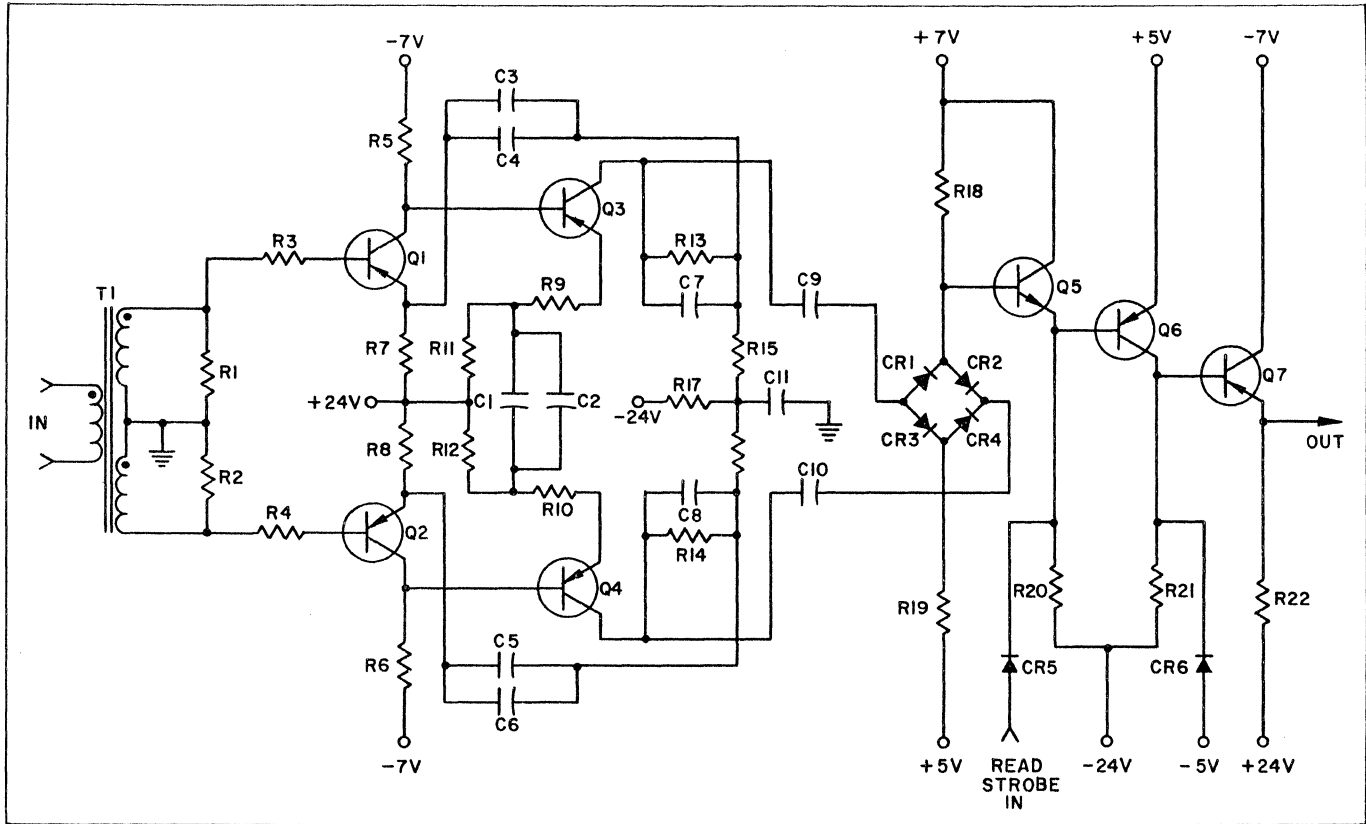the junction of CR_3 and CR_6. Resultant conduction through the diodes

Figure 43. Read amplifier circuit for large storage unit.

produces a negative voltage at the junction of CR_1 and CR_2 with respect to the voltage at the junction of CR_3 and CR_4. The voltage at the junction of CR_1 and CR_2 is directly applied to the base of transistor Q_5.

An output is obtained from the read amplifier only when the read strobe, generated in the timing and control circuits, is applied in coincidence with the input from the associated read winding in the memory module. The normal bias level at the base of Q_5 is +6 volts, established by the divider R_{18} and R_{19}. The read strobe is also referenced to +6 volts, so that the voltage at the Q_6 base biases Q_6 one volt into cut-off. Only when the read strobe and the signal go negative together by more than one volt does Q_6 conduct, establishing +5 volts at the emitter of Q_7. If either the read strobe or the rectifier remains above +5 volts, Q_5 remains cut

off. The base of Q_7 is clamped to -5 volts by CR_6.

TYPICAL MAGNETIC-CORE STORAGE UNITS

Magnetic-core storage units have evolved into two major classes. The first class are the general-purpose units which are random-access in nature and of relatively large capacity. Capacities range from as low as ten thousand binary digits to more than one million binary digits. Units of this class are characterized by their random-access properties and by the utilization of a two-beat cycle in which both reading and writing occur. In most of them it is possible to perform either a read-and-regenerate cycle or a clear-and-write cycle. In some of them the cycle is split so that independent synchronizing pulses may be used to initiate the read and write operations. During the first part of the cycle, a reading operation always takes place, and in this process the selected word is cleared to all ZEROs. The second part of the cycle must always occur but may be delayed by an indefinite period before it occurs. During the second part of the cycle, the information that was read is regenerated or a new word is written into the selected memory cell. Every cell of the memory is effectively an accumulator since a word can be brought down from the memory, modified, and inserted back into the memory in the last part of the cycle.

The rate of operation of the general-purpose storage units varies from 1 microsecond per cycle in the high-speed units to low speeds of 20 to 50 microseconds per cycle. The cycle time is defined as the interval from initiating a complete action in the memory until the next complete action can be initiated. In random-access memories, the cycle time includes a complete read-and-regenerate operation or a complete clear-and-write operation as well as the time necessary for setting up a new address between cycles. The access time of the storage unit is defined as the delay between the moment when all information is fed to the memory to instruct it to perform an operation and the earliest moment at which the information stored at a particular address is available in an output register. This time varies from about ½ microsecond to about 10 microseconds.

The second major class of core storage units are special-purpose units, also referred to as buffer storage units. Early units of this type were buffers designed to effect time matching between two devices operating at different speeds. They were found to be valuable in re-formating the information during the time-matching operation. Special-purpose storage devices perform pure storage functions as well as a number of logical functions usually associated

with the computing art rather than with the storage art. These storage units are usually small in capacity, rarely exceeding 10,000 binary digits. The minimum capacity of a buffer storage unit may be as low as 100 or 200 bits. Below this size, it is usually more economical to use magnetic-core shift registers.

The original type of buffer storage unit was designed to transfer information from one continuous medium to another, such as paper tape to magnetic tape or magnetic tape of one type to another type of magnetic tape. It stores information as characters of four to eight bits parallel rather than as words. Its capacity is small, usually between a hundred and a few thousand characters. It contains two sets of counters, one of which remembers the load address and the other the unload address. The order of the information passing through the buffer storage unit is unaltered. Loading and unloading operations can be intermixed in any way desired. The mode of operatio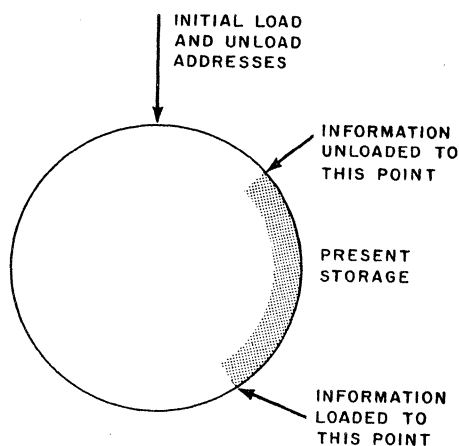n of the unit is illustrated in Figure 44. At the beginning, the unit is cleared and both the load and unload addresses are set to the initial point shown at the top of the diagram. Information is loaded into the unit to the point near the bottom of the diagram. Part of the information is then unloaded. More information may be loaded and unloaded in any manner desired, so that a certain amount of information can be stored between the load and unload addresses. There is instantaneous and simultaneous access to both the load and unload points at any moment. The speed of operation of this unit is high compared with that of the tape unit with which it is associated.

Figure 44. Operating mode diagram of a buffer storage unit.

One derivative of the basic storage unit is a buffer which allows a block of information to be loaded and, at a subsequent time, to be unloaded as a complete block. Units of this type are logically similar to units of the first type; but because they contain less equipment, they can be manufactured more economically. The third type of buffer storage unit is one which performs a major format conversion in the course of its operation. A typical unit

in this category is one which reads information directly from the brushes of a punch-card reader and transmits the information in a sequential stream of characters so that it may be written on a paper or magnetic tape. Another unit of this same class performs the converse operation of receiving information as a serial stream of characters and transmitting it in parallel form to a card punch or a high-speed printer. Buffers of this type have achieved a high degree of sophistication. They not only perform the "corner-turning" operation (serial-to-parallel transfer) but also perform a number of logical functions to control the operation of the magnetic tape unit and of the high-speed printer. They are very nearly complete systems in themselves.

There are a number of other buffer storage units. Some are capable of loading and unloading information in a forward-and-backward direction in order to reverse the information flow. Some perform minor serial-parallel and parallel-serial operations as well as storage operations. In others, sequential and random-access characteristics are combined for the performance of sophisticated format re-arrangement.

A Typical Random-access Storage Unit. Figure 45 is a block schematic of a low-speed, general-purpose, random-access magnetic-core storage unit. It is operated by coincident-current techniques and has a storage capacity of four thousand 28-bit words. The unit uses a split cycle, the two halves of which are initiated by sync A and sync B. If the line labeled "write" is energized at the same time as sync B, new information is written into the selected memory cell during the write part of the cycle; if this line is not energized, the information read out of the memory in the first part of the operation is regenerated into the selected memory cell. The timing cycle of the unit is shown in Figure 46. Times shown in this diagram are not the maximum rates of operation of this memory but are the rates at which it is used in conjunction with a computer of a special type. It should be noted that the X set waveform commences earlier than the Y set waveform. Because the memory is used for rather slow applications, extra time may be added to the cycle to improve performance. By starting the X current before the Y, it is possible to separate the X and Y noise during sensing and to obtain a better signal-to-noise ratio at strobe time.

The drive system employed in this memory is of the type shown in Figure 32. A combination of non-linear switch cores and diodes is used to obtain access to the magnetic-core storage array. In Figure 45 the drivers designated as X-X and Y-X are the current
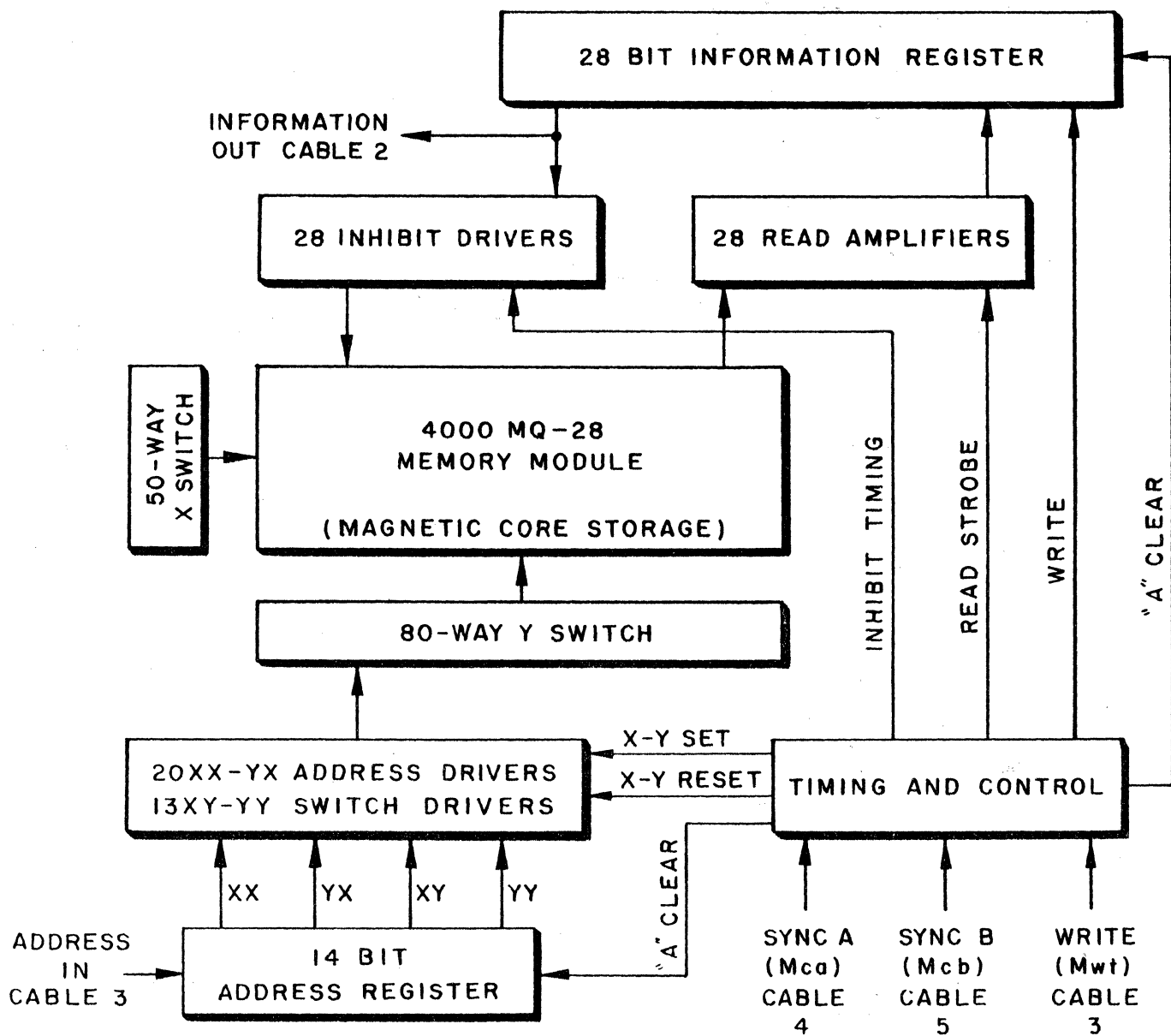
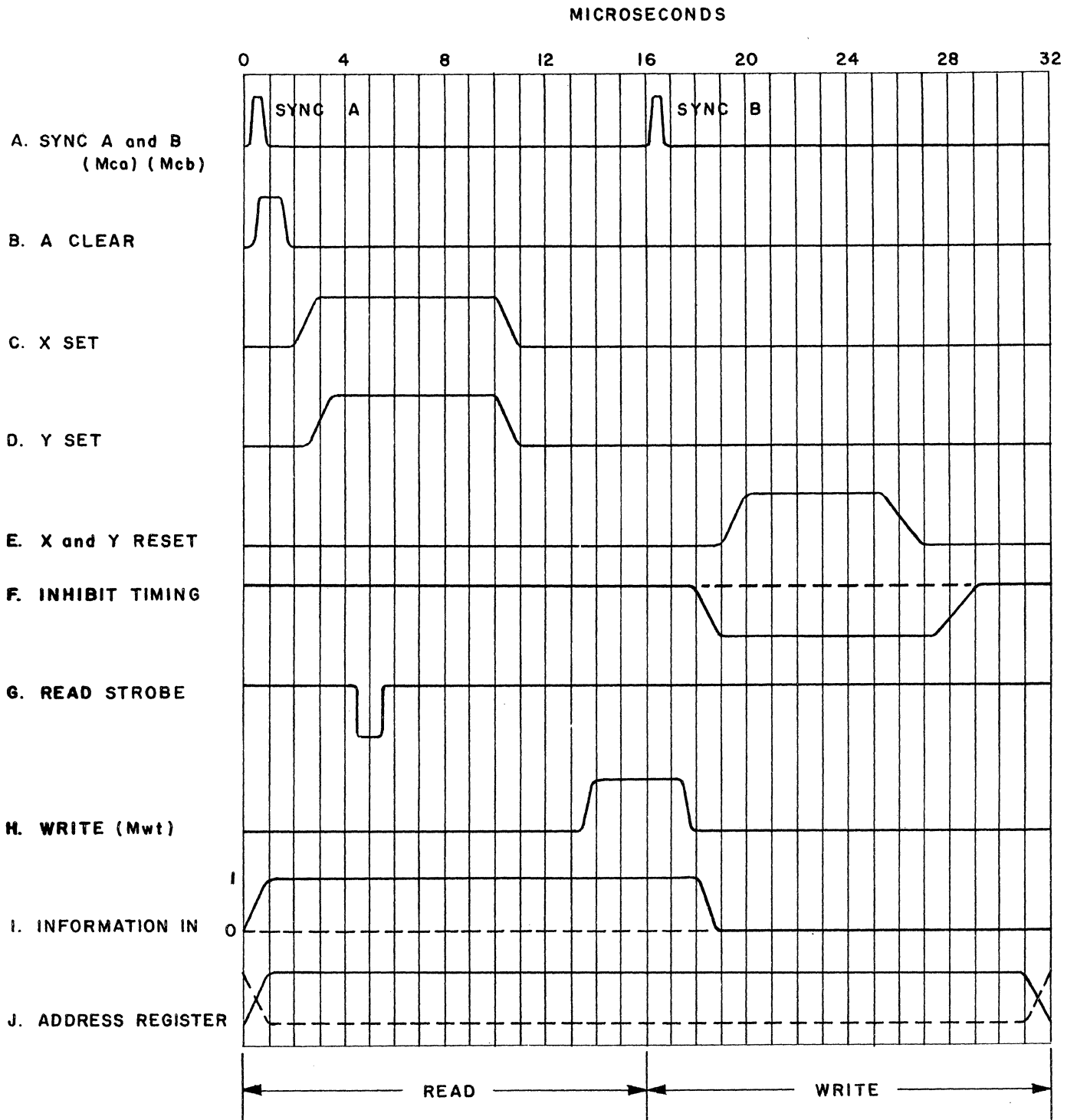Figure 45. Block schematic of a random-access storage unit.

Figure 46. Timing cycle of random-access storage unit shown in Figure 45.
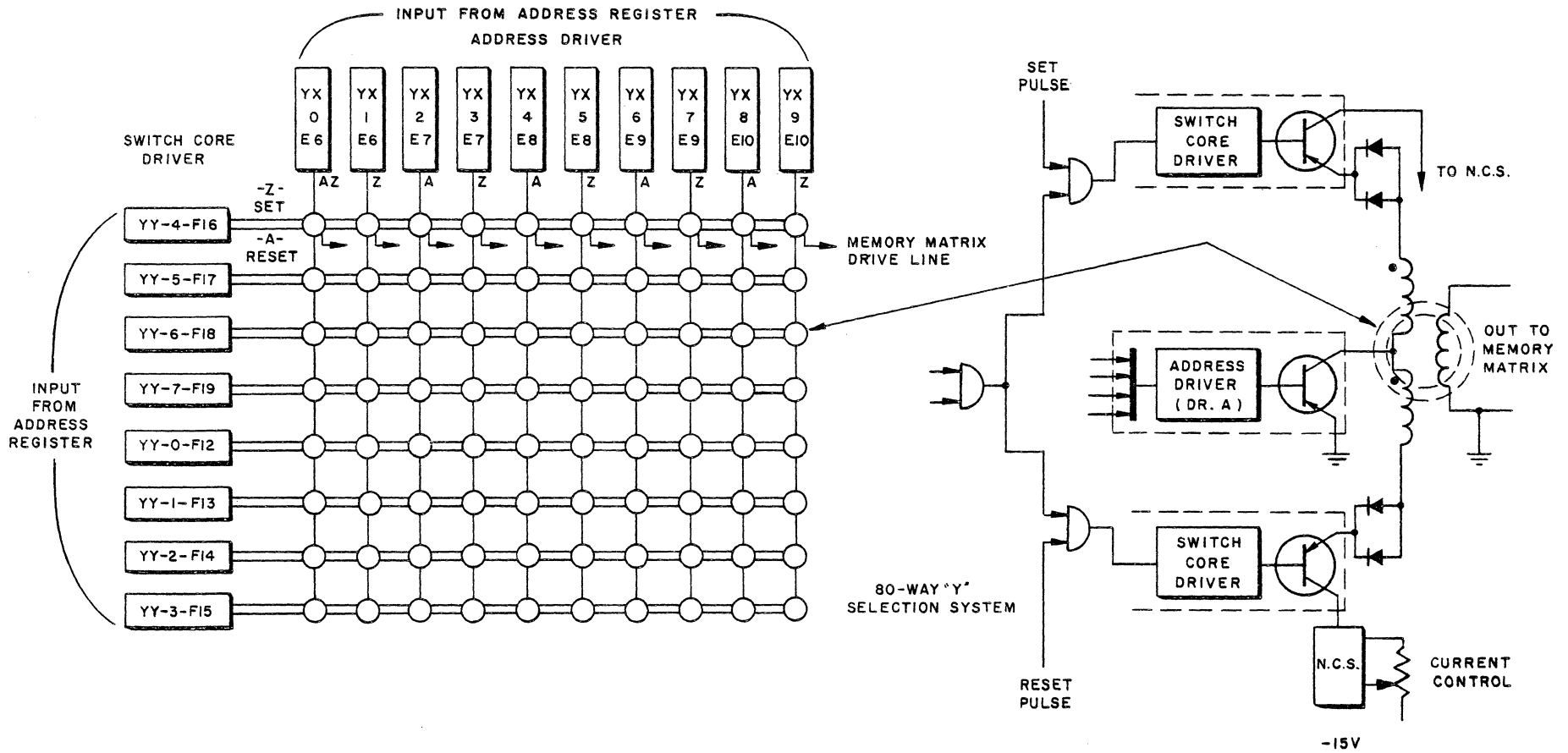
Figure 47. Method of connecting switch drivers in random-access
storage unit shown in Figure 45.

sinks and those designated as X-Y and Y-Y are standard drivers. The latter are actually transistor switches which derive a standard current from current stabilizers. Circuits are so arranged that each driver contains two circuits such as A and A' in Figure 32. The 50-way switch is driven by ten sinks and five pairs of drivers, and the 80-way switch is driven by ten sinks and eight pairs of switch drivers.

Figure 47 shows the method of connecting the switches, and Figure 48 illustrates one stage in the assembly of one of the 28 matrices used in this storage unit. The matrices are folded in order to package the 80-by-50 array conveniently.

A Typical Simple Small Buffer Storage Unit. A simplified block diagram of a small buffer storage unit is shown in Figure 49. This unit has a capacity of 144 eight-bit characters. The mode of operation used in the system was described in the section entitled Special-Purpose Switch Systems. Loading and unloading can be interlaced as desired, either operation requiring a 10-microsecond cycle. The load control and loading switch are used both to drive the storage arrays and, operating as address counters, to remember the load address. In a similar manner, the unloading switch drives the storage arrays and remembers the unload address. The digit drivers insert information into the storage arrays, and the read amplifiers obtain information from the storage arrays.

There are two ways in which the matrices can be scanned. The first of these is indicated by the matrix and switch arrangement illustrated in Figure 50. The matrix uses a configuration of 9 by 16, and is driven by a nine-way switch and a 16-way switch. Since nine and 16 are mutually prime, the two switches may count and scan the matrices in a diagonal manner. All positions will be scanned only once. An incomplete scanning diagram is shown in Figure 50 (b). By working out the diagram to completion, it will be found that ultimately all positions are scanned correctly. The buffer actually contains two sets of switches. Provided that these switches follow the same pattern and start from the same original address, the manner in which the matrices are scanned is unimportant.

Another way of scanning the matrices is indicated by the arrangement in Figure 51. The matrix in this case has a configuration of 8 by 18. Eight and 18 are not mutually prime; therefore, if the mode of scanning indicated in Figure 50 were employed, only half of the 144 cores could ever be scanned. Which half were scanned would depend on the phase of the eight-way and 18-way switches in driving

"Y" WINDING

"X" WINDING
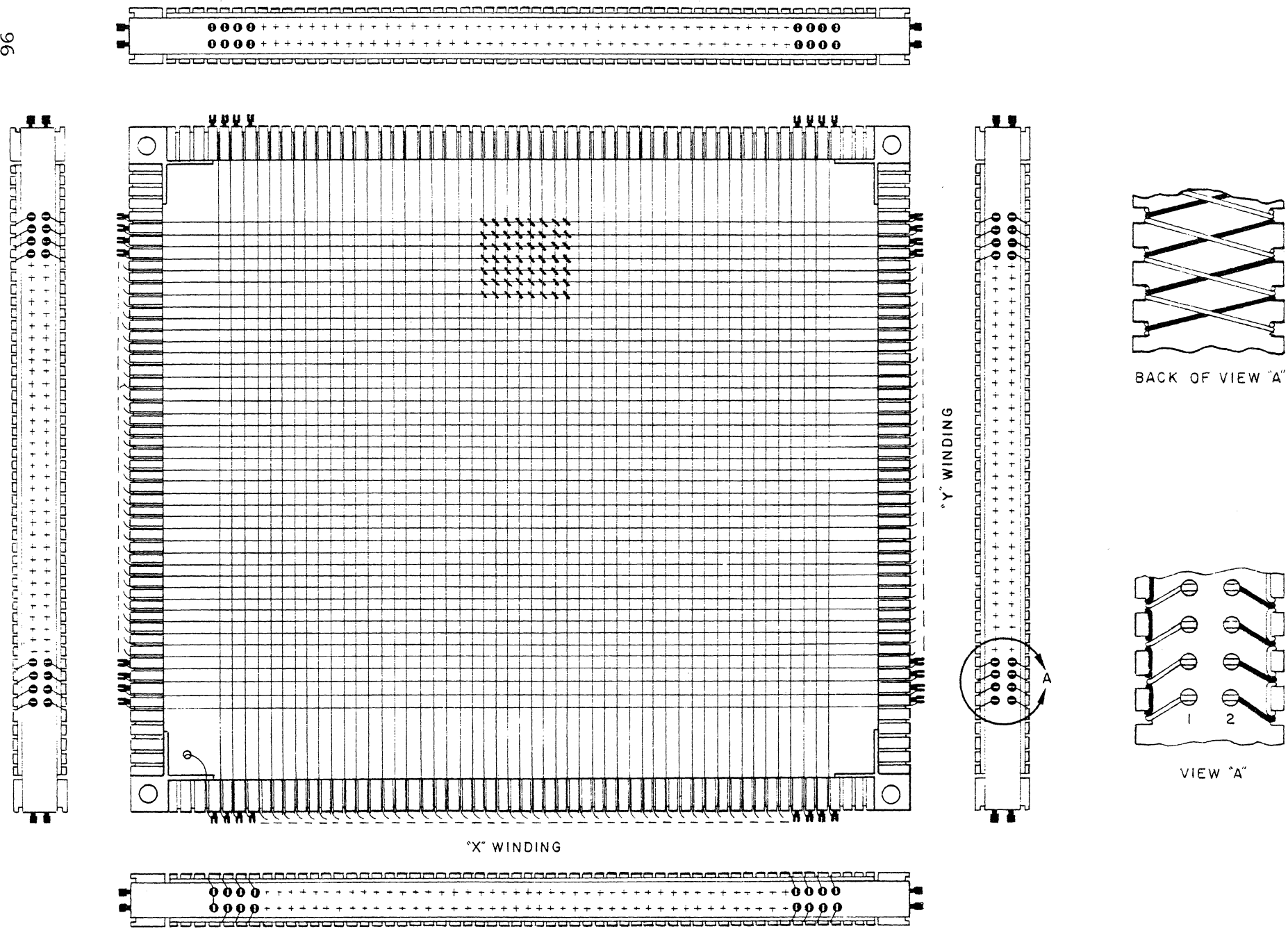
BACK OF VIEW "A"

VIEW "A"

Figure 48.   Stage of assembly of a matrix in random-access
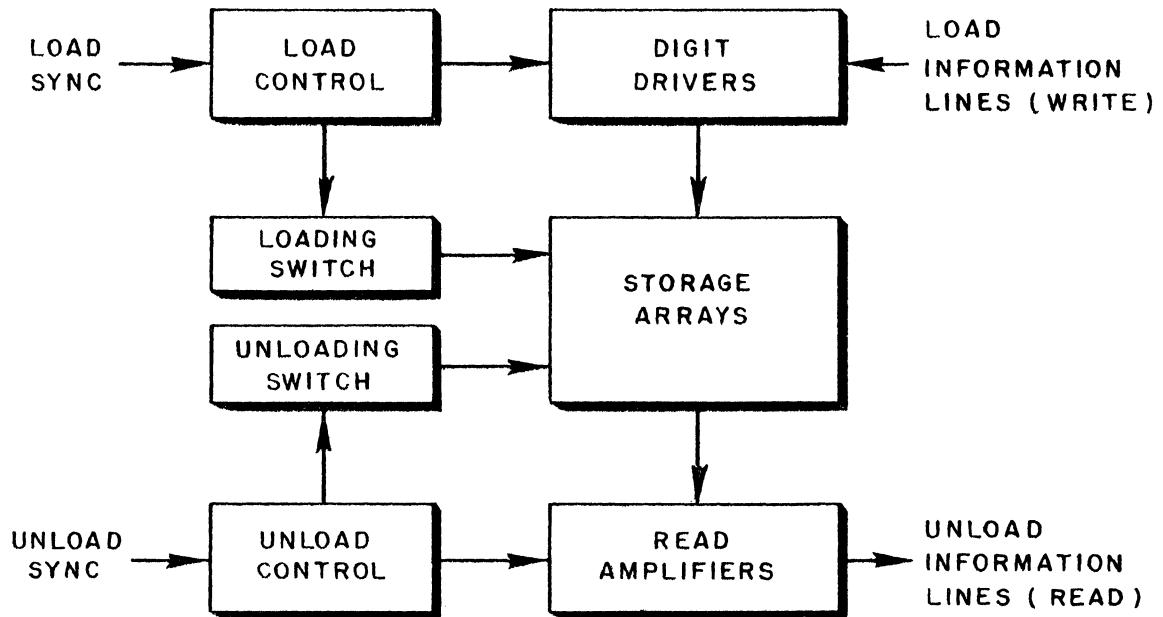   storage unit shown in Figure 45.

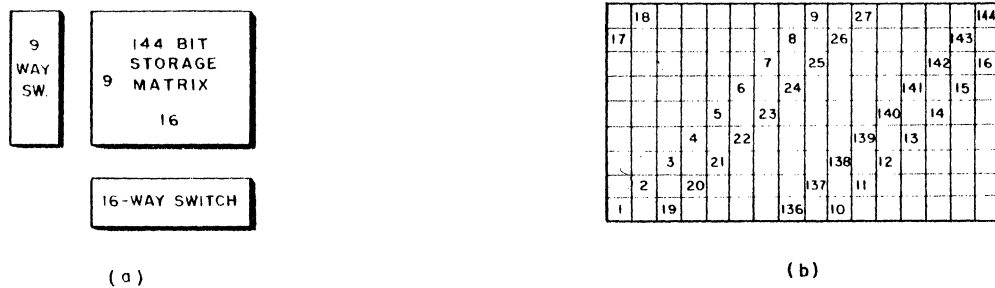Figure 49. Block schematic of a small buffer storage unit.

(a)

(b)

Figure 50. (a) Arrangement of switches and matrices in buffer storage unit shown in Figure 49. (b) Incomplete scanning diagram.

16
WAY
SWITCH

O 8
O 7
O 6
O 5
O 4
O 3
O 2
O 1

144 BIT
STORAGE
MATRIX
8
18

18-WAY SWITCH

(a)

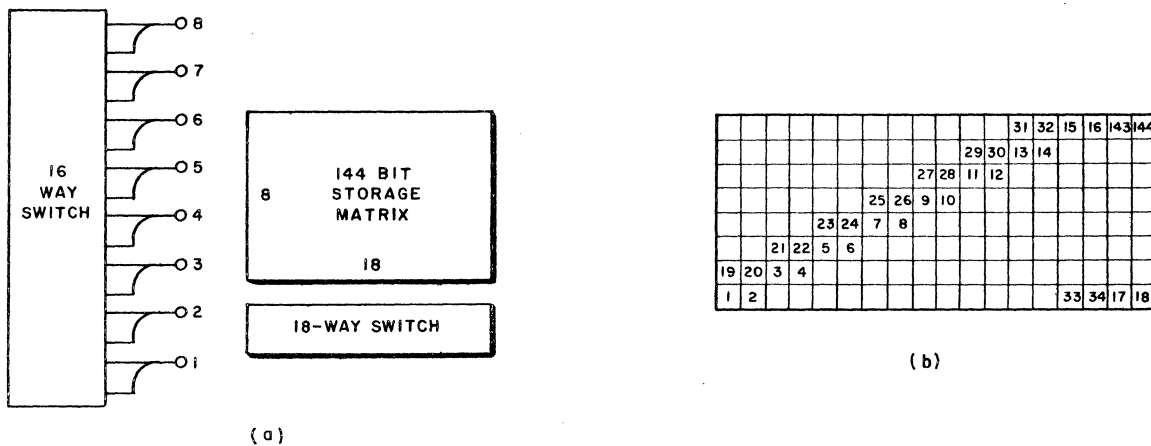| | | | | | | | | | 31 | 32 | 15 | 16 | 143 | 144 |
								29	30	13	14			
						27	28	11	12				
					25	26	9	10					
				23	24	7	8						
			21	22	5	6							
19	20	3	4										
1	2										33	34	17	18

(b)

Figure 51. (a) Second arrangement of switches and matrices in buf-
fer shown in Figure 49. (b) Incomplete scanning diagram.

the 8 by 18 matrix. It can be arranged that the eight-way switch
generates both phases by connecting each successive pair of cores
of a 16-way switch to form eight outputs. This is the system il-
lustrated in Figure 51 (a). The incomplete scanning diagram in
Figure 51 (b) shows a "staircase" shaped scan. All possible
positions in the matrix will be scanned only once. As in the
previous method, as long as the load and unload switches are of the
same type and start from the same origin, this system will operate
without indicating the type of scan being performed.

The system shown in Figure 50 is clean and simple to under-
stand. However, it requires a three-phase driver to drive a nine-
way switch and a two-phase driver to drive a 16-way switch. In the
load control there must be five drivers, three flip-flops, and a
number of gates to drive the two switches. The total for the
system is ten drivers, six flip-flops, and a good deal of logic.
Since the capacity of the storage unit is only 1,152 bits, the
number of transistors required to mechanize this many drivers,
flip-flops, and logic is unreasonably high. In the system shown in
Figure 51 both switches may be driven by a two-phase driver, and
these drivers may be in phase. It is therefore possible to use a
single pair of drivers to drive through both switches in cascade.
The unit requires only four drivers and two flip-flops and con-
siderably less logic than the system illustrated in Figure 50. Even
though the system illustrated in Figure 51 is more expensive in

terms of the number of switch cores, there is a considerable reduction in the amount of electronic equipment. It is therefore the preferred driving scheme for a small buffer storage unit.

Figure 52 shows one set of switches and drivers in a 144-bit buffer. There are two identical sets, one of which is used to control loading and the other to control unloading. Two transistor switches are selected alternately by the flip-flop shown at the bottom of the diagram. They steer current originating in a current stabilizer first to the 18-way switch and then to the eight-way switch. The latter is actually a 16-way switch connected in the manner shown in Figure 51. The current passes through the eight-way switch and then becomes the common bus for the 18-way switch. (See Figures 26, 27, 28, and 29 for illustrations of the use of this bus.) The 18-way switch then routes the current from the bus into the selected matrix line. The current is gathered together again to form the bus for the 8-way switch, which routes the current through the matrices. Finally the current goes to ground after the second passage through the matrices. In Figure 52 the shaded line illustrates a typical current path at one moment in the over-all cycle of the equipment.

Other Features Utilized in Buffer Storage Units. It is possible to use only one set of switches in operating a buffer instead of the two described above. With this mode of operation, a block of information is loaded into the buffer and is then completely unloaded without interlacing of the load and unload operations. The switches are used first to load the cores and are then cleared back to the ZERO address in preparation for the unloading operation. Using one set of switches in this operating mode is economical since approximately one-third of the electronics in the buffer storage unit may be removed.

Re-formating information is a special feature of some buffer storage units. An analysis of the magnetic core array indicates how this function may be added to the unit. The three dimensions of the core array are conventionally specified so that the X and Y co-ordinates represent the address and the Z co-ordinate represents the word length. However, if the three dimensions are considered as axes of reference, it is possible to connect switches to the X and Y co-ordinates during loading and to the Y and Z co-ordinates during unloading. Under these conditions, the information will change its format in the process of passing through the buffer storage unit. This re-formating is a typical corner-turning operation which occurs in card-to-tape conversions and in tape-to-high-speed-printer conversions. It is also possible to scan the X, Y, and Z co-ordinates
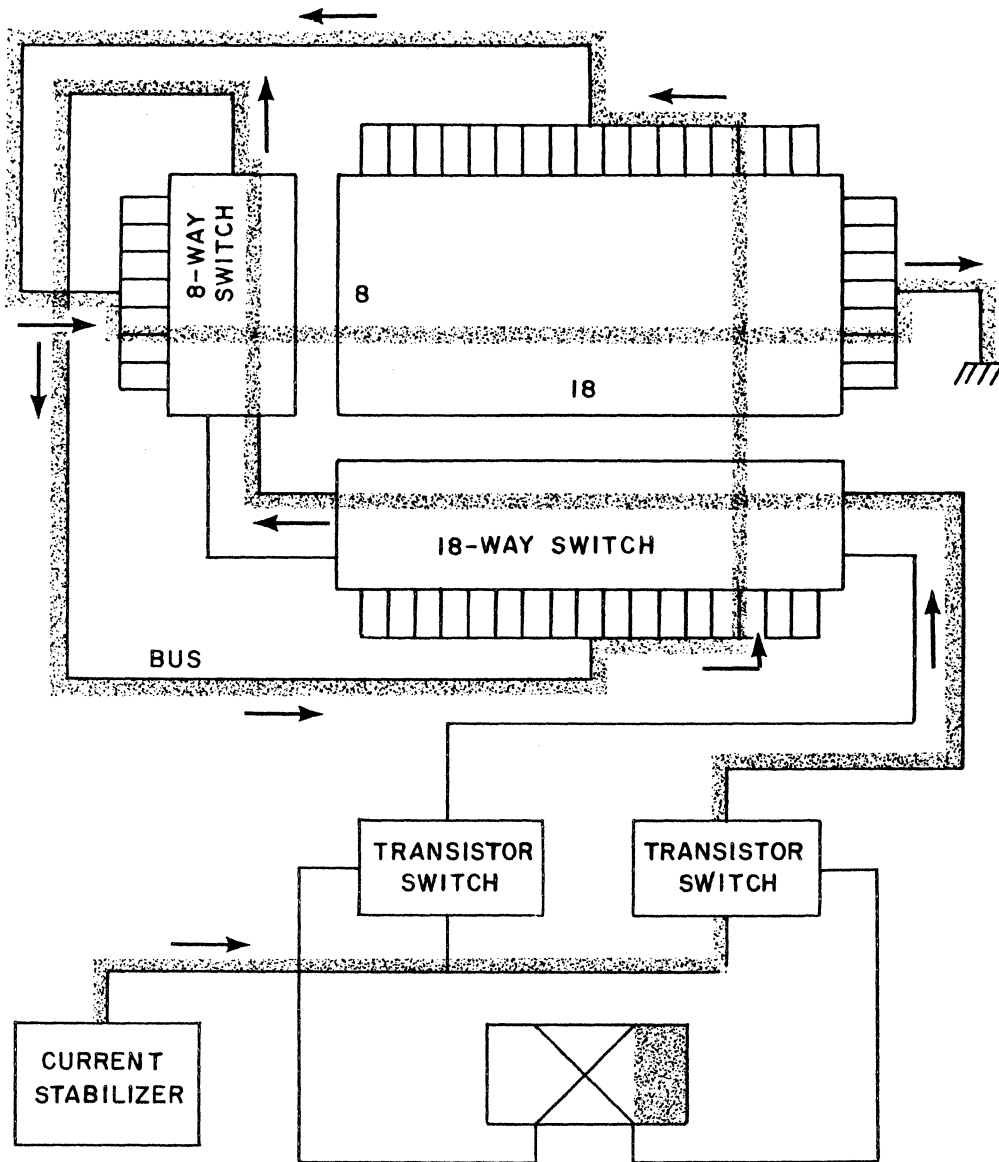
Figure 52. Typical current path in a 144-bit buffer.

simultaneously by using suitable switches. With such a scanning technique, an input in completely serial form may be read on output in parallel form. This mode of operation is useful in buffers operated in conjunction with teletype equipment where information occurs in both serial and parallel forms in different parts of the system.

The individual switch element in a buffer has both logical and storage properties. Steering switch elements may therefore be arranged to perform logical operations that are more complex than the counting operation performed in the simple buffer. Additional switches in the buffer unit may be driven from the pair of drivers which perform logical functions in order to control an input or output device.

Partial core planes may also be used to perform special functions within the buffer. One or two cores may be used as markers to indicate when a particular point in the storage operation has been reached. Incorporating such special-function cores often reduces the number of counters required outside the equipment. Special core planes may indicate when a buffer is full or empty, or even half full or half empty. This function is particularly useful in timing the operation of two devices which operate at different average rates of information flow. A typical instance is the conversion of information from one magnetic tape to another. Usually one of the tape units is faster than the other or, in the worst possible case in which variable block lengths of information appear on the magnetic tape, each of the tape units at some time can be faster than the other. Under these conditions, the system must decide whether to stop at the next inter-block gap so that the slower tape can catch up to the faster one. The half-empty, half-full type of output signal indicates to the system the approximate state of storage within the buffer. With this signal, the system can choose to stop the tape unit and can determine which of the two tape units should stop in the event that information of variable format is being handled.

A special core plane may be attached to a buffer feeding a high-speed printer. A bit is stored in this extra plane each time a print operation is performed. The signal sensed from the plane can cause another signal to be generated which informs the printer when printing is complete. The printer then stops printing and advances the paper. The signal also informs the magnetic tape unit that is should start up and feed a new block of information into the buffer storage unit.

There is a multiplicity of functions that can be added to the buffer storage unit quite simply. They are too diverse and specialized in nature to discuss in detail, but in general most of them can be designed by a serious study of the magnetic core art.

SYSTEM DESIGN OF COINCIDENT-CURRENT CORE STORAGE UNITS

Core storage units may vary greatly in size and application. A basic requirement in achieving a highly reliable and economical storage unit is an effective system design. In designing a core storage unit, one of the greatest difficulties is the initial formalization of the specification. As much as one-fifth of the time required for design and manufacture of a prototype unit may be devoted to formalizing the specification.

The designer should be guided by the following considerations in laying out a system design:

(1) A system should incorporate the least number of components necessary to perform its series of operations correctly. Careful investigation of the system design at the component level is essential.

(2) In general, the cost per bit of a core storage unit decreases as the capacity is increased and as the speed is decreased.

(3) The amount of timing and control equipment is nearly constant in all sizes of storage units.

(4) The number of address circuits per word stored decreases as the number of words increases.

(5) An increase in the amount of equipment associated with digit-plane drivers, read amplifiers, storage registers, etc., is usually required as the word length is increased.

(6) The amount of equipment increases very rapidly as the speed of operation is increased.

(7) Core materials with long turnover times are more economical in operation than those with short turnover times. The cycle time in a system includes not only the storage operating time but also time for "red tape" (setting up addresses, waiting for information to come down from the

memory register, propagation delays). In a medium-speed memory, the actual operating time of a material with a 1-microsecond turnover time is 3 to 4 microseconds, while the red tape requires 3 to 4 microseconds. If a material with twice the turnover time is used, the memory operation requires 6 to 8 microseconds and the red-tape time remains 3 to 4 microseconds. When a 4-microsecond material is used, the operating time is about 12 microseconds and the total cycle time is 16 microseconds.

(8) A sequential-access memory is more economical to operate than a random-access memory. Even though core matrices may be of the random-access type, sequential or semi-sequential access to the addresses is feasible.

Designing a system for a high-speed parallel storage unit presents no unusual problems. The cores are operated at maximum speed, and the number of parallel read amplifiers and digit-plane amplifiers corresponds to the number of parallel bits in the words stored. In some system designs, several storage units are required. They are arranged for interlaced operation to avoid time delays for regeneration in each unit. For example, two 8-microsecond units may be made to operate as one 4-microsecond unit. If all odd-numbered addresses are ascribed to one storage unit and all even-numbered addresses to the other, the system tends to use the units alternately.

In data processing systems, the flow of information is often in the form of four- to seven-bit parallel characters rather than in words of fixed length. The characters frequently flow at the rate of 4 to 5 microseconds per character. Two methods have been adopted for transmitting information in this format. The first method is suitable for storing words of variable length. One word is divided into sub-groups of four to seven characters each. A 20- to 35-bit parallel storage unit with converters at the input and output will store the words in their appropriate character format. The second method is used for storing words of fixed length. Two or more parallel storage units of 20 to 35 bits each together store the complete word. The cycles of these units are interlaced so that information can be transferred either to or from the complete storage unit in a continuous flow.

Occasionally a very long word must be transmitted in a parallel manner, but at a rather slow rate. In this case, the storage unit will take one-half or one-quarter of the word length at a time.

Information is read out in two- or four-character sequences and is then shifted into a long parallel register which presents the word in parallel to the computer.

Serial computing machines often employ a partially parallel storage unit. In designing a system of this type, the designer must try various numerical combinations of address circuits and of digit-plane and read-amplifier circuits in order to achieve the proper balance as well as maximum economy. The fact that storage units are usually parallel, even in serial machines, can be used effectively in most computer designs. Since instructions and addresses are usually required in parallel, they are transferred in a parallel manner to the computer while numerical information is transferred in a serial or semi-serial manner. Such an arrangement can increase the computing speed considerably.

In applications involving electro-mechanical devices, such as tape transports, printers, and card feeds, the storage unit may be required to operate in a slow sequential manner. Because sequential storage operation is more economical than random-access operation, it may be advisable to make minor changes in a system design to utilize sequential units. In units of large capacity the economical advantages of sequential operation are less important than in smaller units. The major cost in large units is represented by the magnetic cores, drivers and sense amplifiers, and not by the power supplies and controls. Large storage units usually have completely random properties, which can be utilized to improve the design of the computing system.

One feature of system design requiring careful attention is ease of maintenance of the equipment. The design must include provision for easy access to the components, plug-ins, suitable monitoring points, and other items of this type. A marginal checking arrangement should be provided. It should not be so complicated that the maintenance engineer must spend a great deal of time performing marginal checks on the system. If ample time is expended on solving maintenance problems at the initial design stage, it is likely that the cost of long-term maintenance will never exceed the procurement cost of the equipment.

DESIGN OF CORE STORAGE UNITS FOR ADVERSE ENVIRONMENTS

Three major problems are encountered in designing a magnetic-core storage unit to operate under adverse environments. First, it is necessary to design circuits which can operate reliably under these conditions. At present the circuit elements represent the major limitation on the extremes of environment for which the design

can be effectively completed. Secondly, it is necessary to design the circuits and magnetic-core portions of the equipment to operate satisfactorily over a wide range of temperature. And, thirdly, it is necessary to design a unit to withstand considerable shock and vibration.

The problem of designing adequate circuits is not peculiar to the magnetic-core storage unit, but special conditions are imposed by this unit in that the drive circuits must be able to handle large currents and large voltages under extremes of temperature and vibration. The best solution is to design the drivers so that they cannot operate continuously, but must operate in an intermittent pulse mode. By this means, dissipation in the unit can be reduced sufficiently for adequate operation.

Operation of a core storage unit through a wide range of temperatures presents a problem which the designer may solve by one of three approaches. The first is to enclose the cores in a temperature-controlled box which will operate at the maximum temperature encountered in the system. A disadvantage of this technique is that time is lost in heating the box to the correct temperature before operation of the storage unit can begin. A second approach is temperature compensation of the entire system to automatically adjust the current to the correct value for any temperature encountered during operation. A third technique which has been successful is to combine heating of the core storage unit and temperature compensation. This approach allows the equipment to be at a low temperature and to be compensated continuously while the storage unit is being heated. When the final operating temperature is achieved in the core matrices, the equipment then operates as a temperature-regulated system. The advantage of this compromise approach is that the system can be switched on quickly and will operate instantaneously.

It has been found that if information is stored in a core which is cycled to extremes of temperature of about 100°C, the flux state in the core is decreased by approximately 1 or 2 per cent for each complete temperature cycle. This loss of flux is significant only if the storage unit must retain its information without regeneration through many temperature cycles. Since this condition is encountered rarely, a temperature-compensation scheme is usually the most adequate approach to the temperature problem.

Under conditions of excessive vibration or shock, the conven-

tional open-wired type of matrix construction is ineffective. Cores should not be encapsulated in a solid plastic because the stress applied to them at the point of contact with the plastic changes their electrical characteristics materially. Furthermore, cores should not be constricted during their electrical operation because magneto striction changes the size of a core abruptly during the transition from one flux state to another. Cores must be cemented or encapsulated in a flexible compound which allows them freedom of movement during magnetostriction and which does not impose any stress on them during the encapsulation process. Satisfactory matrices may be constructed by two techniques.

The first is to cement each core with a flexible plastic into a small hole in a plate. The plate should be made of aluminum or some other highly conductive metal. It is particularly important to keep the stack of cores at a uniform temperature to insure that noise is not introduced by temperature variations in the stack. The cores are then wound by a sewing technique rather than the usual 45-degree winding. This sewing technique is more expensive, but has the advantage that the entire aperture of the core is available for windings rather than the small elipse available with the 45-degree type of winding. Much smaller cores may be used in this array construction than in an ordinary mat construction. Using cores a fraction of a milligram in mass, it is possible to fabricate a very small, compact storage array which can stand large amounts of vibration and shock.

The second technique is to cement conventionally constructed mats with a flexible cement onto aluminum or other conductive plates. The plates and their assembled mats are bolted together in a package, to which terminals and interconnecting wiring are added. The whole unit is then impregnated with a suitable plastic to form a solid, rugged core stack. Arrays constructed by this second technique are cheaper but less reliable under conditions of excessive vibration and shock than the smaller, lighter arrays constructed by the first technique.

Mechanical stress on cores alters their electrical properties. In fact, high vibration or shock can render a core storage device useless. Particular care must be taken in the design to insure that minimum resonance is associated with the magnetic portions of the equipment. The flexible cement used in encapsulating magnetics must be of a type which reduces the impact under shock.

Although magnetic cores are not completely ideal elements for

use in adverse environments, they introduce fewer problems than most other storage mediums or even most electronic devices. The techniques described above enable a designer to devise units which will operate reliably under extremes of environment.

TESTING OF MAGNETIC-CORE STORAGE UNITS

There are two types of test that must be performed on a magnetic-core storage unit. The first are design tests which are performed to ensure that design specifications have been met completely and properly. The second are tests that are performed on the production units.

Most of the design tests are conducted throughout the period of design of the equipment with the intent of achieving maximum tolerance for each component. The final design tests are made under conditions which simulate as closely as possible the final operation of the equipment. It is rarely sufficient when conducting these tests to connect the memory unit to the computer, because of the difficulty of programming the computer to simulate worst-case operating conditions. In actual operation a computer can generate a condition that is much worse than a calculated worst-case condition. For this reason, the design acceptance tests should be highly flexible and very stringent. They should aim for performance under conditions that are more severe than the predicted worst-case conditions. Thus, the designer can be reasonably sure that unpredictable worst-case conditions encountered in using the memory will not cause failure of the equipment. Design acceptance tests should include temperature tests, marginal tests, and as many program checks as can be performed. It is advisable to use a special testing device rather than the computer for performing design tests. With the special tester, it is possible to program rates of operation in excess of computing rates of operation and also to program very slow rates, which are difficult to attain in the average computer.

The production tests are of an entirely different nature than the design tests. They start with incoming inspection of the components. All components are rigorously tested to ensure that they have no areas of incipient failure and that they are within the design tolerances. Every magnetic core used in the equipment is checked against a well specified set of test conditions. The components are then combined into basic sub-assemblies, which are tested thoroughly for possible damage during the assembly process. Present design practices allow for large end-of-life tolerances in

components. For this reason, an operational test of the basic sub-assembly is usually insufficient. An adequate test can be performed only on the individual components to ensure that they are still within tolerance after sub-assembly. The individual core matrices, for example, are rarely tested by dynamic methods. Each core in the matrix is tested individually to ensure that no more than a maximum specified degradation has occurred in the assembly process. At the same time, the windings are checked to make sure that every winding links every core in the correct direction. The purpose of the tests is not to determine whether the sub-assembly works but to check that the components have not been damaged. In a similar manner the frame of the memory is checked to ensure that all wiring is correct and that any components included as part of the frame have not been damaged during assembly.

Theoretically, at this point all sub-assemblies could be plugged into the main frame and the unit would work perfectly. If the unit is tested and found inoperable, the quality-control procedure up to the point of final assembly is in error. If the system design incorporates very large end-of-life tolerances, it should be difficult to cause the new equipment to fail during initial testing. A final series of marginal and functional tests on the completed unit are usually performed under adverse environmental conditions.

MAINTENANCE OF COINCIDENT-CURRENT STORAGE UNITS

Maintenance of early tube-driven core storage units was excessive. To reduce the time and simplify the techniques for maintaining equipment, an engineering maintenance panel was added to each unit at considerable cost. High computational reliability could be achieved only with specified maintenance once in eight hours or, for some units, once in 24 hours. Most of these early tube-driven units that were well designed and maintained properly are still operating with an error probability close to one per thousand hours of computing time.

The introduction of transistor drive and the improvement in tolerancing and design techniques have contributed to the development of storage units of much higher reliability than the earlier equipment. Maintenance requirements of the newer storage units may be divided into three categories. First-level maintenance is applied to large random-access coincident-current units operated in conjunction with data processing equipment. The second level is required for small units or buffer storage units used in special-

purpose computing equipments. Third-level maintenance is used for very small units, usually buffer storage units, combined with computing or other digital equipments.

First-level Maintenance. The storage unit is equipped with facilities which allow changes in supply levels and operating currents for purposes of marginal checking. Programming the equipment for marginal operation is accomplished by generating an information flow into the storage unit most likely to cause failure. If a unit fails during a scheduled marginal check, the component which caused failure is immediately replaced. The frequency of periodic first-level maintenance and the type of tests performed depend on the reliability of the equipment design and will vary widely for different types of equipment. Large units need more frequent maintenance than small ones. New equipment requires a short period between scheduled checks, which may be gradually lengthened as the equipment ages. Scheduled maintenance about every 50 hours is advisable for most new equipments; for older equipments, a schedule of checking once in 200 to 500 hours is adequate.

Second-level Maintenance. Second-level maintenance is applied to small, rather reliable units which are incorporated in moderately complex, special-purpose, data-processing devices. Since devices of this type usually are operated in an "off-line" manner, parity checks are performed while information flows through the equipment. The storage units are equipped with rather primitive means for marginal checking. They may also be equipped with a simple test device which permits checking of the unit without operating the whole equipment.

Maintenance is performed infrequently, usually at a periodicity such that the probability of error between scheduled maintenance periods is relatively high. A probability of 0.2 is considered sufficient. Maintenance may be scheduled only once in three months to a year. Periodicity of maintenance and the nature of the tests that are performed vary widely for different types of equipment, depending on their size and the general reliability of their design.

Third-level Maintenance. Units which are subjected to third-level maintenance are very small and highly reliable. Under their operating conditions, scheduled maintenance is difficult to perform and an occasional error may be tolerated. Often an error-checking device may be used to indicate when the frequency of errors within the unit has risen to a dangerous level.

Third-level maintenance is not scheduled maintenance at all. Whenever observation of the device indicates the occurrence of a

large number of errors, maintenance is performed to eliminate the defective component or sub-assembly. Frequently at this level of maintenance, no attempt is made to replace a component that has failed; instead the defective sub-assembly is located and replaced by a new one. Such an approach to maintenance is not very costly because units of this type are so reliable that the probability of failure is less than once in six months to a year.

Maintenance of Future Storage Units. The magnetic core storage art is rapidly approaching the point at which a fourth level of maintenance can be introduced. If a storage unit is so inherently reliable that the whole package may be considered a single sub-assembly, in the event of failure the entire device may be discarded and replaced by a new one. This type of maintenance can be economically introduced when the unit is small and when the frequency of failure is once in three to five years. At present, the frequency of failure in transistor-driven storage units is once in six months to two years in equipment containing one hundred to three hundred transistors per unit. Highly reliable core storage units with less than fifty transistors per unit will undoubtedly be designed in the near future. A probability of failure of less than once in three to five years can be expected of these future units. At that time, fourth-level maintenance will be more economical than having available trained personnel who can perform the three other levels of maintenance.

NON-DESTRUCTIVE READ-OUT

One of the disadvantages of coincident-current operation of a core storage unit is that information is destroyed during reading and must be rewritten. Reading time is long and loss of information, during transfer from an electronic register and back to the core matrix, may occur. In most computing applications, reading occurs more often than writing. Therefore, the shortened reading time implicit in non-destructive read-out would greatly increase computational speeds. Another disadvantage of coincident-current operation is that information is read out as a single short pulse. Non-destructive read-out would allow repeated interrogation of a core to provide a continuous output.

If a non-destructive reading method is to replace the present destructive method, it should satisfy the following requirements:

(1) Reading time should be short.

(2) Writing time should not be much longer than that required by presently used methods.

(3) The method should be adaptable to storage units of large capacity.

(4) The fabrication cost of a non-destructive system should not be much greater than that of destructive systems.

To date no method which is likely to meet all four requirements has been proposed. Three methods which will be useful in restricted applications are R-F sensing, read-out based on the quadrature-field principle, and read-out using cores with secondary apertures. It is too early to evaluate the merits of these three approaches to non-destructive read-out since no complete system incorporating any one has been constructed yet.

R-F Sensing. Radio-frequency sensing is a non-destructive method of sensing the static state of the magnetic field in a core. The characteristics of the minor loops of a core are different for the ZERO and ONE storage states. A phase change or inversion, a beat frequency, or other similar effect is used to detect the state of a selected core. The disadvantages of using radio frequencies for read-out are that the technique operates on second-order characteristics and that it has not yet been found successful in interrogating core matrices of any reasonable size.

A pulse method for accomplishing non-destructive read-out has been developed recently. Two cores connected in opposition to the sense winding are used for each bit. This arrangement cancels the first-order characteristics and allows the secondary effects to be sensed directly. In order to interrogate a core, a low-current pulse of short duration (a few millimocroseconds) is applied to the core pair. A short pulse is obtained in the sense winding. Depending on the method of connecting the cores, it is possible to differentiate between states either by the polarity of the sense winding output or by the presence or absence of a pulse in the sense winding. At present this technique can be used only in linear-selection storage units of small capacity.

Read-out Based on Quadrature Field. Figure 53 (a) shows a core which is saturated in a direction around the toroid. A solenoid tends to magnetize the core in a direction perpendicular to the original direction of magnetization. Because the material is already in a saturated state, it cannot be further saturated.

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As shown in the vector diagram in Figure 53 (b), the resultant vector is not the vector sum of the two fields but is the original vector rotated through an angle to form the quadrature field. The rotation causes a reduction of flux around the toroid. If the field was in the opposite direction originally, there would be an algebraic increase of flux. The output of a sense winding through the core is a positive pulse for a ONE and a negative pulse for a ZERO. When the quadrature field is released, the core returns to its original state.

A system operating on the quadrature-field principle is truly non-destructive. Cycle times are short and the output pulses produced are of large amplitude and opposite polarities. It is possible that a non-destructive read-out technique based on quadrature field may be developed from the dipole switching mode used to operate some experimental thin-film storage devices. At present, the switching rate of cores used in this mode is so high that it has been impossible to produce pulses of sufficiently short duration to disturb the cores without switching them.

Recently special ferrite cores have been manufactured with two apertures in orthogonal directions. One aperture is used in a conventional storage manner, and the other is used to produce the quadrature field. Although these cores now require large operating currents and are relatively complex to manufacture, they offer considerable promise for a satisfactory non-destructive read-out technique in the future.

Read-out Using Cores with Secondary Apertures. A non-destructive technique may be used to interrogate a storage core which has several possible flux paths. A core with an additional small aperture will have more flux paths than one with a single aperture. For example, there are three flux paths in the core illustrated in Figure 54 (a). The area of path 1 must be greater than the sum of the areas of paths 2 and 3. A flux path encircling the small aperture must be much shorter than a flux path encircling the large aperture.

A large mmf is applied to the core by means of one or more windings through the large aperture only. The entire core is saturated in one direction as illustrated in Figure 54 (b). A winding through the small aperture can cause no change of flux around that hole unless the applied mmf is large enough to change the flux in path 1. A sense winding through the small aperture will produce no output when the core is in this state, and the core

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is said to be blocked. If an mmf in the reverse direction to the original blocking mmf is then applied by means of windings through the large hole, the field in the core will tend to be reversed. If the second mmf is increased slowly, there will be no action until a threshold value is reached. Then part of path 1 and all of path 2 will be reversed and, after another threshold, path 3 will be reversed. The first threshold is caused by rectangular characteristics of the core. The second threshold is caused by the increase in mmf needed to switch path length 1, 3. Because path length 1, 2 is shorter than path length 1, 3, more mmf is required to switch path 1, 3 than is required for path 1, 2. These parameters can be adjusted by varying the material and geometry of the core. The thresholds in paths 2 and 3 can be far enough apart for all practical purposes. When path 2 has been reversed and path 3 has not, the core is said to be unblocked (Figure 54 (c)). If an alternating mmf is applied by means of a winding through the small aperture, an output will appear on a sense winding through that aperture. The direction of magnetization in paths 2 and 3 will reverse continuously, but the unblocked condition of path 1 will not be changed by the interrogating action.
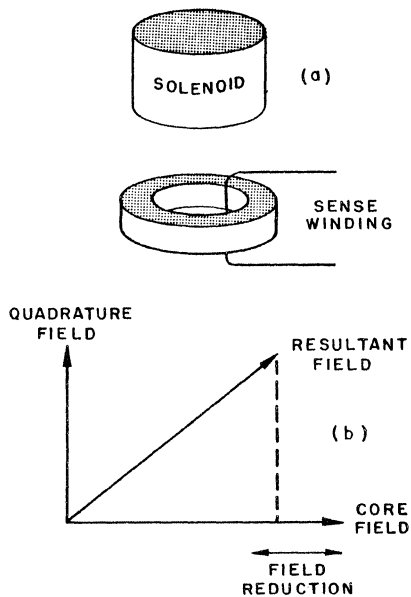

Figure 53. (a) Toroid being magnetized by a solenoid. (b) Vector diagram of quadrature field.
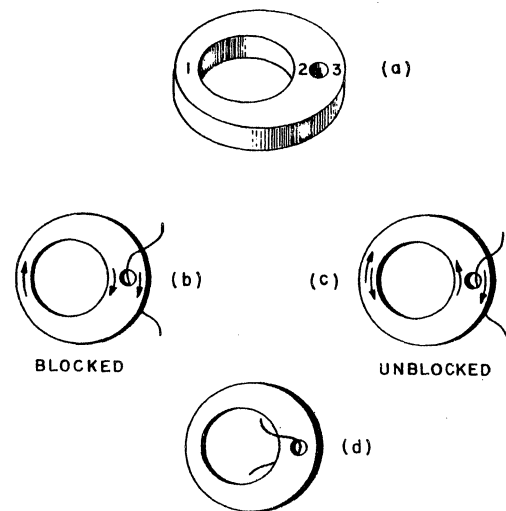

Figure 54. (a) Flux paths of core with small and large holes. (b) Blocked core. (c) Unblocked core. (d) A method of unblocking core.

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The core can also be unblocked by an mmf applied to a winding linking both holes (Figure 54 (d)). A large mmf is needed in order to reverse the path length between 1 and 2. There is only one threshold with this type of winding. The direction of magnetization of paths 2 and 3 cannot be reversed.

Since both the large and small apertures have storage-type thresholds, it is possible to wind cores of this type in a double coincident-current matrix. One matrix links the large holes of all the cores, and the other matrix links all the small holes. The first matrix is used for writing and the second for reading. In order to write, currents are applied to the selection wires of the write matrix and the cores are blocked. Then, if desired, current is applied in the reverse direction and the cores are unblocked. The blocking current should be somewhat larger than the unblocking current. In order to read, coincident currents are applied to the read matrix in a direction which will reverse the magnetization around the small hole, and then the currents are reversed to restore the original direction of magnetization.

A system of this type is truly non-destructive, but it has three disadvantages. First, the cores required must be larger than those used in destructive systems and, consequently, the power required for a writing action is increased. Secondly, it is necessary to wind the cores in a matrix consisting of a double mat of wires and to drive the mats separately. This leads to an increase in costs. Thirdly, read-out time is longer than that of a quadature-field system because two pulses are required for each output. Furthermore, the device operates as a result of flux transference between paths 2 and 3 with consequent slow domain-wall movement. The minimum read-out time is about twice the characteristic switching time of the material plus red-tape time for setting up the reading matrix. In practice, complete flux transference between paths 2 and 3 is not necessary. Operating time can be shortened by employing non-coincident current in the reading and writing cycle. Using very large non-coincident currents for interrogation, it is possible to sample the core in about one normal switching time of the core material. A one-microsecond material, for example, can be interrogated at the rate of a megacycle.

Non-destructive read-out with secondary-aperture cores has been successful in small storage devices where continuous access to stored information is essential. More significant is the application of

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this technique in the work being done on transfluxors and multi-aperture devices (MAD). This work has contributed to the development of highly sophisticated, all-magnetic forms of logic and shift registers.

FUTURE CORE STORAGE UNITS

The development of the magnetic-core storage unit has been in the direction of faster operation and larger capacity. It can safely be predicted that storage devices will operate at a cycle time of much less than 1 microsecond within the next few years. These devices will find applications in millimicrosecond computers which will probably be the next generation of scientific machines. Data processing machines will require core storage units of large capacity which can be driven by low power. Power requirements have been markedly decreased since the first storage units were introduced. Present transistor-driven units require one-tenth the power required in the earlier tube-driven units. Research is in progress to design magnetic core drivers which are controlled by lower-powered transistors than those in use today. Future units will probably need no power transistors but will rely on high-frequency ac lines for driving the magnetic elements. Only control functions will be performed by transistors. Core-diode-transistor logic which has greatly reduced the number of transistors required in a storage unit has already been developed.

A continuous trend in the design of core storage units is the reduction of physical size. Initially units were excessively large and unsuitable for use in mobile equipment. By developing more closely packed matrices, designers have been able to produce very compact units. Storage units employing a packing factor in excess of 50,000 bits per cubic foot including address circuits and memory register are now available. Considerably higher packing factors can be achieved in the future.

Future core storage units will probably be either fairly large, very high-speed devices requiring many transistors or large-capacity, compact, slow, reliable units requiring few transistors. There will undoubtedly be intermediate units of medium capacity which will be highly reliable and compact for mobile use.