

INTERNATIONAL UNIVERSITY SCHOOL OF ELECTRICAL ENGINEERING (EE)

**ELECTRONICS DEVICES LAB**

**Lab 2**

Operational Amplifiers

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# Objectives

This lab introduces the operational amplifier or "op amp". The circuit is already constructed for you on a single IC (integrated circuit) and in this lab we will use the IC in several of its most popular configurations

# Introduction

Ideal operational amplifiers (Op-Amps) are two-ports that can produce an output voltage which is directly proportional to their input voltage (linear operation). Op-Amps can be operated in two ways: open loop and closed loop. The latter circuit connection is the only one that can force the Op-Amp to operate in its linear region. An *equivalent circuit model* can be used to model or simulate the ideal Op-Amp or to incorporate deviations from ideality. The standard *inverting* and *non-inverting configurations* are explored.

The lab experiments include the realization of both configurations and the experimental determination of the circuit parameters that demonstrate the function of the circuit and allow for Op-Amp parameter derivation.

# Theory

## Operational Amplifiers

* 1. **Op Amp Terminal Characteristics**

A 741 Op-Amp is shown in Fig. 2 below. Op-Amps have two input terminals; the input voltage Vi to the Op-Amps is taken across these terminals. One terminal is called inverting or negative and the voltage there is usually denoted as Vn and the other as non-inverting (Vp) so that Vi=(Vp-Vn). The output is taken between Vo and ground. Additional terminals (such as V+ or +Vcc, V- or -Vcc) are used for bias, offset etc.

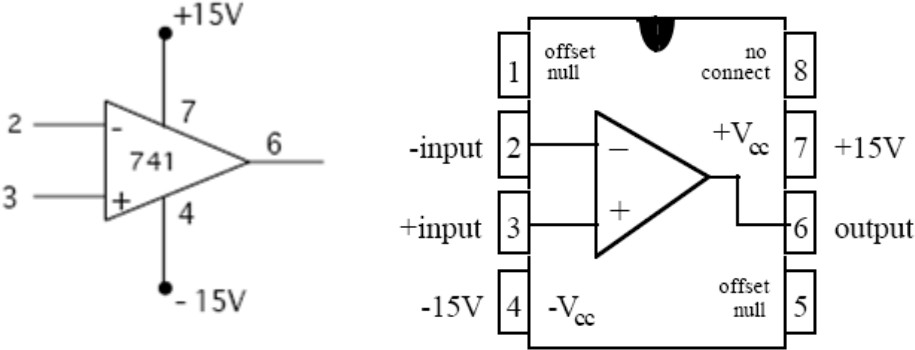


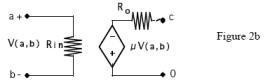
Figure 2: Pinout for the 741 Opamp

The realistic model of an operational amplifier is given in your text and repeated below with equivalent notation. It involves separate input and output circuits. The input consists of an input resistance Ri between the inverting and noninverting terminals. The output consists of a voltage dependent voltage source (with voltage AvVi) in series with an output resistance Ro. Note that the only connection between the input and output is through the proportionality relation of the dependent source.

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The parameters involved are as follows:

1. **Input Voltage Vi:** V(a,b)=Vi=(Vp-Vn).
2. **Output Voltage Vo:** The output voltage of an Op-Amp is proportional to the input voltage, provided it remains less in absolute value than the DC bias voltages V+ and V-.
3. **Input Resistance Ri :** The input resistance appears between the inverting and noninverting terminal (so that Vi appears across Ri) and can be found by dividing the input voltage Vi by the current entering the non-inverting input terminal Vp or exiting the inverting terminal Vn.
4. **Open Loop Voltage Gain μ or Av:** The open loop voltage gain is the proportionality constant in the dependent source equation where V = AvVi (or V=μV(a,b)).
5. **Output Resistance Ro:** The output resistance appears as a resistor in series with the dependent source. In the presence of a non-zero output resistance Ro, the output voltage across a load RL is not all of V = AvVi and can be found by analyzing the voltage divider between Ro and RL.

## Linear Operation and Saturation

Op-Amps have two regions of operation: *linear* and *saturation*. In the *linear region*, the *voltage transfer characteristic*, i.e. the mathematical relationship between the input and output voltages, is linear. This holds true when the output voltage lies in the range



From the definition of voltage gain given above, i.e. Vo = AvVi, one can see that this range corresponds to input voltages in the range of



Av.

In this range the output voltage is directly proportional to the input voltage, by the factor

For input voltages outside this range, the Op Amp is said to be *saturated*, and its

output is bounded by the DC bias voltages. In other words, the output voltage is clamped to V- when Vi<V-/Av and to V+ when Vi>V+/Av.

## Characteristics of an *Ideal* Op-Amp

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1. **Ri = :** According to the definition of input resistance given above, an infinite input resistance means that no current flows into or out of the input terminals. This greatly simplifies the analysis of Op-Amp circuits.
2. **Ro = 0:** In this case the entire dependent source voltage appears across the load resistance or as the input of another device.
3. **μ =AV =** : If the output voltage is to be finite it follows from the definition of voltage gain, that Vi = Vo / Av will go to zero if Av is infinite. This, however, assumes that there is some way for the input to be affected by the output. Indeed this will only happen if there is such a connection namely a *negative feedback mechanism* in the form of *a connection between the output and the inverting terminal* (closed loop operation). If such connection does not exist, then the output will be saturated (open loop operation). For closed loop operation, it is said that a *virtual short* exists between the positive and negative input terminals. This means that if an Op-Amp is operating in its linear region (if it is *unsaturated*) then Vi 0, or equivalently Vp Vn. This also simplifies the circuit calculations at the input terminals, because Vp and Vn can be represented by a single variable. When one of the two terminals is grounded, then the voltage at both terminals is zero and the other terminal is called a *virtual ground*.

## Building Amplifier Circuits Using Op-Amps

There are two standard closed-loop connections for an Op-Amp. Both have in common the connection (Rf) from the output terminal to the inverting input terminal. This connection provides *the negative feedback* and ensures the virtual short. The analysis is simple for *ideal* Op-Amps since:

1. the two input terminals are at the same voltage and
2. there is no current into the input terminals.

The analysis usually derives a gain or amplification. It is important to note that this is the gain of the *whole stage* (or the closed loop gain) and should not be confused with the gain of the Op Amp alone.

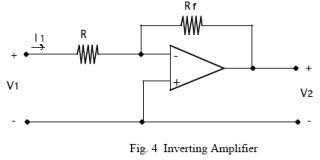
One last note: negative feedback does not guarantee that the amplifier will not saturate. If the input is such that the output, based on the amplification of the whole stage, is expected to be larger than the bias voltage in absolute value (Vo> V+ or Vo< V-) then the output *will* be clamped to V+ (or V-).

## The Inverting Amplifier

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Circuit analysis of the inverting amplifier in Fig. 4 yields the equation,

V2 = K V1 = (-Rf/R)V1 (1)

Thus, the theoretical gain K of the whole stage (that is, the entire Op-Amp circuit of Fig 4.) is given by

K = V2/V1= (-Rf/R).

## 3.4.2. The Non-Inverting Amplifier

Circuit analysis of the non-inverting amplifier shown in Fig. 5 yields the equation,

V2 = (1+Rf/R)V1 (2)

Thus, the theoretical gain K of the whole stage is given

by K = V2/V1= (1 + Rf/R).



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# Pre-Laboratory

## Experiment 1

* 1. Calculate the gain K for the inverting amplifier circuit in Fig. 8 (from section 5.1 below) assuming that the Op-Amp is ideal and using the resistance values specified in 5.1.1.

Perform a DC Voltage Sweeping on Fig.8 Circuitry with the following parameter: Start voltage: -15V

End voltage: 15V Increment: 0.5V

Put the input voltage and output voltage in the same graph. You should get the similar result as the picture I provide to you at the end of the manual. Observe and comment on the working of 741.

## Experiment 2

* 1. Calculate the gain K for the non-inverting amplifier circuit of Fig. 9 (from Section 5.2 below) assuming that the Op-Amp is ideal. The answer should be in terms of R and Rf.
  2. Given the results of question 4.2, calculate the values of R and Rf that produce a circuit gain of 10 and a voltage Vo = 0.5V when Vs = 5V.

Perform a DC Voltage Sweeping on Fig.9 Circuitry with the following parameter: Start voltage: -15V

End voltage: 15V Increment: 0.5V

Put the input voltage and output voltage in the same graph. You should get the similar result as the picture I provide to you at the end of the manual. Observe and comment on the working of 741.

## Experiment 3

Plot the waveform for Fig.10 Circuitry. Put the input voltage and output voltage in the same graph for each case of 500Hz sine wave, triangle wave, and square wave inputs.

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# Laboratory

## Required equipment:

Electronic board with Power Supply Digital Multimeter

741 Operational Amplifier 10KΩ, 100KΩ, 2.2KΩ Resistors

## Experiment 1: Inverting Amplifier

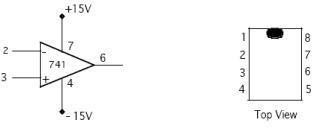


Fig. 7 Op Amp 741

You will be using the "741" Op-Amp which is biased at +12V and -12V. The chip layout is shown in Fig. 7. The standard procedure on such chip packages (DIP15) is to identify pin 1 as the one to the left of the notch in the chip package. The notch always separates pin 1 from the last pin on the chip. In the case of 741, the notch is between pins 1 and 8. Pins 2, 3, and 6 are the inverting input Vn , the non-inverting input Vp, and the amplifier output Vo respectively. These three pins are the only three terminals that usually appear in an Op-Amp circuit schematic diagram.

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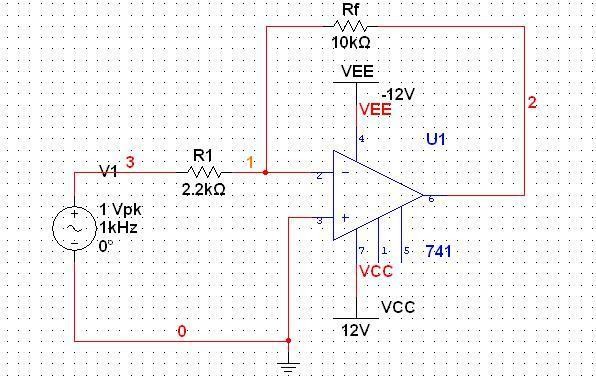


Figure 8

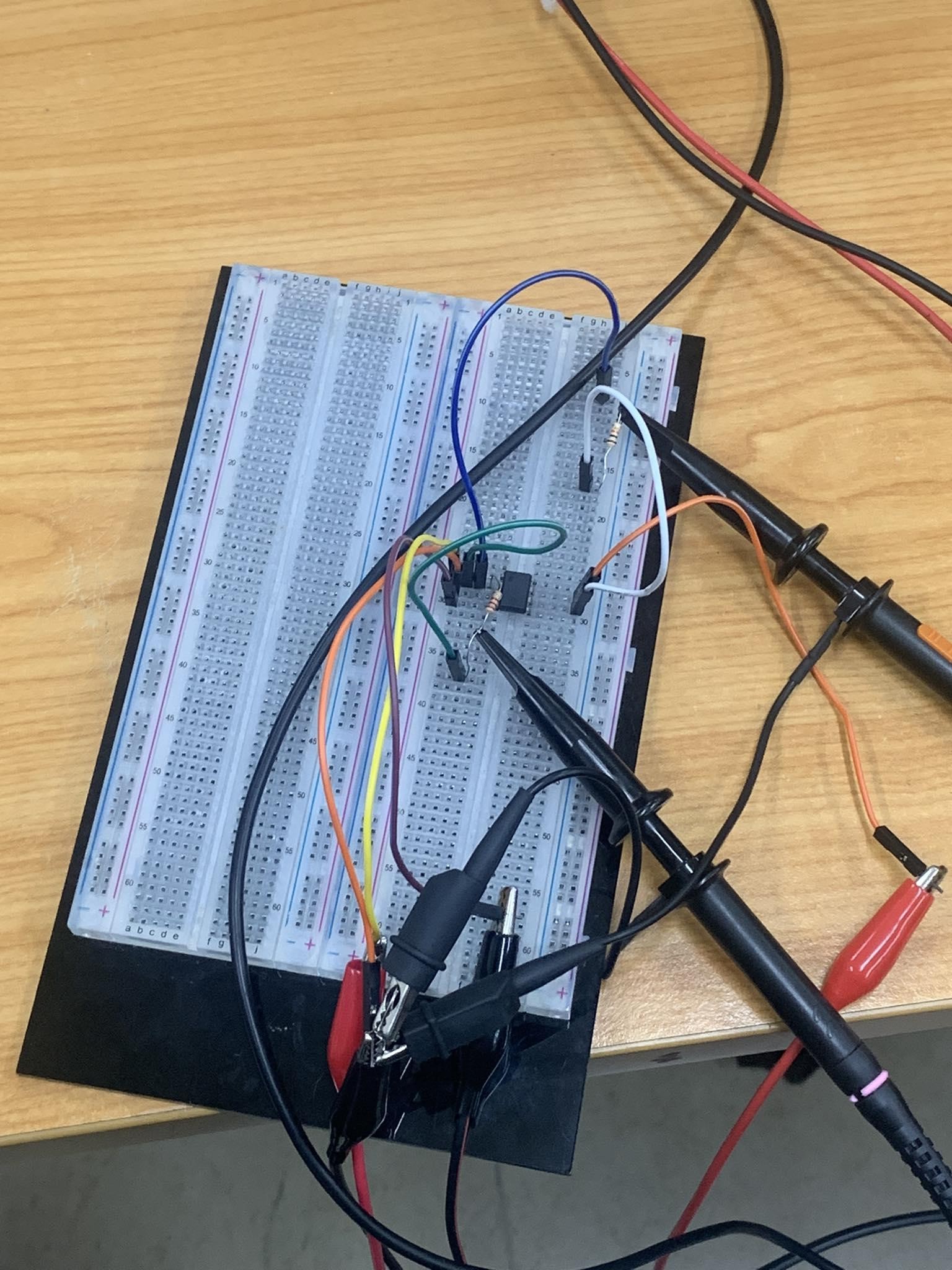
## Procedure

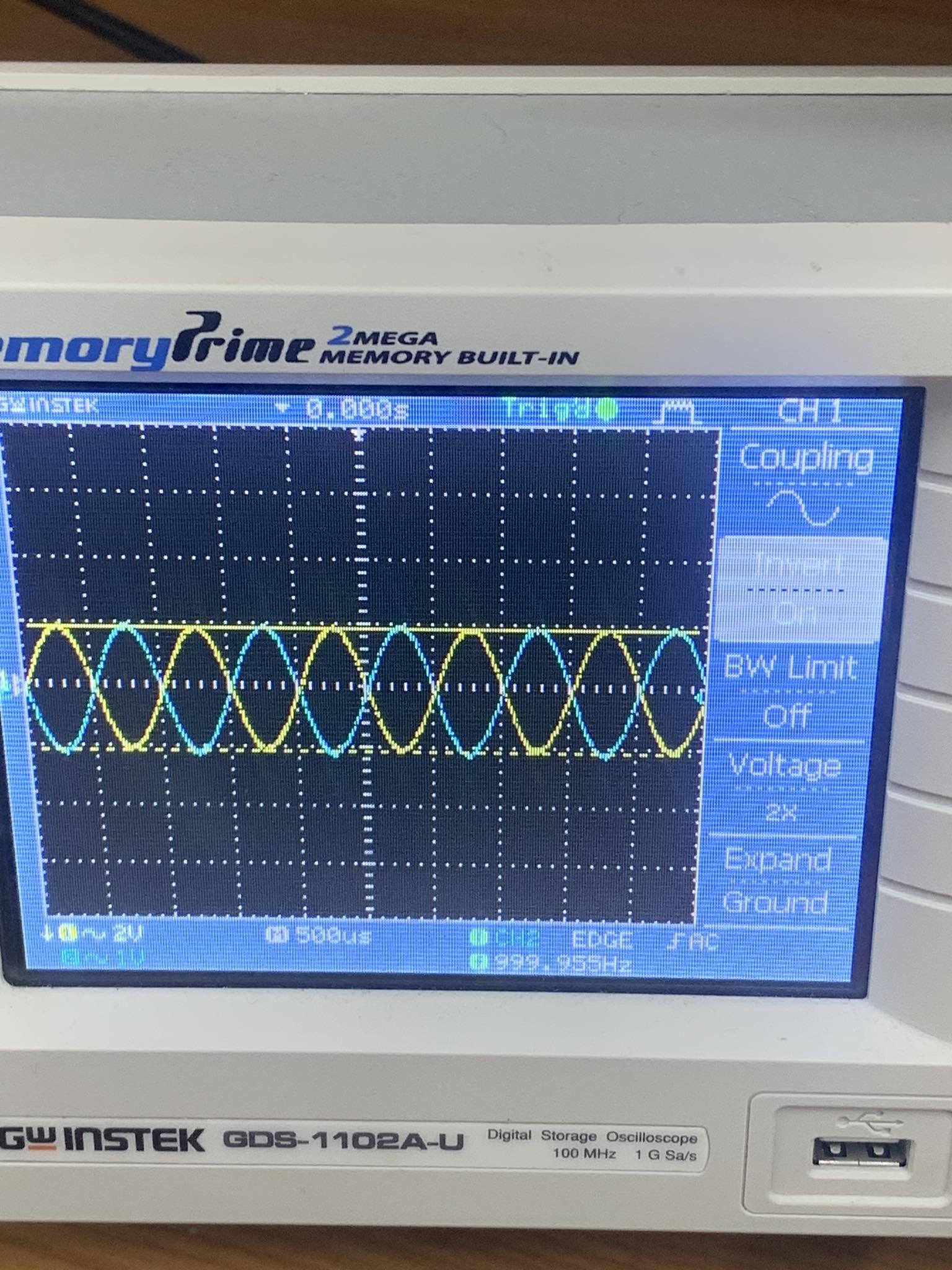
* + 1. Construct the circuit in Fig. 8 with R1 =2.2k , and Rf =10k , 1V input signal at1Khz. Calculate and measure the gain. Sketch the results on the oscilloscope

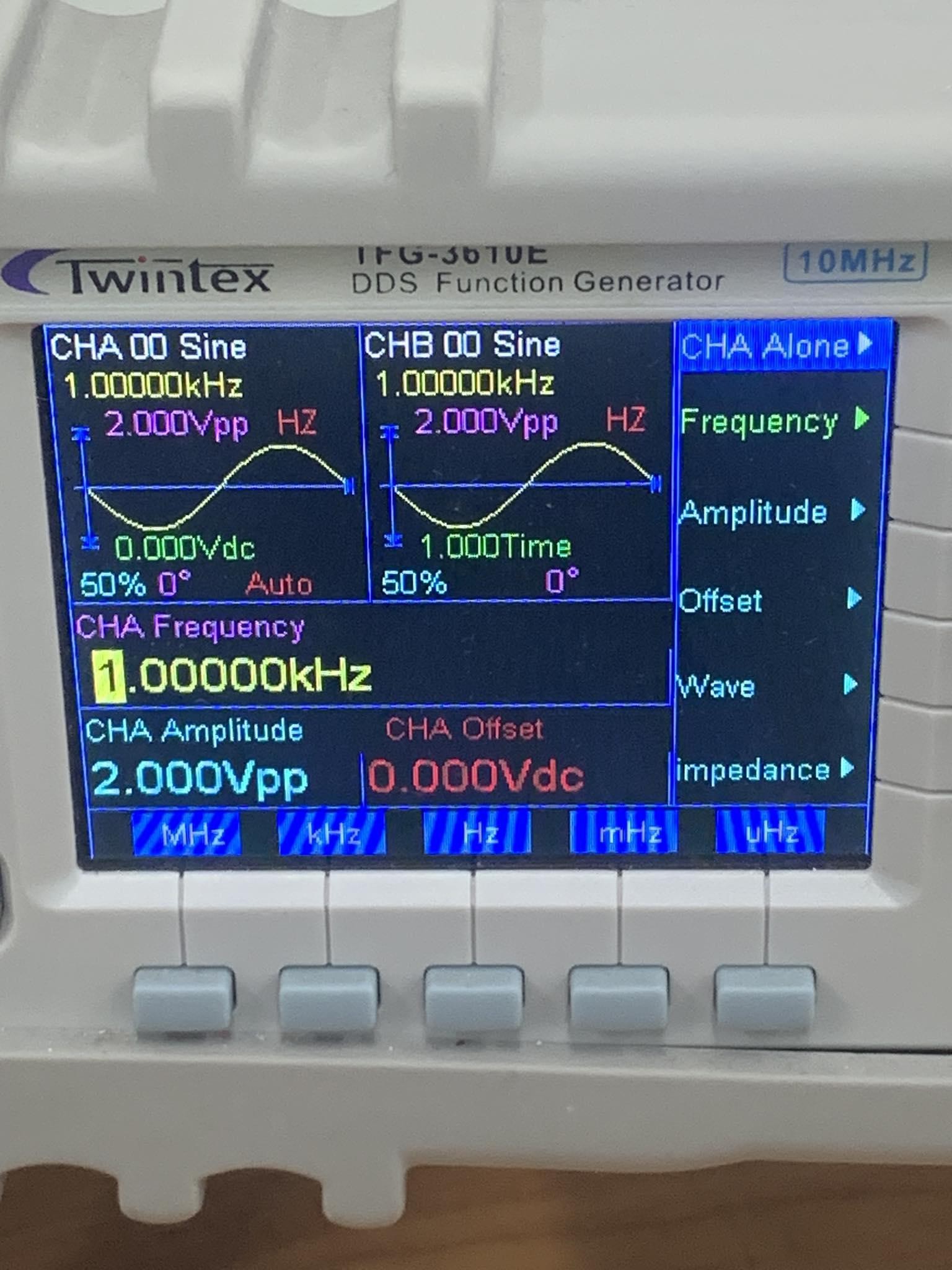
The calculated gain:



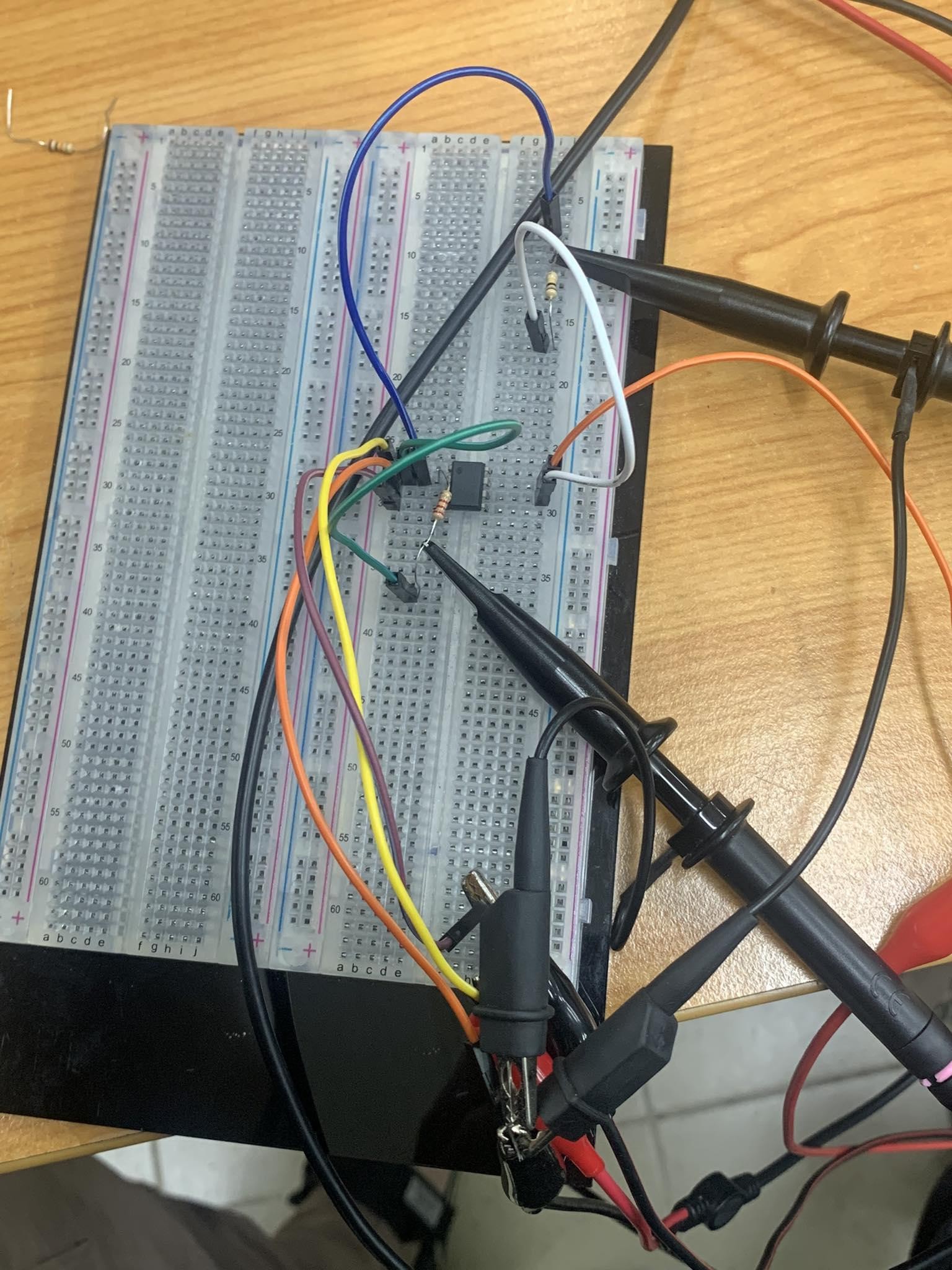
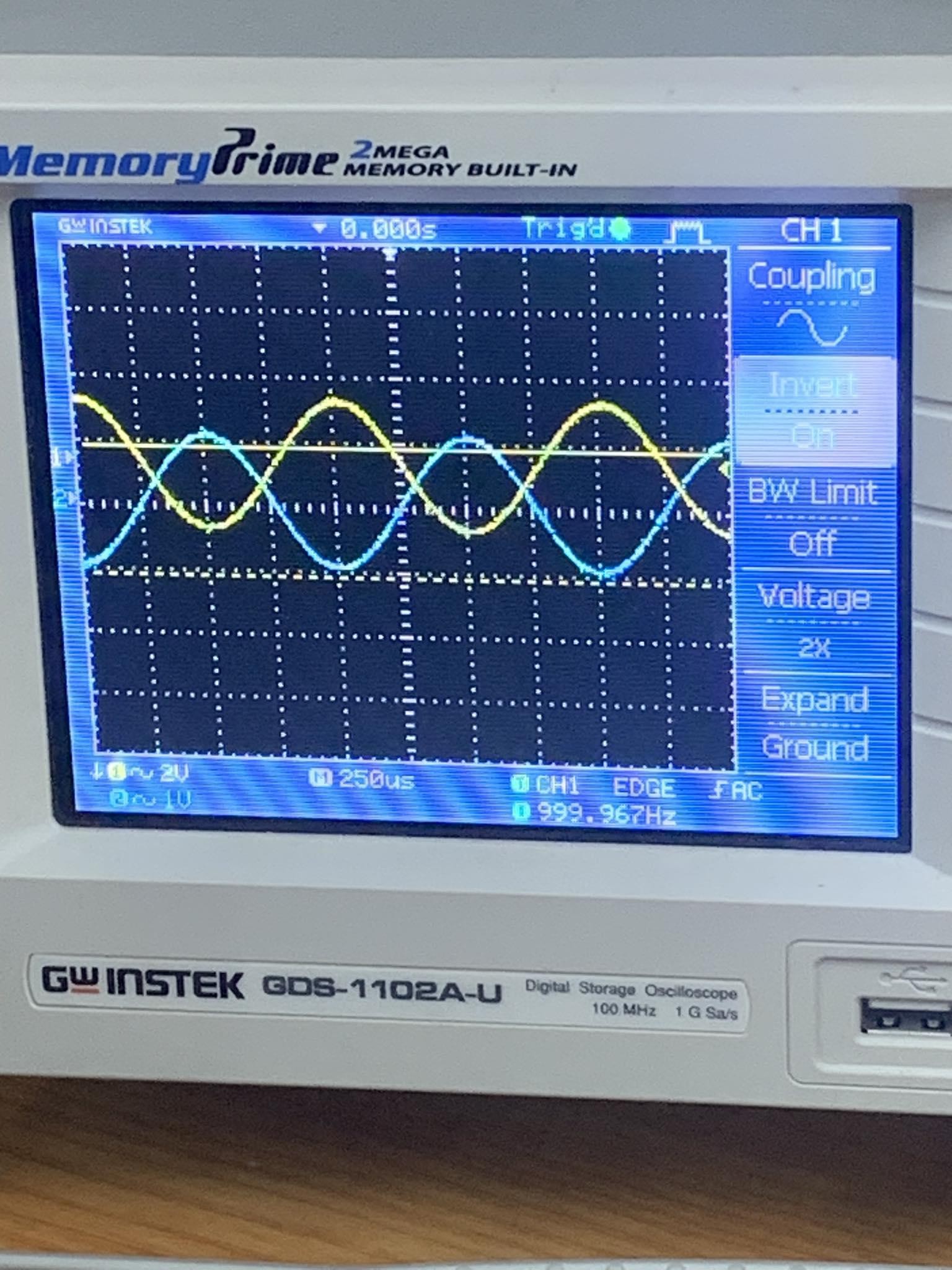
The measured gain:







* + 1. Calculate and measure the gain with R1 = 2.2kΩ and Rf = 100kΩ. Compare results with previous case. Sketch the results on the oscilloscope. Why is this called an inverting amplifier?



The result is more separated than the previous case and easy for us to distinguish between two cases. This is called an inverting amplifier because the results on oscilloscope show that one sine wave graph is horizontally flipped when comparing with the remaining sine wave graph

## Experiment 2: Non-Inverting Amplifier

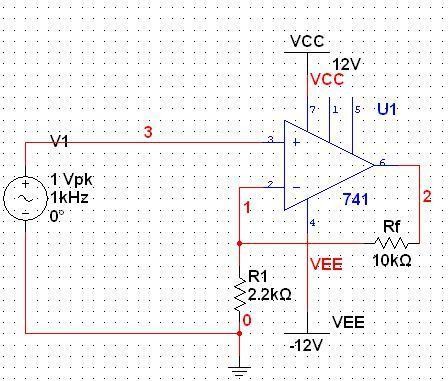


Figure 9

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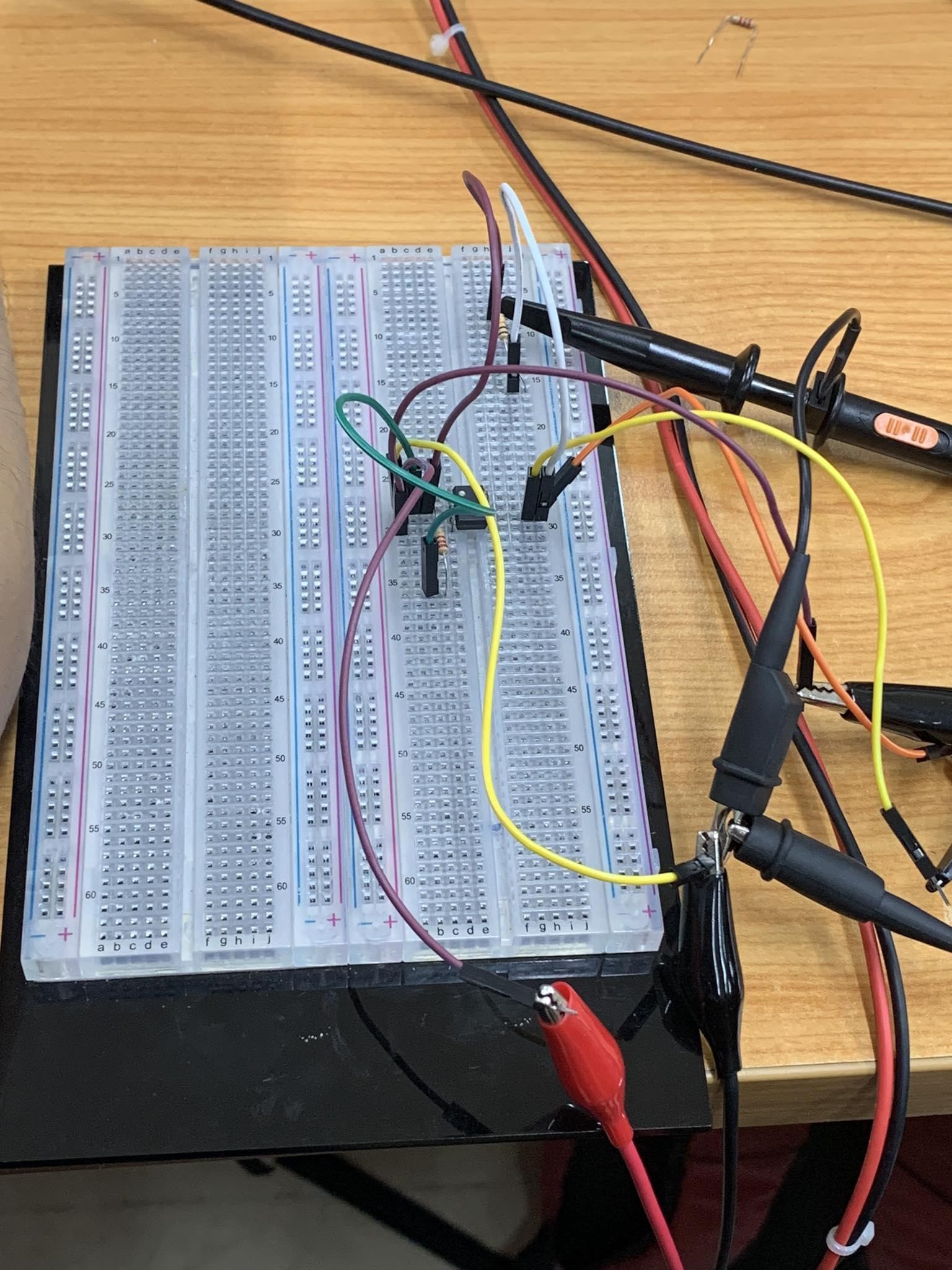


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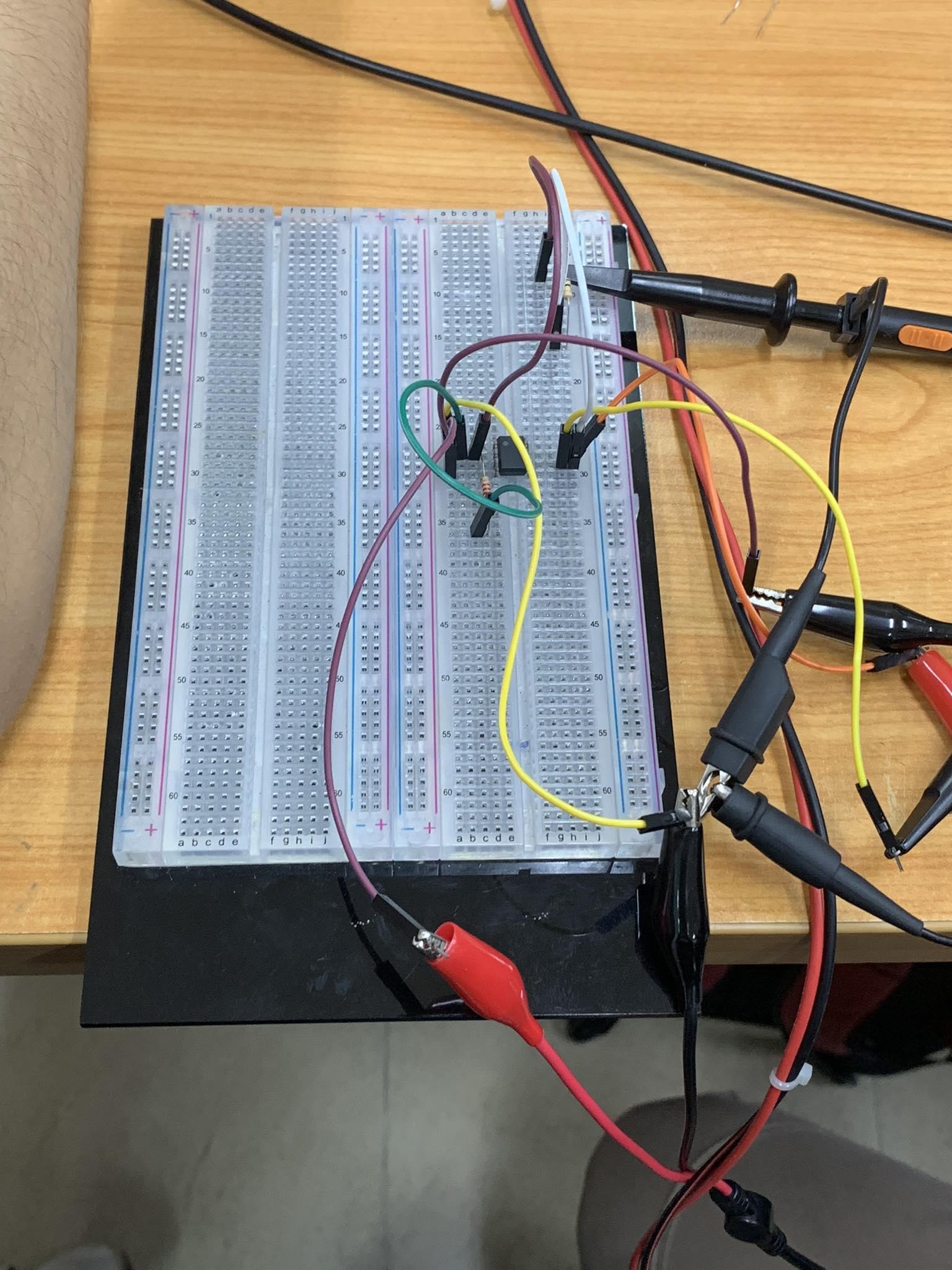
* + 1. Construct the non-inverting amplifier shown in figure 9 with R1 = 2.2kΩ and Rf = 10kΩ. Calculate and measure the gain

Calculated gain:

Measured gain:



* + 1. Repeat section 5.2.1 with R1 = 2.2kΩ and Rf = 100kΩ. Compare the results



## Experiment 3:

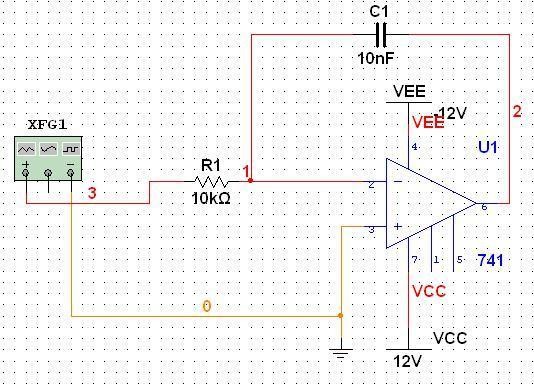
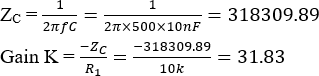
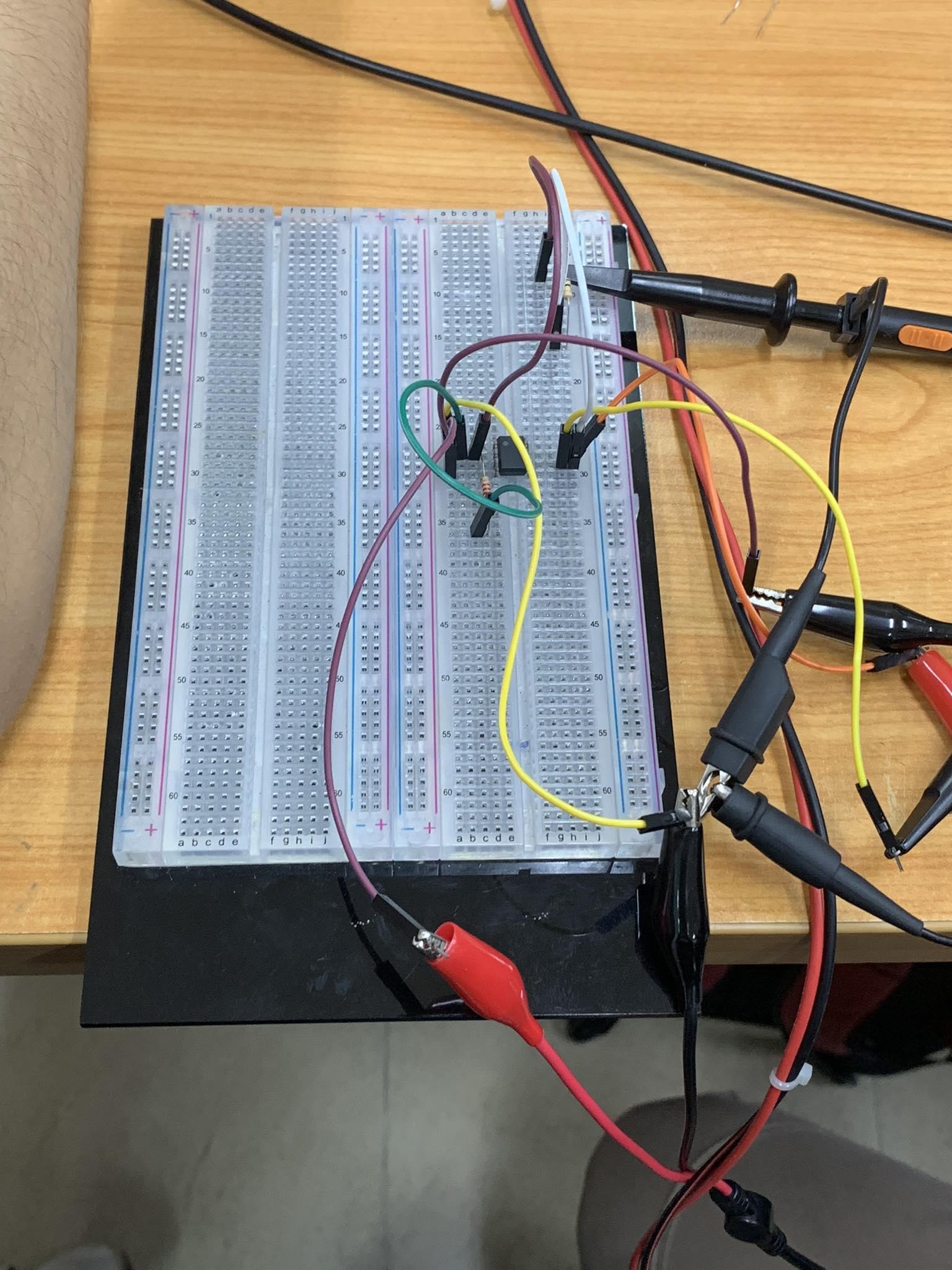
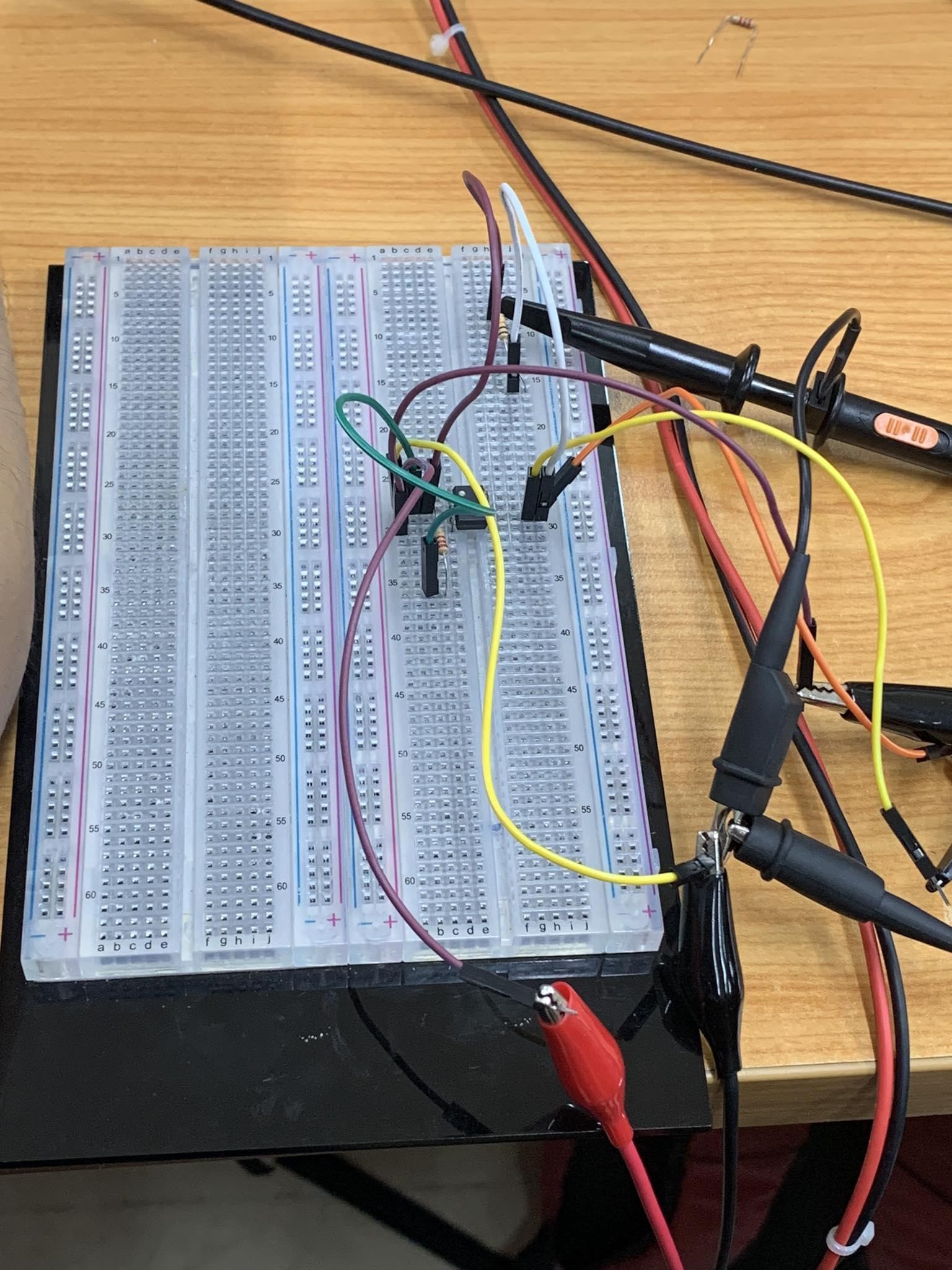


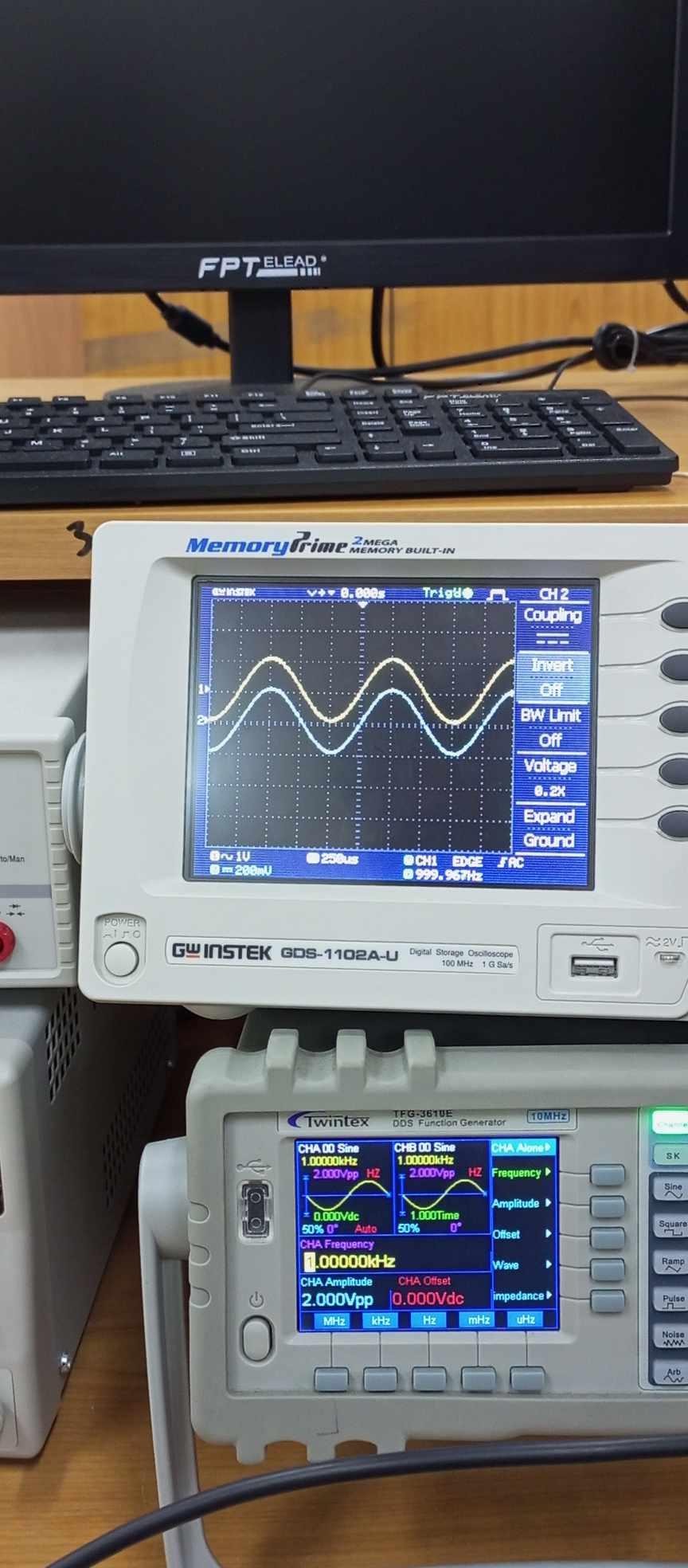
Figure 10

* + 1. Construct the integrator shown in figure 10 with R1 = 10kΩ and C1= 10nF. Calculate and measure the gain

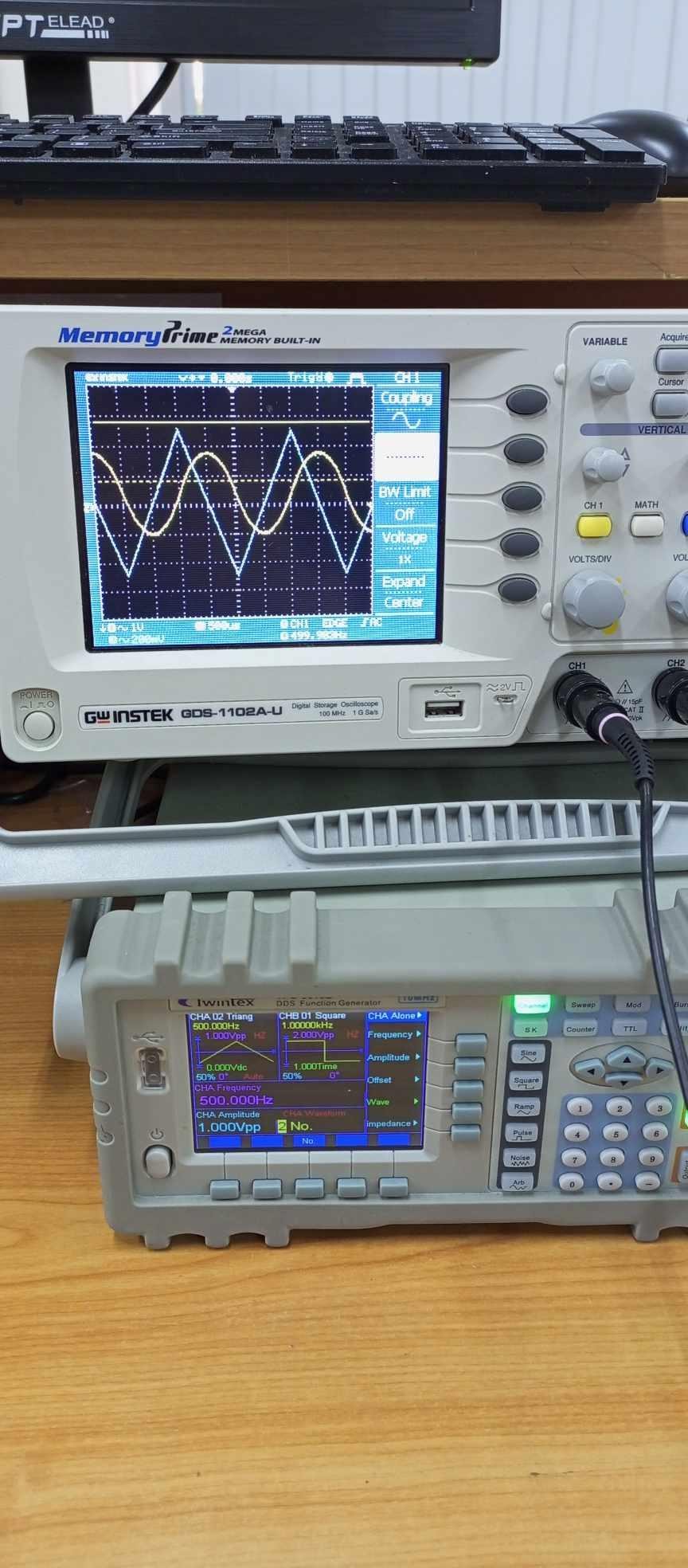
Calculated gain:

Measured gain:

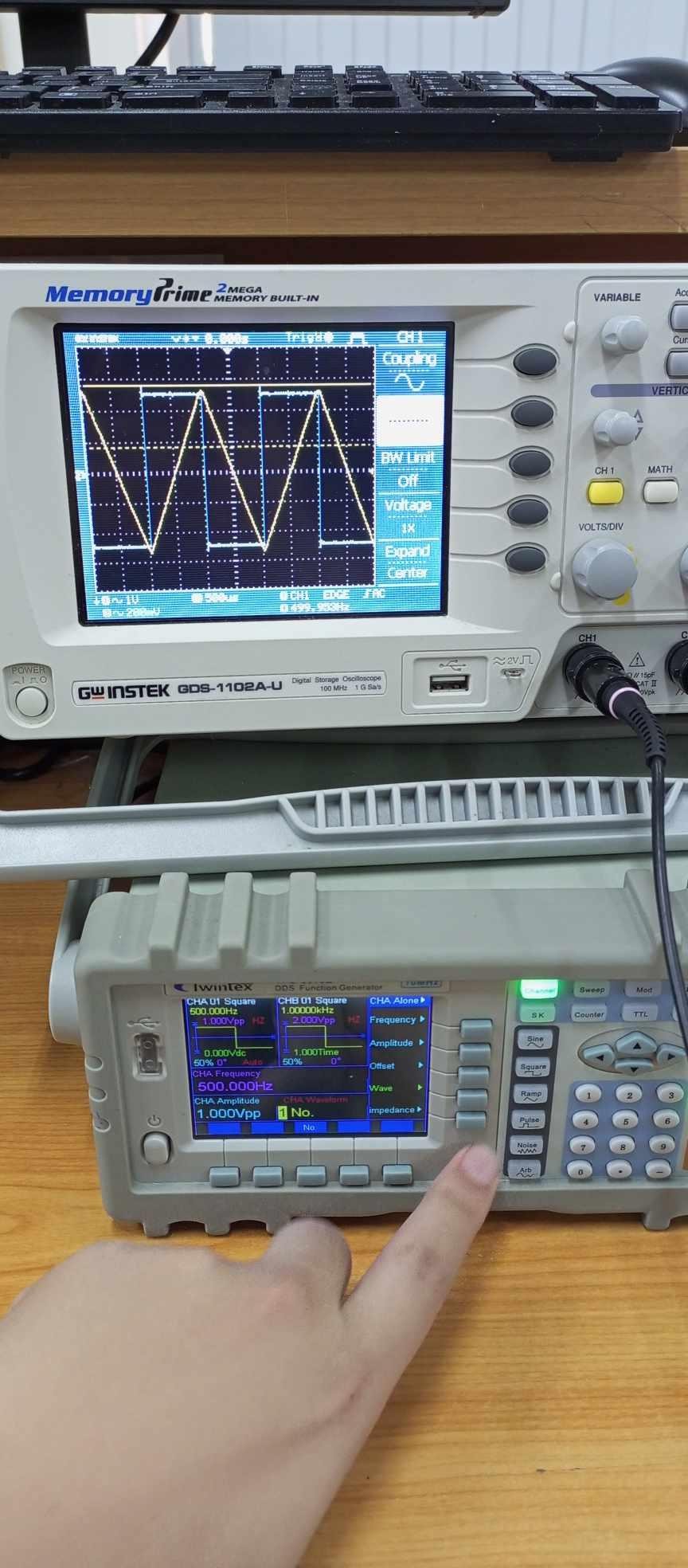


5.1.2 Sketch the input and output waveforms for 500Hz sine wave, triangle wave, and square wave inputs. Explain why we have those sketches.

We have two nearly identical sine wave graph because of the non-inverting amplifier



We have one sine wave graph because the signal is most likely slew rate limited. This means that the output of the amplifier is not fast enough to follow the input signal.

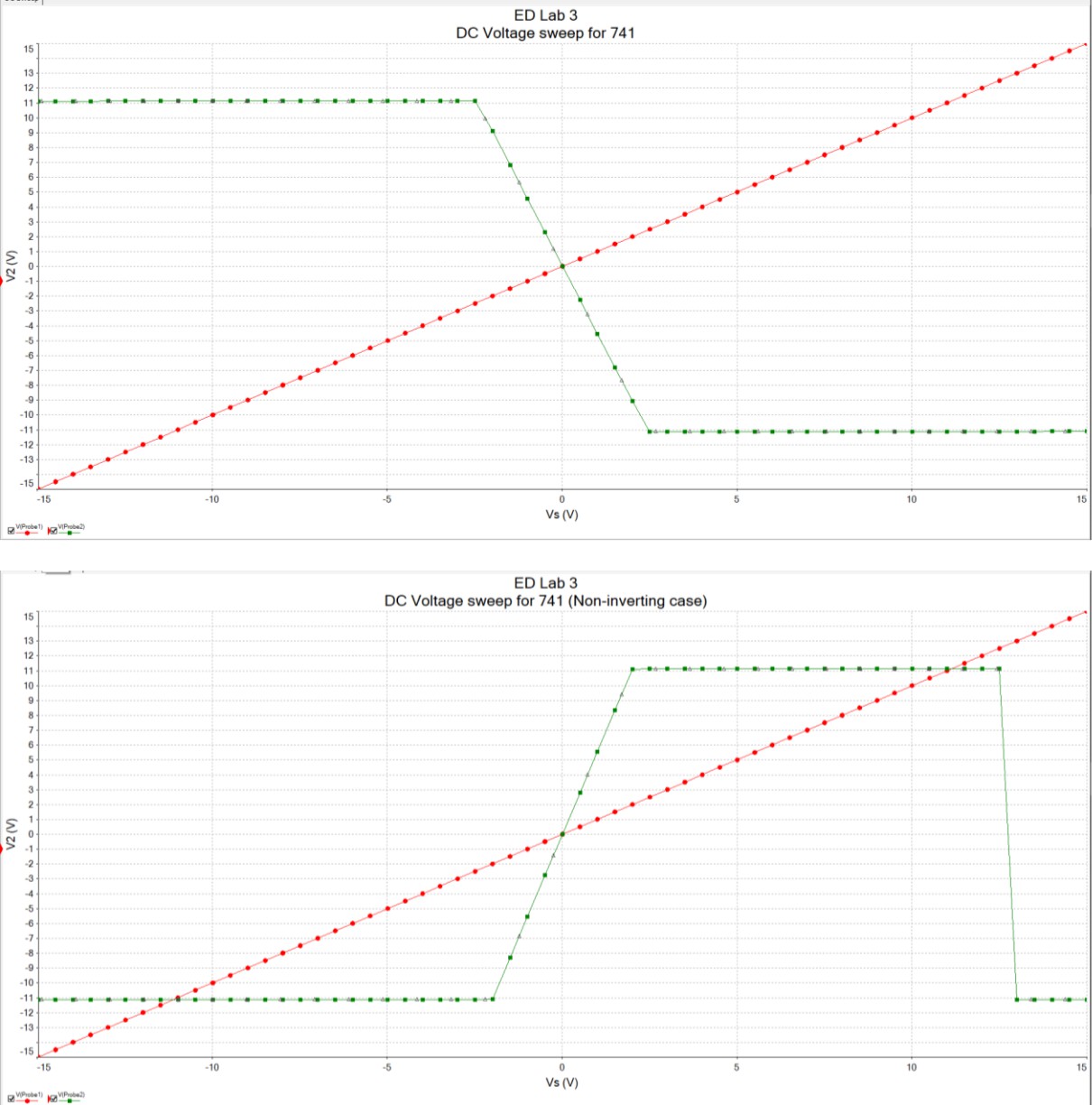


A square wave is often chosen for determining the bandwidth of an amplifier because it contains a wide range of frequencies, including high-frequency harmonics, which can effectively stress the performance of an amplifier across its entire frequency range.

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