A 1.29GHz 582fJ
6-bit Absolute-Value Detector

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Design Summary

Circuit topology and Circuit Style

- Circuit Topology = Optimized Ripple-carry adder (using ANDs and XORs) assuming certain inputs values + Comparator
- Circuit Style=Static CMOS + (4) 2:1 MUX's using transmission gates

Area and Delay

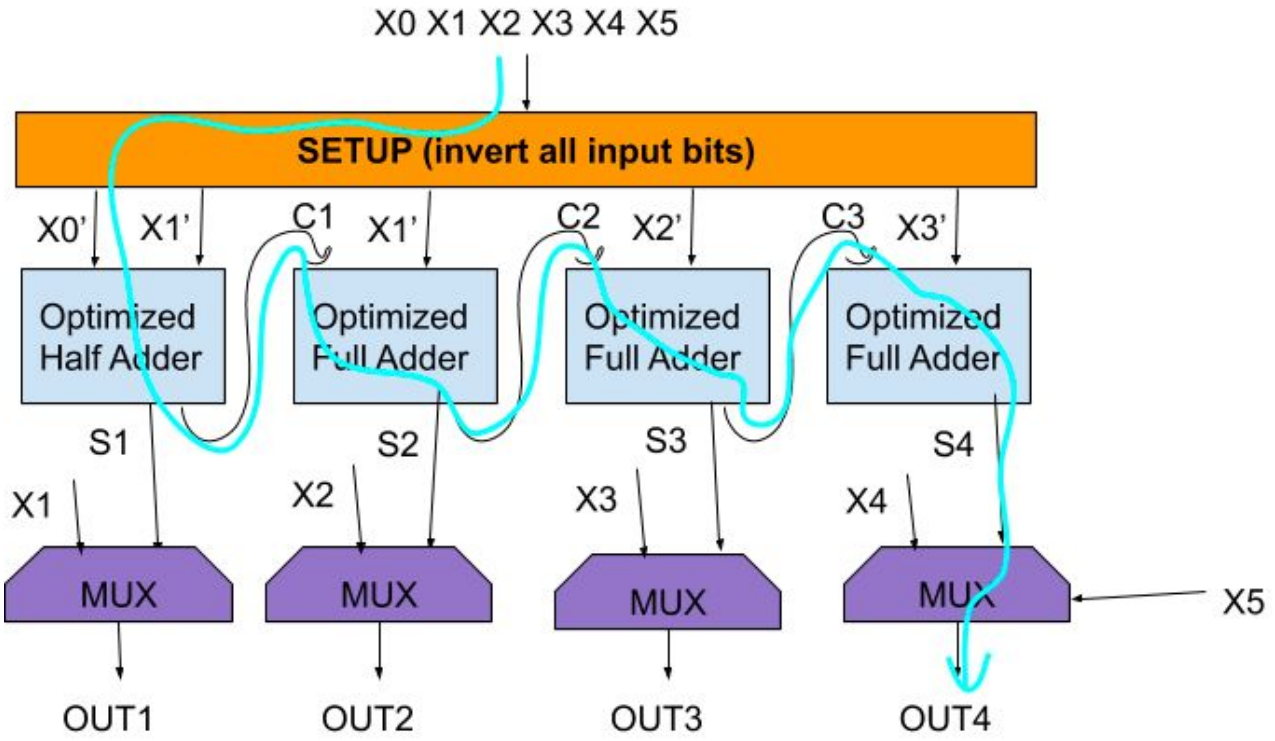
- Moderate Area
- Fast in terms of meeting delay requirements, but at cost of larger energy. Regular design to enable ease of routing in layout

Delay	Layout size	Energy	Verfication
Sch. t_p = [508]ps	X= [51], Y= [38]	Sch. E = [490]fJ	Func: Y / N
Lay. t_p = [600]ps	A = [1990]μm^2	Lay. E = [582]fJ	DRC: Y / N
Critical Input = $X_{[2]}$	AR = [1.33]	Lay. V_{DD} = [1]V	LVS: Y / N

Critical Path Analysis

- **Critical Path of Absolute Value Module**

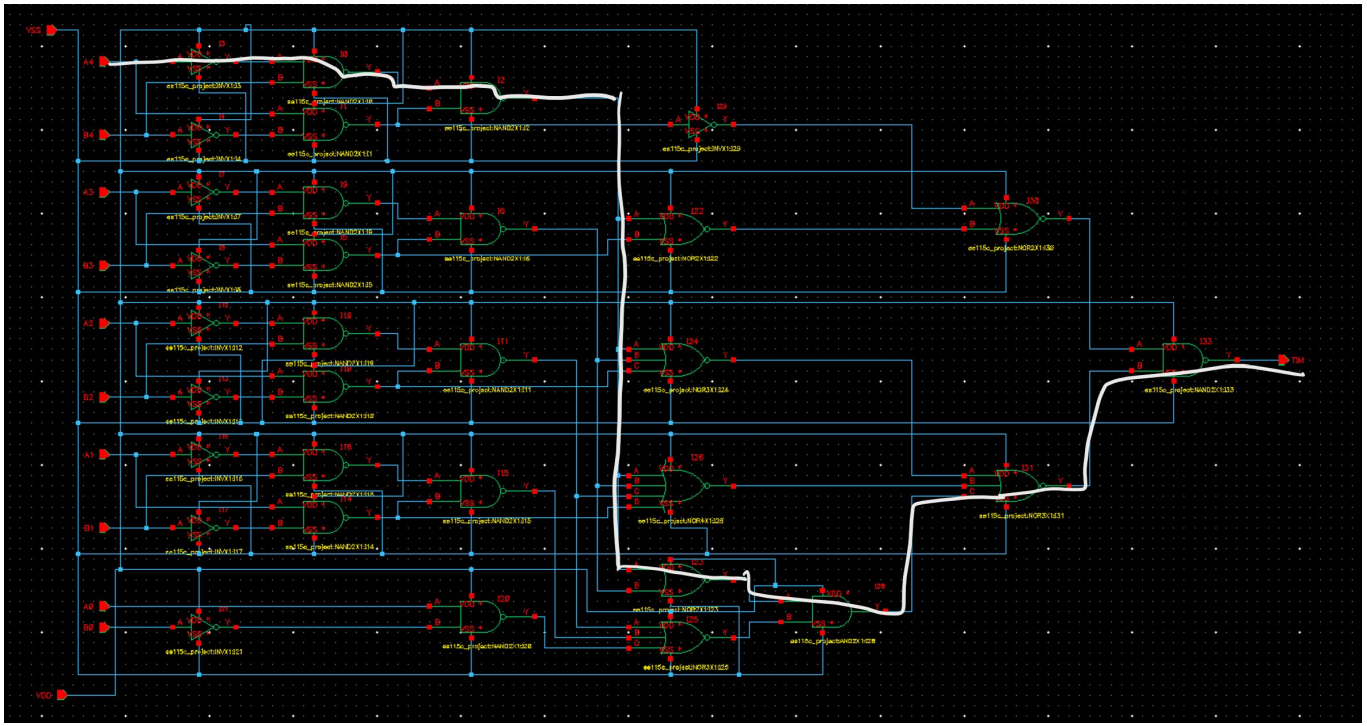
$$t_{critical} = t_{setup}\ (\text{invert all inputs}) + t_{half\_adder} + 3t_{full\_adder} + t_{mux}$$



Critical Path Analysis

- **Critical Path of Comparator Module**

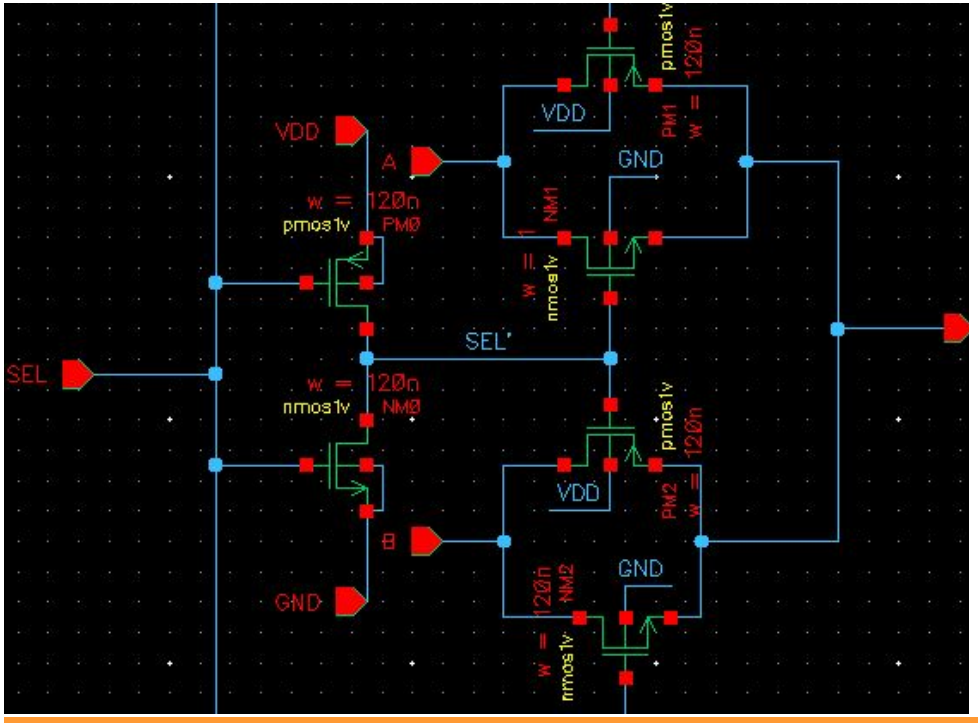
$$t_{critical} = t_{compare\_bits} + t_{AND5} + t_{OR5}$$



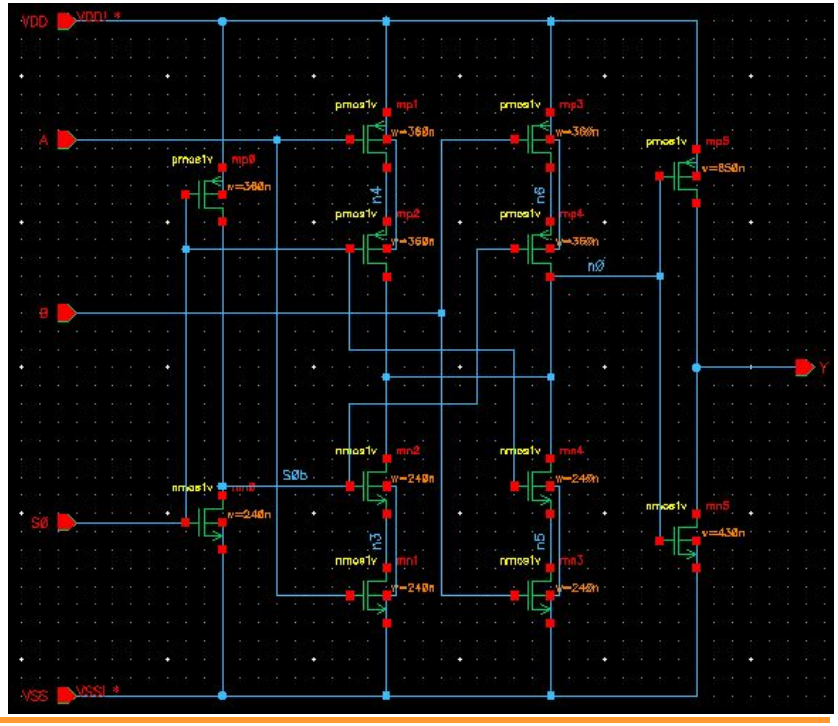
Design Optimization

- Transmission gate logic → significantly less transistors than the standard cell CMOS 2:1 MUX
- Only A or B is selected, but not both
- Sizing is shown below, which is smaller than unit sized inverter for less parasitic capacitance
  - Tradeoff is resistance since W ~ 1/R

OUR 2:1 MUX

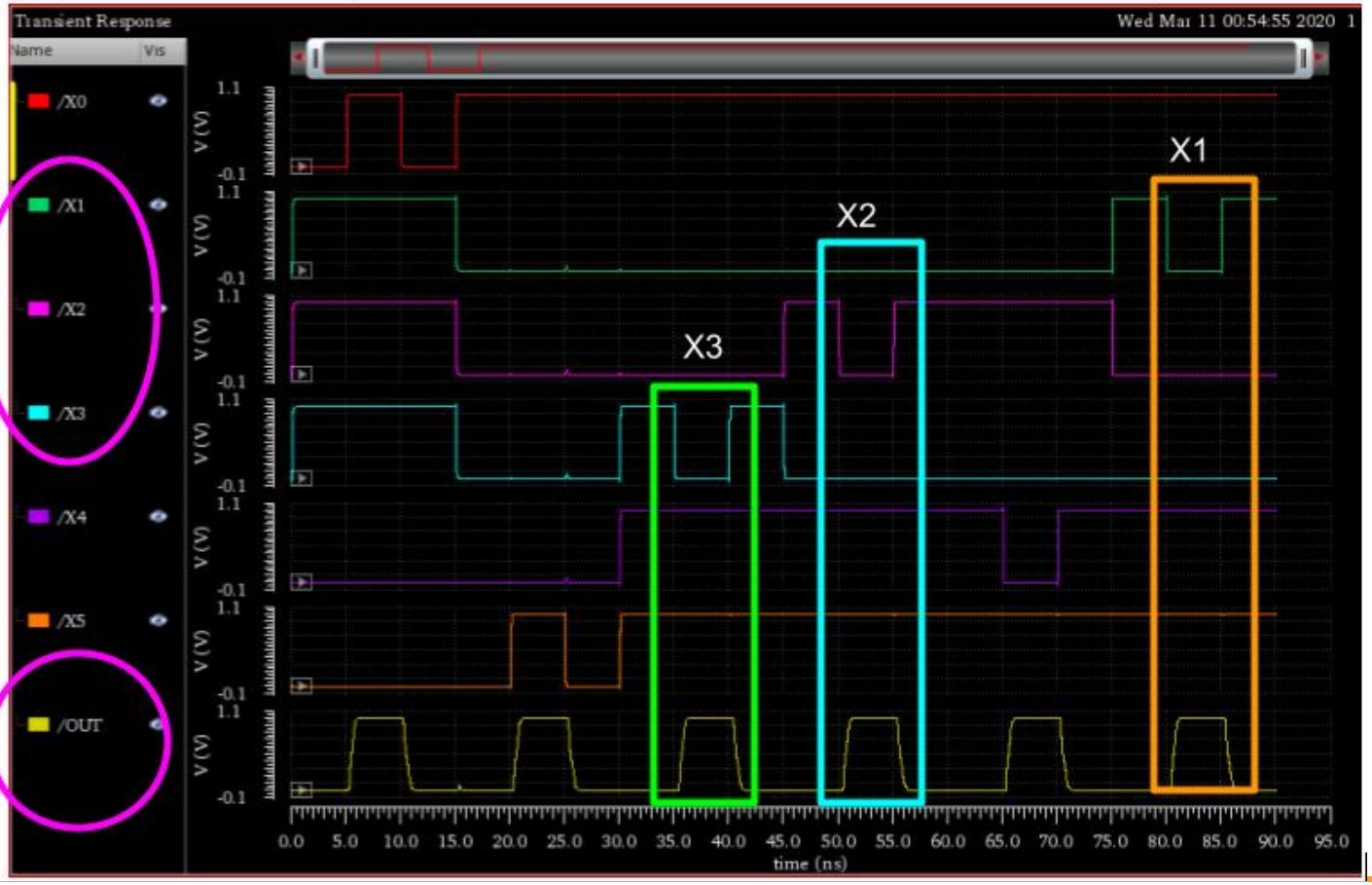


STANDARD CELL 2:1 MUX



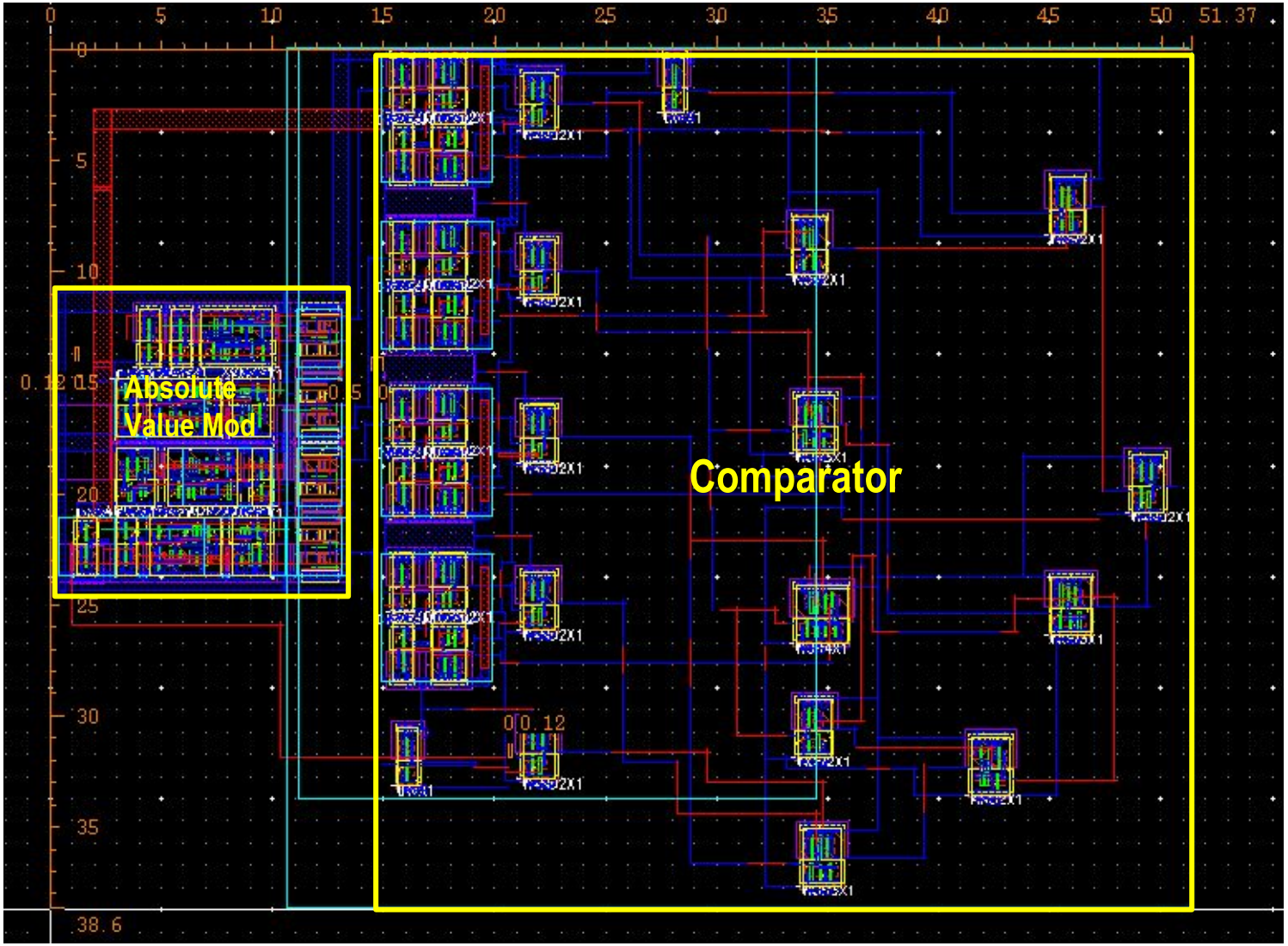
Functionality Check

- 3 most critical input to output paths:
  X3_OUT, X2_OUT, X1_OUT



22	Delay_X5_OUT	450.092p
23	Delay_X4_OUT	492.596p
24	Delay_X3_OUT	600.072p
25	Delay_X2_OUT	599.351p
26	Delay_X1_OUT	583.53p
27	Delay_X0_OUT	395.985p
28	Energy	582.849f

Absolute-Value Detector Layout



1 ***Size***

X = 51.37µm
Y = 38.6µm

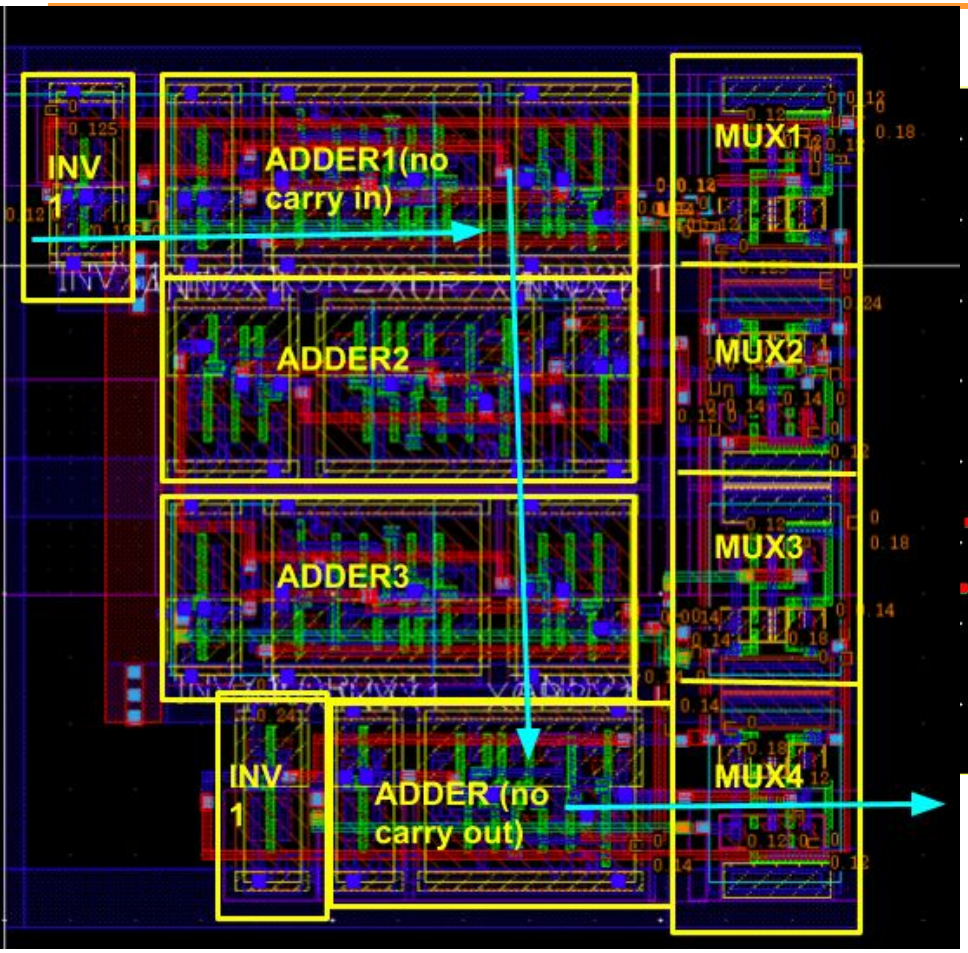
2 ***AR***

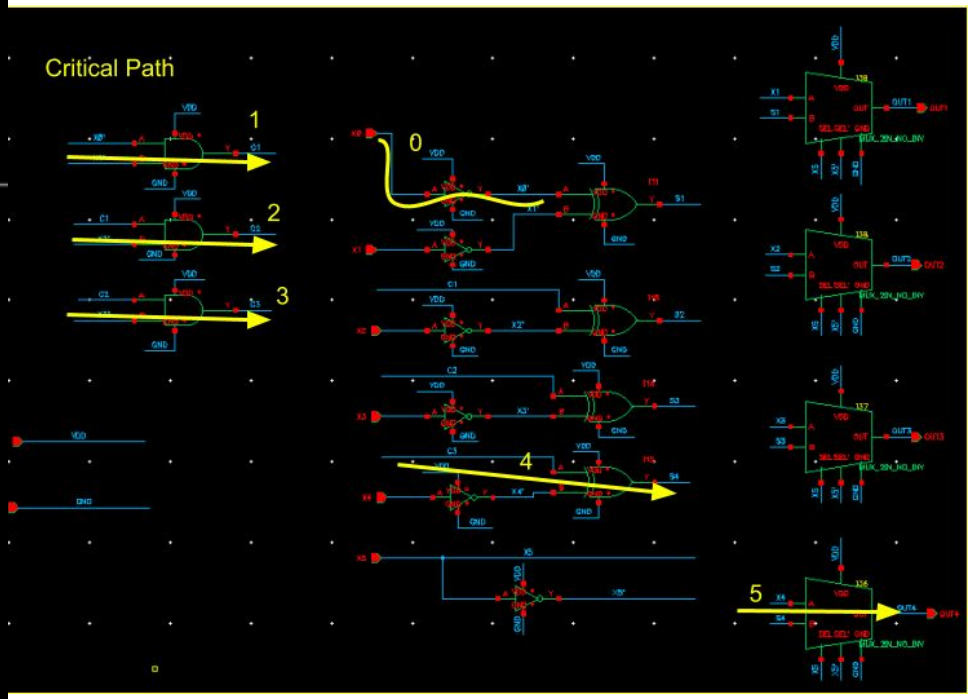
Aspect ratio:
1.33

3 ***Area***

Area:
1990.602µm^2

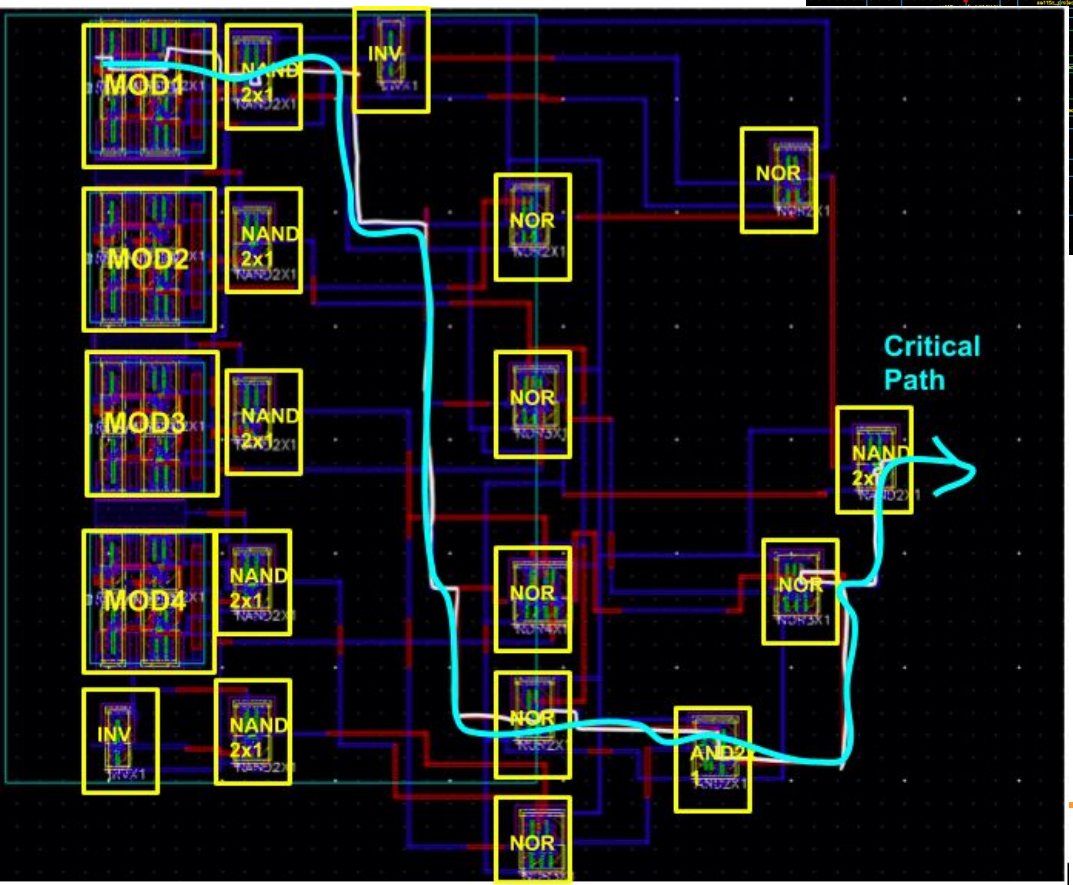
Absolute-Value Detector Layout: Adder

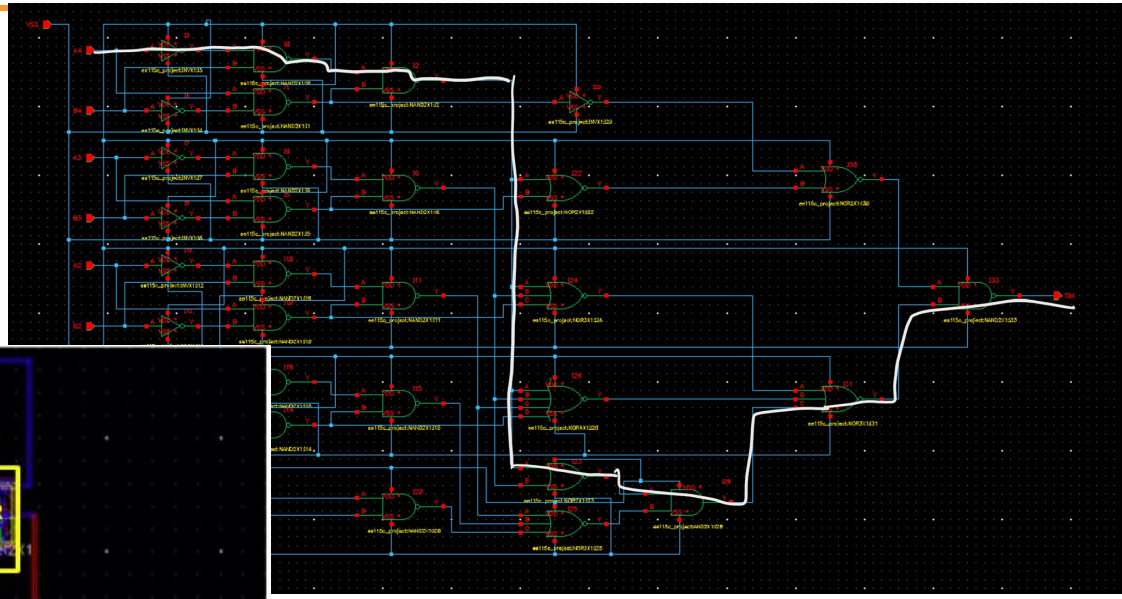




Left: Blue path is critical path in layout
Right: Yellow path is critical path in schematic

Absolute-Value Detector Layout: Comparator





Left: Blue path is critical path in layout
Right: White path is critical path in schematic

Discussion

- **Important Features**
  - Optimized logic using custom ripple carry adder (in ABS detector). It overall reduced energy, gates, and area
  - Minimize delay drastically through transmission gate MUX vs. CMOS MUX
  - Highly regular layout design made easy to route adder and comparator. Could easily build hierarchically and create repeated modules.
- **Future Considerations**
  - Implement carry look ahead adder rather than optimized carry ripple adder to see if there are drastic delay differences
  - Size transistors based on critical path instead of using mostly standard cells
  - Make comparator design more compact and line VDD and GND better