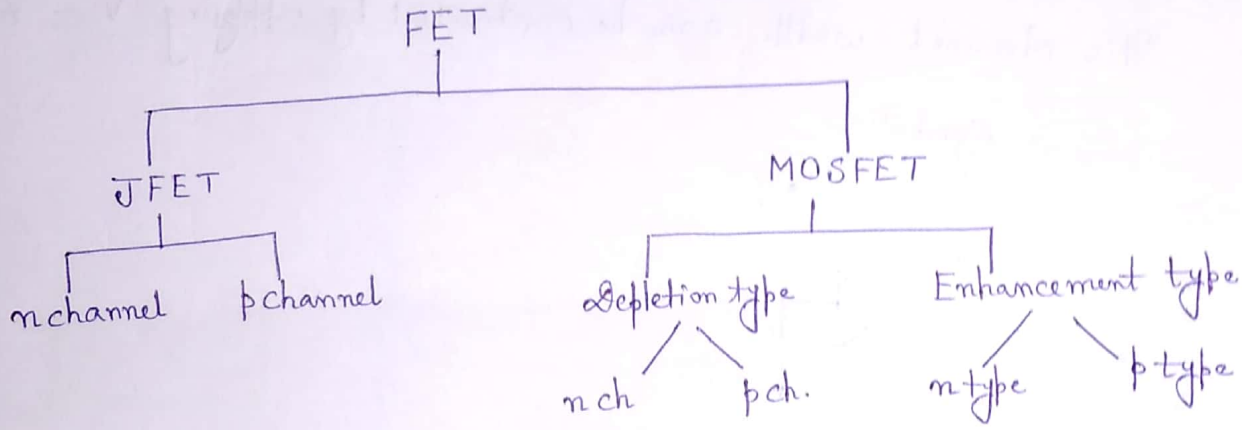
Field Effect Transistor (FET)

FET is a three terminal device in which the output current flow through the device is controlled by the applied electric field between two terminals.

As the output current flow through this device is controlled by applied field it is called FET.

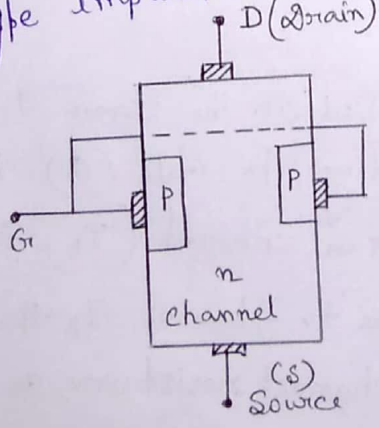
- Current flow through the device is due to majority carrier (for n channel is e^-, and for p channel is h^+) only, so this ~~dee~~ device is called unipolar device.



N channel JFET :-

Construction :-

N channel JFET is a n type Si bar (uniformly doped). The bar has ohmic contacts at the two ends, two terminals are called Source and Drain. n type bar is very lightly doped. Two sides of the bar with heavily doped with p type impurities. Various parts are —



The various parts are -

Source (S) :- The source is the terminal through which the majority carrier enters into the bar.

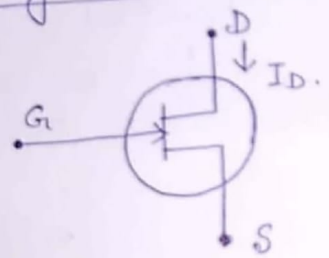
Gate (G) :- Two terminals from p regions are shorted and this common terminal is called Gate.

Drain (D) :- Drain is the terminal through which the majority carrier leaves the bar.

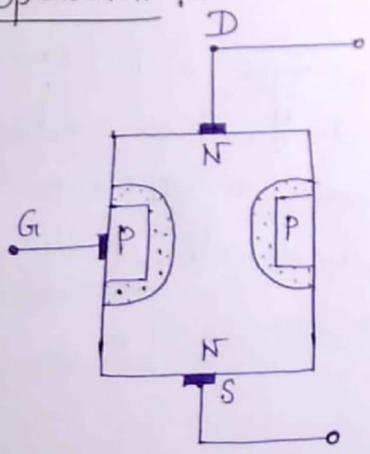
Channel :- The region between of S and D which is ~~sandwid~~ sandwitched between two p regions is called channel.

This channel width can be controlled by applying V_{GS} & V_{DS}.

Symbol

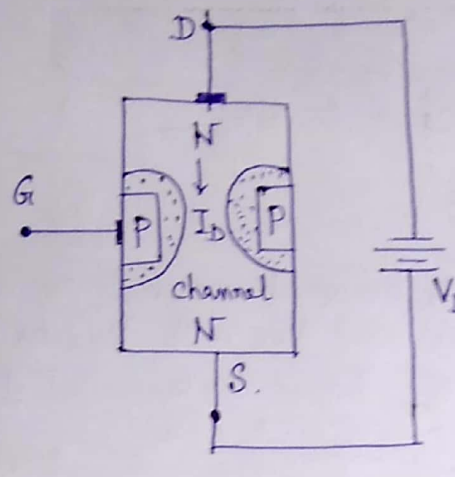


Operation :-



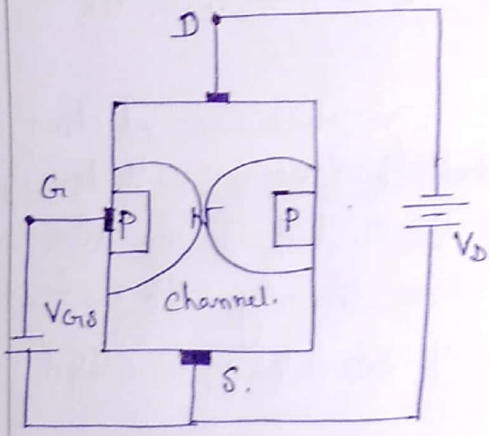
(i) When neither any bias is applied to the gate ($V_{GS} = 0$) nor any voltage to the drain w.r to Source ($V_{DS} = 0$) the depletion regions around the P-N junctions are of equal thickness and symmetrical.

(ii) When positive voltage is applied to the drain terminal (D) w.r to Source (S) without connecting the Gate (G) to supply, electrons flow from S to D and drain current (I_D) flows through the channel from D to S. Due to flow of I_D there is a uniform voltage drop across the channel resistance as we move from D to S.



This voltage drop reverse biases the diode. The gate is more negative with respect to those points in the channel which are nearer to (D) than to (S) so depletion layer penetrate more deeply into the channel at points lying closer to D than to S, so wedge-shaped depletion regions are formed.

The size of the depletion layer formed determines the width of the channel and the magnitude of the current (I_D) flowing through the channel.



(iii) When the gate is biased negative with respect to the source while the drain is positive w.r to the source, P-N junctions are reverse biased and depletion regions are formed. P regions are heavily doped compared to N channel, so depletion channel penetrate deeply into the channel. Depletion region is a region depleted of the charge carrier, it behaves as an insulator. The channel is narrowed, the resistance is increased and I_D is reduced.

If the negative voltage at the gate is increased depletion layers meet at the centre and I_D is completely cut off. The Gate Source voltage (V_{GS}) at which drain current is completely cut off is called <u>Pinch off voltage (V_P).</u>

Characteristics of JFETs :-

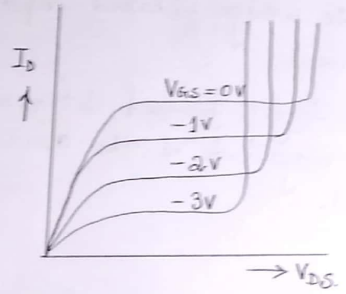
There are two types of static characteristics —

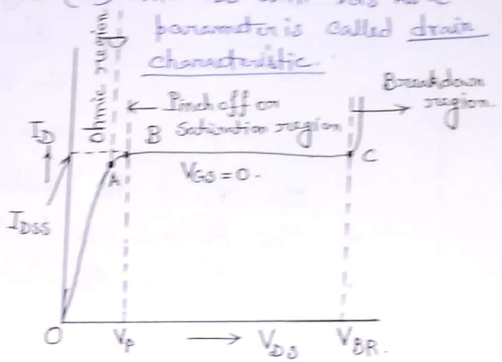
(i) Output or drain characteristics.

(ii) Transfer characteristics.

(i) Drain characteristics :-

The curve drawn between drain current (I_D) and V_{DS} with V_{GS} as a parameter is called drain characteristic.





(i) Ohmic region :- When $V_{DS} = 0$, $I_D = 0$ because electron from S terminal are not emitted and thus there is no collection of e's at the drain terminal, thus $I_D = 0$. But if we increase $V_{DS} < V_P$ then I_D ~~will flow~~ increases linearly with increase in V_{DS} upto knee point. This region of the curve (OA) is called ohmic region.

(ii) Pinch off or saturation region :-

With the increase in drain current I_D the ohmic voltage drop between the source and channel region reverse biases the gate junction, so the channel width decreases. When $V_{DS} = V_P$ the channel is pinched off, so V_P is called pinch off voltage. Here I_D attains a constant value.

From point A (knee point) to the point B (pinch off point) the drain current I_D increases with the increase in V_{DS}. following a reverse square law.

The region of the characteristic curve (BC) in which drain current (I_D) remains almost constant is called pinch off region. It is the normal operating region of the JFET used as an amplifier. The drain current in the pinch off with $V_{GS} = 0$ is referred to the drain source saturation current (I_{DSS}).

Drain current in the pinch off region is given by Shockley's equation.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)^2$$

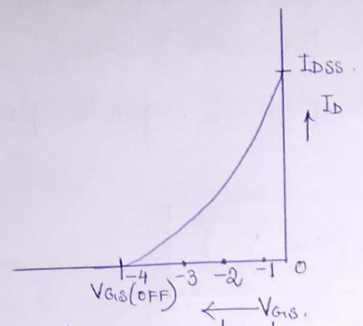
(iii) Breakdown Region :-

If the drain to source voltage (V_{DS}) is continuously increased a stage comes when the gate channel junction breakdown. At this point the drain current increases very rapidly. This happens because the charge carriers making up the saturation current at the gate channel junction accelerate to a high velocity and produce an avalanche effect. This region of the characteristic curve (CD) is called Breakdown region.

So JFET behaves as an ordinary resistor in ohmic region, as a constant current source in pinch off or saturation region and as a constant voltage source in the breakdown region.

2. Transfer characteristics :-

The curve drawn between I_D and V_{GS} keeping V_{DS} constant is called transfer characteristic curve.

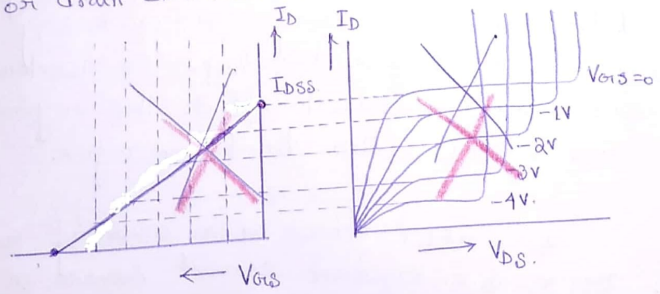


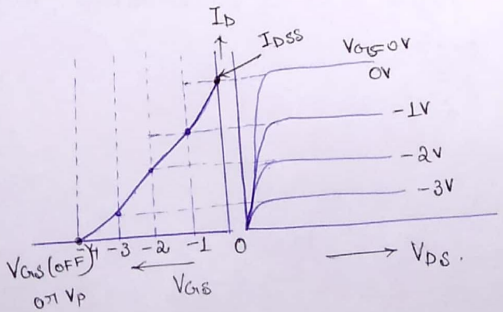
Here (a) drain current decreases with the increase in -ve gate -source bias.

(b) drain current $I_D = I_{DSS}$ when $V_{GS} = 0$.

(c) drain current $I_D = 0$ when $V_{GS} = V_P$.

This curve can be obtained from Shockley's equation or from the output or drain characteristic curves.





JFET parameters :-

Four parameters determine the performance of JFET.

(i) ac drain resistance
(ii) transconductance
(iii) amplification factor.
(iv) dc drain resistance.

(i) ac drain resistance :-

It is defined as the ratio of change in drain source voltage to change in drain current at constant gate source voltage, it is denoted by r_d.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at constant } V_{GS}.$$

r_d ranging from 10KΩ to 1MΩ.

(ii) Transconductance :-

It is defined as the ratio of change in drain current to the change in gate source voltage at constant drain source voltage.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at const } V_{DS}.$$

g_m ~~rangi~~ ranging from 1500 to 2500 (℧ = mho)

(iii) Amplification factor :-

It is defined as the ratio of change in drain source voltage to the change in gate source voltage at constant drain current.

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ at constant } I_D$$

Amplification factor (μ) of JFET indicates how much more control the gate Source voltage has over drain current in comparison to the drain Source voltage.

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\boxed{\mu = r_d \times g_m}$$

μ of a FET as high as 100.