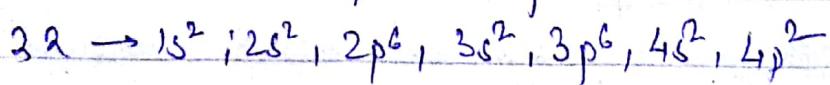


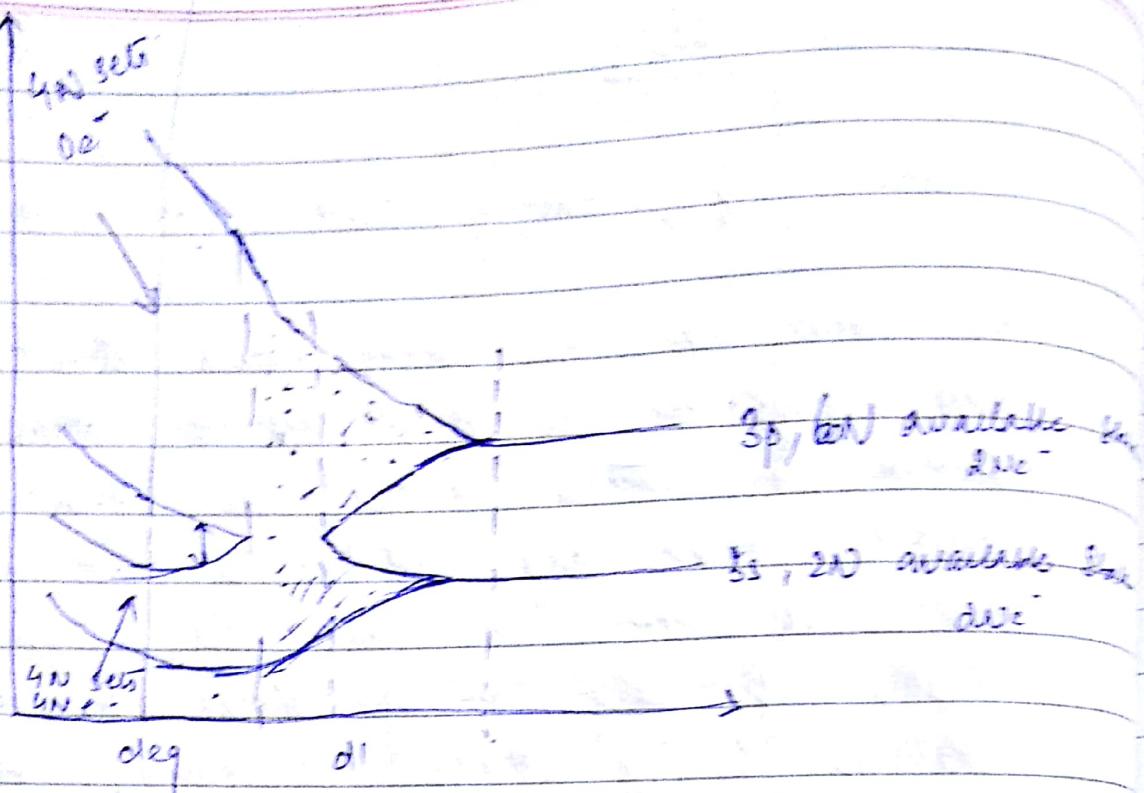
## Formation of energy band in solids

We know that the energy band structure for any substance or any discrete atom is discrete in nature when the atom is isolated from any electrostatic environment.

Now we come to the solid which is a cluster of large no of atoms in a regular manner. If we study the energy band diagram in such solid then we see a patch of ~~these~~ continuous energy bands.

Let us take a system of  $N$  atoms arranged in a regular manner (say cubic structure). When the inter atomic spacing is very large then we have similar discrete energy band structure for each atom. Now, if we decrease the interatomic spacing for the whole system, then interaction b/w the atoms will start. Hence the splitting of the discrete energy level will start. No two electrons can have same set of quantum no's.





If we further decrease the interatomic spacing splitting will be large and bottom of the p subshell will merge with the top of the s subshell.

When the inter atomic spacing is less than  $d_1$  then we get a total of  $2N$  available states &  $4N$  occupied ~~states~~ state / electrons. Now these  $4N$  electrons will occupy the ~~4N~~  $4N$  states having lower energy and the rest  $4N$  states will remain vacant. If we decrease  $d$  further then the occupied  $4N$  states will form the valence band and empty  $4N$  sets will form the conduction band. And the spacing b/w one bottom of conduction band & top of valence band will form the forbidden region (<sup>marg</sup> gap) where there is no available sets i.e., for solids.

## Classification of solids

According to the band gap energy  $E_g$  the solids are classified as

- 1) Insulator 2) Semiconductor 3) Conductor

The band diagram of the above types are as shown below.

### 1) Insulator

For this type of material the band gap is around  $6\text{ eV}$  so on the application of external agencies (like temperature, applied potential) we do not have any free electrons in the conduction band so this type of material does not conduct electricity.

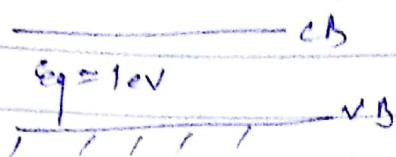
CB

$$E_g = 6\text{ eV}$$

NB

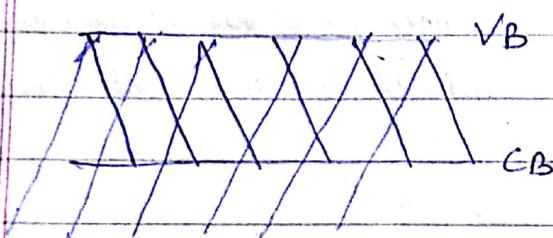
### 2) Semiconductor

For this type of material the value of  $E_g$  is around  $1\text{ eV}$  or less, so we get a few no. of free electron in the conduction band at room temperature. Therefore upon application of external bias (voltage) the material will conduct electricity.



## # Conductor

for this type of material the top of the Valence band will be above the bottom of the conduction band ie we have overlapping so huge no. of free electrons are available at all temperatures. So electricity will flow upon application of very small bias.



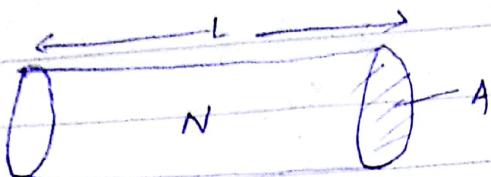
## # Transport Phenomenon in Solids :-

### Drift

Drift of ~~the~~ carriers occur due to the application of electric field

Let us consider a specimen of length  $L$  and cross section  $A$ . This specimen contains  $N$  no. of electrons. An electron takes a time  $T$  second to travel a distance of  $L$  m.

Therefore the total no of electrons passing through any cross section per unit time is  $\frac{N}{T}$



$$\text{The current } I = \frac{Nq}{T} g$$

The drift velocity ( $v$ ) of the electron is given by

$$v = \frac{L}{T}$$

$$\therefore I = \frac{Nq v}{L}$$

The current density  $J$  is given by

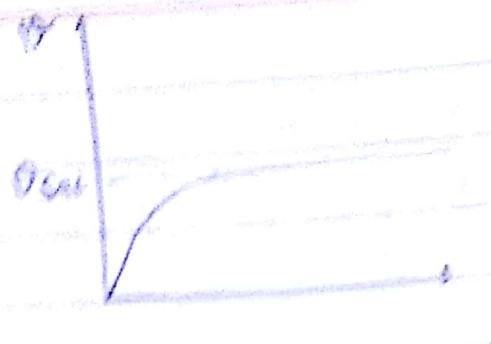
$$J = \frac{I}{A} = \frac{\frac{Nq v}{L}}{A} \quad \text{no. of vol. per unit area} = n$$

$$= n q v$$

Drift velocity per unit electric field = Mobility

~~$v = \mu E$~~

Now, due to the increasing  $E$  the current will increase but after certain limit of the  $E$  the mobility of the carriers will be decreased due to the vibration of the crystal lattice or scattering. Hence the drift velocity will attain saturation value thereby saturating the current.



$$J = \sigma E$$

$$\approx 66$$

where  $\sigma$  is called the conductivity.

Now, if the specimen is a semi conductor then both free electrons and free holes are present. The total current density  $J$  will be contributed by both the carriers. Therefore

$$J_{\text{total}} = J_{\text{electrons}} + J_{\text{holes}}$$



$$\begin{aligned} \text{total current density} &= n \mu_n q E + p \mu_p q E \\ &= (n \mu_n + p \mu_p) q E \\ &\approx \sigma E \end{aligned}$$

$n \rightarrow$  electron conc.

$p \rightarrow$  hole conc.

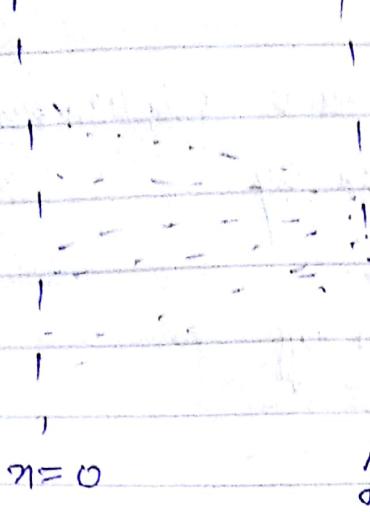
for intrinsic semi conductor

$$n = p = n_i$$

for extrinsic semi conductor

$n \neq p$ , its value will depend on doping

Diffusion

$p(0)$  $p(x)$  $J_p \text{ drift}$ 

Diffusion occurs due to the concentration variation. Let us take a system consisting of free holes having decreasing concentration in the  $x$  direction. The diffusion current density is proportional to the concentration gradient, ~~that is~~  $\frac{dp}{dx}$ , & charge of each carrier therefore  $J_p$  diffusion  $\propto q \cdot \frac{dp}{dx}$ .

$$J_p \text{ diff} = -q D_p \frac{dp}{dx}$$

$$\frac{dp}{dx} = \frac{p(0) - p(x)}{0 - x}$$

$$J_p \text{ diff} = -q D_p \frac{dp}{dx}$$

where  $D_p$  is the proportionality constant called diffusivity or diff constant of hole. It's unit is  $\text{cm}^2/\text{sec}$ .

$$\text{The } J_{\text{ndiff}} = q D_n \frac{dn}{dx}$$

$\therefore$  Total diff current density in a semiconductor =

$$\begin{aligned} J_{\text{diff}} &= J_{p \text{ diff}} + J_{n \text{ diff}} \\ &= -q D_p \frac{dp}{dx} + q D_n \frac{dn}{dx} \end{aligned}$$

 $q D_n$

If both phenomenon occur simultaneously then total current density is given by

$$J_t = J_{t \text{ diff}} + J_{t \text{ diff}}$$



## Fermi Level in Semiconductor

A/c to statistical mechanics electrons in the crystal obey fermi dirac statistics a/c to the following occupancy factor given by

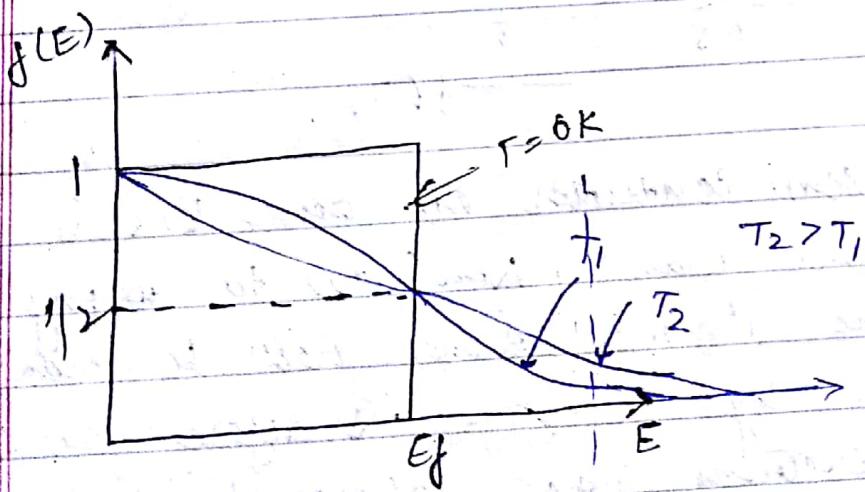
$$f(E) = \frac{1}{1 + e^{(E - E_F)/KT}}$$

where  $E$  is the energy at which occupancy factor is calculated and  $E_F$  is called the fermi energy,

$K \rightarrow$  Boltzmann Constant

$T \rightarrow$  Absolute Temp.

Occupancy factor is defined as the ratio of occupied states and available states.



At absolute 0 for energy level  $E > E_F$   $f(E) = 0$

At  $T = 0$   $E < E_F$   $f(E) = 1$

At  $T > 0$   $f(E) = 1/2$  at  $E = E_F$ .

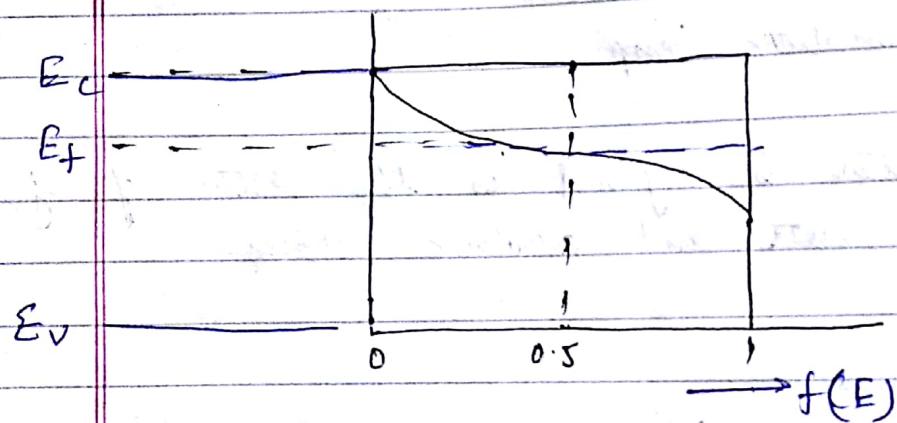
For any Temp +  $E > E_F$   
 $E < E_F$

## Define Fermi Level

It is the energy level upto which all the available states are occupied at OK. It is the energy level at which the occupancy factor is  $1/2$  at all non zero temperatures.

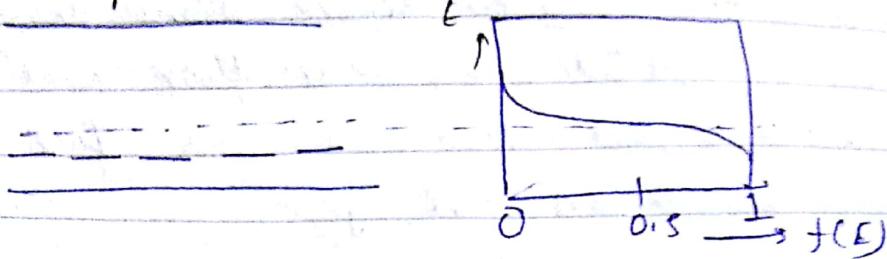
Fermi Level of n type Semiconductor :-

Why



For n type semiconductor the donor level is just below the Conduction Band. Now due to doping the bottom of the Conduction Band will be crowded due to the by electrons. Therefore the chance of lifting electrons from valence band to conduction band will be difficult. Therefore the hole concentration of the valence band will be decreased. The fermi level will be lifted towards the conduction band as doping concentration is increased. Similarly for .

Similarly for p type diag will be as follows:-

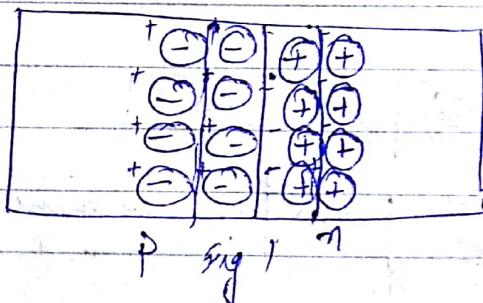


~~Why~~ Effect of temp on fermi level:-

At some temp the conc of carriers due to thermal generation will be much higher than the conc due to doping. At that point the carrier conc will be <sup>dominated</sup> by thermal generation therefore we have equal no of electrons & holes in the crystal. Therefore the semi conductor is ~~intrinsic~~ doped and behave as intrinsic.

2-2-18

### p-n junction diode



First, an intrinsic semi conductor bar is taken. Certain portion of the the bar is doped with n type impurity by employing some doping environment. After that the remaining portion is doped with p type impurity i.e. the diode is formed on a single crystal. If we consider distinct boundary b/w p and n region

so the day will be as follows  
In the afternoon we expect some late afternoon  
so in the end we have from 1 to 4 pm  
Morphogenesis is done with a free embryo  
which is known as a blastula  
budding or the yolk moves to the side  
and into a hole.

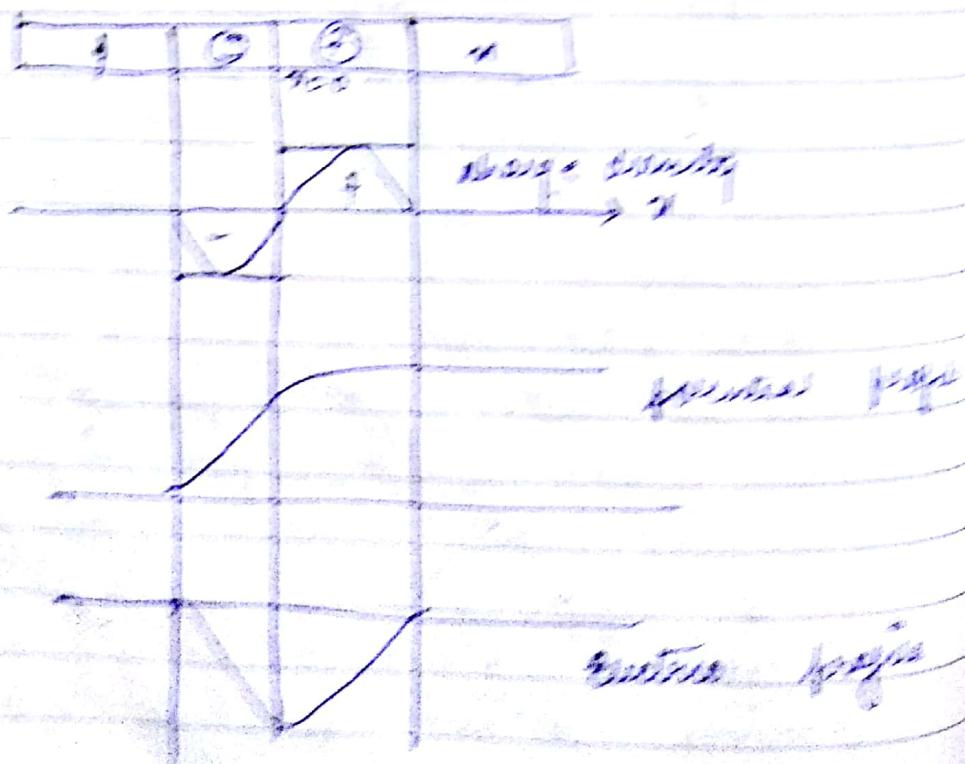
Just after gastrulation we have more in the yolk  
area. If we do not wait, formed  
gastrulation from the bottom one in place and  
because by the process of diffusion a few  
cells a side will try to move to the yolk.  
This region is called vegetal region because  
separated from the animal.

Only movable nervous area are present inside the region  
In this case this is evidence in our lab.

D

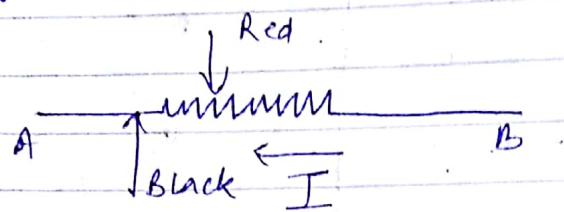
Large, extra fold, ventral part of muscle + in  
gastrulation site:

Gastrulation



Now for practical diode we do not get distinct boundary but distinct junction due to some limitations of fabrication process so we do not get uniform charge density throughout the depletion region.

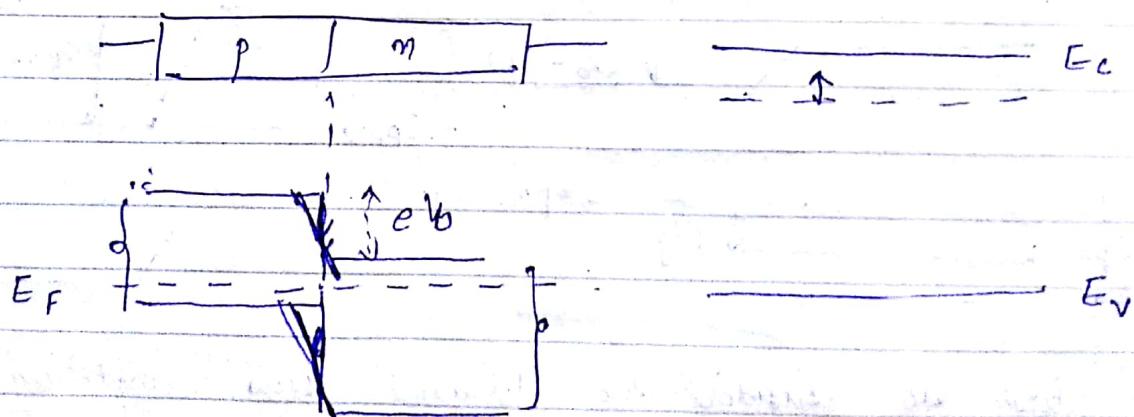
The charge density profile will look like:



If we measure the potential at the edge of the depletion layer then we get the potential profile as shown.



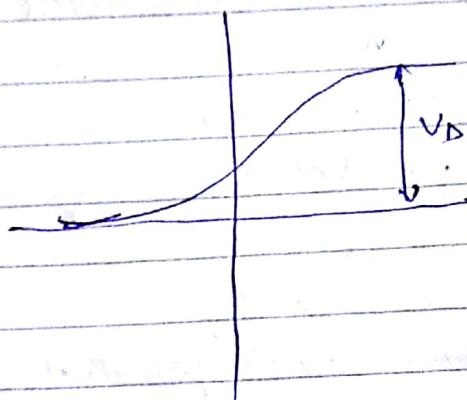
Electric profile :- Electric field  $\vec{E} = - \frac{dV}{dx}$



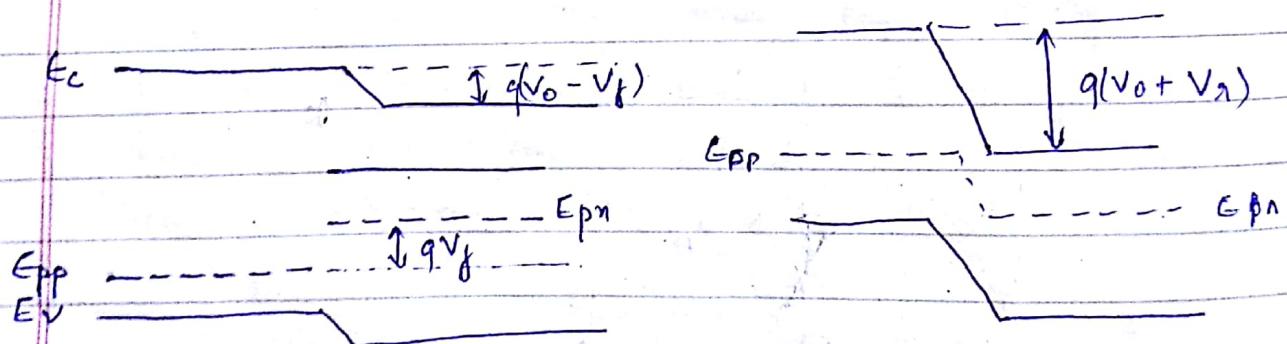
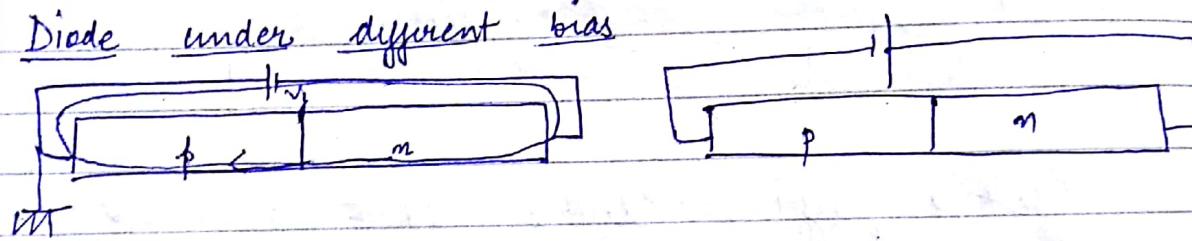
Non degenerate semiconductor men fermi level will be within forbidden region. If we dope the material with high doping conc then fermi level will go up above the C.B for n

type 2 will go below  $V_B$  before  $V_D$  for p type.

$V_0 \rightarrow$  is the barrier potential or contact potential of the diode.



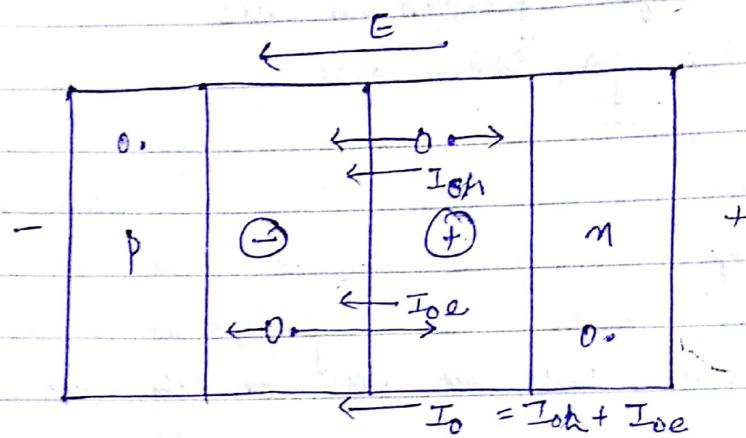
Diode under different bias



First we consider the forward bias condition on diode biased with  $V_f$ .

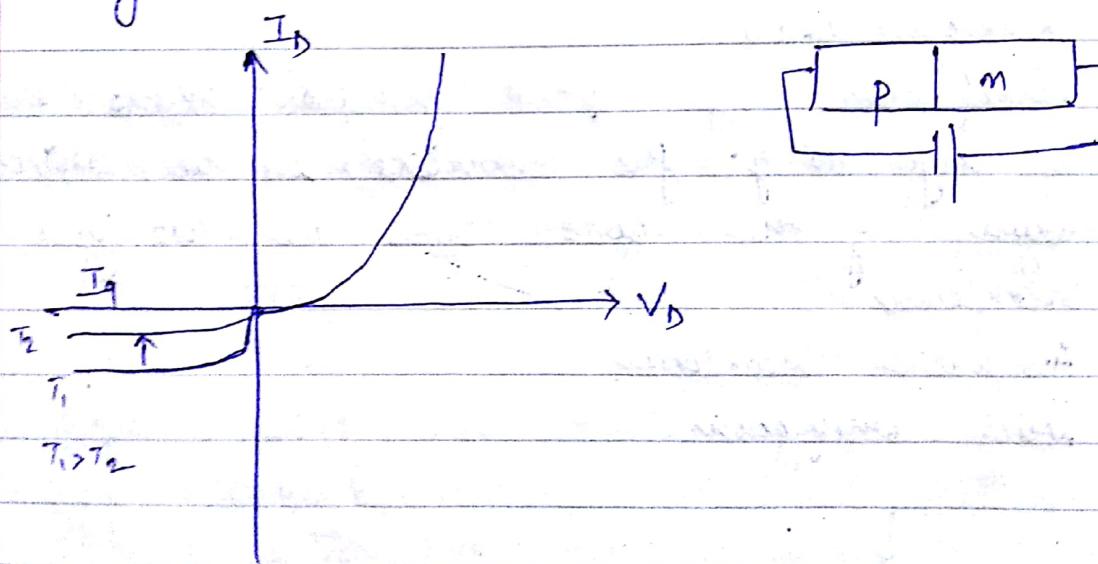
Under reverse biased, the barrier height is increased from  $qV_0$  to  $q(V_0 + V_r)$ .  $\therefore$  drift force across the junction will be more i.e. it will strongly oppose the diffusion.

And we do not get any diffusion current through the junction but in reverse bias condition a very small current  $I_o$  (reverse saturation current) will flow through the junction from n to p which is explained below:-



Now at room temp due to

~~due to~~ thermal generation  $e-h$  pairs will be generated throughout the device. Now



Minority carrier is responsible for drift current or reverse saturation current.

$$I_p = I_0 (e^{eV_B/nkT} - 1)$$

$$\text{In reverse bias condition } I_D = -I_0 e^{eV_D / nKT} - I_0$$

$$\text{forward " " } = I_0 e^{\underbrace{eV_D / nKT}_{\text{diffusion current}}} - \underbrace{I_0}_{\text{drift current}}$$

$$= I_0 e^{eV_D / nKT}$$

$\eta = 1$  for germanium diode  
 $\eta = 2$  for silicon diode

Intrinsic constant

of material:

Band gap for germanium is less than silicon generally  
 will be more for germanium than silicon.  
 germanium will have more minority carrier.

Due to less reverse saturation current silicon is used in  
 silicon diode

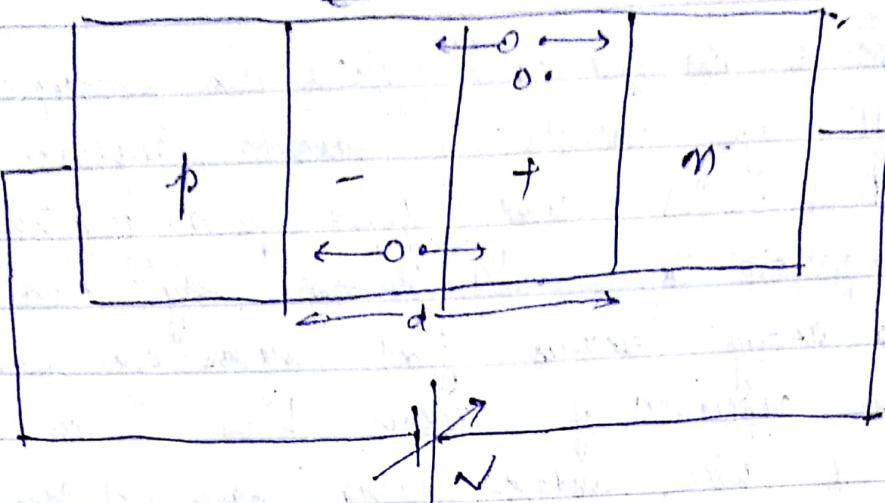
Breakdown diodes

Breakdown of p-n junction means generation  
 of large no of free carriers in the depletion  
 layer of the diode. There are two types of  
 breakdown

- 1) Avalanche breakdown
- 2) Zener breakdown



$$E = V/d$$



$$V = 0 \rightarrow \text{force}$$

$$K \cdot E = \frac{1}{2} m v^2$$

$$V = U + ft \quad P = mv$$

$$= ft$$

$$\frac{P}{m}$$

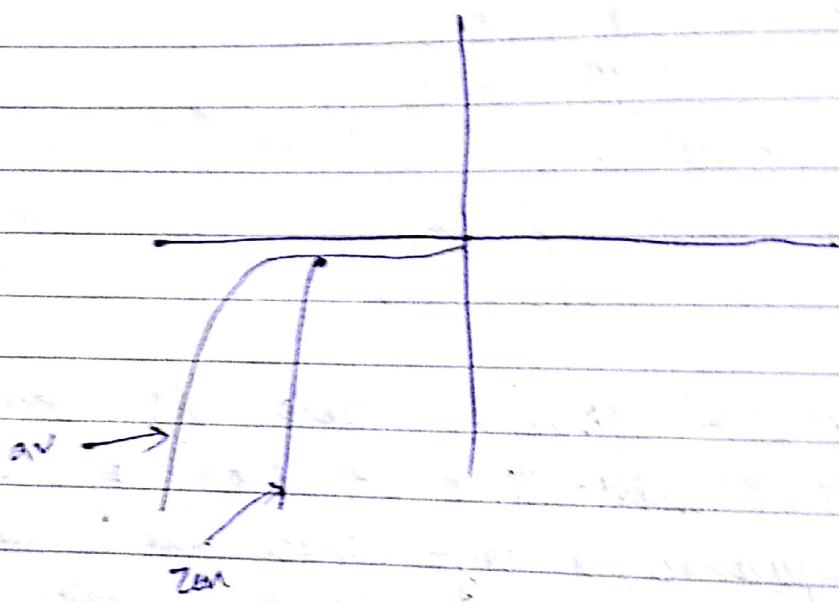
$$= \frac{P}{m}$$

$$v = \frac{qE}{m} +$$

Avalanche - Due to temp e-h pairs will be generated inside the depletion layer and they will experience a drift force due to the presence of electric field. If the diode is lightly doped then these generated free carriers will move sufficient distance and hence gather sufficient kinetic energy before collision. Therefore new e-h pair will be generated when such carrier collides with the crystalline covalent bond. And in this way we have huge no. of e-h pairs in depletion layer & they will cross the junction and generate huge current in the external circuit.

(LP) Page: 11

Laser Breakdown: There are two principles of generation of large currents & direct rupture of covalent bond. For heavily doped p-n junction diode the depletion layer ~~is~~ is very thin so we get a strong electric field across the junction due to the application of reverse bias. Under strong electric field will induce strong force on the bonds & it may result in breaking up creating huge no. of free charges & we get a large current.



Difference

Zener

① heavily doped

Avalanche

lightly doped

② thin

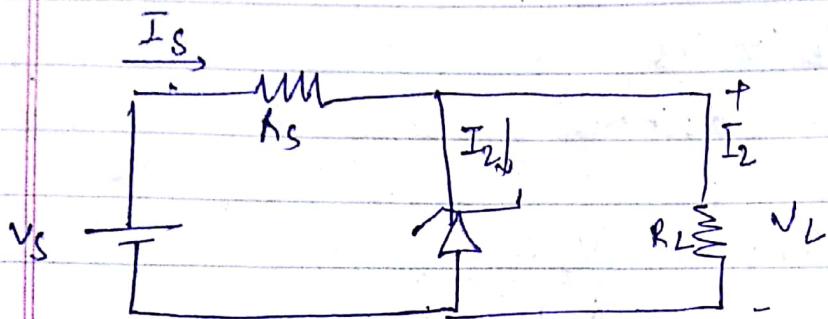
depletion layer is thick

③ Zener breakdown voltage is lower.

Avalanche Breakdown voltage is higher.

(4) -ive  
Temp coeff. of Avalanche Breakdown voltage is +ve.

Zener diode as reference voltage source or voltage regulation

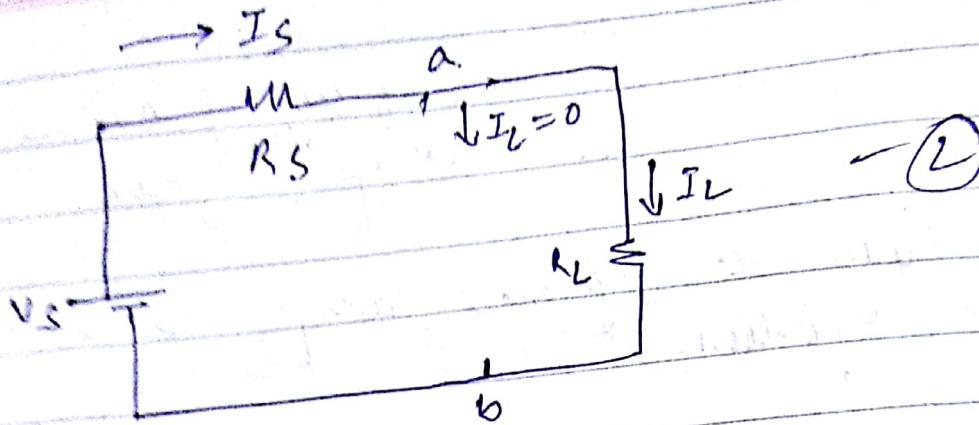


Zener diode is used as reference voltage source because it gives constant voltage across it in one breakdown region. The necessary circuit is as shown.

Here,  $V_s$  is a variable or unregulated power supply.  $R_s$  is the series resistance of Zener diode & as a zener voltage of  $V_z$   
 $R_L \rightarrow$  load resistance.

For this circuit one diode will be in the breakdown region if we apply sufficient  $V_s$

If  $V_s$  is not sufficient then the Zener will be off.

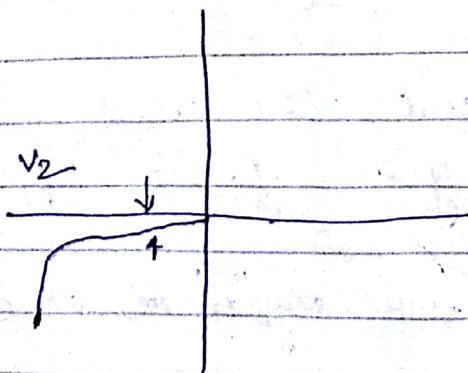


$$I_S = I_L = \frac{V_s}{R_s + R_L}$$

$$V_{ab} = I_L R_L = \frac{V_s R_L}{R_s + R_L}$$

Now this circuit will act as a voltage regulator  
only if  $\frac{V_s R_L}{R_s + R_L} > V_Z$

When the diode operates in the breakdown region  
its terminal voltage is approximately fixed to  
 $V_Z$



In breakdown region eq circuit - will look like M

$$I_S = \frac{V_S - V_Z}{R_S}, I_L = \frac{V_S}{R_L} - \frac{V_Z}{R_L}$$

$$I_R = I_S - I_L$$

Load line & Quiescent point

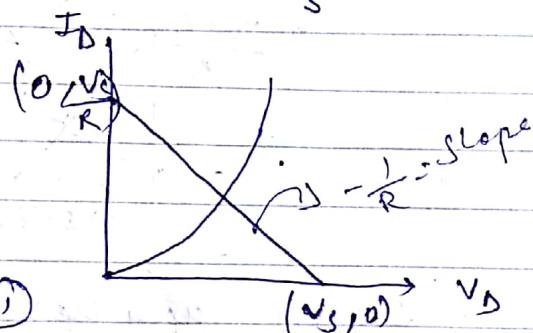
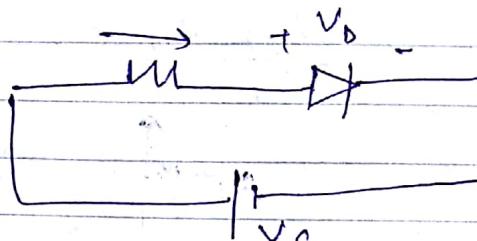
Let us consider a simple diode circuit as shown.

Here, all the voltages and current are dc

The kvl eq<sup>n</sup> of the circuit is given by

$$V_S = V_D + I_D R$$

$$I_D = -\frac{V_D}{R} + \frac{V_S}{R} \quad \text{--- (1)}$$



This line is called dc load line.

Now one diode should follow its own characteristics as well as the kvl eq<sup>n</sup>

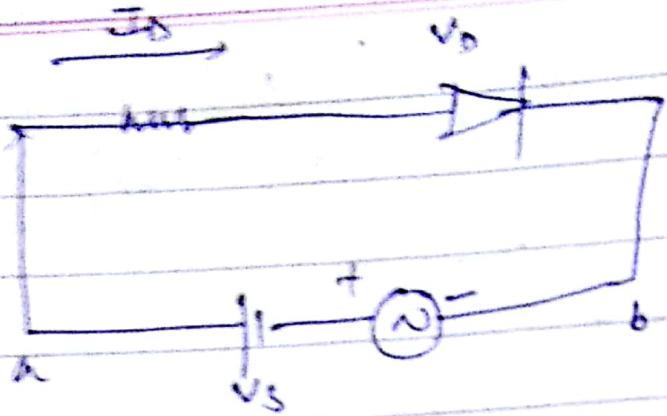
∴ the operative point of the diode should be the intersection b/w the two curves. This intersection point is called dc operating point / Quiescent point or simply Q point.

If we change the value of  $V_S$  then we get-

$$I_D = -\frac{V_D}{R} + \frac{V_S}{R}$$

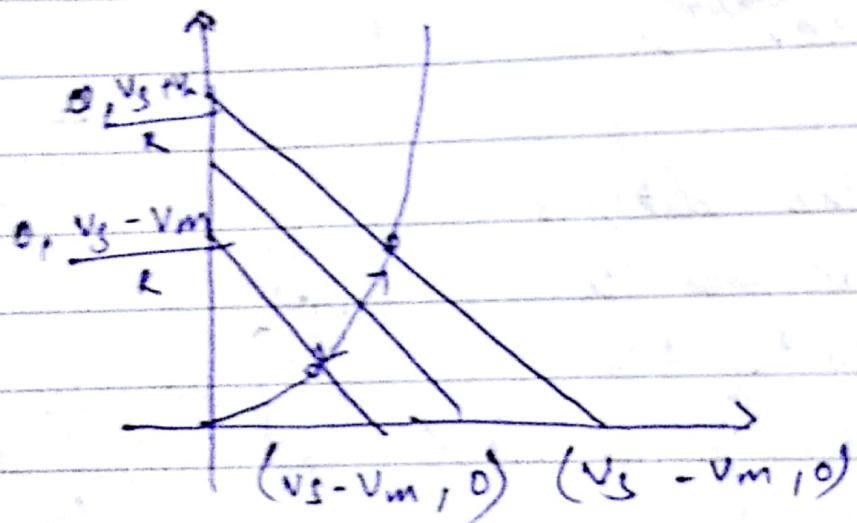
$$I_D = -\frac{V_D}{R} + \frac{V_S}{R}$$

which is parallel to first one



$$V_s + V_f = i_d R + V_o$$

$$V_s + V_m$$



Therefore upon the application of a c signal one diode will offer different resistance at diff points



Ripple factor is defined as the ratio of rms value of ripple (a.c) component of load current and the avg value of the load current.

If ripple factor is high then we say that rectification is poor bcz the purpose of the rectifier is to generate one d.c from the a.c source input.

$$\text{Ripple factor} \leftarrow \gamma = \frac{I_{\text{rms}}}{I_{\text{dc}}} = \frac{\sqrt{I_{\text{rms}}^2 - I_{\text{dc}}^2}}{I_{\text{dc}}}$$

$$= \sqrt{\left(\frac{I_{\text{rms}}}{I_{\text{dc}}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{\frac{I_m}{2}}{\frac{I_m}{\pi}}\right)^2 - 1} = \sqrt{\frac{\pi^2}{4} - 1} = 1.21$$

### Rectifier efficiency ( $\eta$ )

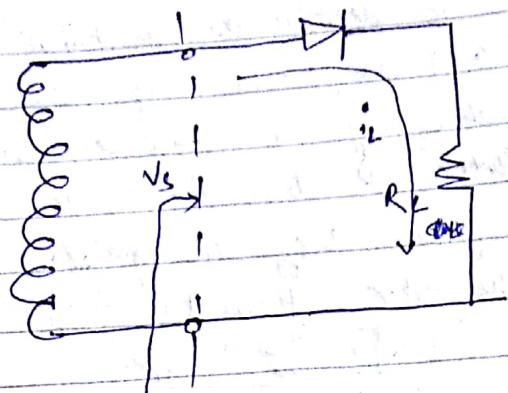
It is defined as the ratio of d.c output power to the a.c input power to the rectifier i.e. it is a measure of how much a.c power is converted into d.c.

∴

$$\eta = \frac{P_{\text{dc}}}{P_{\text{im}}} \times 100 \%$$

$$P_{\text{dc}} = I_{\text{dc}}^2 R_L$$

Input ac power to the secondary  
 $P_i = .$



$V_s \rightarrow$  drop across diode + load

$$P_i = \frac{1}{2\pi} \int_0^{2\pi} V_s i_L d(\omega t)$$

$$= \frac{1}{2\pi} \int_0^{2\pi} (R_f + R_L) i_L^2 d(\omega t)$$

$$(R_f + R_L) I_{rms}$$

$$I_{rms} = \frac{1}{2\pi} \int I_L^2 d(\omega t)$$

$$\eta = \frac{P_{dc}}{P_i} \times 100$$

$$= \frac{I_{dc}^2 R_L}{(R_f + R_L) I_{rms}^2} \times 100\%$$

$$= \left( \frac{I_m / \pi}{I_m / 2} \right)^2 \frac{100}{1 + \frac{R_f}{R_L}} \cdot \cdot \cdot$$

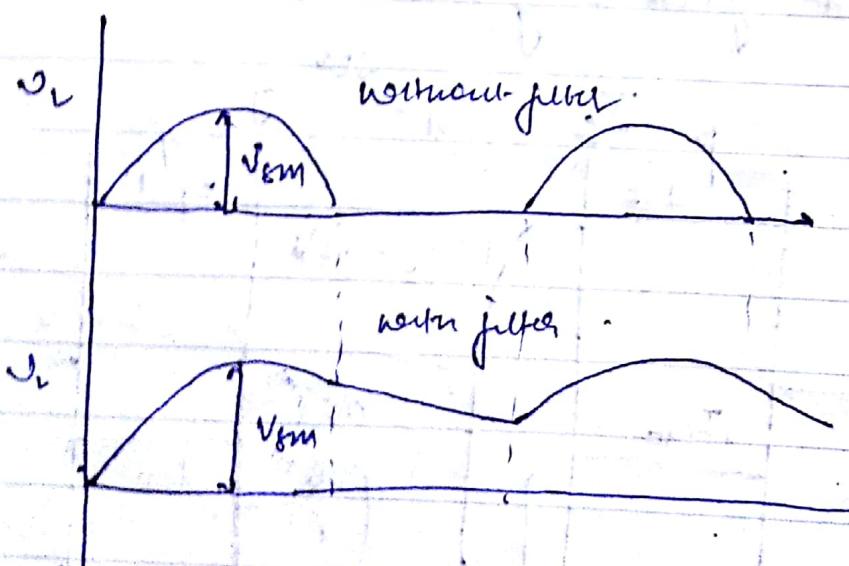
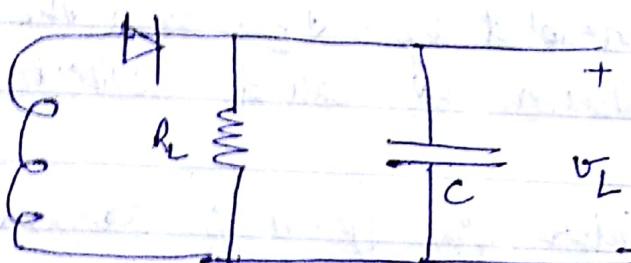
$$= \frac{40.6}{1 + \frac{R_f}{R_L}} \cdot \cdot \cdot$$

~~W.B.~~ The max efficiency obtained from the half wave rectifier = 40.6%. if the diode is ideal ie  $R_f = 0$ .

### Peak Inverse Voltage :-

It is defined as the max reverse bias voltage appears across the diode when it is in the non conducting state ie off diode is off.

i. Rating of the diode should be greater than  $V_{rm}$  ie  $v > V_{rm}$

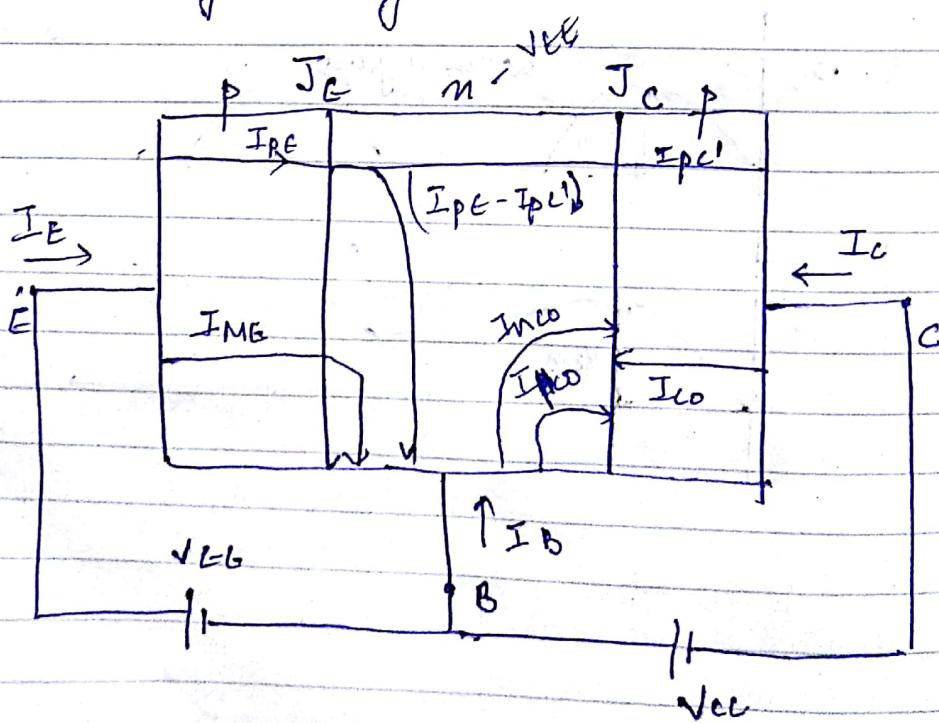


Mod - 2Bipolar Junction Transistor (BJT)

Bipolar Junction Transistor is a multi junction device. It has 3 distinct regions having different side and dopp concentration.

- 1) The emitter region is heavily doped and its side concentration is completely higher. The doping conc is denoted ( $N_E$ )
- 2) The collector region - doping conc is slightly less than that of emitter  $N_E$
- 3) At b/w emitter and collector there is a very thin region called base, and it is slightly doped.
- 4) The junction b/w emitter and base is called emitter junction denoted by  $J_E$  and the junction b/w base & collector is called collector junction denoted by  $J_C$

Now let us consider one  $P-n-p$  transistor and its current flow diagram is shown below.



Let us consider all the currents entering into the device is taken as +ve.

Under normal operating cond'n. The emitter junction is forward biased and the collector junction is reverse biased.

$$\begin{aligned} V_{CE} &= +V_{CB} + V_{BE} \\ &= -V_{EE} - V_{EE} \\ &= -ive \end{aligned} \quad \left. \begin{array}{l} \\ \\ \end{array} \right\} \text{reverse biased}$$

$$I_G = I_{pe} + I_{ne}$$

$$I_{oc} = I_{pe}$$

$$[N_E \gg N_S]$$

$$I_C + I_{pc_1} = I_{Co}$$

$$I_C = -I_{pc_1} + I_o$$

$$= -\times I_{pe} + I_{Co}$$

$$= -\times I_G + I_{Co}$$

$$= -ive$$

$$I_B = (I_{pco} + I_{nco}) - \{ (I_{pe} - I_{pc_1}) + I_{ne} \}$$

-ive

$$V_{EB} = +ve$$

$$V_{CE} = V_{CB} + V_{BE}$$

$$= -ive + (-ve)$$

= -ive