

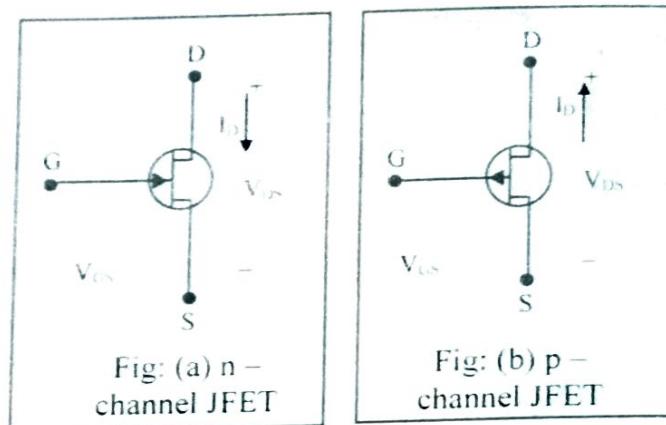
FIELD EFFECT TRANSISTOR

Chapter at a Glance

JFET

JFET is a three-terminal device with one terminal capable of controlling the current between the other two.

Symbol



JFET Parameters

For understanding the important parameters of FET, we re-draw the FET characteristics in simplified manner in fig below. We note that in the pinch-off region, the drain current I_D is practically constant but the graph has a small slope.

(a) Drain Resistance, r_d

The drain resistance r_d of a FET is defined as

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \quad \text{while } V_{GS} \text{ is held constant.}$$

The typical value of r_d ranges from 10 K ohms to 50 K ohm.

(b) Transconductance, g_m

Transconductance, g_m , of a FET is defined as the change in drain current due to a change in the gate voltage i.e., $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$ while V_{DS} is constant.

Typical values of g_m range between 2 - 6 milli-mhos.

(c) Amplification Factor, μ

The amplification factor, μ , is defined as

$$\mu = -\frac{\Delta V_{DS}}{\Delta V_{GS}} \quad \text{while } I_D \text{ is constant.}$$

we can write the equation as

$$\Delta V_{DS} + \frac{\Delta I_D}{\Delta V_{DS}} \Big|_{V_{GS} = \text{constant}} \quad \Delta V_{DS}$$

constant or $\Delta I_D = 0$

$$\frac{\Delta I_D}{\Delta V_{DS}} \Big|_{V_{GS} = \text{constant}} = \frac{\Delta I_D}{\Delta V_{DS}} \Big|_{V_{DS} = \text{constant}} \times \frac{\Delta V_{DS}}{\Delta I_D} \Big|_{V_{DS} = \text{constant}}$$

$$g_m = g_m \propto r_d$$

Small-signal Model of a FET

We have seen the drain current I_D of a FET depends on gate voltage V_{GS} and drain-to-source voltage V_{DS} .

$$I_D = f(V_{GS}, V_{DS})$$

$$\text{Taylor's series expression, } \Delta I_D = \left[\frac{\Delta I_D}{\Delta V_{GS}} \right]_{V_{DS} = \text{const}} \times \Delta V_{GS} + \left[\frac{\Delta I_D}{\Delta V_{DS}} \right]_{V_{GS} = \text{const}} \times \Delta V_{DS}$$

in small-signal notation, e.g,

$$i_d = \Delta I_D; v_{gs} = \Delta V_{GS}; \quad v_{ds} = \Delta V_{DS},$$

$$i_d = g_m v_{gs} + \frac{1}{r_d} v_{ds}$$

This equation forms the basis of the small-signal equivalent circuit of FET as shown in fig.

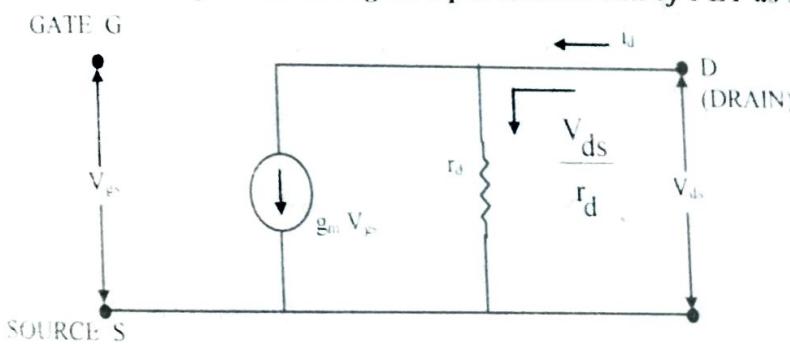


Fig: Small-signal Equivalent Circuit of FET (low frequency)

MOSFET

are called Metal oxide Semiconductor FET (MOSFET) because of its construction in which the gate is insulated by a layer of oxide from the channel. Because of the insulated gate structure, these MOSFET have very high input resistance.

In MOSFETs there are two types, namely the Enhancement type MOSFET and the Depletion type MOSFET.

Enhancement MOSFET

Symbol

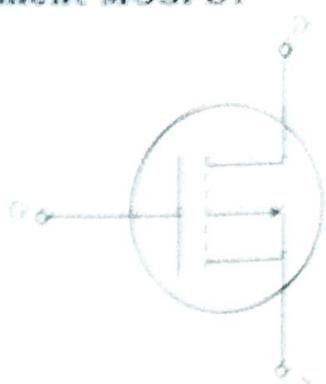


Fig (a): p-channel enhancement type MOSFET

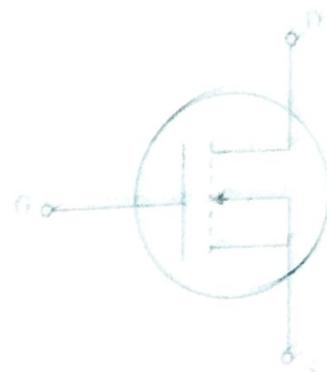


Fig (b): n-channel enhancement type MOSFET

Depletion MOSFET

Symbol

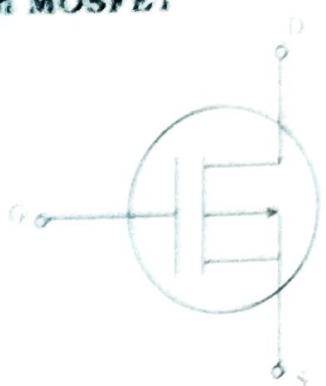


Fig (a): p-channel depletion type MOSFET

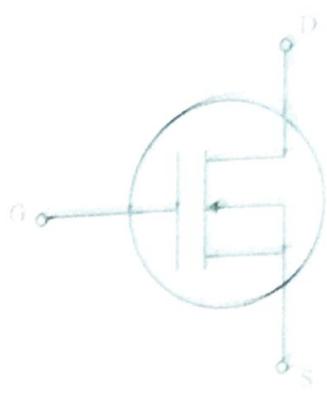


Fig (b): n-channel depletion type MOSFET

Complementary Metal Oxide Semiconductor (CMOS)

CMOS is most popular technology for the implementation of digital systems. The small size, ease of fabrication, and low power dissipation of MOSFETs enable extremely high levels of integration of both logic and memory circuits.

Merits of CMOS Technology

Source of the reasons for CMOS displacing bipolar technology in digital applications are as follows:

- (a) CMOS logic circuits dissipate much less power than bipolar logic circuits and thus one can pack more CMOS circuits on a chip than is possible with bipolar circuits.
- (b) The high input impedance of the MOS transistor allows the designer to use charge storage as a means for the temporary storage of information in both logic and memory circuits. This technique cannot be used in bipolar circuits.
- (c) The feature size (i.e., minimum channel length) of the MOS transistor has decreased dramatically over the years, with some recently reported designs utilizing channel lengths as short as 0.06um. This permits very tight circuit packing and correspondingly, very high levels of integration.

CMOS logic gate circuits:

Combinational logic circuits, which are realized by CMOS technology, used in large quantities in a multitude of applications; indeed, every digital system contains large numbers of combinational logic circuits.

Examples of CMOS logic circuits

We can implement any logic gates (NOT, NAND AND, NOR/OR, XOR/XNOR etc.) or combinational circuits using CMOS technology.

Multiple Choice Type Questions

1. In an ideal voltage controlled voltage source the value of R_s and R_o tend to
 a) 0, 0 b) 0, ∞ c) ∞ , 0 d) ∞ , ∞ [WBUT 2008]

Answer: (c)

2. Compared to the BJT, FET [WBUT 2008]
 I) has a large gain bandwidth product II) is less noisy
 III) has less input resistance IV) has only majority carrier flow

The correct statements are

- a) I and III b) I and II c) II and IV d) III and IV

Answer: (c)

3. Which of the following is not true about a JFET? [WBUT 2008]
 a) It is a current controlled device
 b) It is a majority carrier device
 c) Drain and source are interchangeable in a JFET
 d) It can be used as a voltage variable resistor

Answer: (a)

4. JFET is a [WBUT 2009]
 a) voltage controlled voltage source
 b) voltage controlled current source
 c) current controlled voltage source
 d) current controlled current source

Answer: (b)

5. The action of JFE in its equivalent circuit can best be represented as a [WBUT 2011]
 a) current controlled current source
 b) current controlled voltage source
 c) voltage controlled voltage source
 d) voltage controlled current source

Answer: (d)

6. The effective channel length of a MOSFET in saturation decreases with increase in [WBUT 2011]
 a) gate voltage b) drain voltage c) source voltage d) body voltage

Answer: (b)

7. A source follower using an FET usually has a voltage gain which is [WBUT 2011]
 a) greater than + 100
 b) slightly less than unity but positive
 c) exactly unity but negative
 d) about - 10

Answer: (b)

POPULAR PUBLICATIONS

- 1.8. For a source follower circuit, the voltage gain is [WBUT 2013]
a) zero b) slightly greater than unity
c) slightly less than unity d) none of these
- Answer: (c)
- 1.9. The threshold voltage of an enhancement PMOS is [WBUT 2013]
a) negative b) positive
c) zero with respect to source d) zero with respect to drain
- Answer: (a)
- 1.10. Which of the following devices has highest input impedance [WBUT 2014]
a) MOSFET b) BJT c) JFET
- Answer: (a)
- 1.11. FET is less noisy than BJT because of [WBUT 2015]
a) high input resistance b) low output resistance
c) voltage controlled current d) unipolar current
- Answer: (d)
- 1.12. MOSFET is a [WBUT 2015]
a) current controlled device b) voltage controlled device
c) temperature controlled device d) none of these
- Answer: (b)
- 1.13. JFET is a [WBUT 2016]
a) voltage controlled voltage source b) voltage controlled current source
c) current controlled voltage source d) current controlled current source
- Answer: (b)
- 1.14. When the gate source voltage of N-channel JFET is more negative, the drain current [WBUT 2016]
a) increases b) decreases
c) remains constant d) may increase or decrease
- Answer: (b)
- 1.15. A source follower using an FET has voltage gain which is [WBUT 2017]
a) exactly unit but negative b) slightly less than unity but positive
c) greater than + 100 d) none of these
- Answer: (b)
- 1.16. The threshold voltage of an enhancement PMOS is [WBUT 2017]
a) Positive b) Negative
c) Zero with respect to drain d) Zero with respect to source
- Answer: (b)

Short Answer Type Questions

2.1. Write down the basic difference between enhancement type and depletion type MOSFETs.
Answer:

For enhancement mode MOSFET channel is not formed at zero gate voltage. If we get channel with zero gate voltage then this is depletion mode MOSFET.

2.2. Draw schematically the structure of an *n*-channel JFET and define the terms source, drain, gate and channel. Explain the importance of the term "Field effect".
[WBUT 2013]

Answer:

1st Part:

The basic construction of the *n*-channel JFET is shown in fig., the major part being the *n*-type material that forms the channel between the embedded layers of heavily doped *p*-type material. The ends of the *n*-type channel are connected through an ohmic contact to a terminal referred to as the source (S) and the Drain (D). The two *p*-type materials are connected together and finally to the gate (G) terminal. In essence, therefore, the drain and source are connected to the ends of the *n*-type channel and the gate to the two layers of *p*-type material.

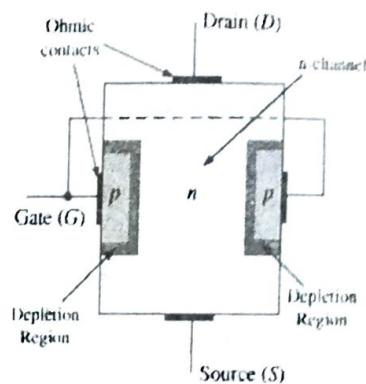


Fig: Junction Field-Effect Transistor

2nd Part:

The basic construction of the *n*-channel JFET is shown in fig., the major part being the *n*-type material that forms the channel between the embedded layers of heavily doped *p*-type material. The ends of the *n*-type channel are connected through an ohmic contact to a terminal referred to as the source (S) and the Drain (D). The two *p*-type materials are connected together and finally to the gate (G) terminal. In essence, therefore, the drain and source are connected to the ends of the *n*-type channel and the gate to the two layers of *p*-type material.

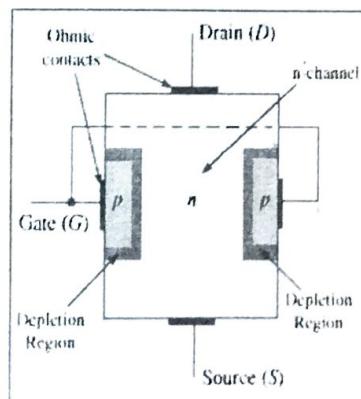


Fig: Junction Field-Effect Transistor

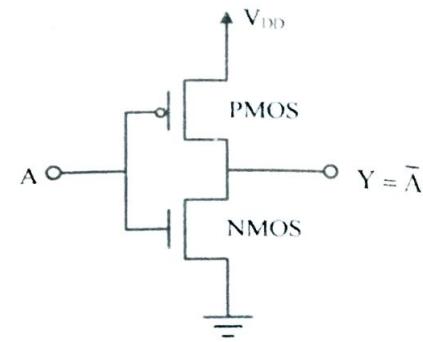
This is a voltage controlled device i.e., the output current is controlled by the electric field (ϵ) created by the applied voltage to the gate terminal. Hence, it is called Field Effect Transistor (FET).

2.3. Draw and explain the working principle of CMOS inverter circuit. [WBUT 2014]

Answer:

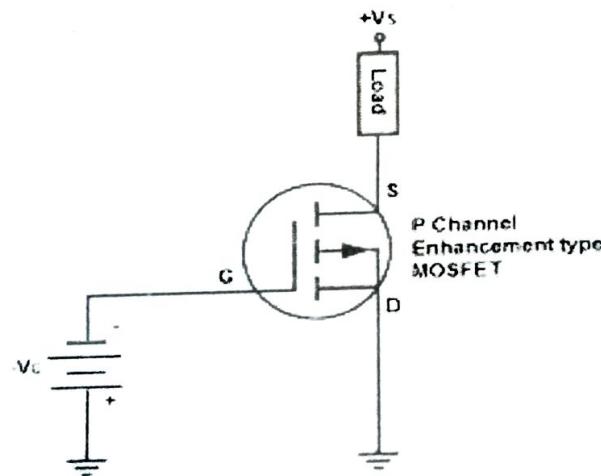
The function of the inverter circuit is described by the Boolean expression $Y = \bar{A}$ where A is input variable and Y is output function.

To synthesize the PDN, we consider the input (A) that requires Y to be low. There is only one such combination, namely, A is high. Thus, the PDN simply comprises single NMOS transistor. To synthesize the PUN, we consider the input A is low that result in Y being high. Putting PDN and PUN together results in the CMOS inverter shown in the figure.



2.4 Why do p-channel enhancement mode MOSFETs require threshold voltage? [WBUT 2016]

Answer:



The p-channel enhancement-type MOSFET fabricated on n-type substrate with p+source and p+drain. Normally, source is connected to high voltage and drain is connected to low voltage. As a negative voltage applies to the gate, the resulting field pushes electrons in n-type substrate away from the surface, leaving behind a carrier-depletion region. As gate voltage exceeds a negative threshold voltage V_t , holes accumulate on the substrate surface. After accumulation of sufficient number of holes in the channel, we get current through the channel due to flow of holes. Therefore we can enhance the concentration of holes by enhancing the gate voltage and in turn we can enhance the channel current. So we need minimum threshold voltage at the gate to maintain channel between source and drain.

2.5. With proper sketch explain the drain characteristics of an n-channel JFET.

[WBUT 2017]

Answer:

The basic construction of the n-channel JFET is shown in fig., the major part being the n-type material that forms the channel between the embedded layers of heavily doped p-type material. The ends of the n-type channel are connected through an ohmic contact to a terminal referred to as the source (S) and the Drain (D). The two p-type materials are connected together and finally to the gate (G) terminal. In essence, therefore, the drain and source are connected to the ends of the n-type channel and the gate to the two layers of p-type material.

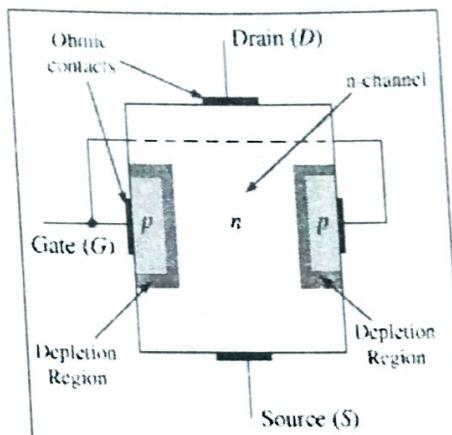


Fig: Junction Field-Effect Transistor

Working Principle*(i) If $V_{GS} = 0V$ and $V_{DS} > 0V$*

In fig., a positive value of V_{DS} has been applied across the channel and the gate has been connected to the source to establish the condition $V_{GS} = 0$. The result is a gate and source terminal at the same potential. The potential drop increases towards drain terminal w.r.t source terminal along the n channel, as a result drain end becomes more reverse biased compared to source end and depletion region penetrates more towards the drain end into the channel as shown in the next figure, i.e.. n-channel is narrow towards the drain end providing more resistance to the flow of drain current I_d . As V_{ds} is increased though it tries to increase I_d , channel will also be narrowed and resistance increases, thereby tries to decrease I_d . Initially for small V_{ds} current increases linearly, it is ohmic region. With increased V_{ds} it becomes non-linear.

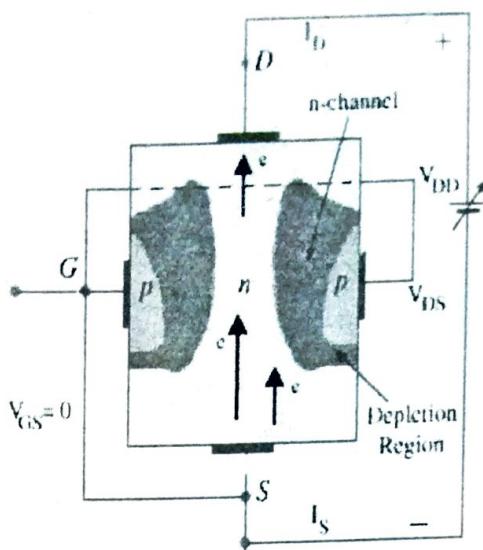


Fig: JFET in the $V_{GS} = 0V$ and $V_{DS} > 0V$

(ii) If V_{DS} is increasing (Pinch off)

As V_{DS} is increased to a level where it appears that, the two depletion regions will almost touch each other as shown in fig., the condition is referred to as the pinch-off condition. The level of V_{DS} is referred to as *pinch-off voltage* and is denoted by V_p . At this condition I_d reaches a saturation value and is termed as saturation region.

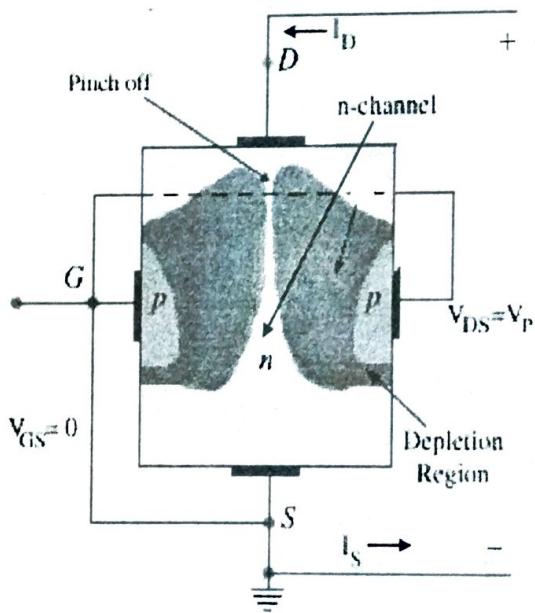
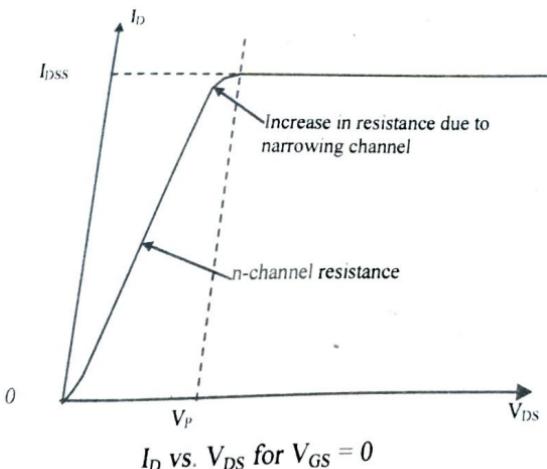


Fig: Pinch-off ($V_{GS} = 0V$, $V_{DS} = V_p$)

The term "pinch-off" is a misnomer because it suggests that the current I_D is pinched-off and drops to 0. However, in reality, I_D maintains a saturation level defined as I_{DSS} as shown in fig. below. A very small channel still exists, with a very high density current.



maximum drain current for a JFET and is defined by the conditions $V_{GS} = 0$

$$(at \text{ pinch-off}) = V_{p0} + V_{GS}$$

$$= V_{DS} \text{ when } V_{GS} = 0 \text{ at pinch-off}$$

and further avalanche breakdown may occur at the depletion region, drain rapidly. This part is termed as breakdown region.

Quenching

voltage of -1 V has been applied between the gate and source terminals. The effect of the applied negative bias V_{GS} is to establish depletion result channel becomes narrower, I_d decreases and will reach off condition earlier. Eventually, V_{GS} (when $V_{GS} = -V_p$) will be to establish complete quenching of current i.e. $I_d=0$ and for all device has been "turned off" or "cut off".

results in $I_D = 0mA$ is defined by

ing a positive voltage for p-channel JFETs.

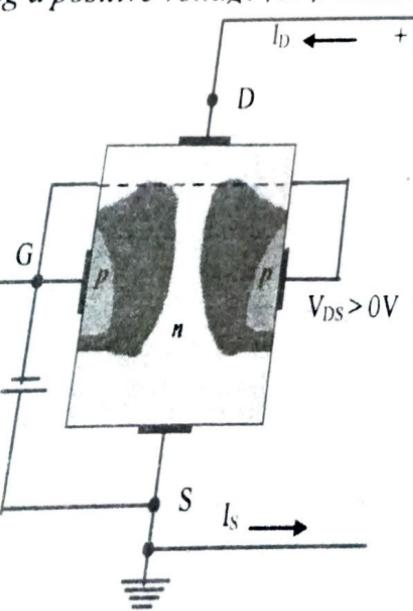
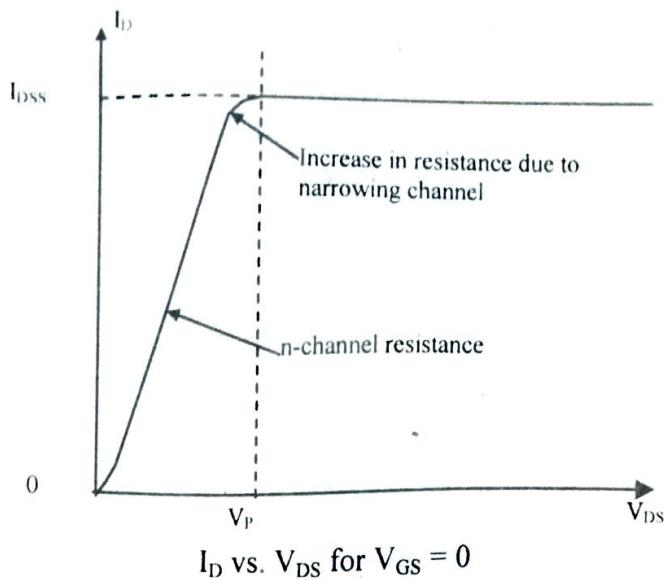


Fig: Application of a negative bias to the Gate of a JEFT



I_{DSS} is the maximum drain current for a JFET and is defined by the conditions $V_{GS} = 0$ and $V_{DS} > |V_p|$

$$V_{DS} (\text{at pinch-off}) = V_{p0} + V_{GS}$$

where $V_{p0} = V_{DS}$ when $V_{GS} = 0$ at pinch-off

If V_{ds} is increased further avalanche breakdown may occur at the depletion region, drain current increases rapidly. This part is termed as breakdown region.

(iii) If V_{GS} is decreasing

In fig., a negative voltage of -1V has been applied between the gate and source terminals for a low level of V_{DS} . The effect of the applied negative bias V_{GS} is to establish depletion region further as a result channel becomes narrower, I_d decreases and will reach saturation or pinch-off condition earlier. Eventually, V_{GS} (when $V_{GS} = -V_p$) will be sufficiently negative to establish complete quenching of current i.e. $I_d=0$ and for all practical purposes the device has been "turned off" or "cut off".

The level of V_{GS} that results in $I_D = 0mA$ is defined by

$V_{GS} = -V_p$, with V_p being a positive voltage for p-channel JFETs.

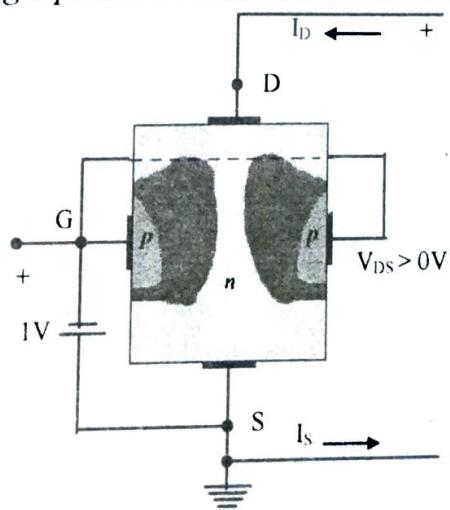
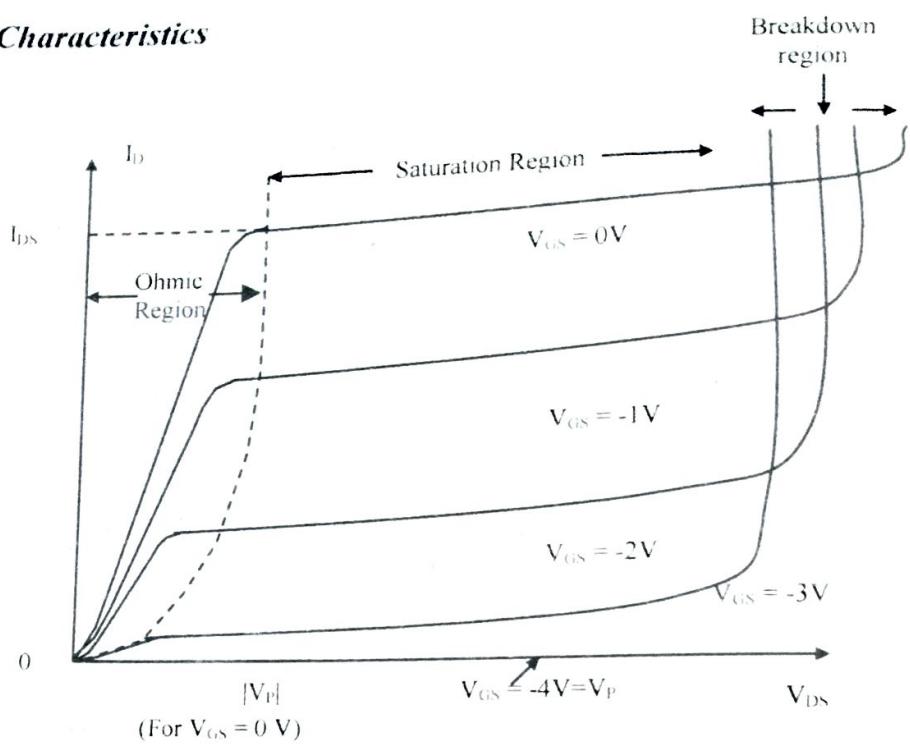


Fig: Application of a negative bias to the Gate of a JEFT

JFET Drain Characteristics



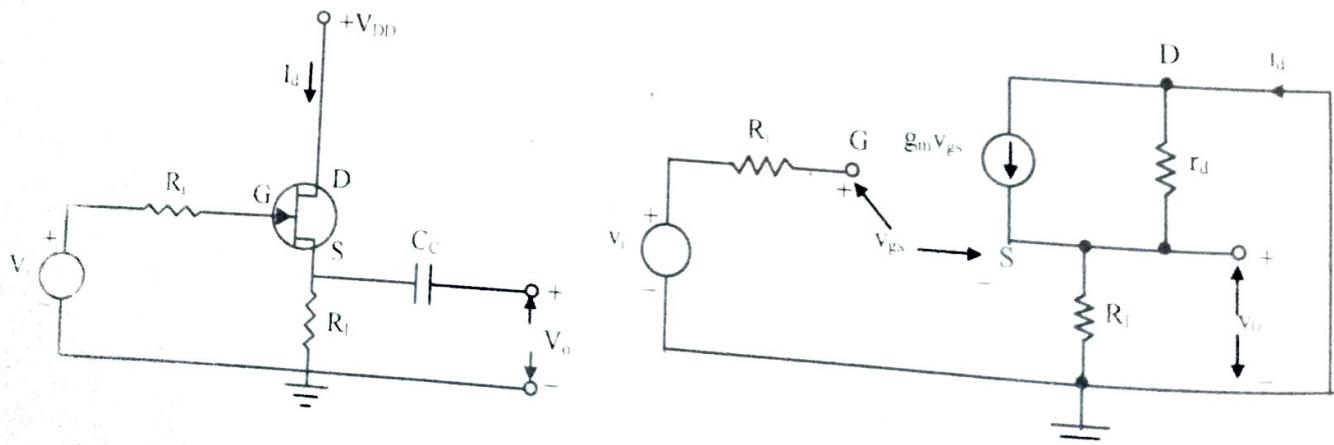
Long Answer Type Questions

- 3.1. a) Draw the circuit diagram of source follower using JFET and explain its operation. What is the highest voltage gain available from such an amplifier circuit? Comment on the input and output impedance. [WBUT 2006]

Answer:

The basic circuit of a common drain amplifier using field effect transistor is shown in the figure.

In this circuit the drain is connected to the d.c. supply and for the a.c. signal analysis the d.c. supply is shorted to ground. Hence signal applied between the gate and the drain is basically between gate and the ground. The output is being taken between the source and the ground (means drain). The equivalent circuit is therefore, drawn as shown in the following figure:



Gain

Applying KVL to the output circuit, we get: $i_d R_o - (i_d - g_m V_{in}) r_s = 0$

$$= V_{in} - i_d R_o$$

$$(r_s + r_i) - g_m r_s (V_{in} - i_d R_o) = 0$$

$$\frac{g_m r_s V_{in}}{[r_s(1-\mu) + r_i]} = \frac{\mu V_{in}}{[r_s + (1-\mu) R_o]}$$

$$\text{Voltage is given by: } V_o = i_d R_o = \frac{\mu V_{in}}{[r_s + (1-\mu) R_o]}$$

$$\text{Gain of the amplifier can be obtained as } A_v = \frac{V_o}{V_{in}} = \frac{\mu R_o}{[r_s + (1-\mu) R_o]}$$

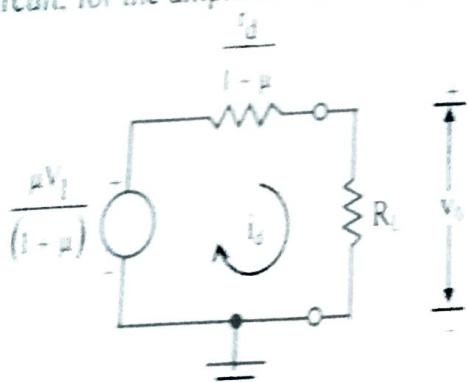
$$r_s \text{ then } A_v \approx \frac{\mu}{(1-\mu)}$$

$\mu > 1$ for the field effect transistors, so the gain of the amplifier will equal to unity ($A_v \approx 1$). The voltage gain of unity means that the output follows the input (gate) signal. Hence the Common Drain configuration may be called **Source Follower** circuit, similar to the emitter follower of bipolar transistor.

ence

$$V_o = \frac{\frac{\mu V_{in}}{(1-\mu)} R_o}{\left[\frac{r_s}{(1-\mu)} + R_o \right]}$$

nt circuit, for the amplifier whose output voltage V_o is given above, is



Z_o of the source follower circuit is obtained from the Fig. as:

$$\approx \frac{1}{g_m}$$

a) Voltage Gain

Applying the KVL to the output circuit, we get: $i_d \cdot R_i + (i_d - g_m V_{os}) r_d = 0$

$$\text{and } V_{os} = V_i - i_d \cdot R_i$$

$$\text{or } i_d (R_i + r_d) - g_m r_d (V_i - i_d \cdot R_i) = 0$$

$$\text{or } i_d = \frac{g_m r_d V_i}{[R_i (1 + \mu) + r_d]} = \frac{\mu V_i}{[r_d + (1 + \mu) R_i]}$$

$$\text{The output voltage is given by: } V_o = i_d R_i = \frac{\mu V_i R_i}{[r_d + (1 + \mu) R_i]}$$

$$\text{The voltage gain of the amplifier can be obtained as } A_v = \frac{V_o}{V_i} = \frac{\mu R_i}{[r_d + (1 + \mu) R_i]}$$

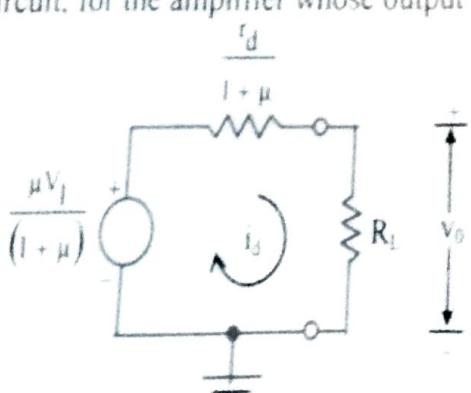
$$\text{if } (1 + \mu) R_i \gg r_d \text{ then } A_v \approx \frac{\mu}{(1 + \mu)}$$

Note: Generally $\mu \gg 1$ for the field effect transistors, so the gain of the amplifier will become almost equal to unity ($A_v \approx 1$). The voltage gain of unity means that the output (Source) follows the input (gate) signal. Hence the Common Drain configuration may be called as the **Source Follower** circuit, similar to the emitter follower of bipolar transistor amplifiers.

b) Output Impedance

$$\text{The output voltage, } V_o = \frac{\frac{\mu V_i}{(1 + \mu)} R_i}{\left[\frac{r_d}{(1 + \mu)} + R_i \right]}$$

Thevenin's equivalent circuit, for the amplifier whose output voltage V_o is given above, is shown in Fig. below.



Output impedance Z_o of the source follower circuit is obtained from the Fig. as:

$$Z_o = \frac{r_d}{1 + \mu} \approx \frac{r_d}{\mu} \approx \frac{1}{g_m}$$

b) What is understood by pinch off voltage?

OR,

Write short note on Pinch-off condition of JFET.

[WBUT 2006, 2008, 2009, 2010]

[WBUT 2015]

Answer:

If V_{DS} is increasing (Pinch off)

As V_{DS} is increased to a level where it appears that, the two depletion regions will almost touch each other as shown in fig., the condition is referred to as the pinch-off condition. The level of V_{DS} is referred to as *pinch-off voltage* and is denoted by V_p . At this condition, I_d reaches a saturation value and is termed as saturation region.

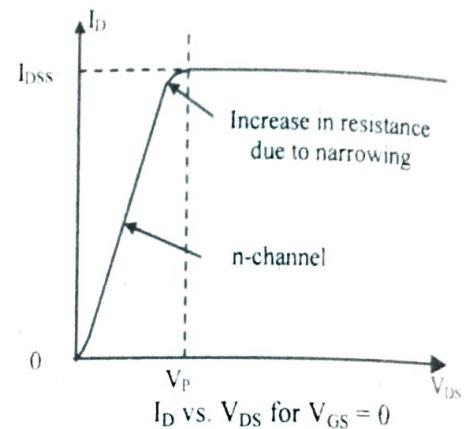
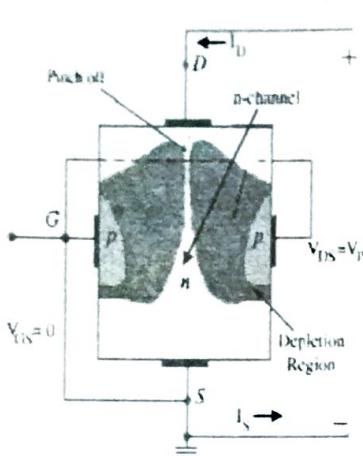


Fig: Pinch-off ($V_{GS} = 0V$, $V_{DS} = V_p$)

The term "pinch-off" is a misnomer because it suggests that the current I_D is pinched-off and drops to 0. However, in reality, I_D maintains a saturation level defined as I_{DSS} as shown in fig. A very small channel still exists, with a very high density current.

I_{DSS} is the maximum drain current for a JFET and is defined by the conditions $V_{GS} = 0$ and $V_{DS} > |V_p|$

$$V_{DS}(\text{at pinch-off}) = V_{p0} + V_{GS} \quad \text{where } V_{p0} = V_{DS} \text{ when } V_{GS} = 0 \text{ at pinch-off}$$

If V_{ds} is increased further avalanche breakdown may occur at the depletion region, drain current increases rapidly. This part is termed as breakdown region.

c) For a depletion mode n channel MOSFET, the pinch-off voltage is negative with respect to source. Explain. For enhancement mode p channel MOSFET, what is the polarity of pinch-off voltage?

[WBUT 2006]

Answer:

Refer to Question No. 3.1(b).

For enhancement mode p channel MOSFET, the polarity of pinch-off voltage is negative.

3.2. Why is a FET known as unipolar device? What is pinch off phenomenon in a JFET? How do you compare this device with a BJT?

[WBUT 2008]

OR

What are the basic differences between BJT and FET?

[WBUT 2012, 2017]

Answer:

It is a unipolar device because current in the device is carried either by electrons or holes.

Refer to Question No. 3.1 (Part b).

1st Part:
Field Effect Transistor

1. It is a unipolar device i.e., current in the device is carried either by electrons or holes.
2. It is a voltage controlled device i.e., voltage at the gate (or drain) terminals controls the amount of current flowing through the device.
3. Its input resistance is very high and is of the order of several mega ohms.
4. It has a negative temperature coefficient at high levels. It means that current decreases as the temperature increases. This characteristic prevents the FET from thermal breakdown.
5. It does not suffer from minority carriers storage effects and therefore has higher switching speeds and cut-off frequencies.
6. It is less noisy than a BJT or Vacuum tube and is thus more suitable as an input amplifier for low-level signals. It is used extensively in high fidelity frequency modulated receivers.
7. It is much simpler to fabricate as an integrated circuit (IC) and occupies a less space on IC chip than that BJT

Bipolar Junction Transistor

1. It is a bipolar device, i.e., current in the device is carried by both electrons and holes.
2. It is a current-controlled device i.e., the base current controls the amount of collector current.
3. Its input resistance is very low as compared to FET and is of the order of few kilo ohms.
4. It has a positive temperature coefficient at high current level. It means that collector current increases with the increase in temperature. This characteristic leads the BJT to thermal breakdown.
5. It suffers from minority carrier storage effects and therefore has lower switching speed and cut-off frequencies than that of FET.
6. It is comparatively noisier than a FET.

3.3. a) What are the disadvantages of FET over BJT?

[WBUT 2008]

b) Why is FET called unipolar transistor?

c) What do you mean by pinch-off condition in JFET?

Answer:

a) The only disadvantage of FET over BJT is 'Low Switching Speed'.

b) Refer to Question No. 3.2(1st Part).

c) Refer to Question No. 3.1(b).

3.4. a) With a neat diagram draw and explain the basic structure of an n channel JFET. [WBUT 2010]

Answer:

The basic construction of the n-channel JFET is shown in fig., the major part being the n-type material that forms the channel between the embedded layers of heavily doped p-type material. The ends of the n-type channel are connected through an ohmic contact to a terminal referred to as the source (S) and the Drain (D). The two p-type materials are connected together and finally to the gate (G) terminal. In essence, therefore, the drain and source are connected to the ends of the n-type channel and the gate to the two layers of p-type material.

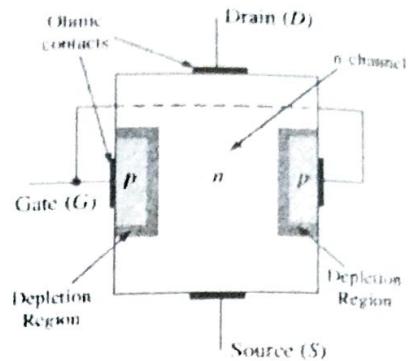


Fig: Junction Field-Effect Transistor

b) Define Transconductance, AC drain resistance, Amplification factor of JFET. [WBUT 2010]

Answer:

For understanding the important parameters of FET, we re-draw the FET characteristics in simplified manner in fig below. We note that in the pinch-off region, the drain current I_D is practically constant but the graph has a small slope.

(a) Drain Resistance, r_d

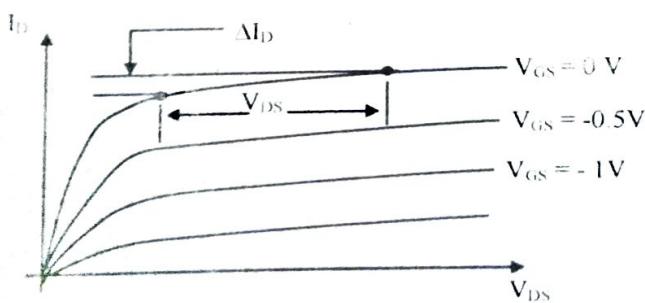
The drain resistance r_d , of a FET is defined as $r_d = \frac{\Delta V_{DS}}{\Delta I_D}$ while V_{GS} is held constant.

The typical value of r_d ranges from 10 K ohms to 50 K ohm.

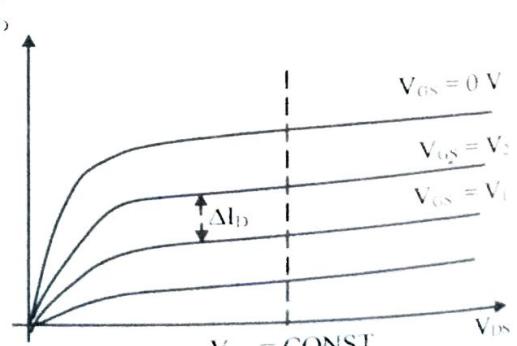
(b) Transconductance, g_m

Transconductance, g_m , of a FET is defined as the change in drain current due to a change in the gate voltage i.e., $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$ while V_{DS} is constant.

Typical values of g_m range between 2 - 6 milli-mhos.



(a) Drain Resistance, r_d



(b) Transconductance, g_m

Fig.: Understanding r_d and g_m from FET characteristics.

ification Factor, μ

If the factor, μ , is defined as, $\mu = -\frac{\Delta V_{DS}}{\Delta V_{GS}}$ while I_D is constant.

re-write the equation as

$$I_D = f(V_{GS}, V_{DS})$$

$$\Delta I_D = \frac{\Delta I_D}{\Delta V_{GS} \mid_{V_{DS} \text{ constant}}} \Delta V_{GS} + \frac{\Delta I_D}{\Delta V_{DS} \mid_{V_{GS} \text{ constant}}} \Delta V_{DS}$$

and $I_D = \text{constant}$ or $\Delta I_D = 0$

$$\frac{\Delta I_D}{\Delta V_{GS} \mid_{V_{DS} \text{ constant}}} =$$

$$= \frac{\Delta I_D}{\Delta V_{DS} \mid_{V_{GS} \text{ constant}}} =$$

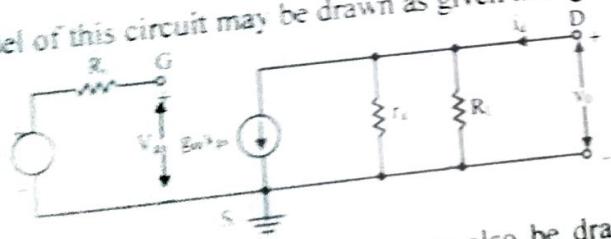
$$= \frac{\Delta I_D}{\Delta V_{GS} \mid_{V_{DS} \text{ constant}}} \times \frac{\Delta V_{GS}}{\Delta V_{DS} \mid_{V_{GS} \text{ constant}}}$$

$$g_m = g_m \times r_s$$

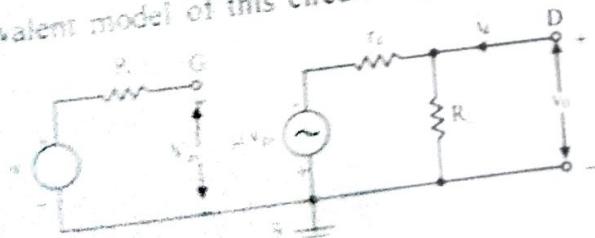
Show the common source JFET amplifier circuit and find out the expression for gain and output impedance. [WBUT 2010]

basic circuit diagram of common source amplifier is shown in Fig. below, in which the source is connected between input and output circuit. The signal V_i to be amplified is applied to the gate terminal of the FET. The output is taken at the drain across the load resistance R_L .

Small signal model of this circuit may be drawn as given in Fig. below.



Thevenin's equivalent model of this circuit may also be drawn as shown in Fig.



Amplification Factor, μ

The amplification factor, μ , is defined as, $\mu = -\frac{\Delta V_{DS}}{\Delta V_{GS}}$ while I_D is constant.

We can re-write the equation as

$$I_D = f(V_{DS}, V_{GS})$$

$$\Delta I_D = \frac{\Delta I_D}{\Delta V_{DS}} \Bigg|_{V_{GS}=\text{constant}} \Delta V_{DS} + \frac{\Delta I_D}{\Delta V_{GS}} \Bigg|_{V_{DS}=\text{constant}} \Delta V_{GS}$$

To maintain $I_D = \text{constant}$ or $\Delta I_D = 0$

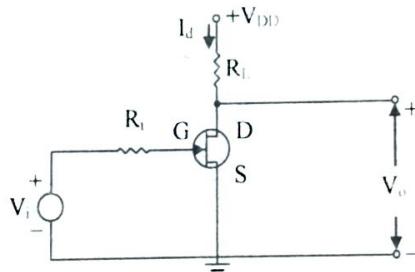
$$\begin{aligned} \frac{\Delta I_D}{\Delta V_{GS}} \Bigg|_{V_{DS}=\text{constant}} &= \frac{\Delta I_D}{\Delta V_{DS}} \Bigg|_{V_{GS}=\text{constant}} \\ &= \frac{\Delta I_D}{\Delta V_{GS}} \Bigg|_{V_{DS}=\text{constant}} \times \frac{\Delta V_{DS}}{\Delta I_D} \Bigg|_{V_{GS}=\text{constant}} \end{aligned}$$

$$\text{or } \mu = g_m \times r_d$$

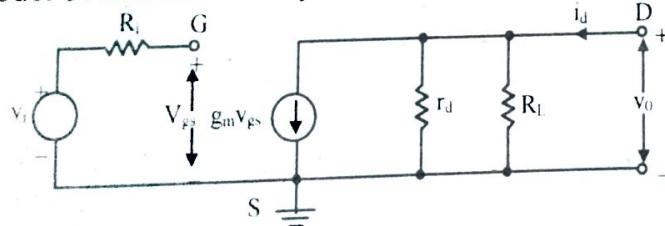
c) Draw the common source JFET amplifier circuit and find out the expression for voltage gain and output impedance. [WBUT 2010]

Answer:

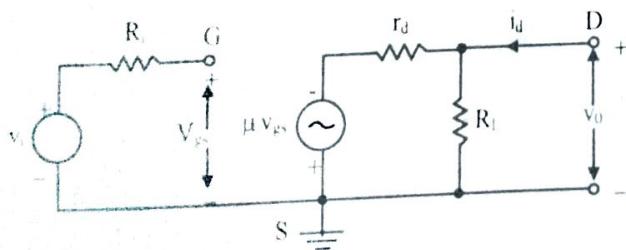
The basic circuit diagram of common source amplifier is shown in Fig. below, in which the source is common between input and output circuit. The input signal V_i to be amplified is applied to the gate terminal of the FET. The output is taken at the drain and across the load resistance R_L .



The small signal model of this circuit may be drawn as given in Fig. below.



The Thevenin's equivalent model of this circuit may also be drawn as shown in Fig. below.



a) *Voltage Gain*

Applying KVL, $V_o = i_d R_L = \frac{\mu V_{gs}}{r_d + R_L} \times R_L$ and $V_i = V_{gs}$

The voltage gain $A_v = \frac{V_o}{V_i}$ of the amplifier can be calculated from the Fig., as

$$A_v = \frac{V_o}{V_i} = \frac{-\mu}{r_d + R_L} \times R_L = \frac{-\left(\frac{\mu}{r_d}\right)}{\left(1 + \frac{R_L}{r_d}\right)} \times R_L = \frac{-g_m}{\left(1 + \frac{R_L}{r_d}\right)} \times R_L$$

If $r_d \gg R_L$, then the voltage gain of the amplifier is given as: $A_v = -g_m R_L$

The negative sign in this expression indicates that there is a phase reversal of 180° between input and output signal.

b) *Output impedance* $Z_o = r_d$

d) Write three differences between JFET and MOSFET.

[WBUT 2010]

Answer:

JFET	MOSFET
1. The gate is not insulated from the channel.	1. The gate is insulated from the channel by a layer of insulating oxide (SiO_2).
2. There are two types: P-type and N-type channel	2. There are four types: P-type enhancement MOSFET N-type enhancement MOSFET P-type depletion MOSFET N-type depletion MOSFET
3. Operated only in depletion mode.	3. Can be operated in depletion as well as enhancement mode.
4. There is a continuous channel.	4. There is continuous channel only in depletion type, but not in enhancement type.
5. High input resistance ($> 10 \text{ M}\Omega$)	5. Very high input resistance ($> 10,000 \text{ M}\Omega$)
6. Drain resistance is higher ($r_d = 100\text{K}$ to $1\text{M}\Omega$)	6. Drain resistance lower ($r_d = 1\text{K}$ to $50\text{ K}\Omega$)
7. $g_m = 0.1$ to 10 mA/V	7. $g_m = 0.1$ to 20 mA/V , or more
8. Inter-electrode capacitances $0.1 - 10 \text{ pF}$	8. Inter-electrode capacitances $0.1 - 10 \text{ pF}$
9. Generally not used in digital circuit.	9. Extensively used in digital circuit.

3.5. a) What is the relation between JFET parameters?

[WBUT 2011, 2015]

Answer: Refer to Question No. 3.4(b).

b) Draw and explain the drain characteristics of an *n*-channel enhancement type MOSFET.
[WBUT 2011]

Answer:
These are called Metal oxide Semiconductor FET (MOSFET) because of its construction in which the metal gate is insulated by a layer of oxide from the channel. Because of the insulated gate construction, these MOSFET have very high input resistance. Among MOSFETs there are two types, namely the Enhancement type MOSFET and the Depletion type MOSFET.

Enhancement MOSFET

Symbol

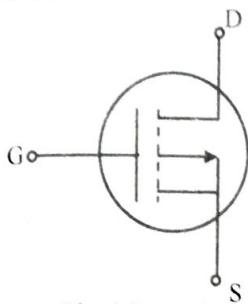


Fig (a): p-channel
enhancement type MOSFET

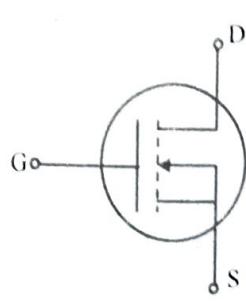


Fig (b): n-channel
enhancement type MOSFET

Construction

The following figure shows the construction of a n-channel MOSFET. Two highly doped n^+ regions are diffused into a lightly doped p-type substrate. One of these n^+ regions works as source and the other one as drain. A thin layer of an insulating material viz., silicon dioxide (SiO_2) is deposited over the surface. The gate metal, namely Aluminum is deposited over SiO_2 layer, for making connection for the gate, source and drain.

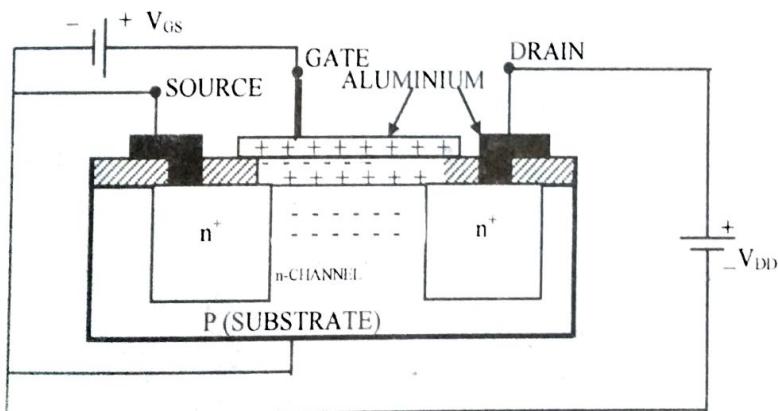


Fig: Enhancement type (n-channel) MOSFET

Operation

The substrate is grounded (connected to the source). If we apply a positive voltage to the gate, an electric field will be developed perpendicular to the SiO_2 surface. The +ve charge on the gate will induce -ve charge in the near end of the SiO_2 layer and +ve charge in the far end of the SiO_2 . Finally, it will induce negative charge in the p-type substrate, as shown. These induced negative charges (also called induced n-channel),

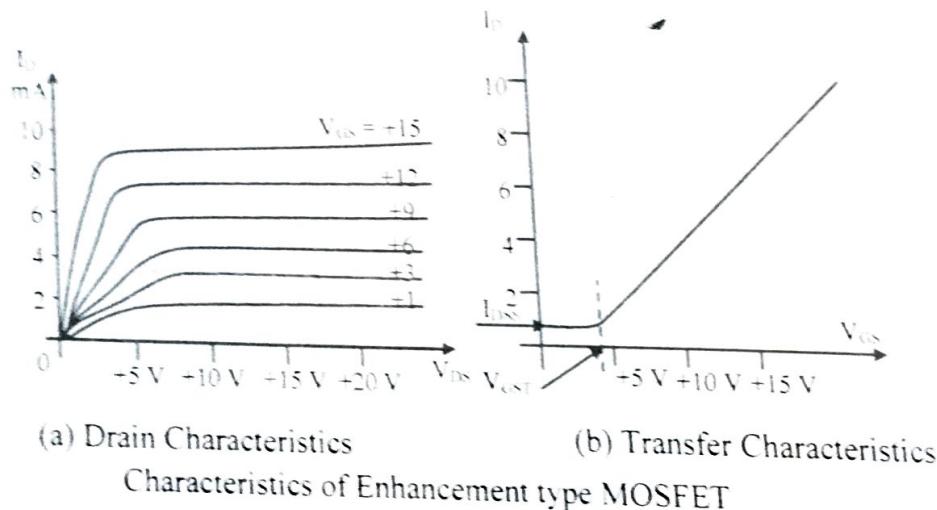
which are minority carriers in the p-type substrate, causes current flow between source and drain.

If the magnitude of +ve voltage on the gate increases, the induced -ve charge in the semiconductor also increases. The drain current is "enhanced" (means: increased) by the +ve gate voltage. Hence such a device is called Enhancement type MOSFET.

Characteristics

In Enhancement type MOSFETs, the drain current increases by making V_{GS} more positive. This is shown in the drain characteristics, Fig (a).

The Fig.(b) shows the transfer characteristics, which gives the relationship between drain current and gate voltage. When $V_{GS} = 0$, the drain current I_{DSS} is very small, only a few nano-amperes. The drain-current starts increasing only after a minimum value of V_{GS} is exceeded: this value of V_{GS} is called the threshold voltage V_{GST} . The drain characteristics in this condition is governed by V_{DS} as in the case of JFET through the modulation of depletion region.



(a) Drain Characteristics

(b) Transfer Characteristics

Characteristics of Enhancement type MOSFET

c) Calculate the drain current at gate voltage of -2V for an n – channel JFET, which has saturation drain current at zero gate bias = 10 mA and pinch-off voltage = -3.5V.

Answer:

$$\text{We know that in JFET, } I_{DS} = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Where, $I_{DS} \rightarrow$ drain current = ?; $I_{DSS} \rightarrow$ saturation drain current = 10 mA
 $V_{GS} \rightarrow$ gate voltage = -2V; $V_p \rightarrow$ pinch-off voltage = -3.5 V
 Therefore, $I_{DS} = 10 \left(1 - \frac{-2}{-3.5}\right)^2 = 34.49 \text{ mA}$

3.6. a) Explain the basic operation of depletion type n channel MOSFET with a suitable diagram.

[WBUT 2012, 2015]

OR,

Explain the basic operation of depletion type n channel MOSFET with a suitable diagram.

[WBUT 2016]

Answer: Refer to Question No. 3.5(b).

- b) As V_{DS} is changed from 0 V to 0.2 V keeping V_{GS} constant, I_D of the FET drops from 10.25 mA to 9.65 mA. What is the transconductance of the FET? If the a.c drain resistance is 32 k Ω , find also the amplification factor of the FET. [WBUT 2012]

Answer:

Transconductance g_m is given by $g_m = \frac{I_d}{V_{GS}} \Big|_{V_{DS}=\text{constant}}$

$$\text{Hence } g_m = \frac{10.25 - 9.65}{0 - 0.2} = \frac{0.6}{-0.2} = 3 \text{ mA/V} \text{ (neglecting the sign)}$$

Again $\mu = g_m r_d = 3 \times 10^{-3} \times 32 \times 10^3 = 96$ being the amplification factor.

- c) What do you mean by pinch off voltage for n-channel JFET? [WBUT 2012]

Answer: Refer to Question No. 3.3(b).

- 3.7. a) What are the advantages of FET over BJT?

[WBUT 2013, 2015]

- b) What do you mean by pinch-off voltage?

- c) As V_{DS} is changed from -1 V to -1.5 V keeping V_{GS} constant, I_D of FET drops from 7 to 5 mA. What is the transconductance of FET? If the ac drain resistance is 200 k Ω , find also the amplification factor of the FET.

Answer:

- a) Following are the advantages of FET over BJT

- (i) FET is unipolar, conduction depends upon the flow of majority carriers only.
- (ii) It offers high input impedance (order of M Ω)
- (iii) It offers low output impedance (order of Ω)
- (iv) It is less noisy than BJT
- (v) Ultra low offset voltage
- (vi) Simpler to fabricate
- (vii) It occupies less space in IC.

- b) Refer to Question No. 3.2.

- c) Transconductance g_m is given by

$$g_m = \frac{I_d}{V_{GS}} \Big|_{V_{DS}=\text{const}}$$

$$g_m = \frac{I_d}{V_{GS}} \Big|_{V_{DS}=\text{const}} = \frac{5 - 7}{-1.5 - (-1)} = \frac{-2}{-0.5} = 4 \times 10^{-3} \text{ mho}$$

Amplification factor is given by $\mu = g_m r_d$

$$= (200 \times 10^3) \times (4 \times 10^{-3}) = 800$$

- 3.8.** In a JFET for an applied $V_{GS} = 0V$ and $V_{DS} = 2.5V$, the drain current appears to be 13.5 mA . What is the value of I_{DS} here? If V_{DS} is increased to $3V$ and the pinch-off voltage is stated $-2V$, what is the value of I_D ?
[WBUT 2014]

Answer:

$$\text{We know that in JFET, } I_D = I_{DS\text{SS}} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$

Where, $I_D \rightarrow$ drain current = ?; $I_{DS\text{SS}} \rightarrow$ saturation drain current
 $V_{GS} \rightarrow$ gate voltage $V_p \rightarrow$ pinch-off voltage

At $V_{GS} = 0V$,

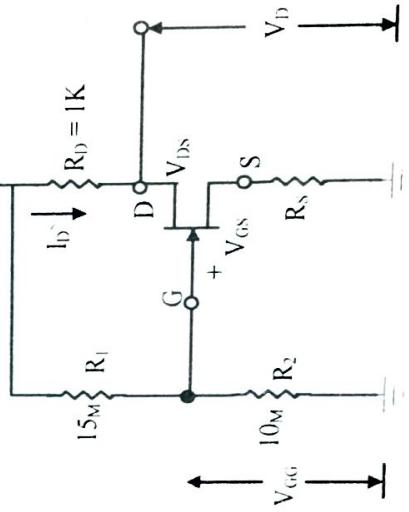
$$I_D = I_{DS\text{SS}} \Rightarrow I_{DS} = 13.5 \text{ mA}$$

If, $V_{GS} = 3V$ and $V_p = -2V$, then

$$I_D = I_{DS\text{SS}} \left(1 - \frac{V_{GS}}{V_p} \right)^2 = 13.5(1 + 3/2)\text{mA} = 33.75\text{mA}$$

- 3.9.** An N-channel JFET amplifier with a voltage divider biasing circuit as shown in the figure has the following parameters: $V_p = -4V$, $I_{DS\text{SS}} = 4mA$. Calculate the value of drain current at the operating point. Verify whether the FET will operate in the pinch-off region.
[WBUT 2015]

$V_{DD} = 25V$



Answer:

Data is insufficient. Consider, R_s is $2K\Omega$

Let us consider the voltage across the R_2 be V_2 .

Now applying the KVL in the lower loop of the above circuit, $V_2 = I_D R_s + V_{GS}$
 $I_D \rightarrow$ Drain current, $V_{GS} \rightarrow$ Gate to source voltage.
 \therefore Voltage drop across R_2 is, $V_2 = \frac{R_s}{R_s + R_2} V_{DD}$

Putting the value of V_2 we get,

$$\begin{aligned} \frac{R_s}{R_s + R_2} V_{DD} &= I_D R_s + V_{GS} \\ 2I_D + V_{GS} &= 10 \end{aligned} \quad \dots (1)$$

In case of JFET the drain current,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2 = 4 \left(1 + \frac{V_{GS}}{4} \right)^2 \quad \dots (2)$$

By solving equⁿ(1) & equⁿ(2), we get the drain current at the operating point is,
 $I_D = 4.8 \text{mA}$

And the gate to source voltage is, $V_{GS} = 0.4 \text{V}$
 Therefore the JFET will not be operated in pinch-off region.

3.10. a) Explain the basic operation of n-channel JFET with suitable diagram.

[WBUT 2016]

Answer: Refer to Question No. 3.4(a).

b) What are the differences between MOSFET and JFET?

[WBUT 2016]

Answer: Refer to Question No. 3.4(d).

c) An n-channel JFET has $I_{DSS} = 12 \text{ mA}$ and pinch off voltage is -4V , find the I_D for $V_{GS} = -2 \text{V}$. If the g_m of a JFET with same I_{DSS} at $V_{GS} = 0$ is 4 milli-mho, find pinch-off voltage. [WBUT 2016]

Answer:

$$\text{We know that, } I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$

The Transconductance is

$$L_g = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{V_D \text{ const}} = \frac{-2I_{DSS}}{V_p} \left(1 - \frac{V_{GS}}{V_p} \right) = g_m \left(1 - \frac{V_{GS}}{V_p} \right).$$

Clearly, $g_m \left(1 - \frac{V_{GS}}{V_p} \right)$ is the value of g_m when $V_{GS} = 0$.

Here $I_{DSS} = 12 \text{mA}$, $V_p = -4 \text{V}$, $V_{GS} = -2 \text{V}$, and $g_m = 4 \text{mS}$.

Substituting these values, we obtain,

$$I_D = 12 \left(1 - \frac{2}{4} \right)^2 = 3 \text{ mA}, \text{ and } V_p = -\frac{2I_{DSS}}{g_m} = -\frac{2 \times 12}{4} = -6 \text{V}.$$

- 3.11. a) Determine the value of g_{mo} for the graph shown in the Figure 1:

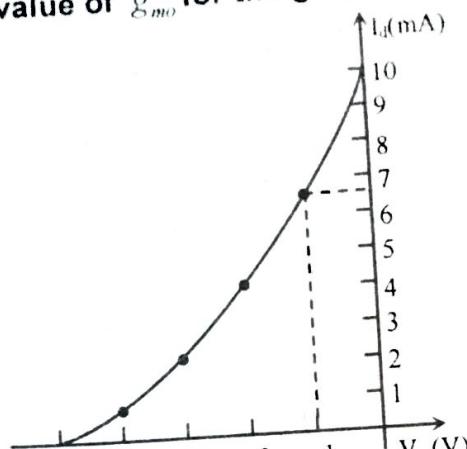


Figure 1

- b) Find out g_m for $V_{gs} = -1.5V$.

c) Draw the Transfer Characteristics of an N-Ch FET. Explain the curve with the help of Shockley's Equation.

d) Draw the small signal equivalent circuits for an FET.

e) The Fixed Bias circuit has operating point defined by $V_{gs} = -2V$, $I_{D_0} = 5.625\text{ mA}$ as shown in Figure 2. If the output conductance is $40\text{ }\mu\text{S}$ then find the following:

[WBUT 2017]

- i) g_m
- ii) r_d
- iii) R_s
- iv) R_o
- v) A_v

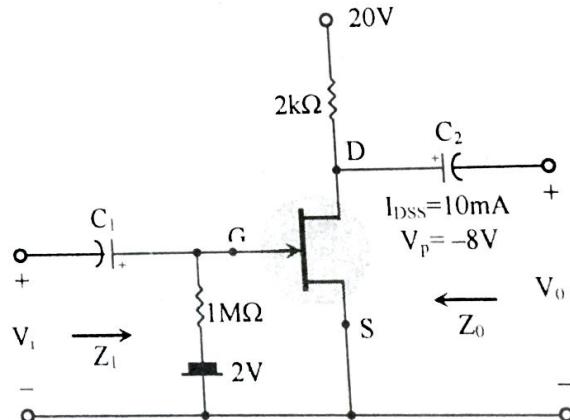


Figure 1

Answer:

a) From Shockley's Equation we know that, the relationship between I_d and V_{gs} is

$$I_d = I_{ds}(1 - V_{gs}/V_p)^2$$

Where, $I_d \rightarrow$ drain current

$V_{gs} \rightarrow$ gate to source voltage

$V_p \rightarrow$ pinch off voltage

$I_{ds} \rightarrow$ drain current at $V_{gs} = 0V$

Now differentiate both sides w.r.t V_{gs} , we get

$$\frac{dI_d}{V_{gs}} = \{2I_{ds}/|V_p|\}(1 - V_{gs}/V_p)$$

$$g_m = g_{mo}(1 - V_{gs}/V_p)$$

$$\begin{aligned} \text{Where, } g_{mo} &= 2I_{ds}/|V_p| \\ &= (2 \times 10 \times 10^{-3})/5 \\ &= 4 \text{ m-mho} \end{aligned}$$

b) At $V_{gs} = -1.5V$,

$$g_m = g_{m0}(1 - V_{gs}/V_p) = 4 \times 10^{-3}(1 - 1.5/5) = 2.8 \text{ m-mho}$$

c) From Shockley's Equation we know that, the relationship between I_d and V_{gs} is
 $I_d = I_{ds}(1 - V_{gs}/V_p)^2$
According to this equation, the transfer characteristics of N-channel JFET is

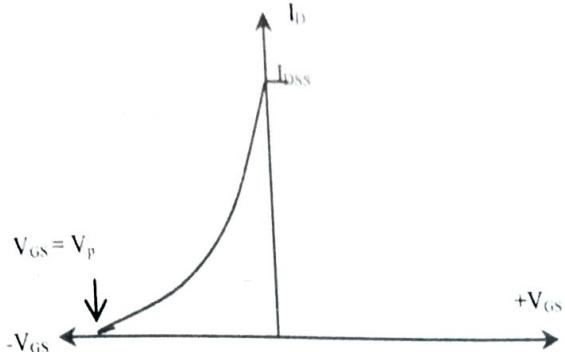
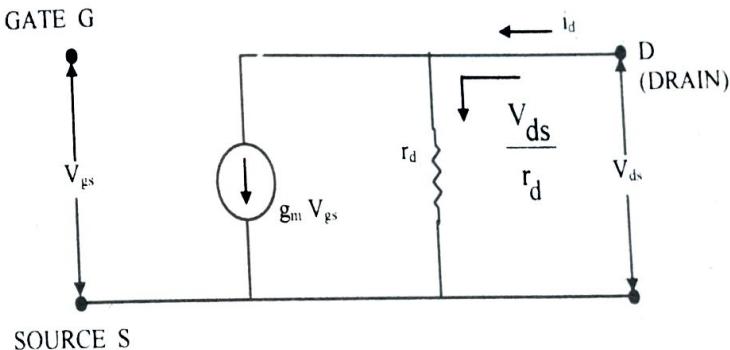


Fig: n-channel JFET Transfer Characteristics

According to Shockley's Equation if V_{gs} is increasing along negative direction, I_d will decrease due to reverse bias between gate to channel of N-channel JFET. At $|V_{gs}| = |V_p|$ (pinch off voltage), $I_d = 0$

d) Small-signal Equivalent Circuit of FET (low frequency)



e)

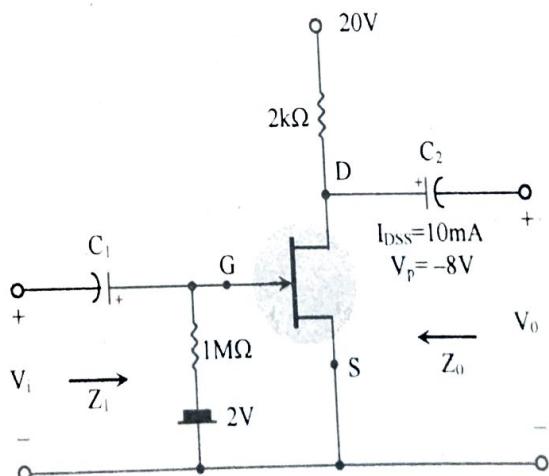


Figure 2

POPULAR PUBLICATIONS

i) g_m

From Shockley's Equation we know that

$$I_{DS} = I_{DSS}(1 - V_{GS}/V_P)^2$$

Now, $I_{DS} = 5.625\text{mA}$

$I_{DSS} = 10\text{mA}$

$V_{GS} = -2\text{V}$

Therefore, $V_P = -8\text{V}$

We know that,

$$\begin{aligned} g_m &= \{2I_{DSS}/|V_P|\}(1 - V_{GS}/V_P) \\ &= \{2 \times 10 \times 10^{-3}/8\}(1 - 2/8) \\ &= 1.875\text{m-mho} \end{aligned}$$

ii) r_d

We know that, Voltage amplification factor(A_V or μ) = $g_m \times r_d$

Where,

A_V or $\mu = 4$ and $g_m = 1.875\text{m-mho}$

$A_V = g_m \times r_d$

$$r_d = A_V/g_m = 4/1.875 \times 10^{-3} = 2.133 \text{ K}\Omega$$

iii) $R_i = 1\text{M}\Omega$

iv) $R_o = r_d \parallel R_D = 2.133 \text{ K}\Omega \parallel 2 \text{ K}\Omega = 1.032 \text{ K}\Omega$

v) $A_V = V_0/V_{GS} = -8/-2 = 4$

3.12. Write short notes on the following:

a) Enhancement and depletion type MOSFET
OR,

Enhancement type MOSFET

[WBUT 2007, 2009]

b) Enhancement and depletion type CMOS

[WBUT 2013, 2017]

c) Pinch – off condition of JFET

[WBUT 2010]

d) CMOS

[WBUT 2011]

e) MOSFET

[WBUT 2012, 2016, 2017]

f) Different parameters of JFET

[WBUT 2014]

g) Emitter-follower circuit

[WBUT 2016]

Answer:

[WBUT 2017]

a) **Enhancement and depletion type MOSFET:**

These are called Metal oxide Semiconductor FET (MOSFET) because of its construction in which the metal gate is insulated by a layer of oxide from the channel. Because of the insulated gate construction, these MOSFET have very high input resistance.

Among MOSFETs there are two types, namely the Enhancement type MOSFET and the Depletion type MOSFET.

Enhancement MOSFET

Symbol

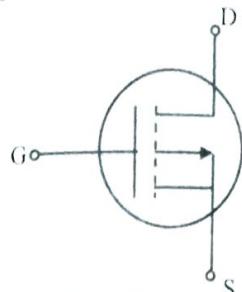


Fig (a): p-channel
enhancement type MOSFET

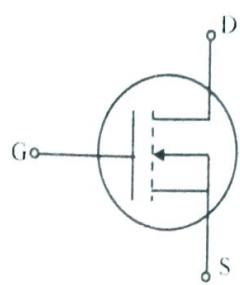


Fig (b): n-channel
enhancement type MOSFET

Construction

The following figure shows the construction of a n-channel MOSFET. Two highly doped n^+ regions are diffused into a lightly doped p-type substrate. One of these n^+ regions works as source and the other one as drain. A thin layer of an insulating material viz., silicon dioxide (SiO_2) is deposited over the surface. The gate metal, namely Aluminum is deposited over SiO_2 layer, for making connection for the gate, source and drain.

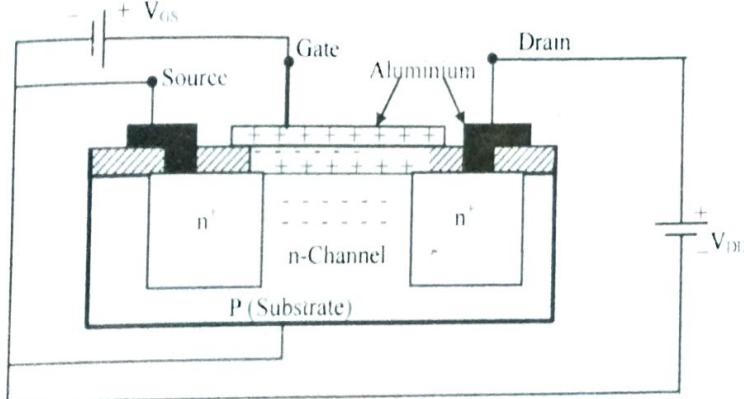


Fig: Enhancement type (n-channel) MOSFET

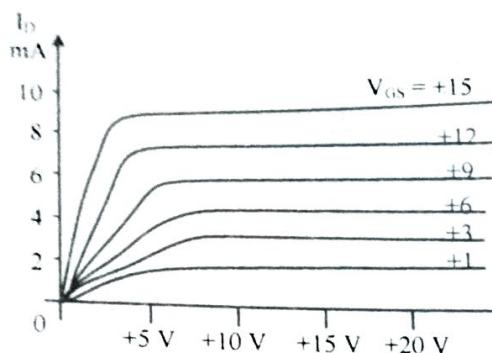
Operation

The substrate is grounded (connected to the source). If we apply a positive voltage to the gate, an electric field will be developed perpendicular to the SiO_2 surface. The +ve charge on the gate will induce -ve charge in the near end of the SiO_2 layer and +ve charge in the far end of the SiO_2 . Finally, it will induce negative charge in the p-type substrate, as shown. These induced negative charges (also called induced n-channel), which are minority carriers in the p-type substrate, causes current flow between source and drain. If the magnitude of +ve voltage on the gate increases, the induced -ve charge in the semiconductor also increases. The drain current is "enhanced" (means: increased) by the +ve gate voltage. Hence such a device is called Enhancement type MOSFET.

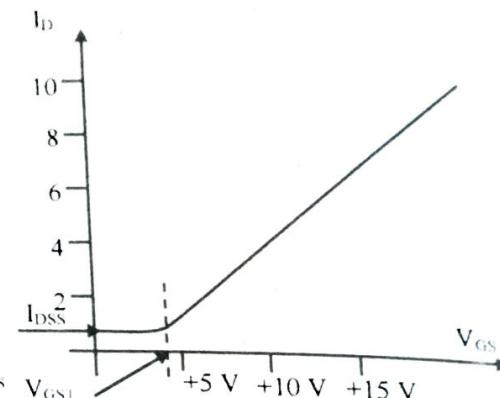
Characteristics

In Enhancement type MOSFETs, the drain current increases by making V_{GS} more positive. This is shown in the drain characteristics, Fig (a).

The Fig.(b) shows the transfer characteristics, which gives the relationship between drain current and gate voltage. When $V_{GS} = 0$, the drain current I_{DSS} is very small, only a few nano-amperes. The drain-current starts increasing only after a minimum value of V_{GS} is exceeded; this value of V_{GS} is called the threshold voltage V_{GST} . The drain characteristics in this condition is governed by V_{DS} as in the case of JFET through the modulation of depletion region.



(a) Drain Characteristics



(b) Transfer Characteristics

Characteristics of Enhancement type MOSFET

Application

This type of MOSFET is useful in switching applications. We have seen that with $V_{GS} = 0$, the drain current is very small and therefore it can be considered to be in "OFF" state. Also, the gate voltage V_{GS} must be above the threshold value V_{GST} for the conduction to start; thus there is immunity to noise voltages whose values are less than V_{GST} . Finally, to switch ON the FET, the gate has to be given a voltage of the same polarity and nearly the same magnitude as the drain voltage. This is a definite advantage from circuit point of view.

Depletion MOSFET

Symbol

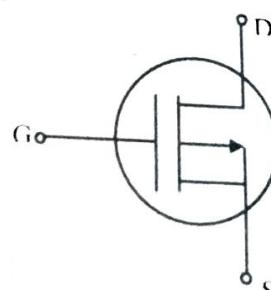


Fig (a): p-channel
depletion type MOSFET

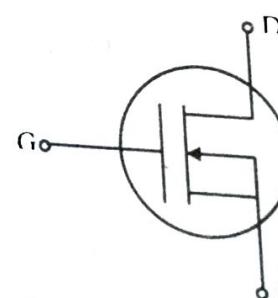


Fig (b): n-channel depletion
type MOSFET

Construction

Fig. below shows the construction of depletion type of MOSFET with n-type channel. Two highly doped n⁺ regions work as source and the other one as drain. Between these two n⁺ regions, an n-type of channel is diffused. A thin layer of SiO₂ is deposited over the

surface. The gate, source and drain connections are made by depositing aluminum over SiO_2 layer.

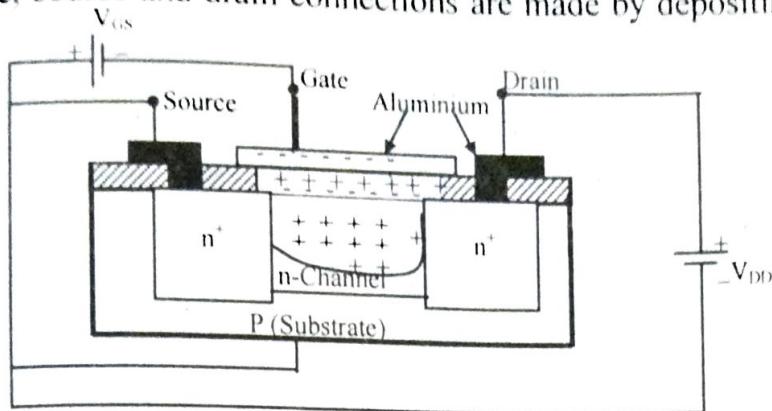


Fig: Depletion type (n-channel) MOSFET

Operation

If the gate voltage is made negative, there will be +ve charges (induced) in the near side of SiO_2 layer. This, in turn, will induce +ve charges in the channel (n-type). The n-type channel has electrons as the majority carriers. Therefore the induced +ve charges will make the channel less conductive. As a result, the drain current will reduce.

As the gate voltage is made more negative the drain current will be lesser. The negative gate voltage causes an effective depletion (i.e., reduction) of majority carriers; hence it has the name depletion MOSFET. On the other hand if +ve voltage is applied to the gate it induces -ve charges in the channel, thereby increasing the conductivity and is equivalent to enhancement mode of operation.

Characteristics

Fig(a) shows the drain characteristics of the depletion type FET. The set of curves for values below $V_{GS} = 0$ are for depletion mode (similar to JFET). The set of curves with values above $V_{GS} = 0$ are for enhancement mode.

Fig.(b) shows the transfer characteristics. On the left-hand side, is the depletion mode, where V_{GS} is -ve. On the right hand side is the enhancement mode where V_{GS} is +ve. At $V_{GS} = 0$, the value of I_d is equal to I_{DSS} . As a value of $V_{GS} = V_{GS(\text{OFF})}$, the I_d reduces to a negligible value; this value $V_{GS(\text{OFF})}$ corresponds to pinch-off voltage V_p of a JFET.

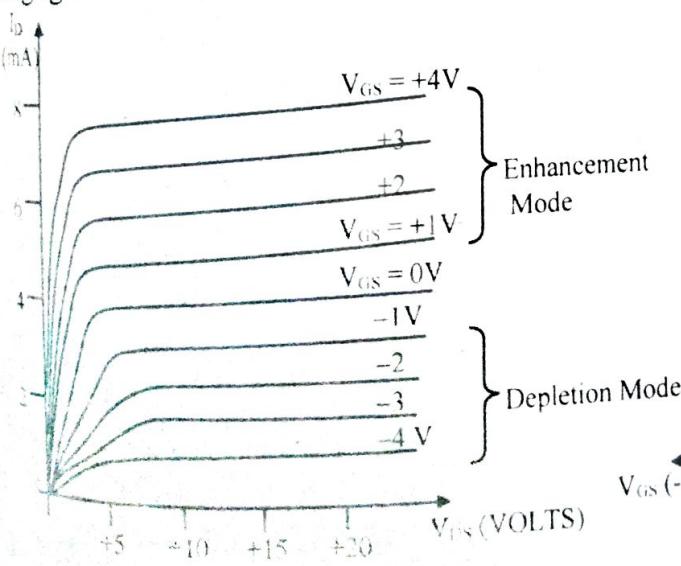


Fig (a): Drain Characteristics

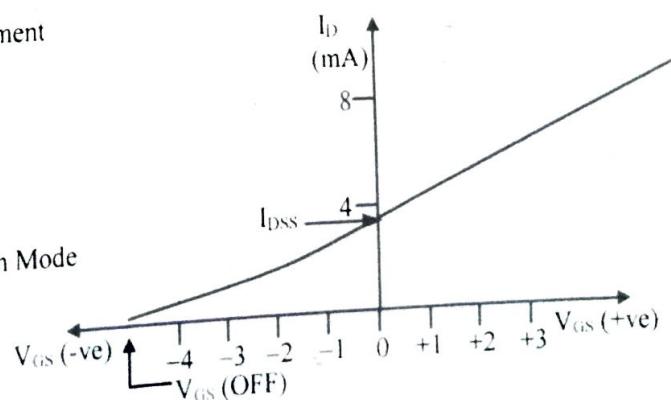
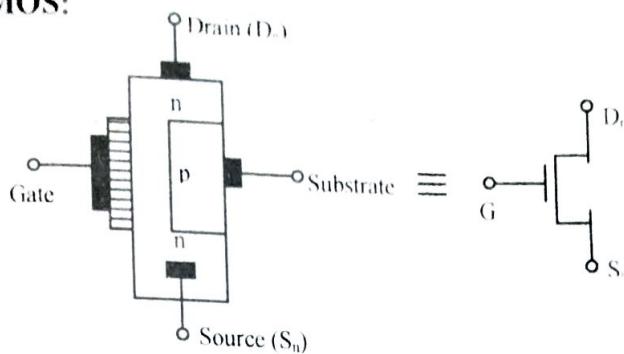


Fig (b): Transfer Characteristics



Depletion Mode n-MOS:

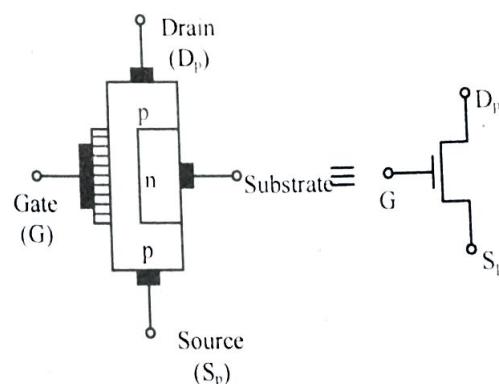


In this circuit, channel normally exists without giving any voltage to the gate terminal with respect to the source. If we give supply voltage (V_{DD}) to the drain terminal then free electrons move from the source to drain. When we give negative voltage to the p-type substrate with respect to gate then free electrons depleted and no more channel will be there and it becomes 'OFF'.

Depletion Mode p-MOS:

In Depletion Mode p-MOS, channel normally exists without biasing to the gate terminal with respect to the source. If we give some potential difference between drain to source then we win gate current due to free holes in the channel.

Now, if we apply positive voltage to the substrate with respect to gate then free holes in the channel will be depleted and the channel will be ceased. In this condition the p-MOS will 'OFF'.



c) Pinch-off condition of JFET:

The basic construction of the n-channel JFET is shown in fig., the major part being the n-type material that forms the channel between the embedded layers of heavily doped p-type material. The ends of the n-type channel are connected through an ohmic contact to a terminal referred to as the source (S) and the Drain (D). The two p-type materials are connected together and finally to the gate (G) terminal. In essence, therefore, the drain and source are connected to the ends of the n-type channel and the gate to the two layers of p-type material.

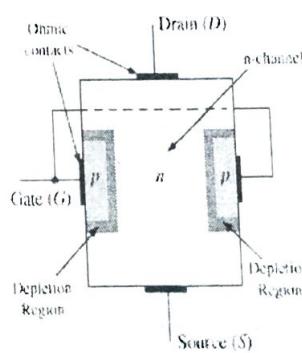
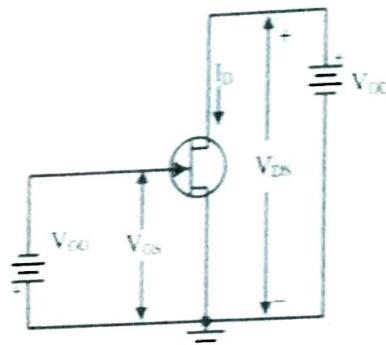


Fig: Junction Field-Effect Transistor
The drain and source are connected to the ends of the n-type channel and the gate to the two layers of p-type material.

Circuit Representation



If V_{DS} is increasing (Pinch off voltage): **Refer to Question No. 3.1(b).**

d) CMOS:

CMOS is most popular technology for the implementation of digital systems. The small size, ease of fabrication, and low power dissipation of MOSFETs enable extremely high levels of integration of both logic and memory circuits.

Merits of CMOS Technology:

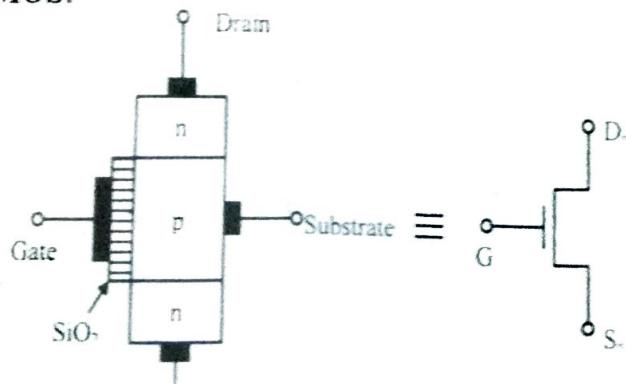
Source of the reasons for CMOS displacing bipolar technology in digital applications are as follows:

- (a) CMOS logic circuits dissipate much less power than bipolar logic circuits and thus one can pack more CMOS circuits on a chip than is possible with bipolar circuits.
- (b) The high input impedance of the MOS transistor allows the designer to use charge storage as a means for the temporary storage of information in both logic and memory circuits. This technique cannot be used in bipolar circuits.
- (c) The feature size (i.e., minimum channel length) of the MOS transistor has decreased dramatically over the years, with some recently reported designs utilizing channel lengths as short as $0.06\mu\text{m}$. This permits very tight circuit packing and correspondingly, very high levels of integration.

CMOS logic gate circuits:

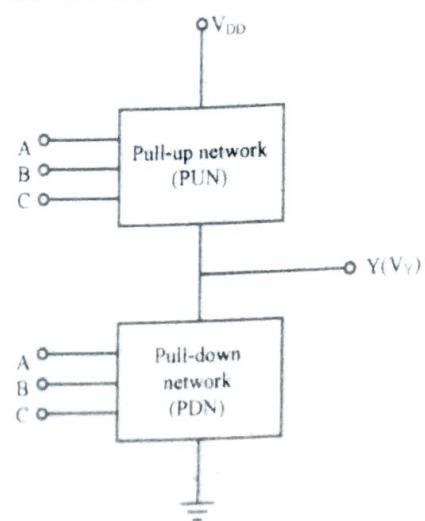
Combinational logic circuits, which are realized by CMOS technology, used in large quantities in a multitude of applications; indeed, every digital system contains large numbers of combinational logic circuits.

Basic structure of CMOS:



The CMOS logic gate consists of two networks. The pull-up network (PUN) constructed of PMOS transistors and the pull-down network (PDN) constructed of NMOS transistors, (shown in the above figure). The two networks are operated by the input variables, in a complementary fashion. Thus, for the three-input gate represented in the figure, the PDN will conduct for all input combinations that require a low output ($Y = 0$) and will then pull the output node down to ground, causing a zero voltage to appear at the output $V_Y = 0$. Simultaneously, the PUN will be off and no direct dc path will exist between V_{DD} and ground. On the other hand, all input combinations that call for a high output ($Y = 1$) will cause the PUN to conduct, and the PUN will then pull the output node up to V_{DD} , establishing an output voltage $V_Y = V_{DD}$. Simultaneously, the PDN will be cut-off and again no AC current path between V_{DD} and ground will exist in the circuit.

Now, since the PDN comprises NMOS transistors and since an NMOS transistor conducts when the signal at its gate is high, the PDN is activated (i.e., conducts) when the inputs are high. In a dual manner, PUN comprises PMOS transistors and a PMOS transistor conducts when the input signal at its gate is low; thus the PUN is activated when the inputs are low.



Examples of CMOS logic circuits

We can implement any logic gates (NOT, NAND/AND, NOR/OR, XOR/XNOR etc.) or combinational circuits using CMOS technology.

e) MOSFET: Refer to Chapter at a glance MOSFET part.

f) Different parameters of JFET:

For understanding the important parameters of FET, we re-draw the FET characteristics in simplified manner in fig below. We note that in the pinch-off region, the drain current I_D is practically constant but the graph has a small slope.

(a) Drain Resistance, r_d

The drain resistance r_d of a FET is defined as

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \quad \text{while } V_{GS} \text{ is held constant.}$$

The typical value of r_d ranges from 10 K ohms to 50 K ohm.

(b) Transconductance, g_m

Transconductance, g_m , of a FET is defined as the change in drain current due to a change

in the gate voltage i.e., $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$ while V_{DS} is constant.

Typical values of g_m range between 2 - 6 milli-mhos.

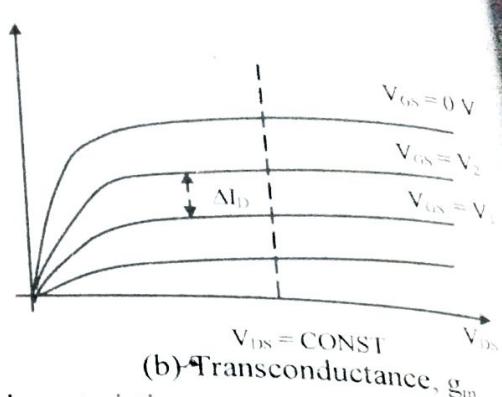
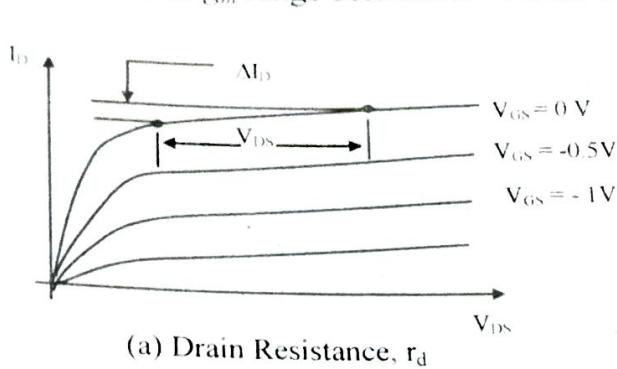


Fig.: Understanding r_d and g_m from FET characteristics

(c) Amplification Factor, μ

The amplification factor, μ , is defined as

$$\mu = -\frac{\Delta V_{DS}}{\Delta V_{GS}} \quad \text{while } I_D \text{ is constant.}$$

We can re-write the equation as

$$I_D = f(V_{DS}, V_{GS})$$

$$\Delta I_D = \frac{\Delta I_D}{\Delta V_{DS}} \Big|_{V_{GS} = \text{constant}} \Delta V_{DS} + \frac{\Delta I_D}{\Delta V_{GS}} \Big|_{V_{DS} = \text{constant}} \Delta V_{GS}$$

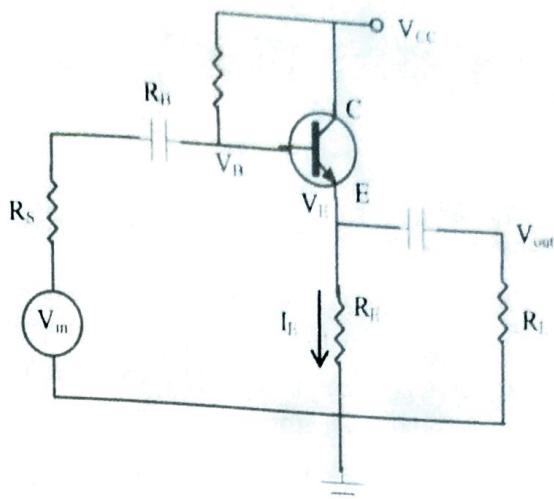
To maintain $I_D = \text{constant}$ or $\Delta I_D = 0$

$$-\frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{\frac{\Delta I_D}{\Delta V_{DS}} \Big|_{V_{DS} = \text{constant}}}{\frac{\Delta I_D}{\Delta V_{GS}} \Big|_{V_{GS} = \text{constant}}} = \frac{\Delta I_D}{\Delta V_{GS}} \Big|_{V_{DS} = \text{constant}} \times \frac{\Delta V_{DS}}{\Delta I_D} \Big|_{V_{GS} = \text{constant}}$$

$$\text{OR} \quad \mu = g_m \times r_d$$

g) Emitter Follower Circuit:

In the emitter follower circuit shown here, the input and output are the base and emitter respectively and the collector is at AC zero. The circuit is therefore a common-collector circuit (for AC).



The negative feedback effect due to R_E can be

$$V_{out} = V_e \uparrow \Rightarrow V_{be} \downarrow \Rightarrow i_b \downarrow \Rightarrow i_c \downarrow \Rightarrow v_e \downarrow$$

We can see the entire output is negatively feedback to the input.

The DC operating point can be found as

$$\begin{aligned} V_{cc} &= R_B I_B + V_{BE} + R_E I_E \\ &= R_B I_B + V_{BE} + R_E (\beta + 1) I_B \end{aligned}$$

$$I_B = \frac{V_{cc} - V_{BE}}{(\beta + 1) R_E + R_B}$$

$$\therefore I_E = (\beta + 1) I_B = \frac{(\beta + 1)(V_{cc} - V_{BE})}{(\beta + 1) R_E + R_B}$$

$$V_{ce} = V_{cc} - V_E = V_{cc} - R_E I_E$$