Computer Architecture

CSEN 3104

Lecture 2

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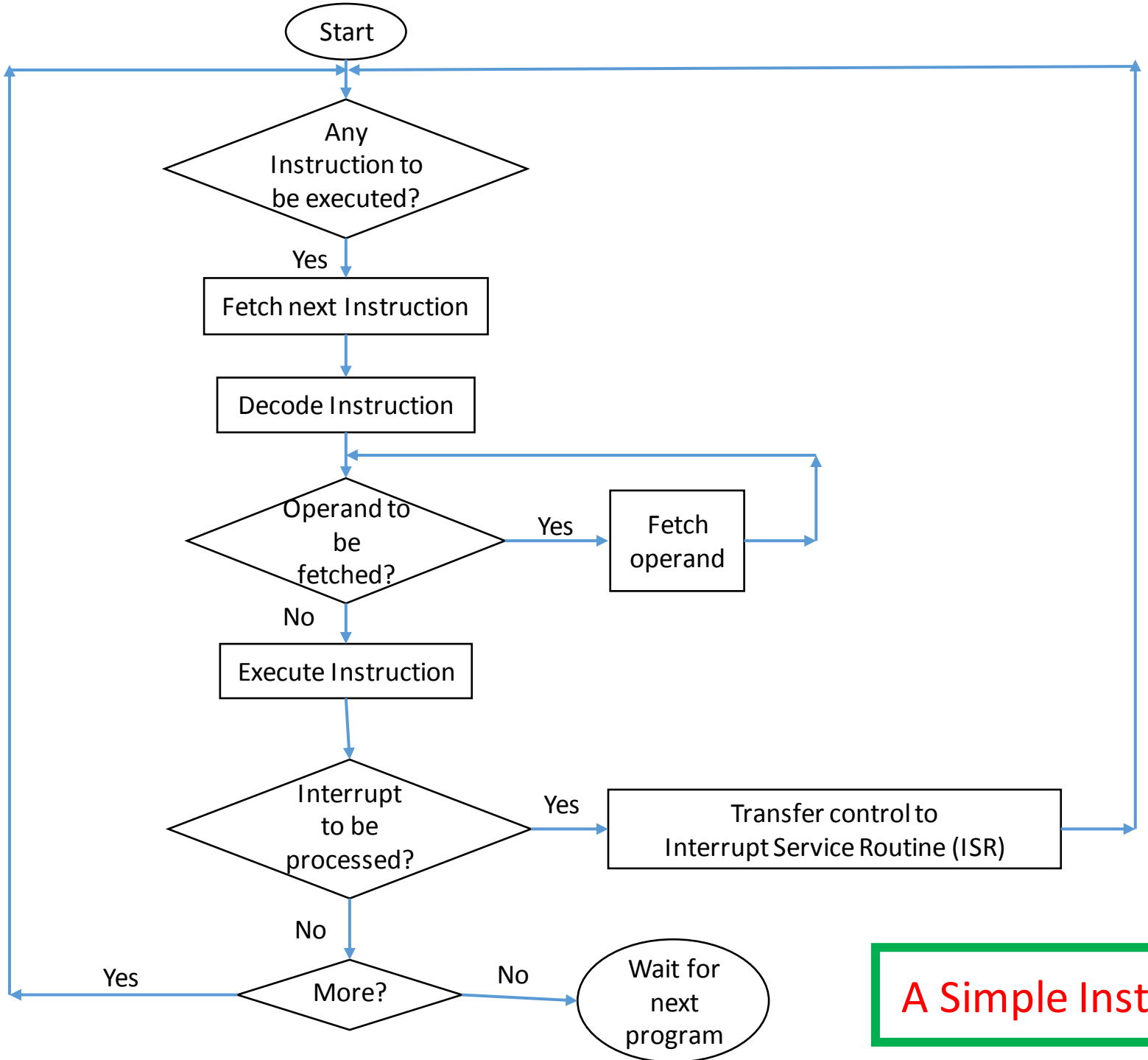

A Simple Instruction Cycle

Instruction Execution Mechanism

- A program is a set of instructions stored in memory
- The program is executed in the computer by going through a cycle for each instruction
- After the program is loaded onto the memory, the CPU fetches the first instruction
- Then the instruction is decoded to understand what actions the instruction dictates
- If required, it fetches the operand from the memory
- Then the CPU carries out those actions i.e. executes the instruction

Contd....

Instruction Execution Mechanism

- If no interrupt is pending to be serviced, the control is transferred to the next instruction
- In case some interrupt is pending to be serviced, the CPU transfers control to the Interrupt Service Routine (ISR)
- After execution of the ISR, control is transferred to the next instruction (from where it came to ISR)
- This cycle is repeated continuously by a computer's CPU, from boot up to shut down.
- The fetch–decode–execute cycle (also known as instruction cycle) is the basic operational process of a computer

Instruction Set Architecture

- Instruction Format
- Operation Code
  - Example: Add, Sub, Complement etc.
- Address field
  - Memory location
  - Processor Register
  - Operand value
- Mode
  - Specifies the addressing mode to get the operand
  - Effective address of the operand
  - In some computer, no separate mode field and the addressing mode is specified in the instruction (opcode) itself
- Example: ADD R1, R0

Instruction Set Architecture

- In certain situations, special fields are used
  - Number of shifts in a SHIFT type instruction
  - Label field in a BRANCH type instruction
- Memory or Registers store the operand values on which the instructions are executed
- Memory addresses are used to specify operands stored in memory
- A register address (k-bit) specifies one out of 2^k registers in the CPU
- A CPU with 32 registers has a register address field of 5 bits

Thank you