Complex Instruction Set Computer (CISC) and Reduced Instruction Set Computer(RISC)

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RISC (Reduced Instruction Set Computers)

➔ CISC: Complex ISC

- Huge no. of instructions
- Complex addressing modes like double indexing
- Increases flexibility of instruction set
- Does not improve performance at all
- Can cause pipeline to stall
- Requires more complex hardware

RISC characteristics

➔Suitable for modern day pipelined processors

- Access to an operand does not require more than one access to memory

  Ex: Load (X(R1)),R2 => Not allowed

  => Indexed + Indirect mode

  - Read from X+[R1] memory first, say Y
  - Then read from [Y] to get the operand
- Only load/store operation can access memory

  Ex: Add (R1),R2 not allowed

- Register / Register Indirect / Index mode have these features

- Ex: The SPARC processor architecture

CISC vs. RISC

➔ Only 25% of CISC instructions used 95% of the time

- Rest 75% hardware supported instructions rarely used
  - Valuable chip area is wasted
  - These instructions require long microcodes

- Remove complex ISCs to software (from hardware)
  - It would be slower
  - But these appear only rarely

CISC vs RISC

- Chip areas so vacated can be used for:
  - Powerful RISC processors
  - Superscalar processors
  - On-chip caches
  - FPUs
  - Hardwired control allowing faster execution cycle

RISC characteristics (contd.)

- Less than 100 instructions in the whole set
- Each instruction has a fixed instruction format (32 bits)
- Only a few addressing modes are used
- Most instructions are register-based
- Memory access is via load/store instructions only
- A large register file (at least 32) is used
- Hardwired control is used
  - Most instructions execute in one cycle

Results:

- Higher clock rate
- Lower clock per instructions (CPI)

Architectural Characteristic	*Complex Instruction Set Computer (CISC)*	*Reduced Instruction Set Computer (RISC)*
Instruction-set size and instruction formats	Large set of instructions with variable formats (16-64 bits per instructions)	Small set of instructions with fixed format and most register-based instructions
Addressing modes	12–24	Limited to 3–5
General-purpose registers	8–24 GPRs, originally with a unified cache for instructions and data	Large numbers (32–192) of registers with mostly split data and instruction cache
CPI	CPI between 2 and 15	One cycle for almost all instructions and an average CPI < 1.5.
CPU Control	Microcoded using control memory	Hardwired without control memory.