



CONFIDENTIAL

HERITAGE INSTITUTE OF TECHNOLOGY

Class test I Examination 2018 Session: July-Dec. 2018
Discipline : B.Tech 3rd Yr

Paper Code: HMTS-3101

Paper Name: Economics for Engineers

Time Allotted: 1 hr

Full Marks: 30

Figures out of the right margin indicate full marks.

Answer all the questions

Candidates are required to give answer in their own words as far as practicable.

1 <input checked="" type="checkbox"/> (a)	Define Economics. What is the difference between micro and macroeconomics?	(2+1+2)+5=10
<input checked="" type="checkbox"/> (b)	What is the meaning of market? Explain any 2 features of monopoly market.	
<input checked="" type="checkbox"/> (c)	From the following balances extracted from the books of Sunshine Enterprise prepare a Trial Balance as on 31 st March 2018: Capital Rs. 4,50,000; Cash in hand Rs. 1,250; Building Rs. 4,00,000; Sales Rs. 2,90,000; Stock (on 1.4.2017) Rs. 53,000; Balance at bank Rs. 4,750; Sundry debtors Rs. 59,000; Sundry creditors Rs. 26,000; Commission paid Rs. 750; Rent & taxes Rs. 6,300; Purchases Rs. 1,65,000; Salaries Rs. 70,300; Telephone charges Rs. 3,400; Discount allowed Rs. 650; Discount received Rs. 1,000; Bills receivable Rs. 8,600; Bills payable Rs. 6,000	
2 <input checked="" type="checkbox"/> (a)	The Selling Price of a product is Rs.80/unit. The Variable Cost is Rs. 60/unit. The Fixed Cost is Rs.4,00,000/-. Compute i)B.E.P.(Quantity) ii) CS ratio iii)B.E.P.(Sales Value) <i>20 0.25 1600</i>	5+5=10
<input checked="" type="checkbox"/> (b)	Explain with the help of a diagram the difference between changes in demand and changes in quantity demanded .	
3 <input checked="" type="checkbox"/> (a)	What is the Law of Demand? Mention any two exceptions to the law.	5+5=10
<input checked="" type="checkbox"/> (b)	What are the characteristics of Perfect Competition?	



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HERITAGE INSTITUTE OF TECHNOLOGY

Class Test I Examination 2018

Session: 2018-2019

Discipline(s): B.Tech. (CSE)

Paper Code: CSEN 3101, Paper Name: Formal Language and Automata Theory

Time Allotted: 1 hour

Full Marks: 30

Figures out of the right margin indicate full marks.

Answer ALL the questions.

Candidates are required to give answer in their own words as far as practicable.

1	Choose the correct alternative from the following	$4 \times 1 = 4$
(a)	For a Moore machine if the input string is of length n then which of the following will be the length of the output string i) n ii) $n + 1$ iii) $n - 1$ iv) None of these	
(b)	Which of the following is the regular expression representing the language $L = \{ \text{all strings containing an even number of } 0's \}$ over the alphabet $\Sigma = \{0, 1\}$ i) $(1^* 0 1^*)^*$ ii) $(1^* 0 1^*)^*$ iii) $(1^* 0 1^*)^* + 0^*$ iv) All of the above	
(c)	Pumping lemma of regular language is used to show that a given language L is i) not regular ii) regular iii) Nothing can be said iv) both (i) and (ii)	
(d)	For a grammar $G = (V_N, \Sigma, P, S)$, consider a production of the form $A \rightarrow a aB$, where $A, B \in V_N$ and $a \in \Sigma^*$. Which of the following type of grammar the given production best fits with: i) only regular ii) only CFG iii) regular and CFG iv) None of these	
2 (a)	Consider the following NFA (over the alphabet $\{a, b\}$). $(a^* + b)(ab^* + \epsilon)$	$(5+3+2) + (4) + (3) = 17$
(b)	i) Let L_1 denotes the set of strings accepted by this NFA. Write the regular expression for L_1 . ii) Convert the given NFA to its equivalent DFA using subset construction method iii) What is the shortest string <i>not</i> accepted by the given NFA? aab	$f : Q_1 \rightarrow$ $= Q_2$
(c)	Let's consider L_2 denotes the language over the alphabet $\{a, b\}$ such that $\alpha \in L_2$ iff $ \alpha \geq 2$, the second symbol of α is a , and the second last symbol of α is b . Design an NFA to accept L_2 .	
(c)	Using the pumping lemma, prove that $L_3 = \{a^m b^n \mid m, n > 1 \text{ and } \gcd(m, n) = 1\}$ is not regular. $(a^m b^n)$	



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Class Test I Examination 2018

Session: 2018-2019

Discipline(s): B.Tech. (CSE)

Paper Code: CSEN 3101 Paper Name: Formal Language and Automata Theory

3.	(a) Write a Context Free Grammar (CFG) for any one of the following languages L_4 & L_5 . Write only the productions in your grammar and mention which is the start symbol.	(4) + (5) = 9
	i) $L_4 = \{\alpha \in \{a, b, c\}^* \mid \#a(\alpha) + \#b(\alpha) = \#c(\alpha)\}$. Here, $\#d(\alpha)$ means the number of occurrences of the symbol d in the string α , where $d \in \{a, b, c\}$. ii) $L_5 = \{a^i b^j c^k d^q \mid k = i + j, \text{ and } i, j, q \geq 0\}$	
(b)	Convert the CFG that you obtain for either L_4 or L_5 at Part (a) to Chomsky Normal Form (CNF). Show all the relevant steps briefly.	

HERITAGE INSTITUTE OF TECHNOLOGY

5th Semester Class Test I Examination on 2018

Session : 2018-19

Discipline: Computer Science Engineering

Paper Code : CSEN3102

Paper Name : Database Management Systems

Time Allotted : 1 hr

Full Marks : 30

Figures in the right margin indicate full marks.

Answer all the questions

Candidates are required to give answer in their own words as far as practicable.

1.	<p>Consider the Relational Schema mentioned below:</p> <p>EMP(emp_name, street, city) WORKS(emp_name, comp_name, salary) COMPANY(comp_name, city) MANAGES(emp_name, man_name)</p> <p>Write Relational Algebra Expressions for the following:</p> <ol style="list-style-type: none"> Find the names of all employees who do not work for "SBI". Find the names of all employees who live in the same city as the company for which they work. Find the names of all employees who earn more than every employee of "IBM". 	$1 + 2 + 2$ $= 5$
2. (a)	<p>Consider the universal relation $R = \{A, B, C, D, E, F, G, H, I, J\}$ and Functional Dependencies $F = \{AB \rightarrow C, A \rightarrow DE, B \rightarrow F, F \rightarrow GH, D \rightarrow IJ\}$</p> <p>Consider the following decomposition for the relation schema R</p> $R1 = \{A, B, C, D, E\} \quad R2 = \{B, F, G, H\} \quad R3 = \{D, I, J\}$ <p>Determine whether the decomposition has the Lossless (Non-Additive) Join Property, with respect to F.</p>	$5 + 3 + 4$ $= 12$
(b)	<p>Determine the highest normal form (1NF, 2NF, 3NF, BCNF) of the schema S which includes R1, R2, R3.</p> <p><i>(Hint: Normal form of the Schema is not for individual relations, but all the relations together)</i></p>	
(c)	<p>Find two different Minimal/Canonical Covers for the set of Functional Dependencies $F = \{A \rightarrow BC, B \rightarrow CA, C \rightarrow AB\}$.</p> <p>Let these two sets be called G and H respectively. State whether G and H are equivalent with proper reasoning.</p>	
3.	<p>Suppose you are given the following requirements for a simple database for the Indian Premier League (IPL):</p> <ul style="list-style-type: none"> • The IPL has many teams; each team is identified by its name. • Each team has a name, a city, a coach, a captain, and a set of players. • Each player belongs to only one team. • Each player may be identified by his player_id. • Each player has a name, a specialization (such as batsman, bowler, keeper, all-rounder etc.), and a base price. • Each player also has injury records consisting of type and description. • A team captain is also a player. One team has only one captain. • A game is played between two teams (referred to as host team and guest team) • Each game has a date (such as Apr 23rd, 2017) and a result (such as KKR beat RCB). <p>(a) Construct a clean and concise ER diagram for the IPL database clearly depicting each entity, required attributes, degree and cardinality of the relationships. Take care of any weak entities, recursive relationships, and role names if such are present. You may wish to add any relevant explanation for your ER diagram.</p> <p>(b) Find the Relations / Tables that are needed to convert your ER diagram to a Relational Model.</p> <p>(c) State the Candidate Key(s) for all the Relations in the previous part.</p>	$5 + 5 + 3$ $= 13$



HERITAGE INSTITUTE OF TECHNOLOGY

B.Tech 3rd Year, 5th Semester Class test I Examination 2018 Session: Jul – Dec 2018

SECTION A + B + C

Paper Code: CSEN3103

Paper Name: Operating Systems

Time Allotted: 1 hr

Full Marks: 30

Figures out of the right margin indicate full marks.

Candidates are required to give answer in their own words as far as practicable.

Answer any five from questions from 1

1(a) Comment – 'It is the process that executes not the program'.	2				
✓(b) Explain the reasons due to which a process may leave the CPU.	2				
✓(c) Comment on the statement: 'The performance of the FCFS becomes poor when a smaller job is scheduled after a larger job.'	2				
(d) At a particular time of computation the value of a counting semaphore is 7. Then 20 P operations and 15 V operations were completed on this semaphore. Find out the resulting value of the semaphore.	2				
✓(e) Consider the following pseudo code: semaphore S = 1; semaphore E = 1; If (thread_count++ < 100) spawnnewthread(); wait(E); // critical section – begin ----- ----- // critical section – end signal(S); Assume that above pseudocode gets called a hundred times, what is the count of semaphore E?	2				
(f) Consider the methods used by processes P1 and P2 for accessing their critical sections whenever needed, as given below. The initial values of shared boolean variables S1 and S2 are randomly assigned. <table border="1" style="margin-top: 5px; width: 100%;"> <thead> <tr> <th style="text-align: left; padding: 2px;">Method Used by P1</th><th style="text-align: left; padding: 2px;">Method Used by P2</th></tr> </thead> <tbody> <tr> <td style="padding: 2px;">while (S1 == S2) ; Critical Section S1 = S2;</td><td style="padding: 2px;">while (S1 != S2) ; Critical Section S2 = not (S1);</td></tr> </tbody> </table>	Method Used by P1	Method Used by P2	while (S1 == S2) ; Critical Section S1 = S2;	while (S1 != S2) ; Critical Section S2 = not (S1);	2
Method Used by P1	Method Used by P2				
while (S1 == S2) ; Critical Section S1 = S2;	while (S1 != S2) ; Critical Section S2 = not (S1);				
Which one of the following statements describes the properties achieved? Explain. (a) Mutual exclusion but not progress (b) Progress but not mutual exclusion (c) Neither mutual exclusion nor progress (d) Both mutual exclusion and progress					
✓(g) Consider the following code. B is a shared variable with initial value of B=2. What would be the maximum value of B if we execute the following codes in any order? P1() { C=B-1; B=2*C; } P2() { D=2*B; B=D-1; }	2 <div style="position: absolute; top: 0; right: 0; width: 100px; height: 100px; background-color: white; border: 1px solid black; border-radius: 50%; display: flex; align-items: center; justify-content: center; font-size: 2em; font-weight: bold;">B C D 3 2 4</div>				

HERITAGE INSTITUTE OF TECHNOLOGY

B.Tech 3rd Year, 5th Semester Class test I Examination 2018 Session: Jul – Dec 2018

SECTION A + B + C

Paper Code: CSEN3103

Paper Name: Operating Systems

Answer any two from the rest of the questions:

- 2 a) Assume that the jobs arrive for execution as per the data given as follows: 3+3=6

Process	Arrival Time	Burst Time
P_1	0.0	7
P_2	2.0	4
P_3	4.0	1
P_4	5.0	4

Give the gantt chart illustrating the execution of these jobs using
a) preemptive, b) non-preemptive SJF scheduling policies. What are the average waiting times
for this computing session?

- (b) Draw the gantt chart and find the average waiting time and turnaround time for the following processes using priority scheduling algorithm? 4

Process	P1	P2	P3	P4	P5
Burst time	5	13	8	6	12
Priority	1	3	0	4	2

18.4

3. (a) Consider the following snapshot of a system with 5 processes, P0 through P4 and three resource types A, B and C. 2+3+1=6

	A	B	C
Instances	10	5	7

At time t_0 , snapshot of the system:

	Allocation			Max			Available		
	A	B	C	A	B	C	A	B	C
P0	0	1	0	7	5	3	3	3	2
P1	2	0	0	3	2	2			
P2	3	0	2	9	0	2			
P3	2	1	1	2	2	2			
P4	0	0	2	4	3	3			

7 4 3
2 4 4
6 0 0
0 1 1
4 3 1

Answer the following questions using the Banker's algorithm:-

- What is the content of the matrix Need?
- Is the system in a Safe state?
- If a request from process P1 arrives for (1, 0, 2), can the request be granted immediately?



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HERITAGE INSTITUTE OF TECHNOLOGY

BTech 3rd Year, 5th Semester Class test I Examination 2018 Session: Jul – Dec 2018

SECTION A + B + C

Paper Code: CSEN3103

Paper Name: Operating Systems

(b)	<p>Answer the following questions:</p> <p>(i) An executing process goes into which state when it asks for an I/O operation? (a) Ready to run (b) Run ✓ (c) Wait (d) None of the above</p> <p>(ii) Which types of threads are not scheduled by operating system? (a) User ✓ (b) Kernel (c) Concurrent (d) All of the above</p> <p>(iii) What is the ready state of a process? ✓ a) when process is scheduled to run after some execution b) when process is unable to run until some task has been completed c) when process is using the CPU d) none of the mentioned</p> <p>(iv) A process can be terminated due to a) normal exit b) fatal error c) killed by another process d) all of the mentioned</p>	4
4.(a)	<p>What do you mean by resource allocation graph? Draw the resource allocation graph for the following arrangement: The sets P, R and E (P, R, E have their usual meanings)</p> <p>$P = \{P_1, P_2, P_3\}$</p> <p>$R = \{R_1, R_2, R_3, \sim\}$</p> <p>$E = \{P_1 \rightarrow R_1, P_2 \rightarrow R_3, R_1 \rightarrow P_2, R_2 \rightarrow P_2, R_2 \rightarrow P_1, R_3 \rightarrow P_3, P_3 \rightarrow R_2\}$</p> <p>[There are 1 instance of R_1, 2 instances of R_2, 1 instances of R_3, 3 instances of R_4. Explain in the above situation whether there would be a deadlock or not.]</p>	1+2+1
(b)	<p>Explain how the reader writer problem can be solved by the use of semaphore</p>	6



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HERITAGE INSTITUTE OF TECHNOLOGY

B.Tech. 3rd Year 1st Sem. Class test I Examination 2018 Session : 2018-19
Discipline :CSE,.....

Paper Code :CSEN3104..... Paper Name : Computer Architecture.....

Time Allotted : 1 hr

Full Marks : 30

Figures out of the right margin indicate full marks.

Answer all the questions

Candidates are required to give answer in their own words as far as practicable.

1	a) Match the correct combinations of multiple data processing on the right using various architecture combinations on the left: (a) Vector Processors (i) At the same time <i>b</i> (b) Array Processors (ii) At different times <i>a</i> (iii) Using same space <i>a</i> (iv) Using different space <i>b</i>	2 + 3 x 1 = 5																																										
	b) For two instructions I and J WAR hazard occur, if (i) $R(I) \cap D(J) \neq \emptyset$ (ii) $R(I) \cap R(J) \neq \emptyset$ (iii) $D(I) \cap R(J) \neq \emptyset$ (iv) none of these																																											
	c) The task of vectorizing a compiler is (i) To find the length of vectors <i>p</i> (ii) To convert sequential scalar instructions into vector instructions <i>p</i> (iii) To process multi dimensional vectors <i>p</i> (iv) To execute vector instructions <i>v</i>																																											
	d) What will be the speed up for a 4 segment linear pipeline when the number instruction is 64? (i) 4.5 (ii) 3.82 (iii) 8.16 (iv) 2.95																																											
2.	<table border="1"><tr><td></td><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td></tr><tr><td>S1</td><td>X</td><td></td><td></td><td></td><td></td><td>X</td></tr><tr><td>S2</td><td></td><td>X</td><td></td><td></td><td>X</td><td></td></tr><tr><td>S3</td><td></td><td></td><td>X</td><td></td><td></td><td></td></tr><tr><td>S4</td><td></td><td></td><td></td><td>X</td><td></td><td></td></tr><tr><td>S5</td><td></td><td>X</td><td></td><td></td><td></td><td>X</td></tr></table>		0	1	2	3	4	5	S1	X					X	S2		X			X		S3			X				S4				X			S5		X				X	5 x 2 = 10
	0	1	2	3	4	5																																						
S1	X					X																																						
S2		X			X																																							
S3			X																																									
S4				X																																								
S5		X				X																																						
	a) Determine Forbidden Latency , Permissible Latency and Initial Collision Vector. b) Draw the permissible state diagram.																																											



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HERITAGE INSTITUTE OF TECHNOLOGY

B.Tech. 3rd Year 1st Sem. Class test I Examination 2018 Session : 2018-19
Discipline :CSE.....

Paper Code :CSEN3104..... Paper Name : Computer Architecture.....

- c) List all simple cycles. Especially point out the Greedy Cycles (GC).
d) What is Minimum Average Latency (MAL) of the pipeline? Is there any GC corresponding to this MAL?
e) What is the lower bound on this MAL (i.e. Minimum Achievable Latency)? What is the upper bound?

3a)	You have the following Instruction Stream coming into a chained Vector Processor <i>Load VR, A[3:0]</i> <i>Add VR, #1</i> <i>Mul VR, #2</i> <i>Store A[3:0], VR</i> A is a vector of length 4. VR is a Vector register. Show how the above code is executed in a Vector processor with four pipeline stages (Load / Add / Multiply and Store). Also calculate how many clock cycles will be required to complete the execution.	(3 + 3) + 2 = 8
3b)	Explain the terms Vector Strides and Stride Mining.	
4	Show in detail how the following two matrices are multiplied in O(n) time on an SIMD machine where PEs are stored in a 2D Mesh: $\begin{pmatrix} 1 & 1 & 2 & 3 \\ 4 & 5 & 6 & 7 \\ 7 & 6 & 5 & 4 \\ 3 & 2 & 1 & 1 \end{pmatrix}$ and $\begin{pmatrix} 2 & 3 & 2 & 3 \\ 4 & 5 & 4 & 5 \\ 6 & 7 & 6 & 7 \\ 3 & 2 & 3 & 2 \end{pmatrix}$	7

HERITAGE INSTITUTE OF TECHNOLOGY

5th Semester Examination 2018

Pass Test

Session

3253

Discipline

Computer Science Engineering

Paper Code: AEIIE3105

Figures out of the right margin indicate full marks.

Answer all the questions

	1. (a) Which one of the following is a logical instruction? (a) ADD B (b) XRA M (c) STAX B (d) RST 1 (b) 8085 μ P has _____ number of active flag bits (a) 4 (b) 5 (c) 7 (d) 8 (c) What is the function of P flag of 8085 μ P? Which instructions use CY flag for its operation? (d) Discuss the function of following pins of 8085 μ P (any two) – i) ALE ii) INTA iii) HOLD iv) READY (e) Write a program to add two 16 bit numbers, where the numbers are stored at memory locations starting from 8000 _H . Store the result in memory locations (including carry).	$1 + 1 +$ $(1+1) +$ $(1+1) + 4$ $= 10$
2. (a)	Among the followings which Interrupt has the highest priority (a) INTR (b) RST 5.5 (c) RST 6.5 (d) RST 7.5	$1+(2+2) +$ $3 + 2 = 10$
(b)	Write the name of different machine cycles of i) STA 8000 _H ii) INR M instructions. Also calculate the time required to execute the instructions where the clock frequency of 8085 μ P is 2 MHz.	133.333 10 ⁵
(c)	Draw and discuss the SIM instruction format.	151.111 10 ⁵
(d)	What is the use of subroutine call instruction? Give a suitable example.	
3. (a)	Design an interface between 8085 μ P and one 8KB RAM memory chip. Starting address of RAM memory is 8000 _H .	4+3+3 = 10
(b)	Draw and discuss the control word register (CWR) format of 8255 PPI in I/O mode.	
(c)	Write a program in BSR mode to blink one LED connected at PC ₀ line. Assume that a delay subroutine is available at memory location 8100 _H .	



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HERITAGE INSTITUTE OF TECHNOLOGY

Class test II Examination 2018 Session : ...July-Dec.

Discipline : B.Tech.(All Streams)

Paper Code: HMTS-3101 ...Paper Name: Economics For Engineers

Time Allotted: 1 hr

Full Marks: 30

Figures out of the right margin indicate full marks.

Answer all the questions

Candidates are required to give answer in their own words as far as practicable.

1 (a)	A machine is purchased for Rs. 3,00,000 and import duty is Rs 10,000, maintenance charges are Rs 20,000. If the rate of depreciation is 5%, 10%, 15% for next three years respectively, then find the book value after 3 years.	5+5=10														
(b)	<table border="1"><thead><tr><th>year</th><th>Cash flow</th></tr></thead><tbody><tr><td>0</td><td>-15000</td></tr><tr><td>1</td><td>2000</td></tr><tr><td>2</td><td>4000</td></tr><tr><td>3</td><td>5000</td></tr><tr><td>4</td><td>6000</td></tr><tr><td>5</td><td>7000</td></tr></tbody></table>	year	Cash flow	0	-15000	1	2000	2	4000	3	5000	4	6000	5	7000	
year	Cash flow															
0	-15000															
1	2000															
2	4000															
3	5000															
4	6000															
5	7000															
	If the rate of return is 10% per annum compounding annually, find the discounted payback period.															
2(a)	Using Net Present Value method determine whether the following project is viable at a discounting rate of 10%: Initial investment Rs. 20 crores Estimated cash inflows at the end of 1 st to 5 th year – Rs. 6 crores; Rs. 9 crores; Rs. 5 crores; Rs. 3 crores; Rs. 2 crores.	5+5=10														
(b)	What is the meaning of depreciation? What is the need of charging depreciation?															
3(a)	What are the common budgets employed in business? Briefly enumerate <i>Operating Budget</i> .	5+5=10														
3(b)	What are the differences between equity and debt?															



HERITAGE INSTITUTE OF TECHNOLOGY

Class Test II Examination 2018

Session: 2018-2019

Discipline(s): B.Tech. (CSE)

Paper Code: CSEN 3101 Paper Name: Formal Language and Automata Theory

Time Allotted: 1 hour

Full Marks: 30

Figures out of the right margin indicate full marks.

Answer ALL the questions.

Candidates are required to give answer in their own words as far as practicable.

1	Choose the correct alternative from the following	$3 \times 1 = 3$
(a)	<p>Consider the following three languages:</p> <p>$L_1 = \{a^n b^n c^m \mid m, n \geq 1\}$ CFL</p> <p>$L_2 = \{a^n b^m c^n \mid m, n \geq 1\}$ CFL</p> <p>$L_3 = \{a^n b^n c^n \mid n \geq 1\}$ CFL</p> <p>Which of the following statements is correct?</p> <p>(a) $L_3 = L_1 \cap L_2$</p> <p>(b) $L_1 \& L_2$ are CFL, but L_3 is not a CFL</p> <p>(c) $L_1 \& L_2$ are not CFL, but L_3 is a CFL</p> <p>(d) both (a) and (b)</p>	<i>mark</i>
(b)	Recursively enumerable languages are not closed under:	
	(a) Concatenation (b) Complement (c) Union (d) Intersection	
(c)	<p>A PDA behaves like an FSM when the number of auxiliary memory it contains is</p> <p>(a) 0 (b) 1 (c) 2 (d) None of the above</p>	
2	For each of the following given languages, mention which one is supposed to be accepted by a deterministic push down automata or non-deterministic push down automata or both or none of these.	$(5 \times 1) + (7) = 12$
(a)	<p>(i) $L(G) = \{ww^R \mid w \in \{a, b\}^*\}$</p> <p>(ii) $L(G) = \{a^n b^{n+2} \mid n > 0\}$</p> <p>(iii) $L(G) = \{a^n b^n c^m \mid n, m > 0\}$</p> <p>(iv) $L(G) = \{a^{n+m} b^{n+m} c^m \mid n, m > 0\}$</p> <p>(v) $L(G) = \{a^n b^m \mid n, m > 0\}$</p>	
(b)	Design a Turing machine that accepts the following language L_4 :	
	$L_4 = \{0^n 1^m 0^n \mid m, n \geq 1\}$	
3.	Design a PDA for a language L_5 , where $L_5 = \{w \in \{a, b\}^* \mid n_a(w) > n_b(w), \text{ where } n_a(w) \& n_b(w) \text{ denote the number of a's and the number of b's in } w \text{ respectively}\}$	$(5) + (4) + (1+5) = 15$
(a)		
(b)	Using the pumping lemma, prove that the language $L_6 = \{a^n b^{n^2} \mid n \geq 0\}$ over $\Sigma = \{a, b\}$ is not context-free. Carefully consider all the cases.	
(c)	Consider a CFG $G = (V_N, \Sigma, P, S)$. You are given a problem to determine whether G is ambiguous or not. Is the problem un-decidable or unsolvable? Provide a proof in support of your answer.	



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HERITAGE INSTITUTE OF TECHNOLOGY

5th Semester Class Test II Examination 2018

Discipline: CSE

Session: 2018-19

Paper Code: CSEN3102

Paper Name: Database Management Systems

Time Allotted: 1 Hour

Full Marks: 30

Figures in the right margin indicate full marks.

Answer all the questions.

Candidates are required to give answer in their own words as far as practicable.

1. (a)	<p>(i) Which of the following is not a consequence of concurrent operations? (A) Lost update problem (B) Update Anomaly (C) Dirty Read (D) All the above</p> <p>(ii) A relation schema R is in _____ Normal Form if, whenever a nontrivial functional dependency $X \rightarrow A$ holds in R, either X is a superkey of R, or A is a prime attribute of R. (A) 2ND (B) 3RD (C) Boyce Codd (D) None of the above</p> <p>(iii) If a transaction T has obtained an exclusive lock on item Q, then T can (A) read Q (B) write Q (C) both read and write Q (D) write Q but not read Q</p>	$(3 * 1) + 7 = 10$
(b)	<p>Let T_1 and T_2 be transactions that operate on same data items A, B, C. Let $r_1(A)$ mean that T_1 reads A, $w_1(A)$ mean that T_1 writes A. The same convention is followed for T_2. Two schedules S_1 and S_2 are given. Using precedence graphs, determine if they are Conflict Serializable or not. If a schedule is serializable, write down the Equivalent Serial Schedule(s).</p> <p>$S_1: r_1(A); w_1(A); r_2(A); w_2(A); r_1(A); w_1(A)$ $S_2: r_1(A); w_1(A); r_2(A); w_2(A); r_1(B); w_1(B); r_2(C); w_2(C)$</p>	
2. (a)	Explain the ACID properties of transactions with examples for each.	$(4+2+4) = 10$
(b)	$\beta = \begin{bmatrix} T_1 & T_2 \\ R(A) & \\ & R(A) \\ & W(A) \\ & \\ R(A) & \\ & W(A) \end{bmatrix}$ <p>Consider the above schedule S. If there is any problem with this schedule, then identify the same.</p>	
(c)	Using 2 Phase Locking Protocol, will it be possible to execute the above schedule S ? Clearly justify your answer and show your solution by placing locks at correct places, if applicable.	
3. (a)	"A Recoverable Schedule does not suffer from the Dirty Read Problem". Provide your arguments for or against this statement. An example in support of your arguments would be appreciated.	$(4 + 6) = 10$
(b)	Clearly write the steps required to be followed in case of Recovery following Immediate Update in a concurrent scheduling environment. Mention clearly how the System Log will be processed for any Undo/Redo procedure.	

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HERITAGE INSTITUTE OF TECHNOLOGY

BTech 3rd Year, 5th Semester

Class test II

Examination 2018

Session: Jul – Dec 2018

SECTION A+B+C

Paper Code: CSEN3103

Paper Name: Operating Systems

Time Allotted: 1 hr

Full Marks: 30

*Figures out of the right margin indicate full marks.**Candidates are required to give answer in their own words as far as practicable.***Answer any five from questions from Q1 and from the rest, answer any two questions.**

1(a) ✓	Define and explain the following memory management issues briefly: (i) Allocation; (ii) Relocation; (iii) Sharing; (iv) Protection	0.5*4 =2
(b) ✓	Differentiate between internal and external fragmentation of memory.	2
(c) ✓	Explain briefly the following terms: (i) Best fit policy; (ii) Next fit policy; (iii) First Fit policy;	2
(d) ✓	What is meant by the term 'storage compaction'? Explain in brief.	2
(e)	Explain the term 'demand paging'.	2
(f) ✓	Differentiate between a page and a page frame.	2
(g) ✓	Define the term page fault. Explain it with the help of an example.	2

2 a)	Consider the data given in following table:	3
	Partitions Size (KB)	2 KB 4 KB 20 KB 10 KB
	Job sizes (KB)	2 KB 10 KB 3 KB 7 KB 6 KB 8 KB 20 KB 4 KB
	Burst time (ms)	3 8 2 1 5 1 8 6

When will the job of size 20 KB get the memory and be completed, if the best fit algorithm is used for allocating jobs to various memory partitions?

(b)	Consider a logical address space of 16 pages of 512 words each, mapped onto a physical memory of 32 page frames. Answer the following: i) How many bits are there in the logical address? ii) How many bits are there in the physical address?	2+2=4
(c)	How many pages of size 1024 words each, are contained in a program with a logical address having 32 bits?	3
3. (a)	Consider the following page reference using three frames that are initially empty. Find the page faults using (i) FIFO and (ii) LRU algorithms, where the page reference sequence: 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 1, 2, 0, 1, 7, 0, 1.	3+3=6



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HERITAGE INSTITUTE OF TECHNOLOGY

BTech 3rd Year, 5th Semester Class test II Examination 2018 Session: Jul – Dec 2018

SECTION A+B+C

Paper Code: CSEN3103

Paper Name: Operating Systems

(b)	Answer the following questions: (i) Run time mapping from logical to physical address is done by (a) memory management unit, (b) CPU, (c) PCI, (d) none of the mentioned (ii) Memory management technique in which system stores and retrieves data from secondary storage for use in main memory is called a) fragmentation b) paging c) mapping d) none of the mentioned (iii) The address of a page table in memory is pointed by a) stack pointer, b) page table base register, c) page register, d) program counter (iv) A solution to the problem of external fragmentation is : a) compaction, b) larger memory space, c) smaller memory space, d) None of these	1*4=4
4.(a)	Suppose a disk drive has 300 cylinders, numbered 0 to 299. The current head position of the disk is at 90. The queue of pending requests in FIFO order is 36, 79, 15, 120, 199, 270, 89, 170. Calculate the average cylinder movements for the following algorithms: •FCFS •SSTF •C-SCAN	2+2+2=6
(b)	Explain masquerading and replay attack.	2+2=4
5.(a) (b)	Define thrashing? What are the reasons of thrashing? Explain. Consider a paging system with the page table stored in memory. i) if a memory reference takes 200 nanoseconds, how long does a paged memory reference take? ii). If we add TLBs, and 75 percent of all page-table references are found in the TLBs, what is the effective memory reference time? (Assume that finding a page-table entry in the TLBs takes zero time, if the entry is there.)	1+3=4 2+2=4
(c)	Explain Belady's anomaly with example.	2



HERITAGE INSTITUTE OF TECHNOLOGY

B.Tech 5th Semester Class Test II Examination 2018

Session 2018-2019

Discipline(s): Computer Science and Engineering

Paper Code CSEN3104

Paper Name: Computer Architecture

Time Allotted: 1 hour

Full Marks: 30

Figures out of the right margin indicate full marks.

Answer ALL the questions

Candidates are required to give answer in their own words as far as practicable

1	<p>Choose the correct alternative for the following</p> <p>Cache memory</p> <p>(a) increases performance (b) decreases performance (c) increases machine cycle (d) none of these</p> <p>For which shared / distributed memory systems is the snooping protocol suited?</p> <p>(a) Crossbar connected systems (b) Bus based systems (c) Systems with butterfly network (d) None of the above is correct</p> <p>Which of the following is not a property of a memory module?</p> <p>(a) inclusion (b) consistency (c) capacity (d) commutative</p> <p>Zero address instruction format is used for</p> <p>(a) RISC architecture (b) CISC architecture (c) Von-Neumann architecture (d) Stack-organized architecture</p> <p>CC-NUMA stands for</p> <p>(a) Cache coherent NUMA (b) Cyclical Co-ordination NUMA (c) Cache Co-ordinated NUMA (d) None of the above</p>	$5 \times 1 = 5$															
2	<p>(a) Draw a Data Flow Graph for approximate calculation of</p> $\cos x = 1 - x^2/2! + x^4/4! - x^6/720$ <p>(b) A 50 MHz processor was used to execute a program with the following instruction mix and clock cycle counts</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left; padding: 2px;">Instruction Type</th> <th style="text-align: left; padding: 2px;">Instruction Count</th> <th style="text-align: left; padding: 2px;">Clock Cycle Count</th> </tr> </thead> <tbody> <tr> <td style="padding: 2px;">Integer Arithmetic</td> <td style="padding: 2px;">50000</td> <td style="padding: 2px;">2</td> </tr> <tr> <td style="padding: 2px;">Data Transfer</td> <td style="padding: 2px;">70000</td> <td style="padding: 2px;">3</td> </tr> <tr> <td style="padding: 2px;">Floating point arithmetic</td> <td style="padding: 2px;">25000</td> <td style="padding: 2px;">1</td> </tr> <tr> <td style="padding: 2px;">Branch</td> <td style="padding: 2px;">4000</td> <td style="padding: 2px;">2</td> </tr> </tbody> </table> <p>Calculate the effective CPI, MIPS rate and execution time for this program</p> <p>(c) Write down algorithm for odd-even transposition sort and explain it using a set of data.</p>	Instruction Type	Instruction Count	Clock Cycle Count	Integer Arithmetic	50000	2	Data Transfer	70000	3	Floating point arithmetic	25000	1	Branch	4000	2	$(4) + (6) + (5) = 15$
Instruction Type	Instruction Count	Clock Cycle Count															
Integer Arithmetic	50000	2															
Data Transfer	70000	3															
Floating point arithmetic	25000	1															
Branch	4000	2															
3	<p>(a) Differentiate between processor consistency and release consistency in the relaxed consistency model of Memory Consistency</p> <p>(b) Suppose that in an MIMD system, there are 20 processors. Each has its own cache. Suppose two processors each caches a single shared variable X. How many messages are sent across the system for maintaining cache coherency of X if a) Snooping protocol is used? b) If a Centralized Directory Based Protocol is used? Explain your answer</p> <p>(i) Explain the concept of VLIW architecture, highlighting how it is different from instruction level parallelism</p>	$(4) + (4) + (2) = 10$															



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HERITAGE INSTITUTE OF TECHNOLOGY

5th Semester Examination 20182nd Class Test

Session : 2018-19

Discipline : Computer Science Engineering

Paper Code: AEIE3105

Paper Name: Microprocessors & Microcontrollers

Time Allotted: 1 hr

Full Marks: 30

Figures out of the right margin indicate full marks.

Answer all the questions

Candidates are required to give answer in their own words as far as practicable.

1. (a)	What physical address is represented by 1000: 0FFFH ? (i) 1FFFF _H (ii) 10FFF _H (iii) 11FFF _H (iv) C0FFF _H	1 + 1 + 2 + 3 + 3 + 3 + 2 = 15
(b)	Data bus of 8086 µP is (i) 20 bit bidirectional (ii) 20 bit unidirectional (iii) 16 bit bidirectional (iv) 16 bit unidirectional	10000 0FFF 10FFF
(c)	What is the function of instruction queue in 8086 µP?	
(d)	Explain the function of following instructions (any two) – i) MOVS B ii) XLAT iii) CLD iv) STC	
(e)	What is the function of O and T flag bits of 8086 µP?	
(f)	Explain the function of following pin of 8086 µP (any two) – i) DT/R ii) DEN iii) BHE	
(g)	Write a program to load 2000 _H in DS register and 4000 _H in SI register.	
2. (a)	Size of internal ROM in 8051 µC chip is- (i) 128 Byte (ii) 256 Byte (iii) 2KB (iv) 4KB	1 + 1 + 3 + 3 + 4 + 3 = 15
(b)	After RESET operation SP register content is- (i) 00 _H (ii) 07 _H (iii) 0F _H (iv) FF _H	
(c)	Explain the function of following signals of 8051 µC (any two). i) EA ii) PSEN iii) TxD	
(d)	Explain the function of following instructions of 8051 µC (any two). i) MOVC A,@A+DPTR ii) SETB P1.0 iii) DJNZ R1,L1	
(e)	Discuss the internal RAM memory organization of 8051 µC.	
(f)	Explain the interrupts of 8051 µC.	

OR

Write the name of addressing modes of 8051 µC with suitable example.