What does HDL stand for?

HDL is short for Hardware Description Language

(**VHDL** – **V**HSIC **H**ardware **D**escription **L**anguage)
(Very High Speed Integrated Circuit)

Origin of the VHDL

- VHDL originated in the early 1980s
  - The American Department of Defense initiated the development of VHDL in the early 1980s
    - because the US military needed a standardized method of describing electronic systems

Standardization

- IEEE standard, labeled IEEE Std 1164-1993 is the package STD_LOGIC_1164 which we will use.
- Official VHDL language description available from IEEE (IEEE Standard VHDL Language Reference Manual- VHLD also recognized as the ANSI standard).

What does VHDL do?

- VHDL is standard languages for
  - specifying
  - verifying
  - designing of electronics
- Used to model
  - digital system (an entity)
    - Simple logic gate, ALU, comparator or as complex as a complete electronic system

VHDL- Program Structure

- **Entity description has 2 components**

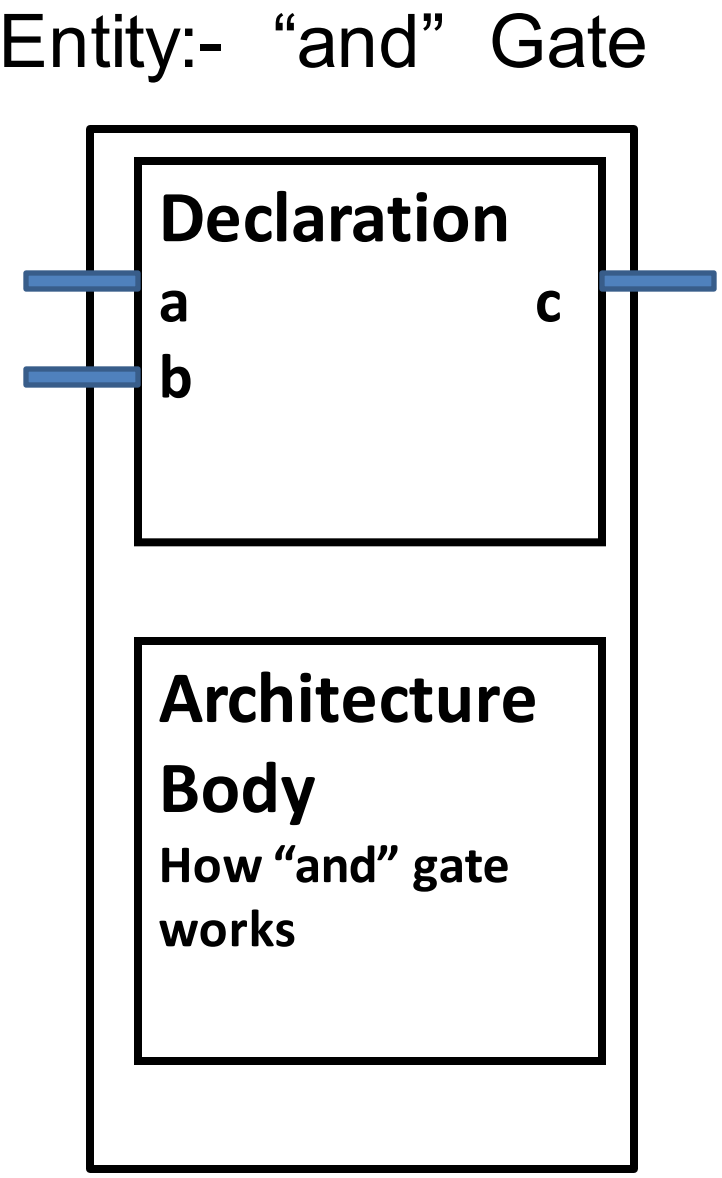
– Declaration:-**Interface description-** a list of the interconnections (ports) -- in and out signals

– a,b,c are the ports

(interface/interconnections)

– **Architecture body-** some description of how the block works

- – AND gate is the architecture



Entity Declaration

- **entity** NAME_OF_ENTITY **is**

  port (*signal_names*: **mode** *type*;
  signal_names: **mode** *type*;
  :
  signal_names: **mode** *type*);

  end [NAME_OF_ENTITY] ;

signal_name:- external interface signals

mode :- reserved word :-in,out, inout

Entity Declaration

```
entity and1 is
Port( A,B: in  std_logic;
      c: out std_logic);
end and1;
```

(package STD_LOGIC_1164)

Types

- *std_logic, std_ulogic, std_logic_vector, std_ulogic_vector*: indicate the value and strength of a signal.
  Std_ulogic and std_logic (preferred over the bit or bit_vector types.)
- std_logic :-
- 'U‘ - Uninitialized, 'X‘-Forcing Unknown,
- '0', -- Forcing 0 '1', -- Forcing 1,
- ‘Z', - High Impedance 'W', Weak Unknown
- 'L', -- Weak 0 'H', - Weak 1
- '-' -- Don't care

Types

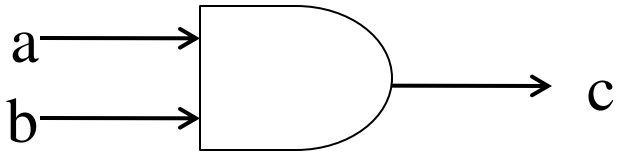
- *bit* – 0 and 1
- *bit_vector* – (e.g. bit_vector (0 to 7)
- *boolean* – value TRUE and FALSE
- *integer* –range -(2**31-1) to (2**31)
- *real* – range of real values
- *character* – any printing character
- *time* – to indicate time

Architecture Body

- 3 modeling styles (specify internal details of entity):-

1. Dataflow Model: set of concurrent assignment statements (i.e RTL)
2. Behavior Model :Sequential assignment statements within a process block (describe the complete truth table)
3. Structural Model:- as a set of interconnected components

Dataflow Model
andgate




```
Entity andgate IS
        PORT(   a: IN std_logic;
                b: IN std_logic;
                c: OUT std_logic);
END andgate;
```

```
ARCHITECTURE  dataflow OF andgate IS
        BEGIN
                c <= a AND b;
END dataflow;
```

NOTE: VHDL is case-insensitive

Xilinx 9.1i Interactive Software Environment used to write and simulate VHDL programs in CSEN3114

END