Pipelining in VLIW Processers

Fetch Decode Execute
Write Back.

Execute
3 operations
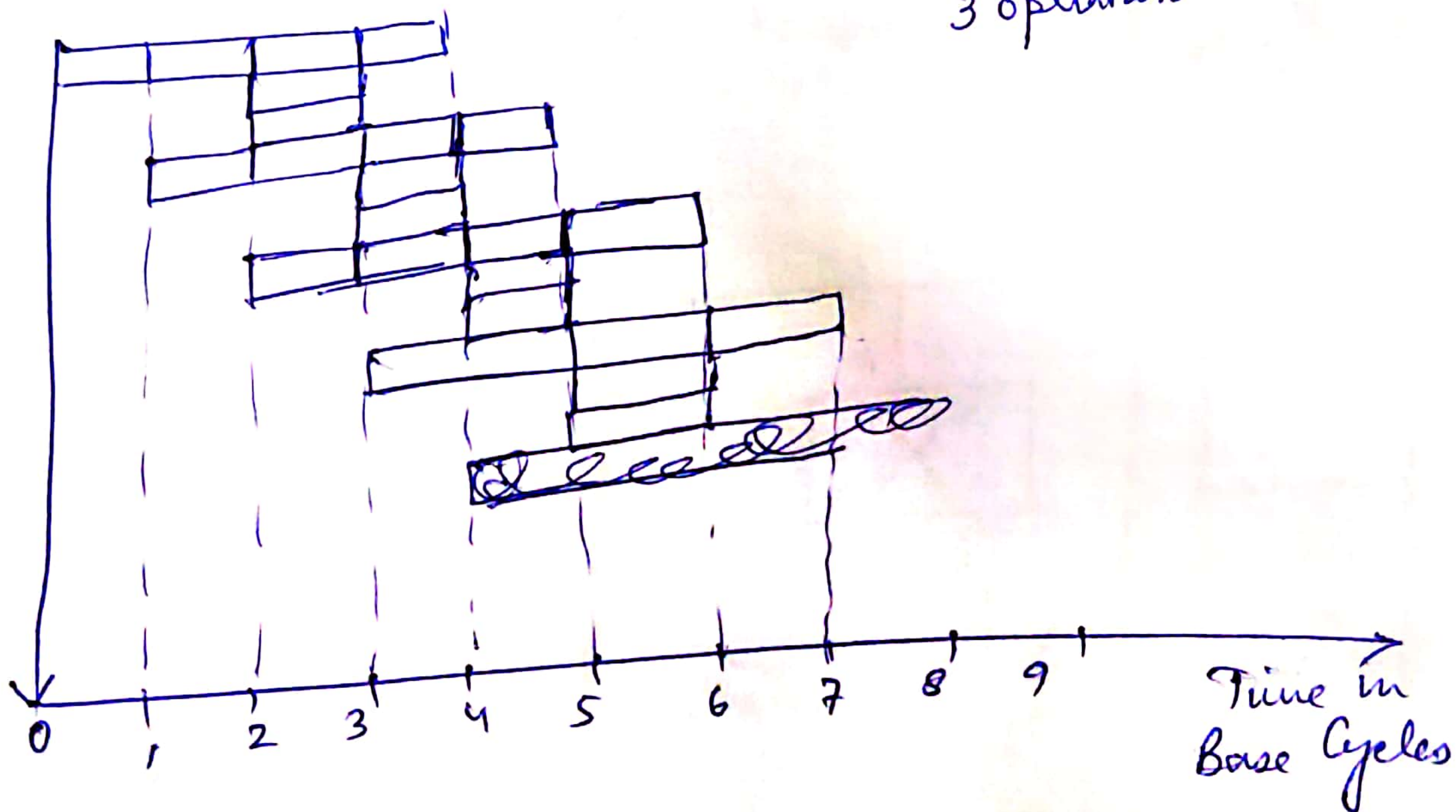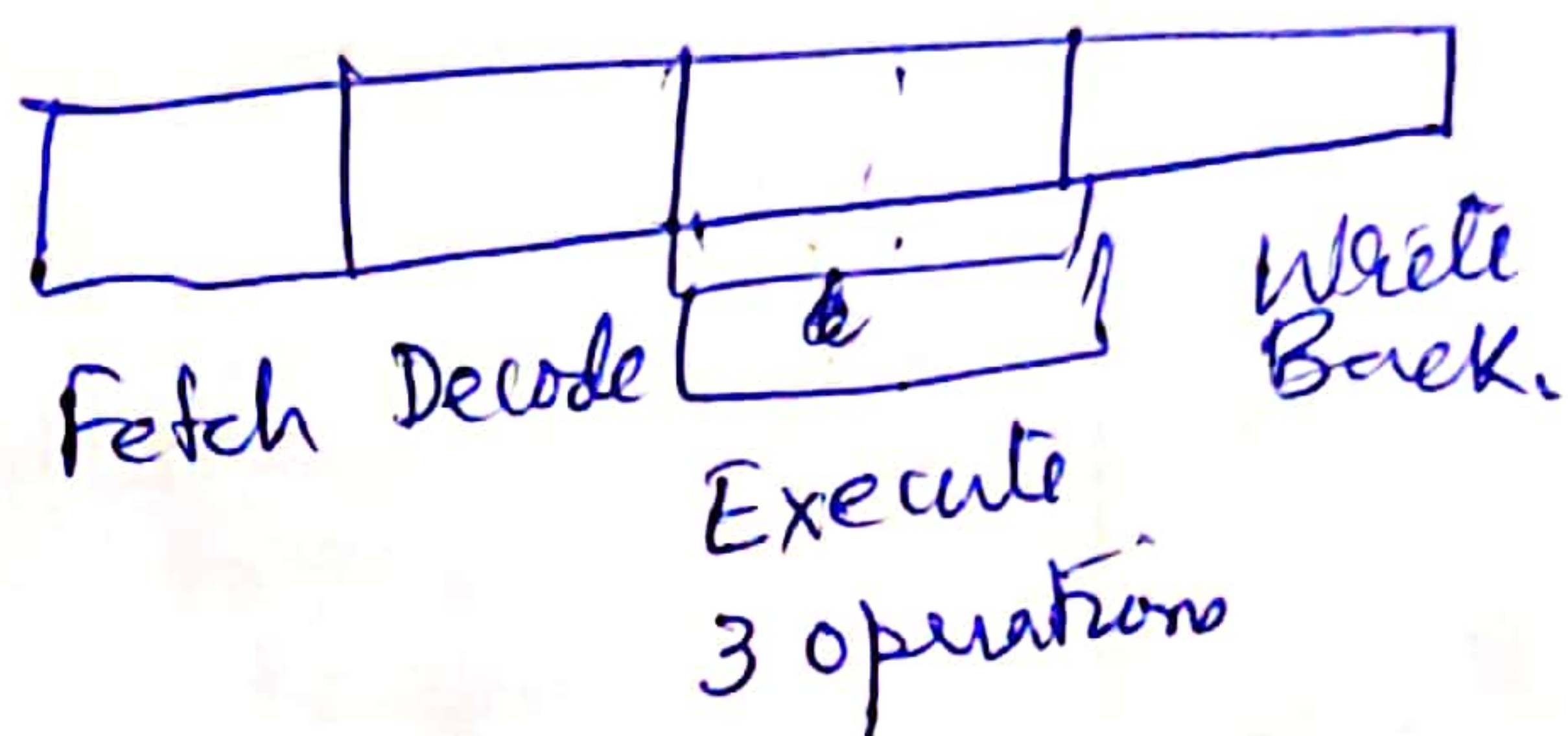
VLIW execution with degree m = 3.

Time in Base Cycles

0 1 2 3 4 5 6 7 8 9

UMA Multiprocessor Model

(Processors)

```
┌─────┐      ┌─────┐                    ┌─────┐
│ P₁  │      │ P₂  │    . . . .         │ Pₙ  │
└─────┘      └─────┘                    └─────┘
   ↕            ↕                          ↕
┌──────────────────────────────────────────────┐
│        System Interconnect                     │
│  (Bus, Crossbar Switch, Multistage NW)         │
└──────────────────────────────────────────────┘
   ↕         ↕              ↕               ↕
┌─────┐  ┌─────┐       ┌─────┐          ┌─────┐
│ I/O │  │ SM₁ │       │ SM₂ │ . . . . .│ SMₘ │
└─────┘  └─────┘       └─────┘          └─────┘
```

P_1 P_2 P_n

System Interconnect
(Bus, Crossbar Switch, Multistage NW)

I/O   SM₁   SM₂   SMₘ
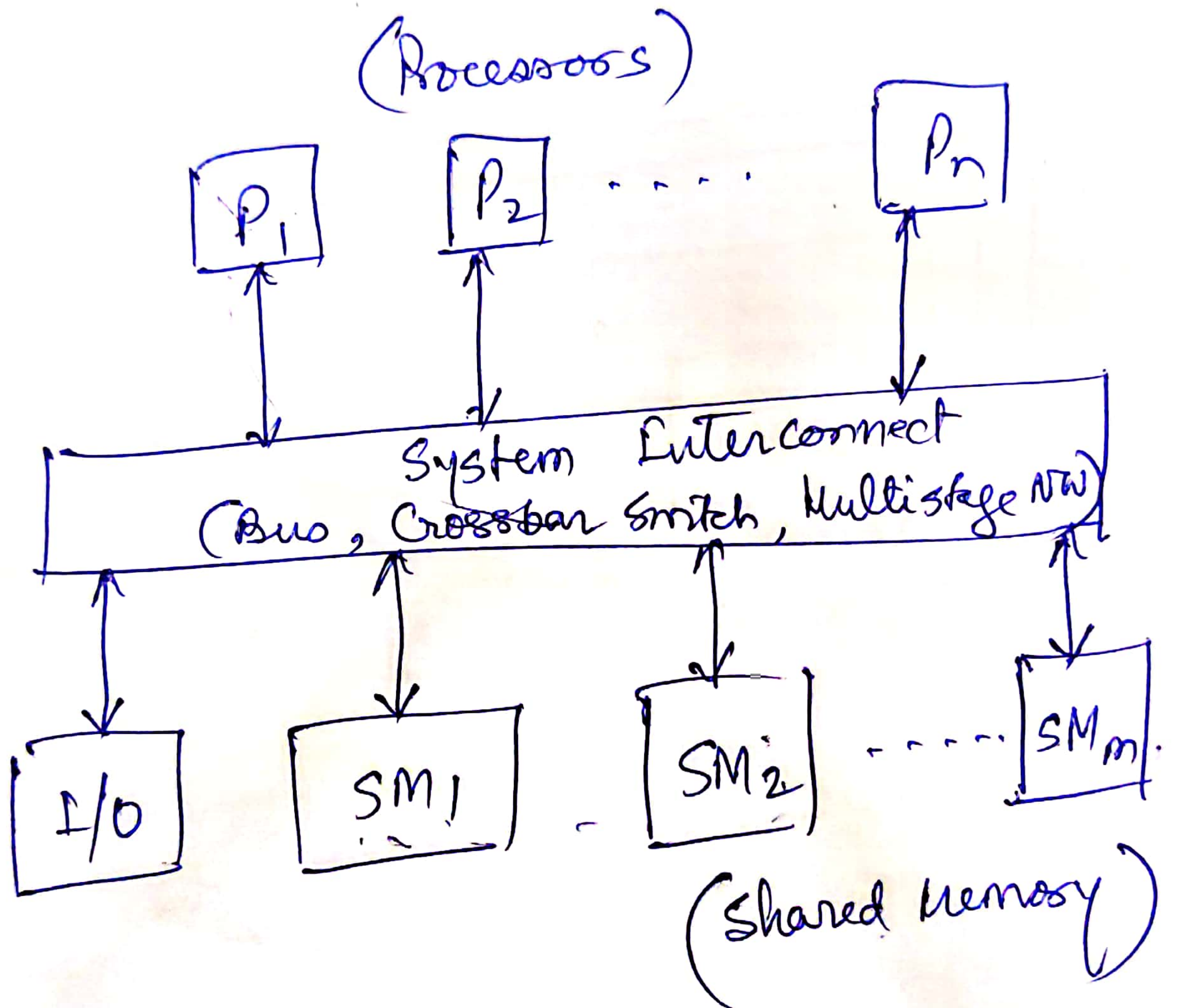
(Shared Memory)

Uniform

NUMA model
(shared local memories)

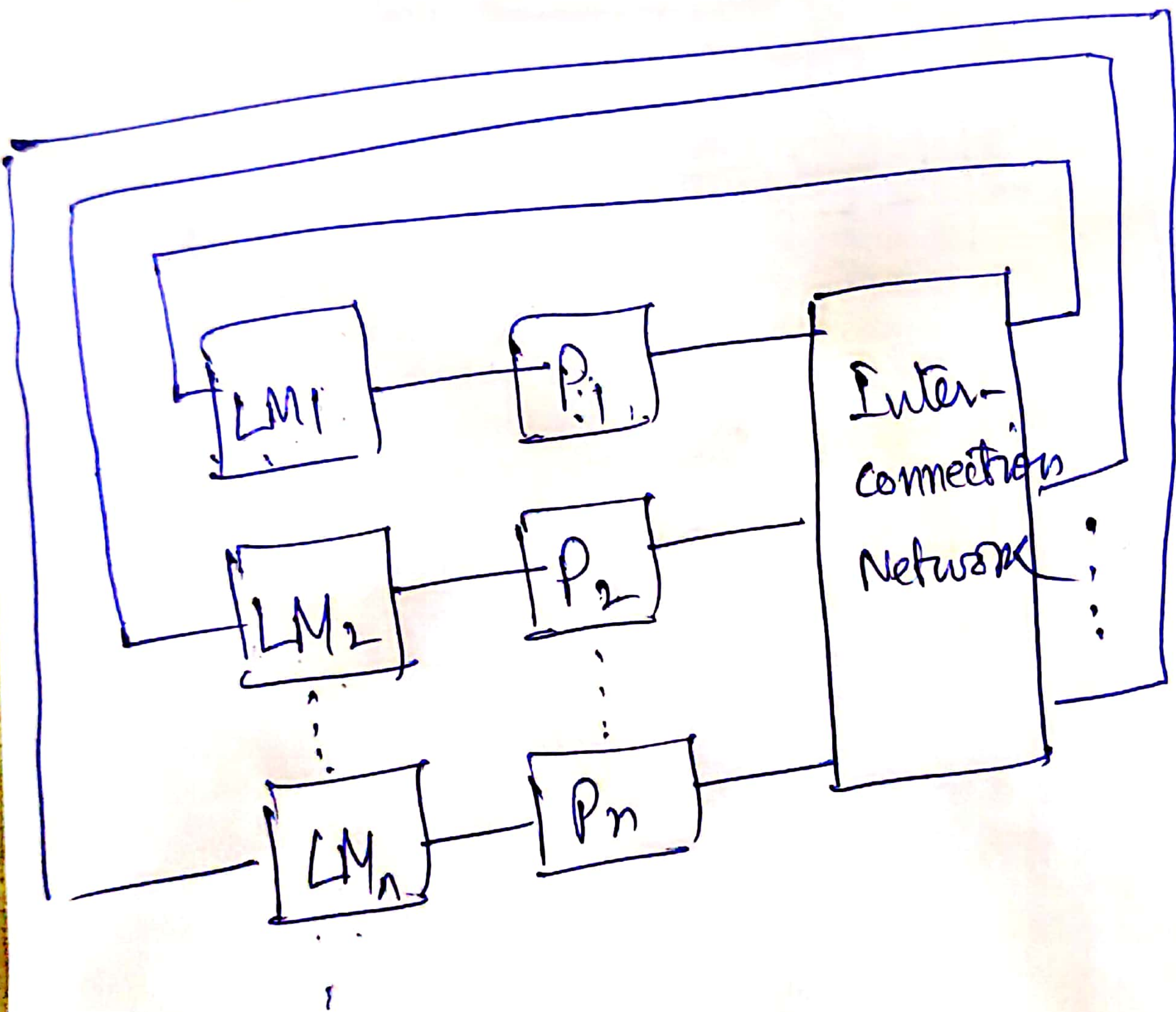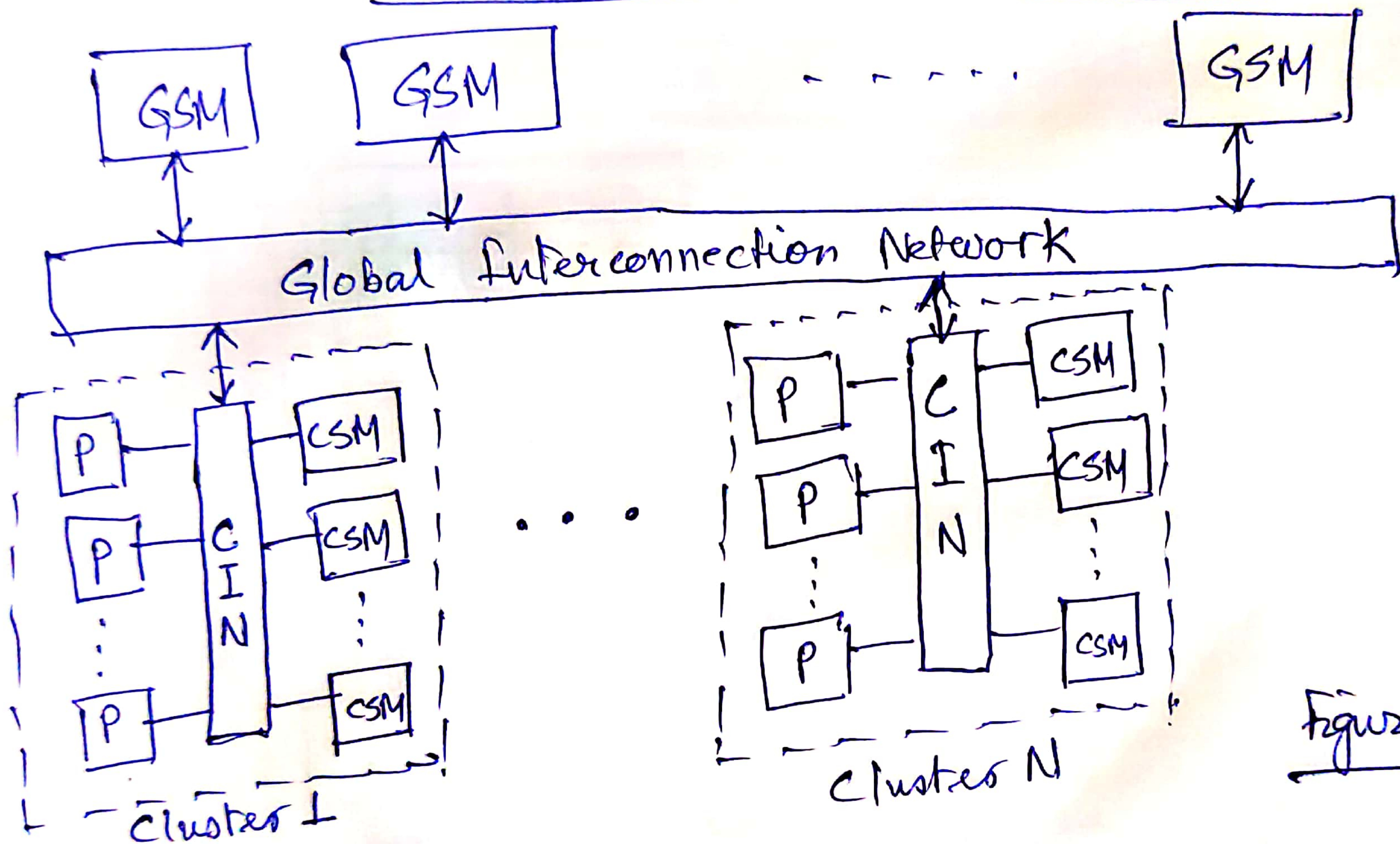| LMI | P₁ | |
| LM₂ | P₂ | Inter-connection Network |
| LMₙ | Pₙ | |

Figure (a)

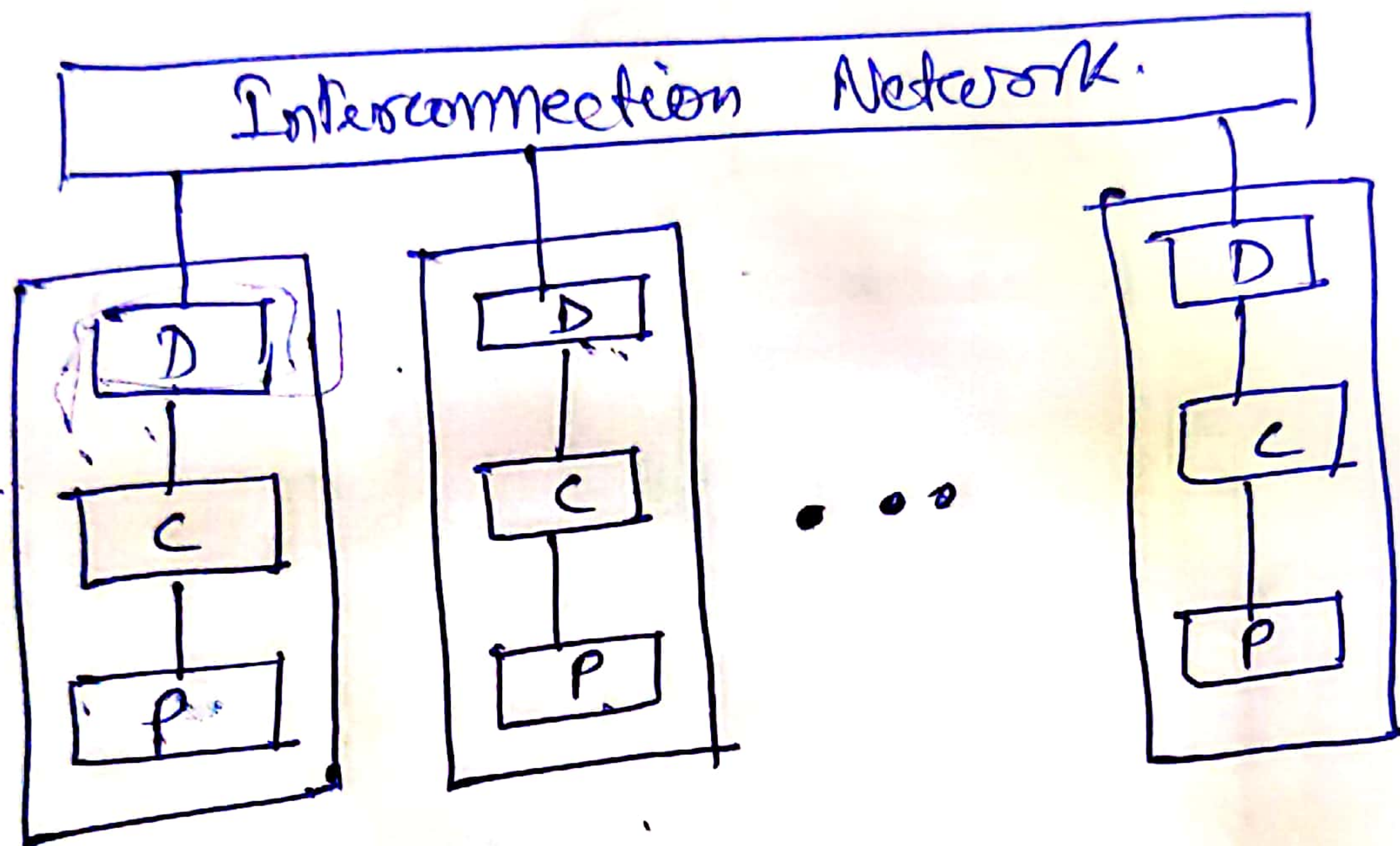# Hierarchical Cluster Model (NUMA)

Figure (b)

P: Processor
CSM: Cluster Shared Memory
GSM: Global Shared Memory
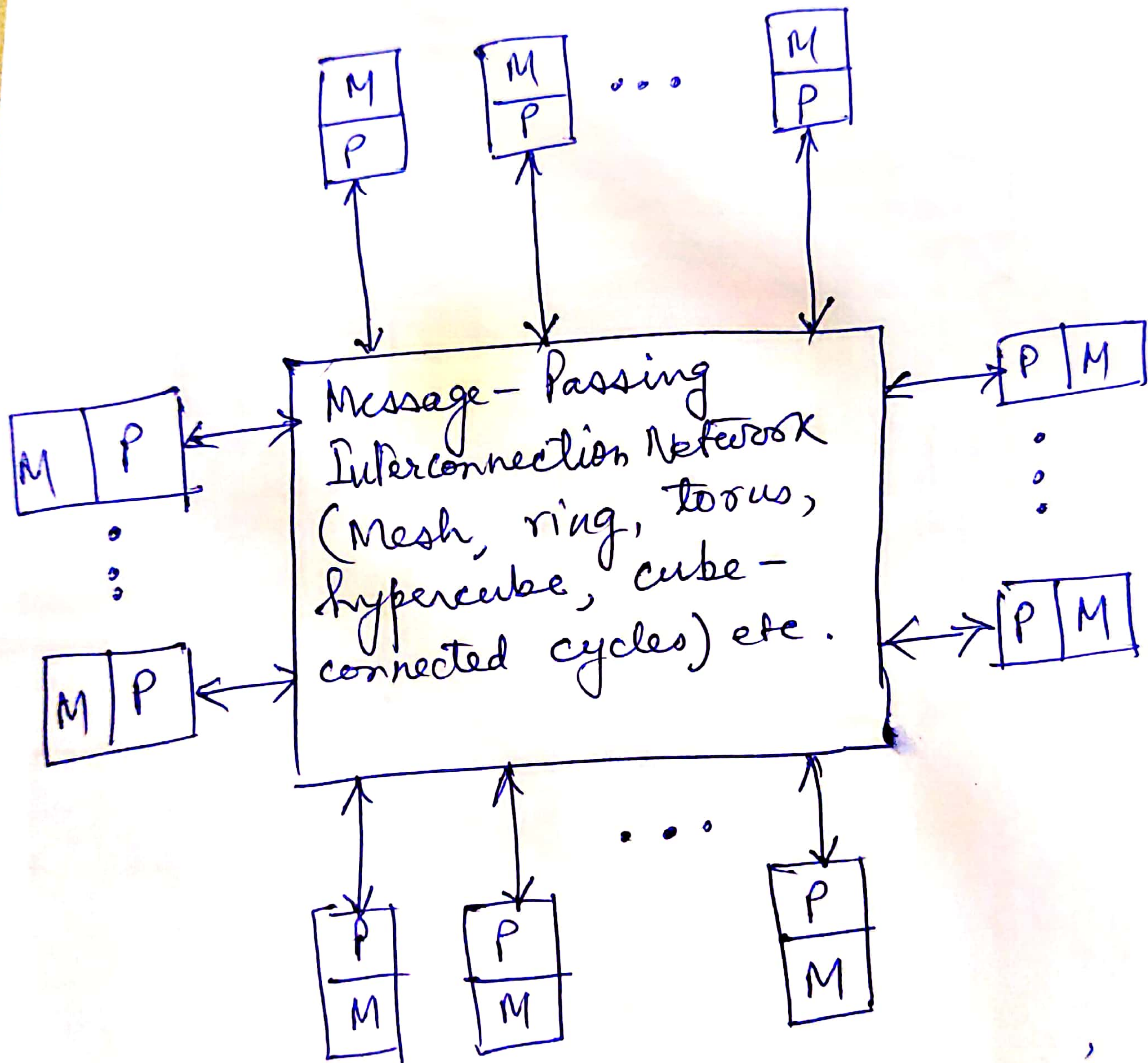CIN: Cluster Interconnection Network.

COMA Model

P : Processor
C : Cache
D : Directory

NoRMA Architecture

Generic Model of a message-passing multi-computer.

CC-NUMA Shared Memory
Multiprocessors