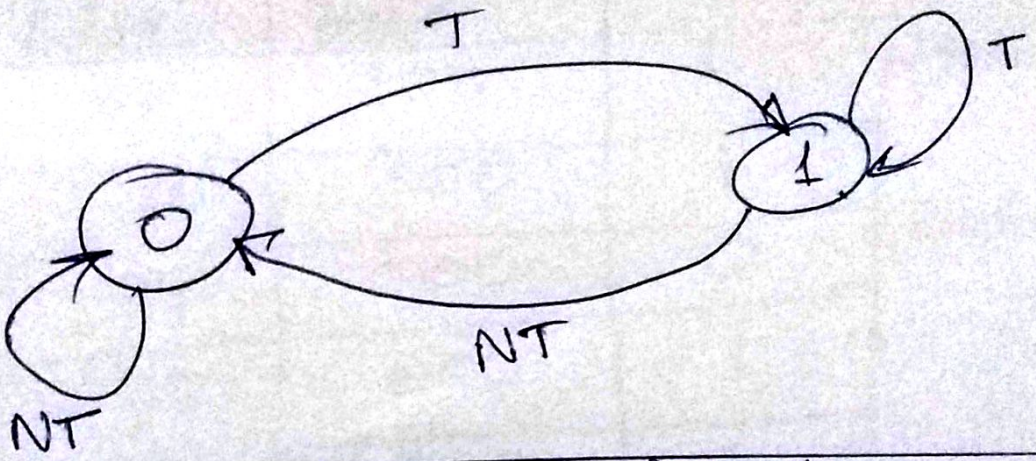
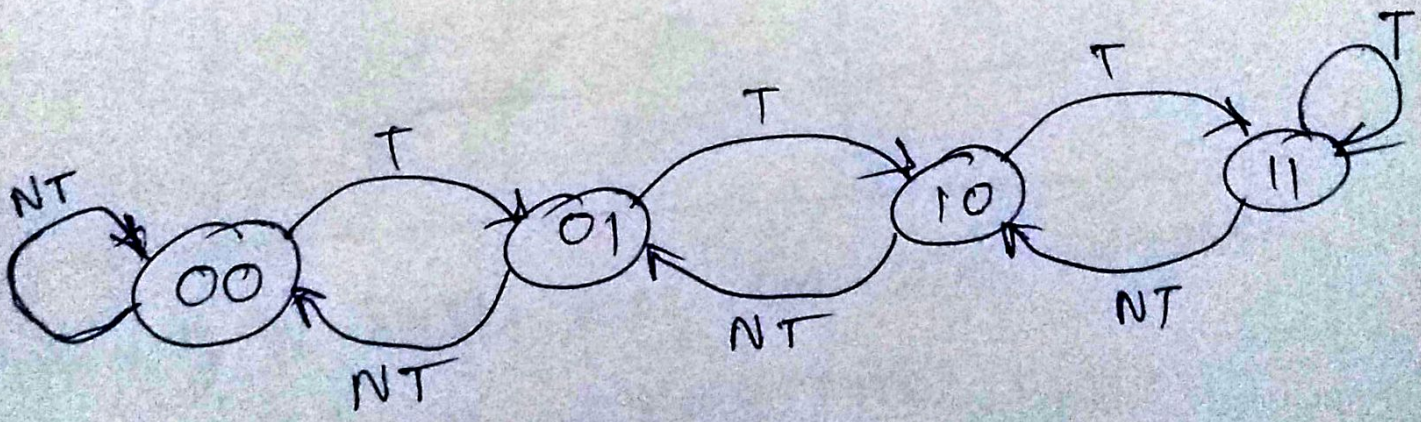
1-bit Branch Prediction



2-bit Branch Prediction



Branch History Buffer (BHB)

	Branch Instr. Addr.	Branch Target Addr	1-bit Prediction	
000	80	100	1	(Branch Taken)
001	129	200	1	
010	34	300	0	(Branch Not Taken)
011	75	600	1	
100	100	700	1	
101	261	800	0	
110	518	900	0	
111	15	1000	1	

Size of the buffer may be 256 or 1024.

Let Initially PC = 100.

32-bit Addr = ...0000110 0100

Least Significant 3-bits = 100.

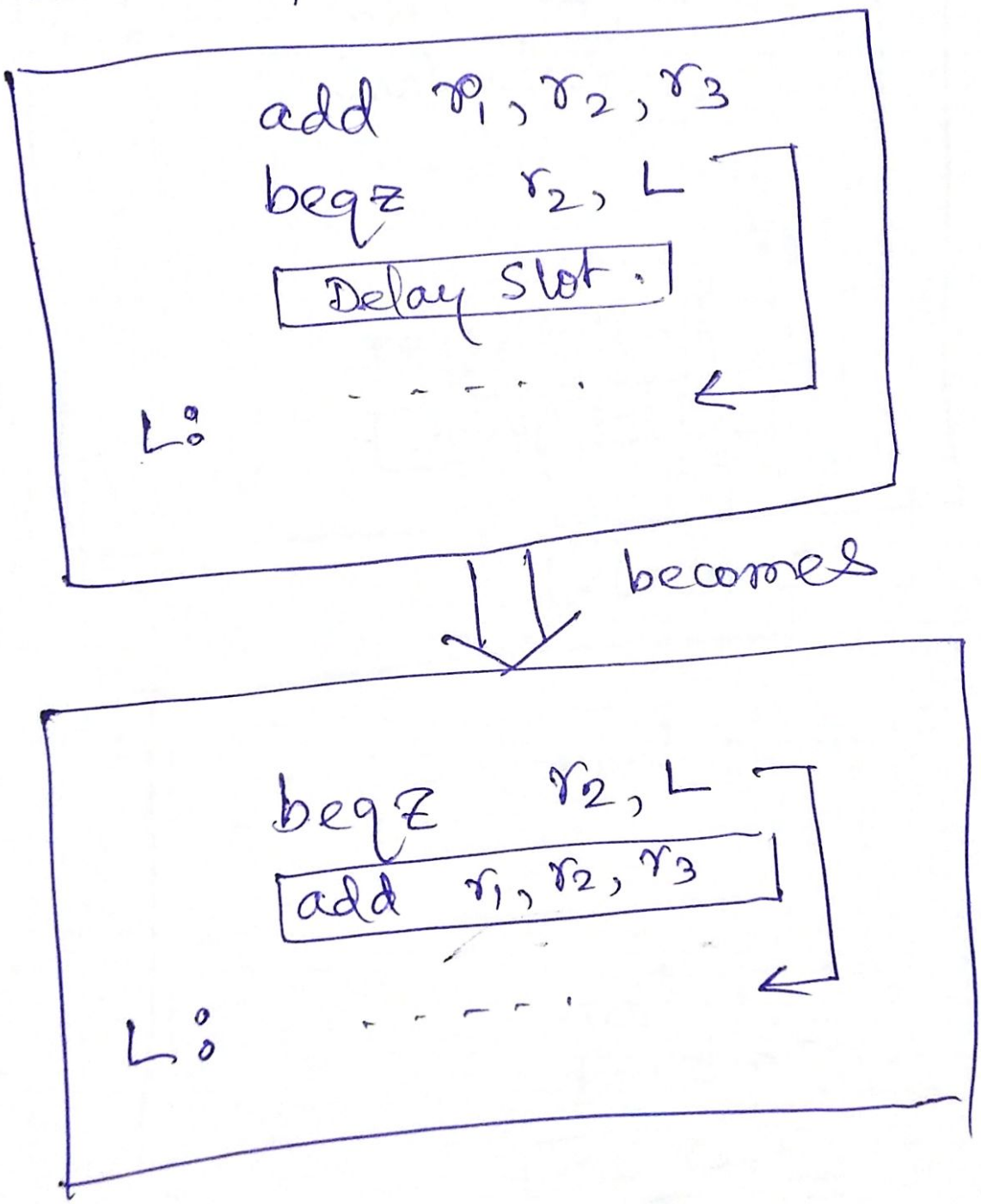
So, it matches in 5th row of BHB.

Prediction Bit = 1 So, Branch to be taken

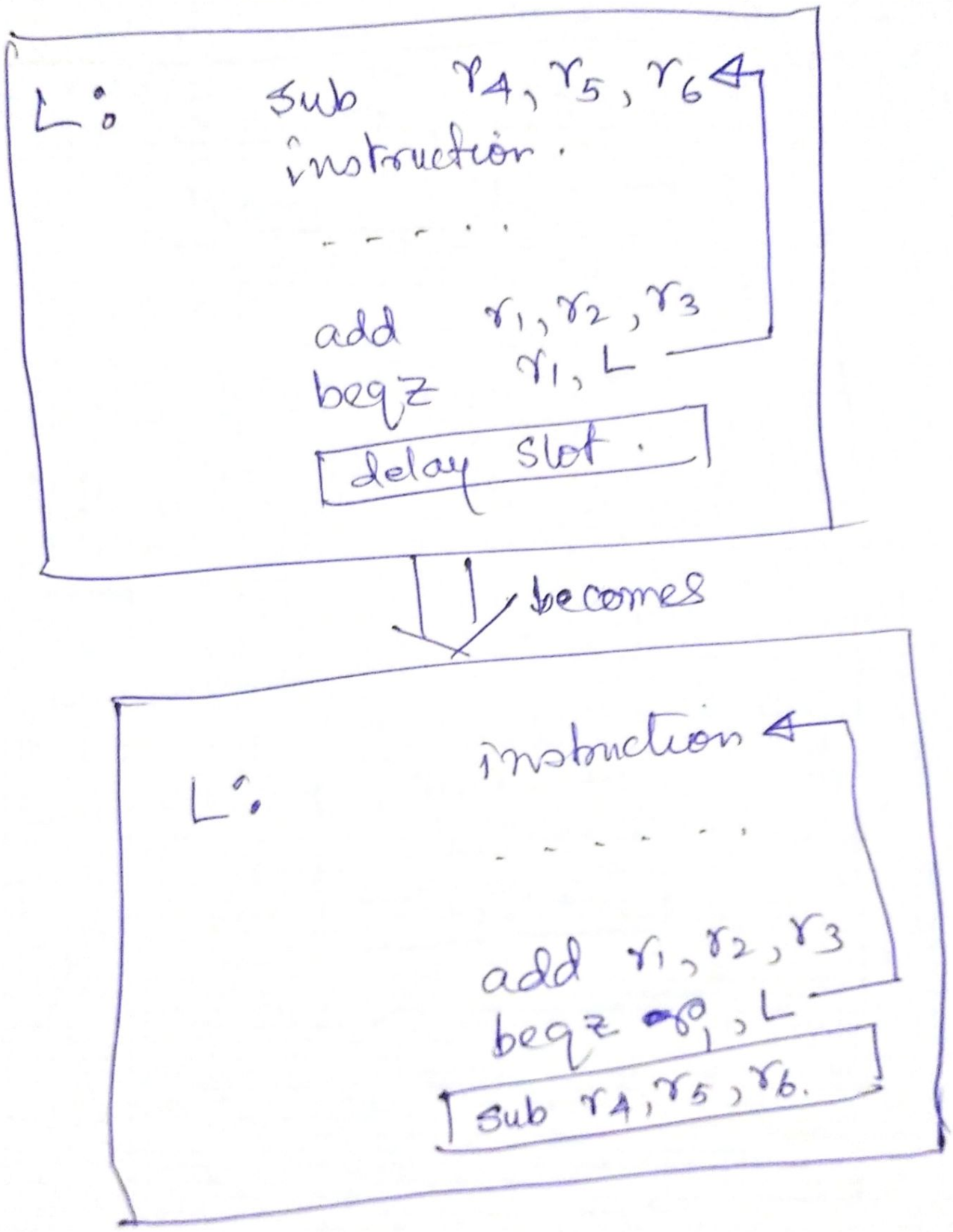
So, next PC = 700.

Scheduling Branch Delay Slots

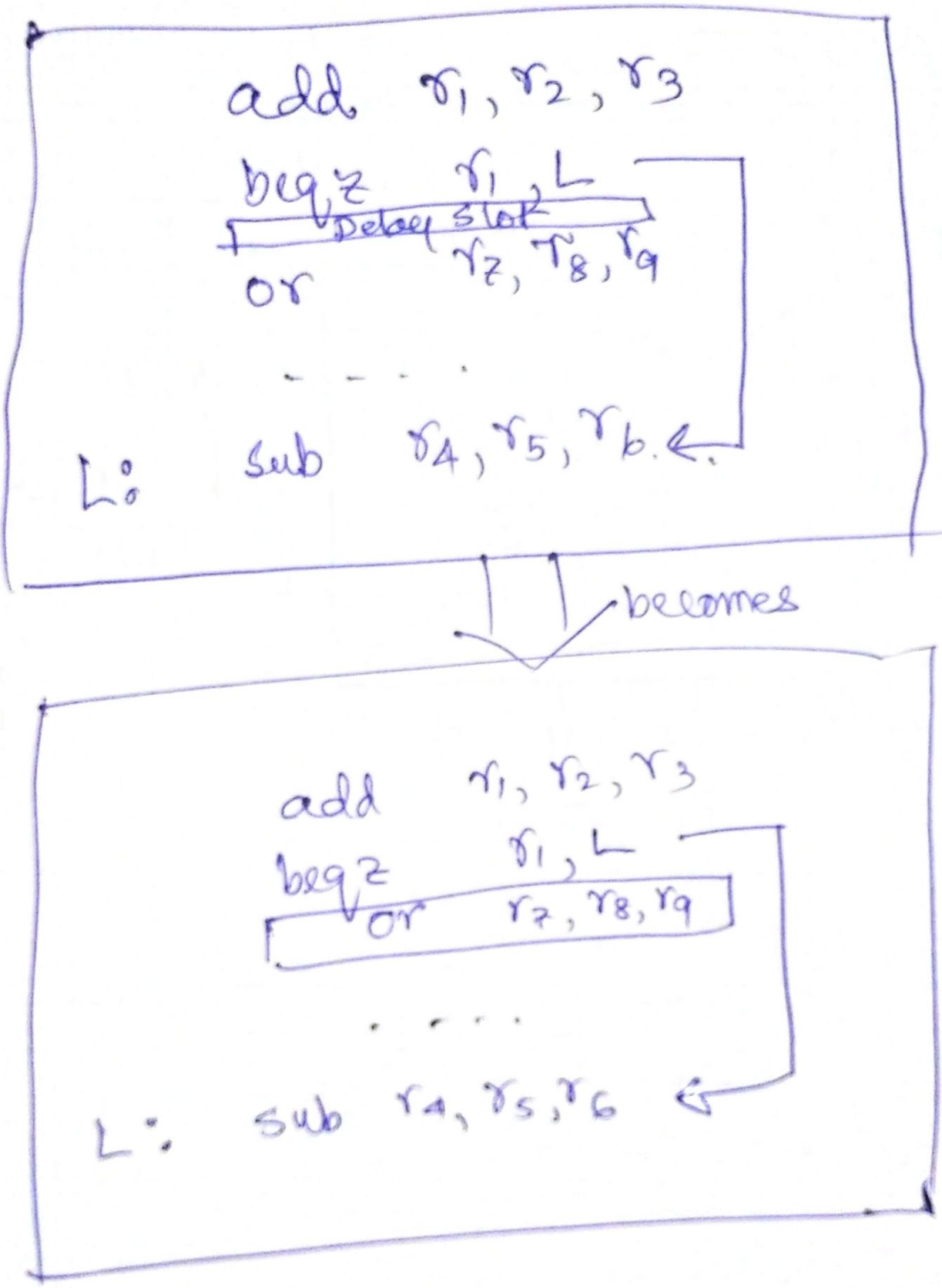
(A) From Before Branch instruction



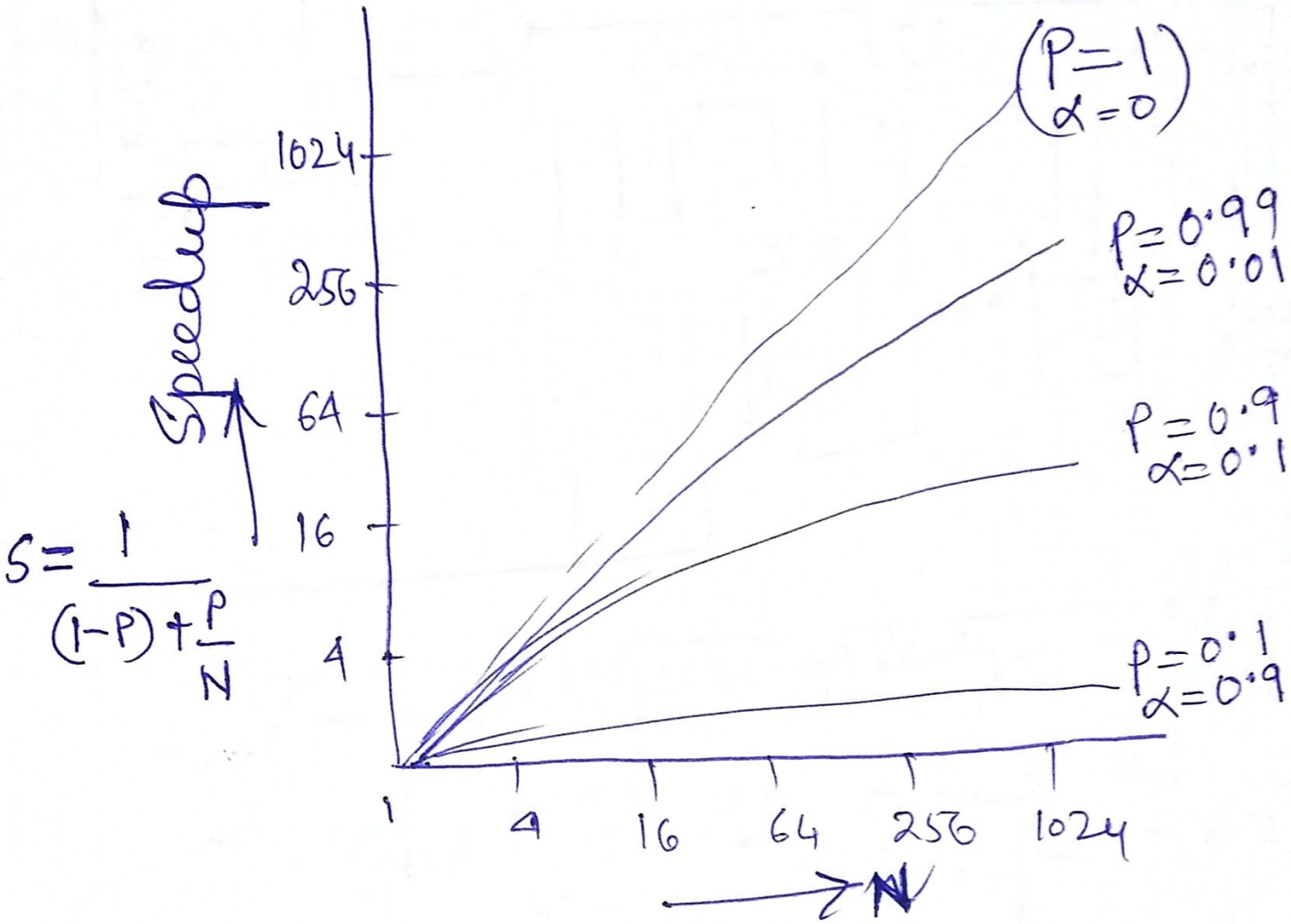
(B) From Branch Target



(c) From Fall Through

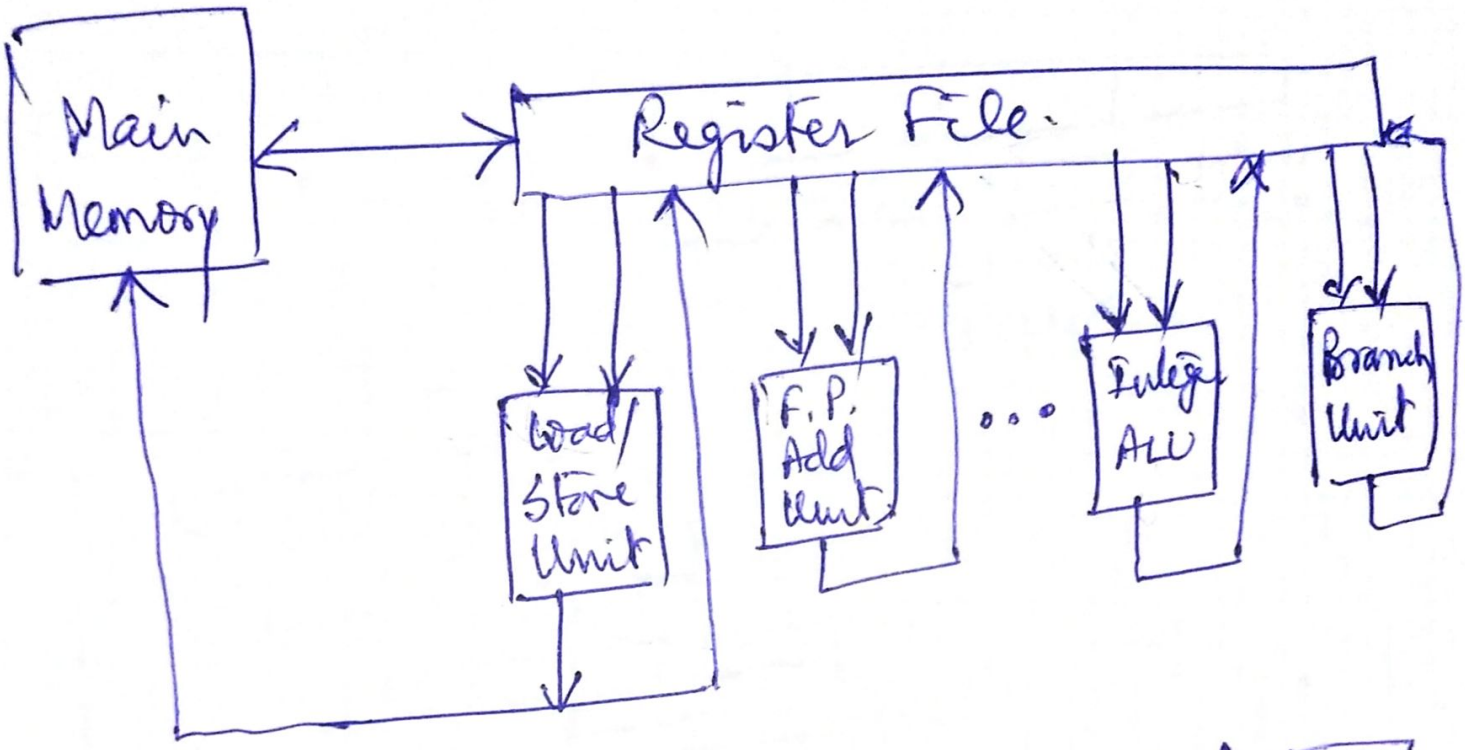


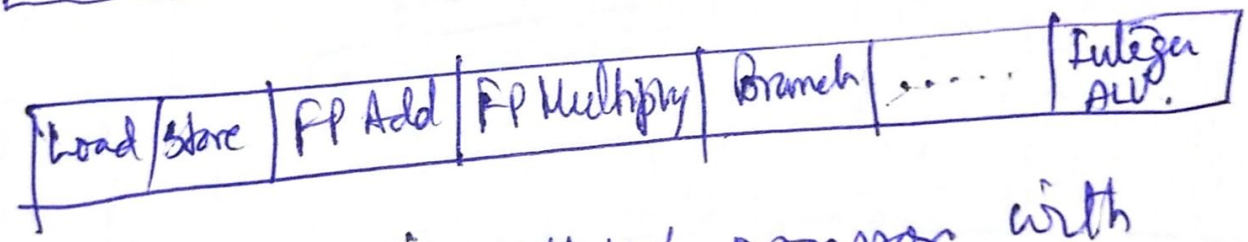
Amdahl's law



$$S = \frac{1}{(1-P) + \frac{P}{N}}$$

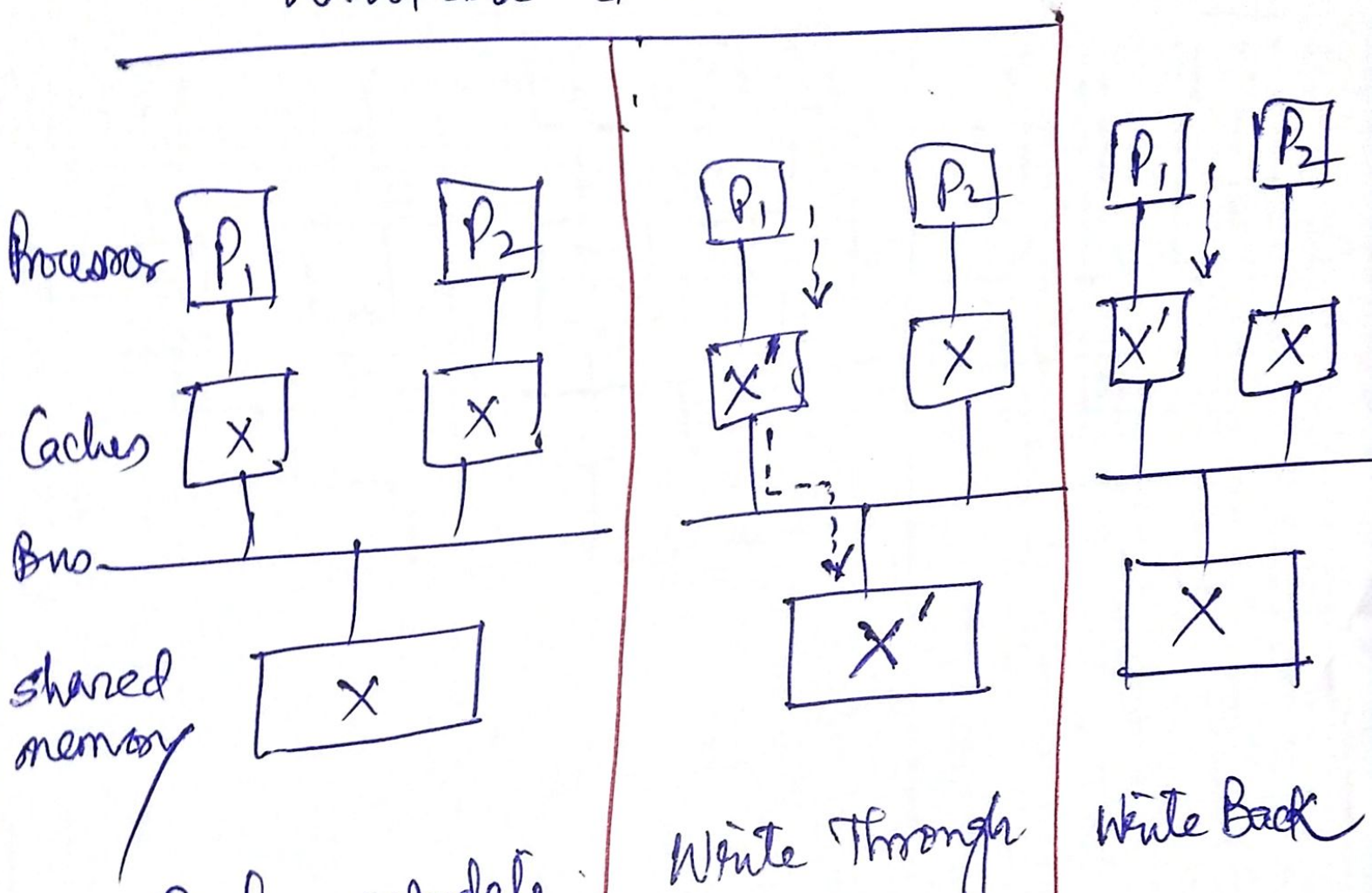
VLIW Architecture



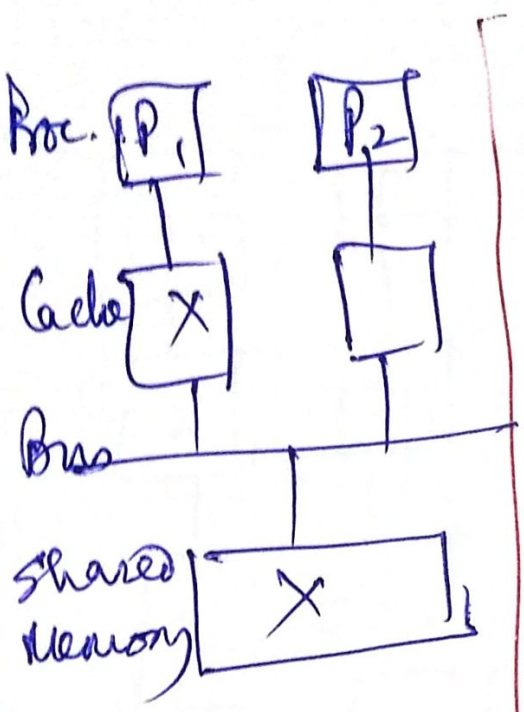


A typical VLIW processor with degree m = 3.

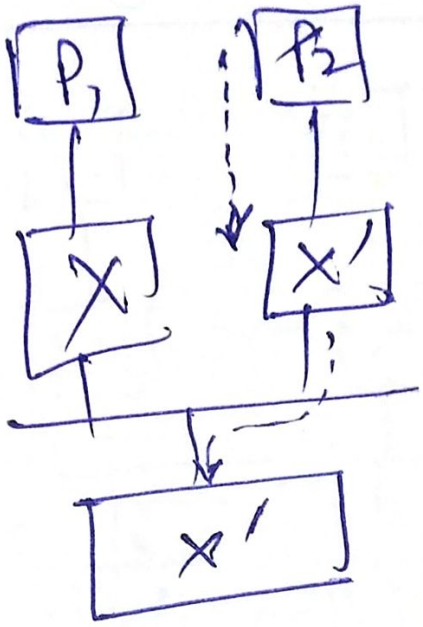
Cache Inconsistency in sharing of Writable data



Inconsistency after Process Migration

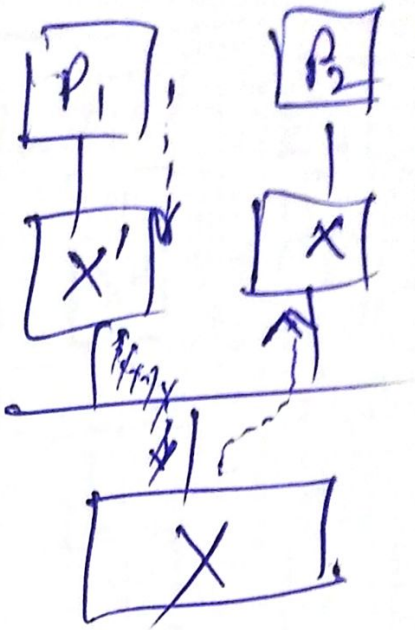


(Before migration)



(Write through)

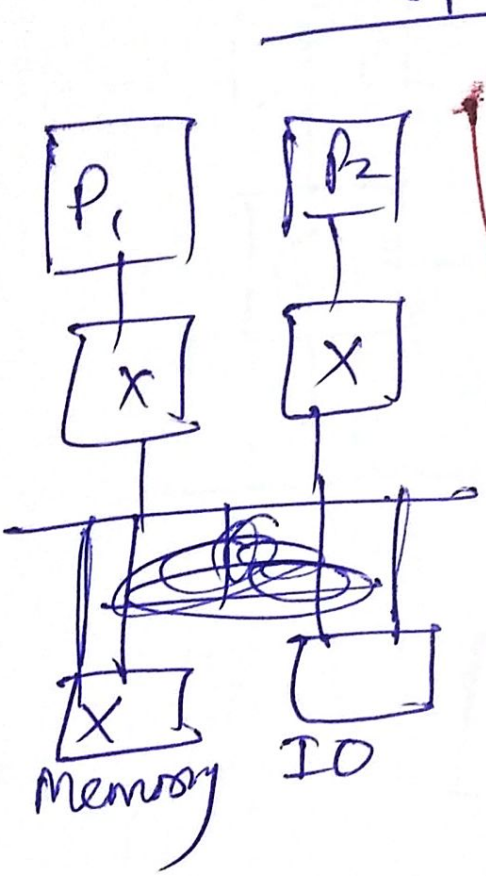
Process migrates from P_2 to P_1

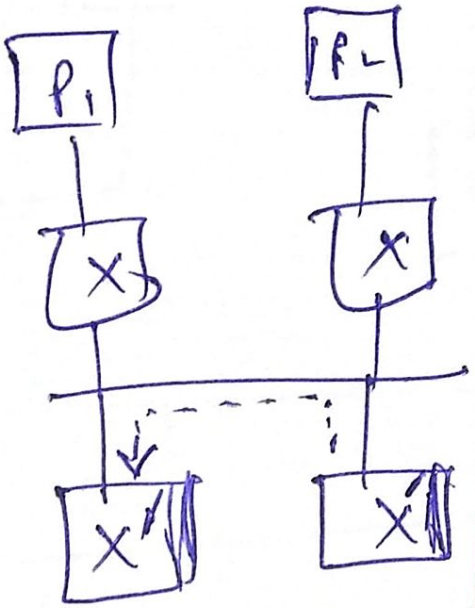


(Write Back)

Process migrates from P_1 to P_2 containing a shared variable X

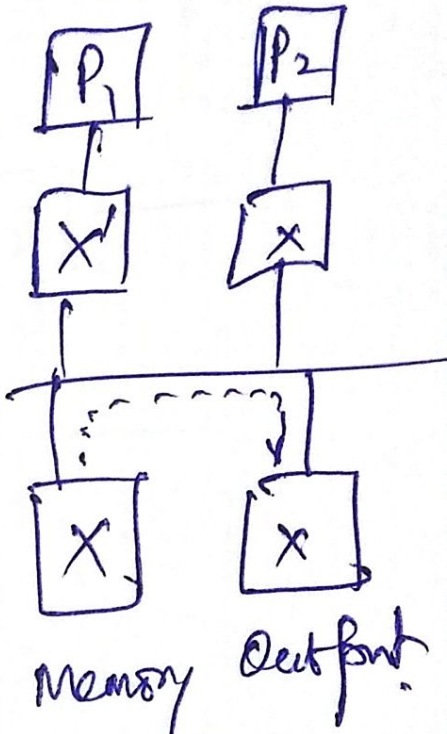
Inconsistency due to IO operations bypassing the cache





(Write through)

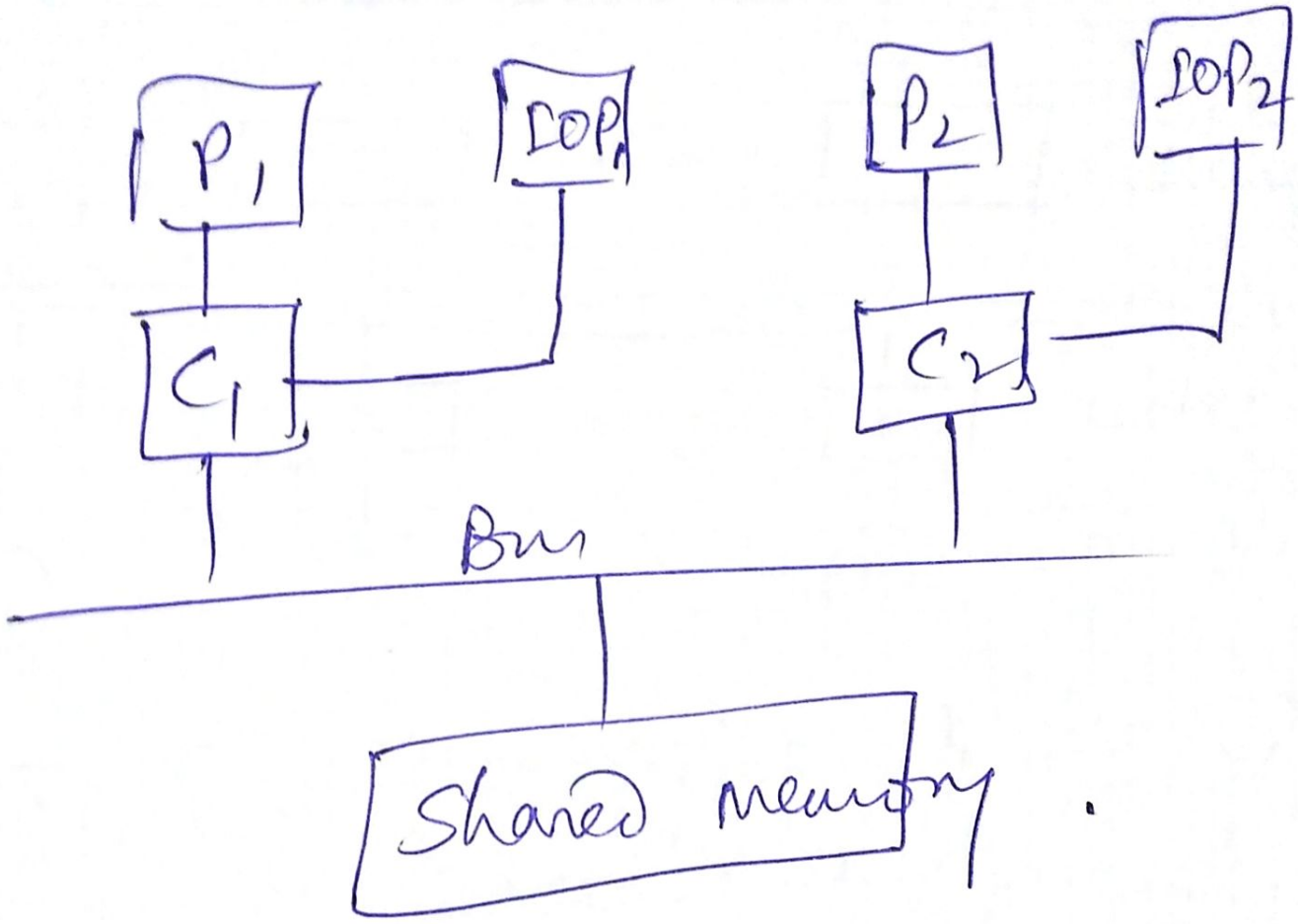
Inconsistency between cache 1 and the shared memory



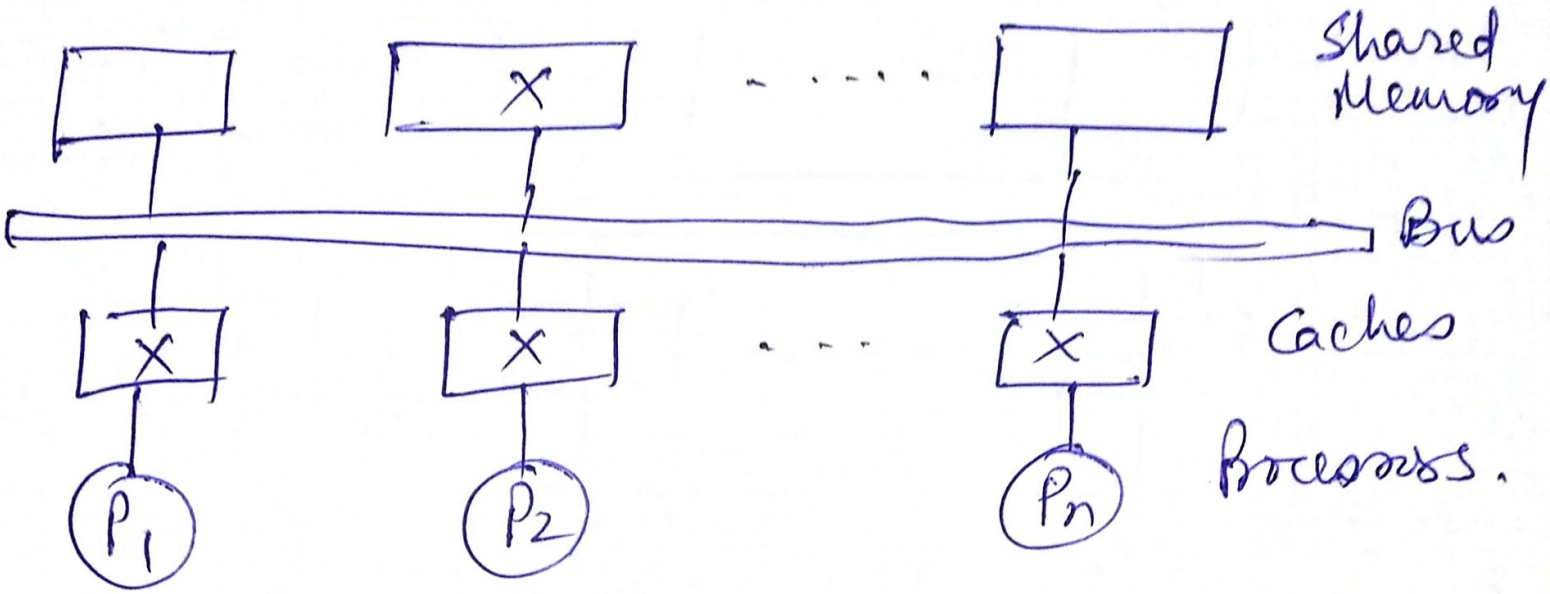
(Write Back)

Inconsistency occurs.

A possible Solution

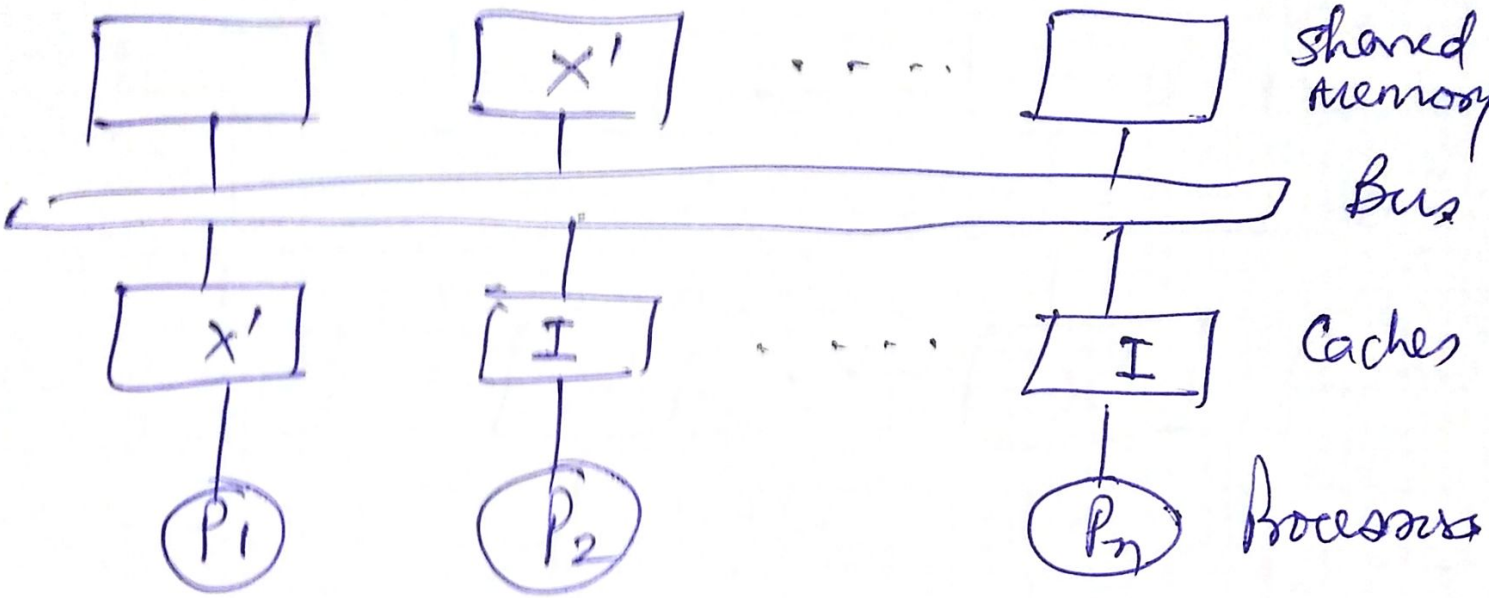


Snoopy Bus Protocols (a)



(a) Consistent copies of block X are in shared memory and three processor caches.

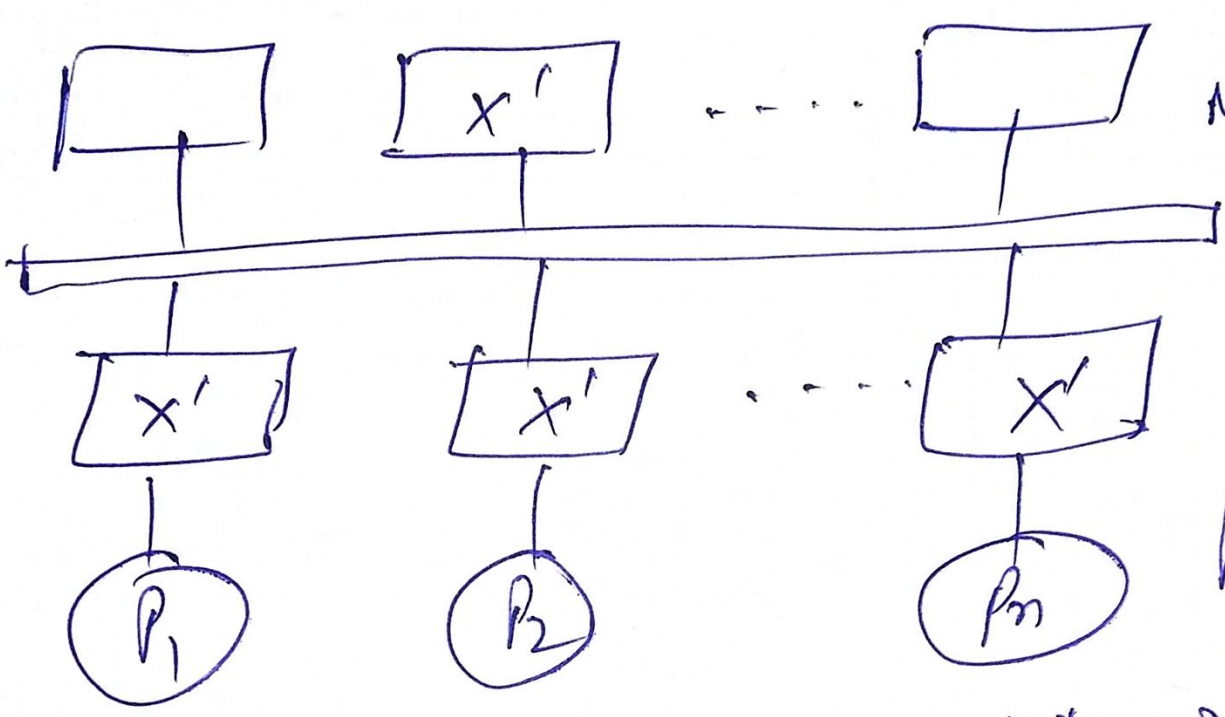
Snoopy Bus Protocols (b)



(b) After a write invalidate operation by P_1

WRITE-INVALIDATE

Snoopy Bus Protocols (c)



(c) After a write update operation by P_1

WRITE-UPDATE