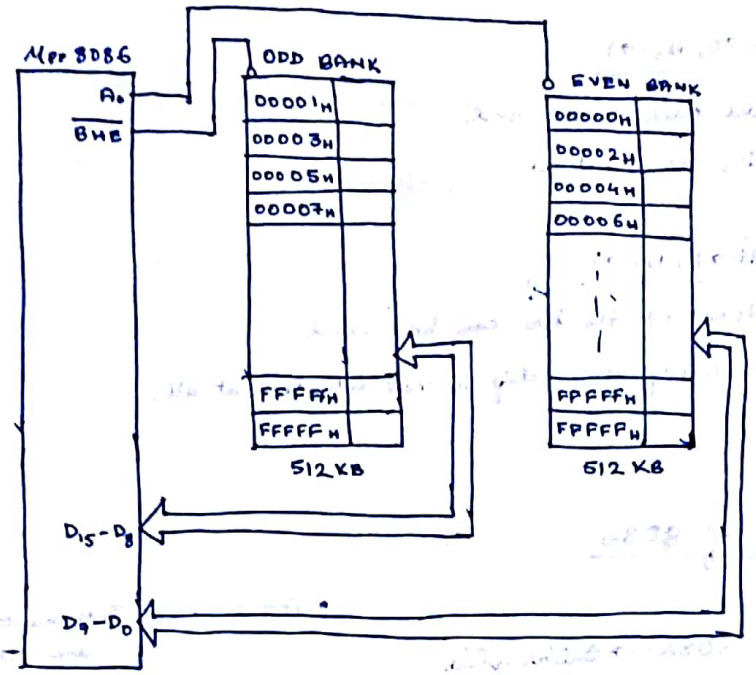
Odd-Even Memory Banks

SELECTION



• BHE → Bus High Enable

• Describe how the Odd and Even Banks are Selected.
— Explain the four States

$\overline{BHE}$	A_0	
0	0	→ 16 bit data $D_{15}-D_0$
0	1	→ 8 bit (Higher) D_8-D_{15}
1	0	→ 8 bit (Lower) D_0-D_7
1	1	→ Memory data transfer is disabled

2^{20} → 1 MB Memory

= 1024 KB Memory

= 512 KB ODD
+
512 KB EVEN

$C0000_H$ → EVEN
$C0001_H$ → ODD

MOV CX, $[1000_H]$ → 2 [1000] → CL (Uses D_7-D_0) — EVEN BANK
[1001] → CH (Uses $D_{15}-D_8$) — ODD BANK

• BHE indicates that the higher byte is enabled.

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$\overline{BHE} \rightarrow 1$, $A_0 \rightarrow 0$

- When A_0 is low, Even Bank is selected.

If $\overline{BHE} = 1$, Odd Bank is not Selected.

∴ bits $D_{15} - D_8$ are disabled.

- $\overline{BHE} \rightarrow 0$, $A_0 \rightarrow 1$

Odd Bank to be used.

$D_{15} - D_8$ enabled.

- $\overline{BHE} \rightarrow 1$, $A_0 \rightarrow 1$

None of the bus can be used.

∴ basically the chip is not selected at all.

Interrupt of 8086

- Total 256 Interrupts are there.

available on D_9 bit ←

IF → 1 8086 → Interrupted

0 8086 → Non-interrupted

STI, CLI } Used to set or reset the IF.

reset → Non-interrupted

INTR → Interrupt Request Line

- TRAP Flag available on D_8.

- On the 1st stack content, TRAP and INTR content will be stored.

CS	IP (Instruction Pointer)	Line #01
C000	1001	MOV .....

↓

C1001H

Priority

type

- Interrupt 00_H
  - → Divided by 00_H
- Type 01_H → Single Step Execution } ①
- Type 02_H → NMI (Non-Maskable Interrupt) } ②
- Type 03_H → INT 00 – FF H } ③
- Type 04 → Overflow [Overflow flag is set, if after processing two +ve data we get -ve output, or after processing two -ve data we get +ve output]

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