Subject Name: Computer Architecture
Paper Code: CSEN 2203

Pages and Chapter portions of Books for your reference

Teaching Status as on 15/2/2017

Introduction: Review of basic computer architecture; Measuring and reporting performance,
Amdahl's Law & Gustafson's Law.

Pipelining:

1) Basic concepts, Instruction and arithmetic pipeline –
   Hwang and Briggs : Chapter 3 pages 145 to 156,
   3.2.2-Arithmetic Pipeline example page 170 – 172

2) Scheduling in Pipeline
   a. Hwang and Briggs: 3.3.5 Job Sequencing and Collision Prevention
   b. Hwang : Scanned portion already mailed to you.

3) Data hazards, control hazards and structural hazards, techniques for handling hazards.
   Hwang and Briggs : 3.3.4 page 200 -203 Hazard detection and Resolution
   Hwang:- Branch Prediction page 293,
   Delayed branch with code motion into a delayed slot
   page 296 Example 6.8

Hierarchical memory technology:
Inclusion, Coherence and locality properties; Cache memory organizations, techniques for reducing cache misses; Virtual memory organization, mapping and management techniques, memory replacement policies.

Instruction-level parallelism:

1) Basic concepts
   i. Hwang page10 – page12, Flynn's Classification,
   ii. Hwang page14 – page16 System Attributes to performance
   iii. Hwang page 19 – 20 Loosely Coupled,page 22-32
   iv. Tightly Coupled Systems-Hwang and Briggs page461
   v.
2) , Array processor architectures
   i. Hwang and Briggs Chapter 5 pages 325 to 332 (with Example 5.1 and Example 5.2 of page 330)
3) vector processors
   Hwang and Briggs 3.4 page 212 to 218
   3.4.3 pages 226 to 229 Pipelined Vector Processing Methods
   Page 310 Chaining
   Hwang Chapter 8 – pages 403 to 407,
   Page 408, 8.1.2 Vector Operand Specification ,

Pages437-441, 8.3.2 Vector loops, Strip-mining And Chaining
Page 185 Figure 4.15 Scalar Pipeline Execution vs Vector Pipeline Execution

4) Superscalar processor architectures
   a. Hwang pages 177-178 , 4.2.1,Chapter 6 pages 310 – 311,

5) Superpipelined processor architectures
   i. Hwang pages 312-318
6) VLIW processor architectures
   a. Hwang page 182 to 184 .

Interconnection networks:
Introduction:
Hwang pages 24- 32

Crossbar, Delta, Omega, Shuffle-Exchange, Banyan , Hypercube, Butterfly Networks.

Multiprocessor architecture:
Introduction Hwang pages 19 - 25

Taxonomy of parallel architectures; Centralized shared- memory architecture: synchronization, memory consistency; Distributed shared-memory architecture. Cluster computers.
Non von Neumann architectures:
Data flow computers, RISC architectures, Systolic architectures.
References:
1) **Kai Hwang:** Advanced Computer Architecture – Parallelism, etc.
2) **Hennessey & Patterson :** Computer Architecture – A Quantitative Approach
3) **Hamacher et el:** Computer Organization (5th Ed) & above
4) Kai Hwang & Briggs: Computer Architecture & Parallel Processing