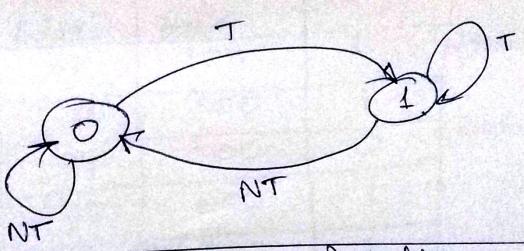
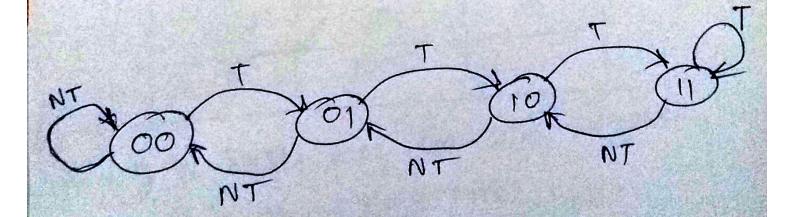
## 1-läet Branch Prediction



2-lock foranch frediction



Branch History Buffer 1-leit Branch Posdiction Branch Target Tuelle Addr Addr. (Branch Takey) 100 000 200 129 001 (Possel Not Take) 300 010 34 600 75 011 700 100 100 800 261 101 900 518 110 1000 15 111

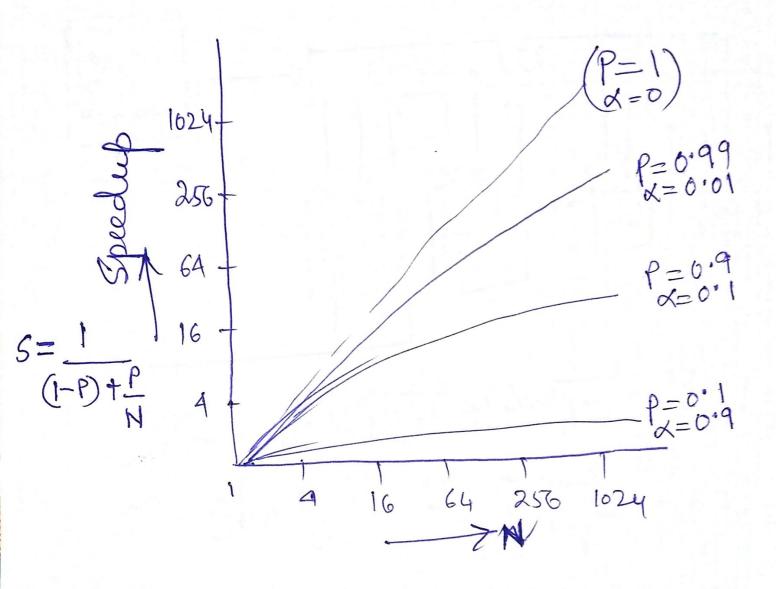
Sire of the beeffer may bee 256 or 1024, PC=100. Let Durtally -..0001100100 32-led Addr = 3-loits = 100. Least Inquificant in 5th row of BHB. 50, Boarch to be fallen 50, it matches Prediction Bil =1 50 Prediction PG = 700

Scheduling Branch Delay Slots From Before Branch intronction add P, 72, 83 Delay Slot. becomes begz rz, L add ri, rz, rz

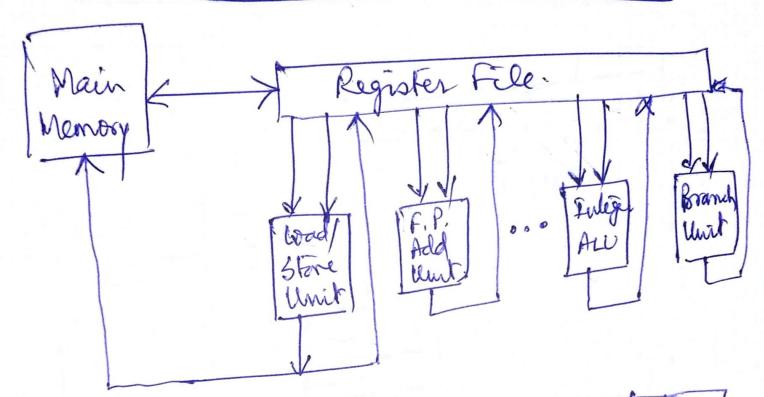
From Boanch Target 5wb 74, 75, 7647 instruction. add 71,72,73 begz 71, L delay Slot. 1 becomes instruction 4 add 1, 12, 83 begz og, L-Toub 84,85,86.

(c) from fall Through add 51, 52, 53 Deg 2 To L Sub 84, 55, 76. becomes add 1, 12, 73 beg 2 81, L L. Sub 14, 85,76 &

## Amdahl's law



## VLIN Architecture



Load Store FP Add FP Wilhpry



A typical VLIW processor with degree m = 3.

in sharing of Cache Inconsis Pency Writable data Processor P. Caches [X] shared Winte Back Write Through Before updale (Inconsorbency between C1 and C2). Dulonorotaury leefween Cy & Cz) Inconsistency after Process Mégration

TX'N IX Cacho X ( write Back) (Write through)
from P2 to P, poces nigrales from P, to Pr shared variable

Inconsistency due to 10 operations bypasong the cache Memory Deut But Memory (Input) Memory ID ( Winte Back) (Write though) In unsidely Inonostema beteveen behe I am The shared menrooy occurs.

A possible Solution COP, Shared meuron

Snoopy Bono Roslocols (a) --- (X) Caches X Pn Brocesonss. (P2) (a) Consistent copies of block X are in shared menory, and three processor caches.

Sucopy Bors Bolocols (6) Shared aremosy Bus

| I | Caches
| Paper Ancesons Aflir a surite imalidate Speration ley P,

WRITE-LNVALUSATE

Snosby Bus Portocols (e) JX -- · · [x] Houses After a white appointe operation lley P

WRITE - UPDATE