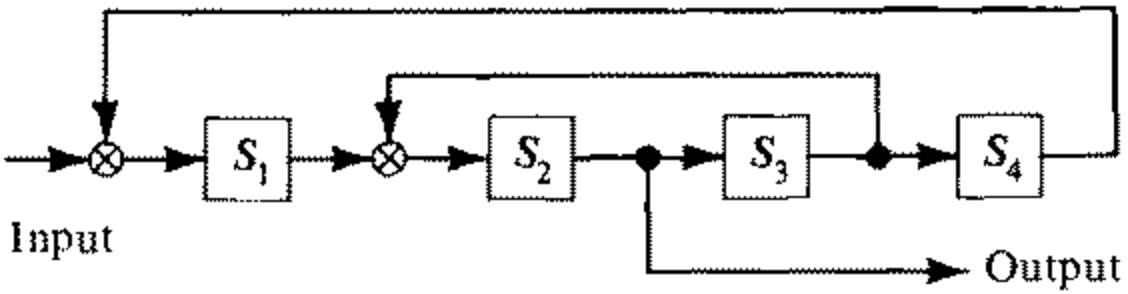
Non-linear Pipeline Collision free Scheduling

3.9 Consider the following pipelined processor with four stages. All successor stages after each s must be used in successive clock periods.



Answer the following questions associated with using this pipeline with an *evaluation time* o pipeline clock periods.

(*a*) Write out the reservation table for this pipeline with six columns and four rows.
(*b*) List the set of forbidden latencies between task initiations.
(*c*) Show the initial collision vector.
(*d*) Draw the state diagram which shows all the possible latency cycles.
(*e*) List all the simple cycles from the state diagram.
(*f*) List all the greedy cycles from the state diagram.
(*g*) What is the value of the minimal average latency (MAL)?
(*h*) Indicate the minimum constant latency cycle for this pipeline.
(*i*) What is the maximal throughput of this pipeline?