Sem V | ETRX | EXTC | IT | Instrumentation

Mumbai – 2017

VIVA QUESTIONS

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8051 Based Questions

Examiner
How many pins does 8051 have?
Q: 1

You
8051 is a 40 pin IC.

Examiner
8051 Address Bus?
Q: 2

You
8051 has a 16-bit address bus.

Examiner
8051 Data Bus and ALU?
Q: 3

You
8051 has an 8-bit data bus and an 8-bit ALU.
This means it can transfer 8-bits in one cycle and also operate on 8 bits in 1 cycle. Therefore 8051 is called an 8-bit microcontroller.

Examiner
Explain PC of 8051?
Q: 4

You
PC – Program Counter, is a 16-bit register. It contains address of the next instruction. It gets incremented as soon as an instruction is fetched.

Examiner
Explain SP and Stack of 8051?
Q: 5

You
SP – Stack Pointer, is an 8-bit register. It contains address of the top of stack. Stack is a data structure present in the Internal RAM. It operates in LIFO manner. During a Push, SP gets incremented and during a Pop, SP gets decremented. Default Value of SP is 07H. On the first push, Sp will be come 08H, and then data will be stored. Hence Bank1 will not be affected!

Examiner
What is the difference between a μP and a microcontroller ?

You
A μP is just a processor. It needs external RAM, ROM, I/O etc.
A μC is self sufficient. It has an internal Processor, RAM, ROM, I/O ports, Timers etc. It's basically a one chip computer, hence gives a compact ckt.

Examiner
How many general purpose registers does 8051 have?
Q: 7

You
8051 has 32 GPRs. They are divided into 4 banks, each having 8 registers, R0… R7.

Internal Examiner Joins the Viva!

Internal Examiner ~ Acche Din aayenge ;-)
Why are registers divided into banks?
Q: 8

You ~ Bharat Sir's Student
To reduce the number of o
Each instruction needs a d
register names, there will
number of opcodes. Hence the registers are divided into banks. This still gives us 32 registers, but uses only 8 opcodes, as there are only 8 register names!

Internal Examiner~ Acche Din aayenge ;-)
Which is the default register bank? How do you change banks?
Q: 9

You ~ Bharat Sir's Student
Bank 0 is the default register bank.
We can change banks using RS1 and RS0 of PSW register.
(Show table and examples from our notes)

Internal Examiner ~ Acche Din aayenge ;-)
What is the use of RxD and TxD?
Q: 10

You ~ Bharat Sir's Student
Used for Serial Communication (Bit by Bit).
Serial communication is slow but is cheaper so is preferred for long distance communication.

Internal Examiner ~ Acche Din aayenge ;-)
What is the crystal frequency of 8051?
Q: 11

You ~ Bharat Sir's Student
8051 is connected with a crystal of 12 MHz.
For Serial communication applications, we use a crystal of 11.0592 MHz to produce the standard baud rates.

Internal Examiner ~ Acche Din aayenge ;-)
Explain Power on Reset Signal?
Q: 12

You ~ Bharat Sir's Student
Power on Reset is used to activate the reset signal when 8051 is powered ON. On reset, PC becomes 0000H, That's the reset vector address. From here the BIOS program is executed!

Internal Examiner ~ Acche Din aayenge ;-)
How many I/O ports does 8051 have?
Q: 13

You ~ Bharat Sir's Student
8051 has 4, 8-bit I/O ports: P0, P1, P2, P3.

Internal Examiner ~ Acche Din aayenge ;-)
Explain multiplexing in 8051?
Q: 14

You ~ Bharat Sir's Student
Multiplexing is done to reduce the number of lines.
A0-A7 and D0-D7 are multiplexed, to form AD0-AD7.
ALE is used to identify whether the bus carries address or data.
If ALE = 1, bus carries address else data.

External Examiner
What are the alternate functions of the ports?
Q: 15

You
P0: Multiplexed address/ Data Bus (AD7-AD0).
P1: None – Used only as a port.
P2: Higher order address bus (A15-A8).
P3: Serial Port (RxD and TxD), Interrupts (INT0#, INT1#), Timer Clk inputs (T0,T1) and control Signals (WR# and RD#)

Internal Examiner
What is the role of EA#
Q: 16

You
It decides whether the first 4 KB of program memory space (0000H… 0FFFH) will be assigned to internal ROM or External ROM.
If $\overline{EA}$ = 0, the External ROM begins from 0000H.
In this case the Internal ROM is discarded.
8051 now uses only External ROM.
If $\overline{EA}$ = 1, the External ROM begins from 1000H.
In this case the Internal ROM is used.
It occupies the space 0000H… 0FFFH. Call: 9820408217 for doubts!

External Examiner
What is the role of PSEN#
Q: 17

You
8051 has a 16-bit address bus (A15 – A0).
This should allow 8051 to access 64 KB of external Memory as 2^{16} = 64 KB.
But, 8051 can access 64 KB of External ROM and 64 KB of External RAM, making a total of 128 KB. Both have the same address range 0000H to FFFFH.
There are separate control signals for External RAM and External ROM.
$\overline{RD}$ and $\overline{WR}$ are control signals for External RAM.
$\overline{PSEN}$ is the READ signal for External ROM.

Internal Examiner
8051 is based on Harvard Model… explain
Q: 18

You
If we use a common memory space for programs and data that's called Von Neuman Model. E.g.:: 8086. It can access 1 MB of memory. That's a combination of programs and data.
In Harvard model, we use separate memory spaces for programs and data. 8051 is based on Harvard Model.
There is is 64 KB Program Memory implemented using ROM, and 64KB data Memory implemented using RAM.

Internal Examiner
What is the use of timers?
Q: 19

You ~ Bharat Sir's Student
Timers are used to produce delay by the method of counting. Hence timers are also called counters.

External Examiner
Compare hardware and software Delay
Q: 20

You ~ Bharat Sir's Student
A Delay is a time gap between two events.
If we produce the delay using a dummy loop (usually NOP), then it is called a software delay.
If we use a Timer to produce it, then it is called a Hardware delay.
Software delays are cheaper as a timer is not needed.
Hardware delays are more efficient as they keep the processor free during the delay. The counting is done by the timer, so the processor is free to perform other operations.

Internal Examiner
Describe timers of 8051 in brief?
Q: 21

You ~ Bharat Sir's Student
8051 has two 16bit up counters called T0 and T1.
Having two timers means we can produce two delays simultaneously.
Being 16-bit timers, they count upto FFFFH.

External Examiner
Whats the different between timers and counters
Q: 22

You ~ Bharat Sir's Student
A Timer counts at a fixed freq using the internal clock ($f_{osc} \div 12$).
It is used to produce a delay as the counting period is predictable.
A counter counts at a external frequency applied at To and T1 pins.
This is used to count external events.
Plesae recollect the FACTORY example given in the class by Bharat sir.

Guess Who? #9820408217
Excellent answer… Keep it up ☺
All the best!

External Examiner
Explain all memories of 8051
Q: 23

You ~ Bharat Sir's Student
Internal RAM: size 128 bytes. Address range: 00H… 7FH
Internal ROM: size 4KB. Address range: 0000H… FFFFH
Extrenal RAM: size 64KB (max). Address range: 0000H… FFFFH
External ROM: If EA# = 0: size 64KB (max). Address range: 0000H… FFFFH
External ROM: If EA# = 1: size 60KB (max). Address range: 1000H… FFFFH

External Examiner
Explain PSW of 8051
Q: 24

You ~ Bharat Sir's Student
Please explain all flags with examples from class notes!
For help, visit: www.bharatacharyaeducation.com

Internal Examiner
How RAM can 8051 access, max?
Q: 25

You ~ Bharat Sir's Student
128 bytes of internal Ram PLUS 64 KB of external RAM

Internal Examiner
How RAM can 8051 access, max?
Q: 26

You ~ Bharat Sir's Student
Total of 64KB including internal and external ROM.

Internal Examiner
How many SFRs does 8051 have? Name ALL!
Q: 27

You
21. All 8 bit registers.
A,B: for programming.
PSW: Flag Register
SP: Stack Pointer
DPH and DPL: Data pointer
P0, P1, P2, P3: Port Latches
TCON, TMOD: For Timer Programming
TL0, TH0: Count for Timer 0
TL1, TH1: Count for Timer 1
SCON, SBUF: for serial port
IE, IP: for Interrupts
PCON: for Power Saving

Bharat Sir
Shabbaash! I was sure you could answer that ☺
Keep it up!

External Examiner
What addresses are allotted to the SFRs and why?
Q: 28

You ~ Bharat Sir's Student
SFRs are allotted addresses so that they don't further increase the number of opcodes.
They are allotted addresses 80H… FFH as they are completely unused. (Internal RAM ends at 7FH)
Of course this is not a coincidence… this is how the chip memory sizes were planned!

External Examiner
Explain structure of Internal RAM
Q: 29

You ~ Bharat Sir's Student
VERY IMPORTANT QUESTION.
Big Answer… Please refer #BharatSir Classroom and printed notes and give full diagram and answer! (www.bharatacharyaeducation.com)

External Examiner
How is overflow determined?
Q: 30

You ~ Bharat Sir's Student
Overflow is determined by Ex-Or of C7 and C6.
It basically means that the result is out of range for a signed number.
Range for 8-bit signed number (-80h…00h…+7Fh).

External Examiner
What does # signify in an instruction?
Q: 31

You ~ Bharat Sir's Student
A "#" next to a number, indicates that it is data, else it is treated as an address .
MOV A, #25H; A gets data 25H
MOV A, 25H; A gets contents of location 25H

External Examiner
What does an @ signify in an instruction?
Q: 32

You ~ Bharat Sir's Student
A "@" next to a number, indicates that it is giving an address, else it gives data .
MOV A, @R0; A gets contents of location pointed by R0
MOV A, R0; A gets data of R0

External Examiner
What is the difference between MOV, MOVX and MOVC?
Q: 33

You ~ Bharat Sir's Student
MOV if for Internal RAM.
MOVX is for External RAM.
MOVC is for ROM.
If the address if 1000H and more, it is for External ROM.
IF the address is less than 1000H, then depends on EA#
If EA# is 0, it is for External ROM, If EA# is 1, it is for Internal ROM

External Examiner
Where is the stack present and why?
Q: 34

You ~ Bharat Sir's Student
In 8051 the stack is present in the Internal RAM. That's because SP is an 8-bit register. It can only give an 8-bit address. Internal RAM is the only memory of 8051 with an 8-bit address. Hence stack is present in the Internal RAM.

External Examiner
Explain addressing modes of 8051 ?
Q: 35

You ~ Bharat Sir's Student
Please explain ALL in detail from the printed notes.

External Examiner
Why is Indexed addressing mode created for ROM?
Q: 36

You ~ Bharat Sir's Student
ROM is generally used for storing Programs and RAM for data.
But some permanent data like 7-seg codes are stored in ROM.
Such data is always stored in the form of Look Up Tables.
Indexing is the ideal way to access a look up table.
In MOC A, @ A + DPTR, we initialize DPTR as a pointer to the look up table and A as the index. Hence Index addressing mode is created for ROM.

External Examiner
How do you interchange the nibbles of a number?
Q: 37

You ~ Bharat Sir's Student
Rotate it 4 times in any one direction: RL A, RL A, RL A, RL A.

External Examiner
Where is ADDC used?
Q: 38

You ~ Bharat Sir's Student
To add 2 large numbers.
Lower Bytes are added using ADD, higher Bytes using ADDC.

External Examiner
Where is DA A used?
Q: 39

You ~ Bharat Sir's Student
To add two BCD numbers (Decimal Numbers). First enter the numbers, Add them, Perform DA A, by its adjustment logic, it gives the correct BCD answer.
Please show examples from classroom lecture or videos from www.bharatacharyaeducation.com.

External Examiner
MOV A, #25H, DA A;
Show the working of DA A in this example?
Q: 40

You ~ Bharat Sir's Student
Won't work. DA A stands for Dec Adjust "After Addition"!

External Examiner ~ somebody's gonna get a hurt tonight
What is the difference between 8051, 8031, 8751 and 89C51?
Q: 41

You ~ www.BharatAcharyaEducation.com
Intel 8051: 4KB Internal ROM.
Intel 8031: No Internal ROM.
Intel 8751: 4KB Internal EPROM.
ATMEGA 89C51: 4KB Internal FLASH ROM.

External Examiner
What is the use of various Logic Instructions?
Q: 42

You ~ Bharat Sir's Student
To make any bit 0: AND that bit with "0" & remaining bits with "1"
To make any bit 1: OR that bit with "1" & remaining bits with "0"
To complement a bit: XOR that bit with "1" & remaining bits with "0"

External Examiner
How do we perform NAND, NOR or XNOR?
Q: 43

You ~ Bharat Sir's Student
AND followed by NOT is a NAND.
OR followed by NOT is a NOR.
XOR followed by NOT is a XNOR.

External Examiner
What is the use of Rotates?
Q: 44

You ~ Bharat Sir's Student
They are used to determine the value of a bit. Rotate the register as many times, that the bit comes into carry flag. Checking Carry flag we can determine the value of any desired bit.

External Examiner
How do you find out if a number is +ve, -Ve, even or odd?
Q: 45

You ~ Bharat Sir's Student
+ve, -ve: Rotate left, check carry flag. Even, odd: Rotate right, check carry flag.

External Examiner
Can the binary number (1000 0011) can have two values?
Q: 46

You ~ Bharat Sir's Student
Yes. Depending upon whether we are working in signed or unsigned system. Unsigned: 83H. Signed: -7DH.

Bharat Sir
Excellent answer… Most students get this one wrong!
Keep it up!

External Examiner
Difference between:
MOV A, #25H
MOV A, 25H
MOV C, 25H
Q: 47

You ~ Bharat Sir's Student
A gets data 25H
A gets contents of byte location 25H
Carry Flag gets contents of bit location 25H

External Examiner
Perform (-25H) + (-35H). Show effect on Flags?
Q: 48

You ~ Bharat Sir's Student
Answer: -5AH.
Flags: Overflow = 0, AC = 1, PF = 0, CF = 1.
In case of doubts please refer #BharatSir classroom examples or simply watch the PSW video at: www.bharatacharyaeducation.com

External Examiner
Explain some bit operations of 8051
Q: 49

You ~ Bharat Sir's Student
SETB P0.0: Makes P0.0 ← 1
CLR P0.0: Makes P0.0 ← 0
CPL P0.0: Makes P0.0 ← Its complement

External Examiner
Explain the difference between SJMP, AJMP and LJMP
Q: 50

You ~ Bharat Sir's Student
Very long answer. Please refer printed notes.

External Examiner
What are Vectored and Non Vectored interrupts?
Q: 51

You ~ Bharat Sir's Student
Interrupts that have a Fixed ISR Address, it is called Vectored.
All interrupts of 8051 are vectored.
A non vectored interrupt does not have a fixed ISR address., like INTR of 8086.

External Examiner
How many interrupts does 8051 have?
Q: 52

You ~ Bharat Sir's Student
5 interrupts .
2 external interrupts, INT0# and INT1#
2 Timer overflow interrupts: Timer0 and Timer1
A common serial interrupt caused due to Ri or Ti.

External Examiner
What are their vector address?
Q: 53

You ~ Bharat Sir's Student
INT 0: 0003H.
Timer 0: 000BH.
INT 1: 0013H.
Timer 1: 001BH.
Serial Port: 0023H.
0000H is the reset vector address!

External Examiner
How do you indicate that you are using a timer or a counter?
Q: 54

You ~ Bharat Sir's Student
By the C/T# bit in TMOD register.
1: Counter; 0: Timer

External Examiner
What are the typical steps in timer programing?
Q: 55

You ~ Bharat Sir's Student
Choose the mode, Give the count, Start the timer, Wait for overflow, Clear corresponding flags.

External Examiner
What is the max count in each mode of timer?
Q: 56

You ~ Bharat Sir's Student
Mode 0: 13-bit ➔ 1FFFH
Mode 1: 16-bit ➔ FFFFH
Mode 2: 8-bit ➔ FFH
Mode 3: 8-bit ➔ FFH

External Examiner
What is the use of SMOD?
Q: 57

You ~ Bharat Sir's Student
SMOD is a bit present in PCON register.
It is used to double the baud rate for serial communication, in Modes 1, 2,3.

External Examiner
What .ASM file?
Q: 58

You ~ Bharat Sir's Student
It is an Assembly language file
The Assembler converts into .OBJ file, which is in machine language.
The Linker converts it into a .EXE file that can be executed..

External Examiner
What is the use of DB, DW directives?
Q: 59

You ~ Bharat Sir's Student
These are data types used for declaring variables.
DB: 8-bit. DW: 16-bit.

External Examiner
What is the use of "org" Directive?
Q: 60

You ~ Bharat Sir's Student
It is called Origin. It gives the starting address from where, the subsequent info will be loaded into memory.

External Examiner
What is the use of "equ" directive?
Q: 61

You ~ Bharat Sir's Student
It is used to define a constant. Pronounced as equate.

External Examiner
What is the difference between RET and RETI?
Q: 62

You ~ Bharat Sir's Student
RET is used for ordinary subroutines. It will simply Pop the return address from the stack and load it into PC.
RETI is sued for returning from ISRs.
It will not only Pop return address into PC, but also re-enable interrupts, which were disabled when 8051 starts an ISR.

External Examiner
Draw and Explain IE and IP SFRs
Q: 63

You ~ Bharat Sir's Student
Please refer Printed notes.
For detailed explanation on this topic, please see the 8051 Interrupts video at **www.BharatAcharyaEducation.com**

External Examiner
Draw and explain any one SFR?
Q: 64

You ~ Bharat Sir's Student
Please prepare all 7 SFR diagrams before going for Viva. PSW, TCON, TMOD, SCON, IE, IP, PCON, are all very important. One will most certainly be asked.

External Examiner
Give example of power down and idle modes?
Q: 65

You ~ Bharat Sir's Student
Phone screen going blank after around 30 secs: Idle mode
Calculator: Power down mode

External Examiner
What is the use of 9^{th} bit in modes 2,3 of serial communication?
Q: 66

You ~ Bharat Sir's Student
To decide between a broadcast or selective transmission in multiprocessor communication.
If 9^{th} bit = 1: broadcast (all receive)
If 9^{th} bit = 0; only those receivers with SM2 = 0 will receive.

External Examiner
Why is Mode 1,3 baud rate called variable baud rate?
Q: 67

You ~ Bharat Sir's Student
Because it is based on Timer 1 overflow rate which can be changed by changing the value of the count. For each different count we can produce a different baud rate

External Examiner
What is 8282/74373? Where is it used?
Q: 68

Bharat Sir's Student
It is an 8-bit latch. It is used to latch the address from the multiplexed address – data bus. It captures address when ALE is 1.

External Examiner
What is the preferred crystal frequency for serial communication applications?
Q: **69**

Bharat Sir's Student
11.0592 MHz.
This is so that we can produce the standard UART baud rates of 9600, 4800, 2400, and their derivatives.

External Examiner
What is the difference between synchronous and asynchronous communication?
Q: 70

You ~ Bharat Sir's Student
Synchronous: Common clock. Start Stop not needed.
Asynchronous: No Common clock. Start Stop needed.
Refer detailed explanation given in the class.

ARM Based Questions

External Examiner
Which implementation off ARM are we using?
Q: 71

You ~ Bharat Sir's Student
ARM7TDMI

External Examiner
What does ARM stand for?
Q: 72

You
Advanced RISC Machines

External Examiner
What does RISC stand for?
Q: 73

You
Reduced instruction set computers

External Examiner
Give some features of ARM7TDMI
Q: 74

You

- *32 bit Microcontroller.*
- *32 bit data bus*
- *32 bit address bus*
- *2^{32} = 4GB memory.*
- *32 bit instructions*
- *32 bit registers*
- *37 registers… 16 available at a time (R0… R15)*
  7 operating modes

External Examiner
Explain ARM7 Pipelining
Q: 75

You ~ Bharat Sir's Student
ARM 7 has a 3 stage pipeline: Fetch decode and execute

External Examiner
Explain triadic instructions?
Q: 76

You ~ Bharat Sir's Student
ARM has triadic instructions.
ADD R0, R1, R2; Here R0 ← R1 +R2

External Examiner
Whats the use of SP, LR and SPSR?
Q: 77

You ~ Bharat Sir's Student
SP gives address of top of stack
LR called Link Register, gives the return address to be put back into PC while returning to main program
SPSR is the saved value of CPSR form the main program

External Examiner
Whats the difference between IRQ and FIQ?
Q: 78

You ~ Bharat Sir's Student
IRQ is normal interrupt request.
FIQ is Fast Interrupt Request
FIQ gets serviced faster because, it uses a new set of registers from R8-R12.
This eliminated the need for storing and resting the values of these registers from the main program and hence saves time.

External Examiner
What is the full form of ARM7TDMI?
Q: 79

You ~ Bharat Sir's Student

ARM7: Family Name.
T: Includes Thumb Instruction set.
D: Allows hardware debugging of the circuit via JTAG interface.
M: Includes Long Multiply Instruction.
I: Includes embedded ICE Microcell for breakpoints and watch-points in program.

Bharat Sir ~ Winter is HERE.
Well done… Keep it up!
If it gets too much, just say "I DEMAND A TRIAL BY COMBAT"

External Examiner
Compare RISC and CISC
Q: 80

You ~ Bharat Sir's Student
Very important but very long ans. Too many points. Please refer printed notes

External Examiner
What is Thumb state? How does it improve code density
Q: 81

You ~ Bharat Sir's Student
In normal state, instructions are of 32 bits each.
In thumb state, instructions are 16-bits.
So we can store double the number of instructions in the same space, hence code density improves.

External Examiner
How many operating modes does Arm have? Explain briefly
Q: 82

You ~ Bharat Sir's Student
7 operating modes

- *User – Normal Programming Mode*
- *SYSTEM – Used by the user to invoke system functions*
- *Supervisor – Privileged Mode for executing BIOS and OS Kernel functions*
- *IRQ – Normal Interrupt Mode*
- *FIQ – Fast Interrupt Mode*
- *UND – Error mode when undefined instruction is encountered*
- *ABT – Abort when invalid location is being accessed typically due to low privilege*

External Examiner
What are the different types of Non – Volatile Memories?
Q: 83

You ~ Bharat Sir's Student
***ROM**: Read Only Memory. This is the original type of ROM. Cannot be written.*
***PROM**: Programmable ROM. Can be written but only once. Also called OTPROM.*
***EPROM**: Erasable PROM. Can be erased by exposure to UV rays.*
***EEPROM**: Electrically EPROM. Can be erased by applying higher voltage.*
***Flash ROM**. Special type of EEPROM. Allows block-wise erasure so erasure is faster.*

External Examiner
What are the different types of Volatile Memories?
Q: 84

You ~ Bharat Sir's Student
***RAM**: Random Access Memory. It is of two types.*
***SRAM**: Static RAM. Uses Flip-Flops to store data so works faster. Very Expensive.*
***DRAM**: Dynamic RAM. Uses capacitors to store data. Slower. Cheaper.*
***SDRAM**: Synchronous Dynamic RAM. Uses common clock with CPU to synchronize.*
***RDRAM**: Rambus RAM. Uses dedicated bus with CPU to transfer data..*

External Examiner
What memories are used in your mobile phone?
Q: 85

You ~ Bharat Sir's Student
It uses DRAM for primary memory, and Flash for secondary storage. Even the memory card is Flash ROM.

External Examiner
What memories are used in your computer?
Q: 86

You ~ Bharat Sir's Student
Primary Memory: DRAM ~ 4GB
Secondary Memory: Hard Disk ~ 1TB
Cache Memory: SRAM ~ 3MB
Portable Memory: CD – 700MB, DVD – 4.7GB. Pen Drives: Flash ROM of any size.