Syllabus 2nd Internal CSEN2203

Module 2:

Array and vector processors,SIMD-Hwang and Briggs –Chapter 5- upto page343,
Superscalar, Superpipelined and VLIW processor architectures.

Interconnection networks:
Crossbar, Delta, Omega, Shuffle-Exchange, Banyan , Hypercube, Butterfly Networks.
(Hwang and Briggs pages350-358,)

Module 3:

Measuring and reporting performance:
CPI,MIPS etc**.** Amdahl's Law & Gustafson's Law.

Hierarchical memory technology
Inclusion, Coherence and locality properties;
Cache memory organizations,
Cache Miss Penalty, Techniques for reducing cache misses;
Virtual memory organization, mapping and management techniques, memory replacement policies.

Multiprocessor architecture:
Taxonomy of parallel architectures;
Centralized shared- memory architecture,
Distributed shared-memory architecture.
Cluster computers.
Hwang Chapter 1.2,1.3-NUMA , cc-NUMA, UMA, COMA, UMA clusters,NORMA

Module 4:

Issues with Multiprocessor Architectures:
Synchronization,
memory consistency; Cache Coherence protocols (brief discussion only);

Non von Neumann architectures:
Data flow computers, RISC architectures, Systolic architectures.

References:

1) **Kai Hwang:** Advanced Computer Architecture – Parallelism, etc.
2) **Hennessey & Patterson :** Computer Architecture – A Quantitative Approach
3) **Hamacher et el:** Computer Organization (5th Ed) & above
4) Kai Hwang & Briggs: Computer Architecture & Parallel Processing