- In the following program, we are creating a square wave of 50% duty cycle on P1.5 bit. Timer 0 is used for generation of time delay. Calculate the frequency of square wave generated on P1.5.

(a square wave is generated which has equal high and low period.)

```
MOV TMOD, #01H   2T
L1: MOV TH0, #FFH   2T
    MOV TL0, #FFH   2T
    CPL P1.5 → Complement  1T
    CALL DELAY   2T
    SJMP L1 → Short Jump  2T
```

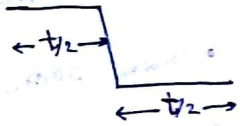
Time Delay

FFFF
↑ 16 T
FFFD

```
DELAY: SETB TR0   1T
L2: JNB TF0, L2   16T
    CLR TR0   1T
    CLR TF0   1T
    RET   2T
```

30 + (2) → First Line is out of Loop

Calculating Frequency:



$$t = (2 \times 30 + 2) \times 1.085\ \mu s = 67.27\ \mu s$$

$$\therefore f = \frac{1}{t} = 0.014\ MHz \quad (Ans)$$

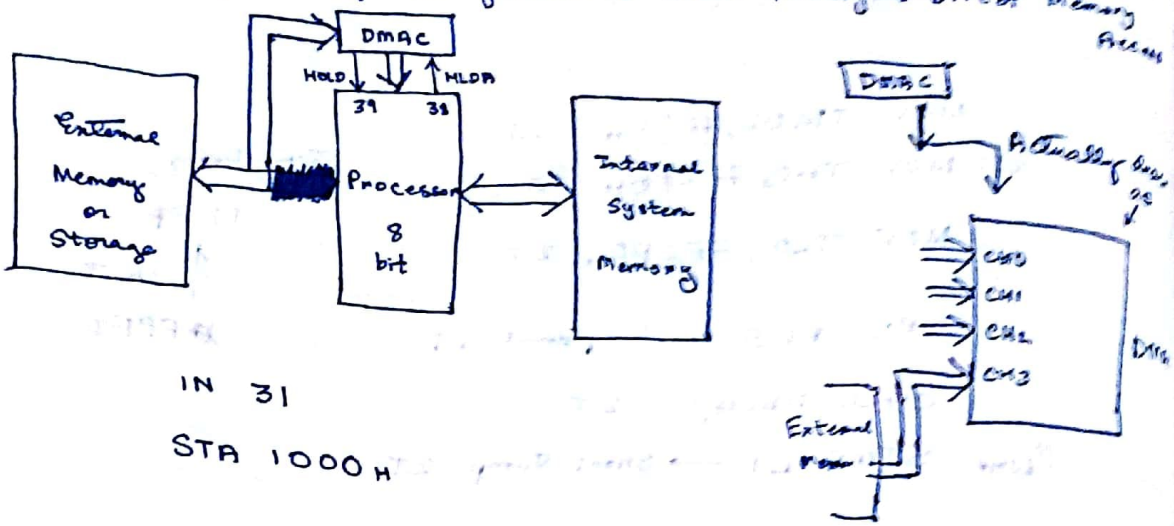
Interrupts

There are 6 interrupts. } Enough for Sem
What are they?
PIN no.

Questions
- Short Notes
- How data transfer is taking place bypassing the Mpr.

DMA (Direct Memory Access) 8257/8237

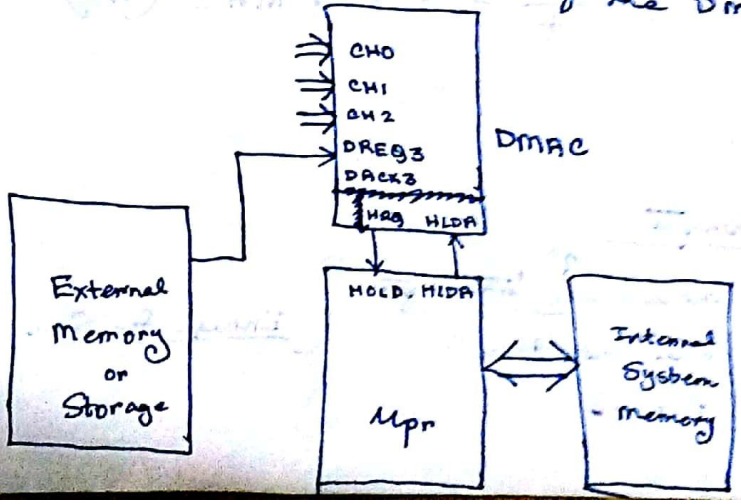
If we bypass the processor to access memory → Direct Memory Access



IN 31

STA 1000H

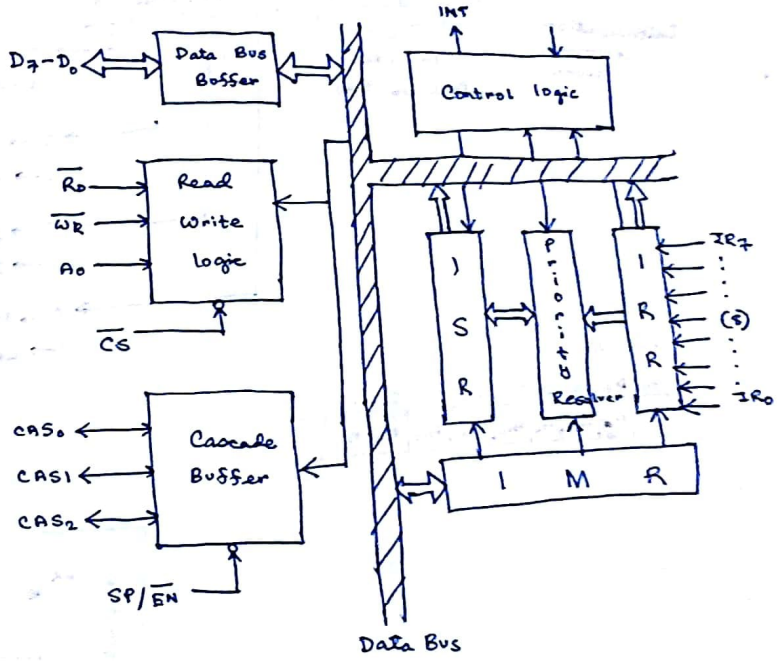
- DMAC will send a high instruction through the HOLD pin.
- The DMA processor requests the processor to perform DMA operation and for that it requires the bus control.
- The processor will then perform as a slave/peripheral to the DMA controller, until control is transfered back
- After receiving DMAC's request the processor acknowledges the request by sending a HLDA signal.
- Inside DMAC, there are 16 internal registers, each of 16 bit.
- 8257/8237 has 4 channels.
- Priorities are set to the channels by the DMAC.



- The DMA controller must be given the info that, from which initial location and how much of data is to be tranfered from the internal system memory. This data is available in the internal registers — MAR(16) and COUNT(16). There are 4 sets of MAR and COUNT registers, one for each channel.
- Other registers — MODEReg(16), Command Reg(16)
- MAR → Memory Address Register
  COUNT → Maximum Count

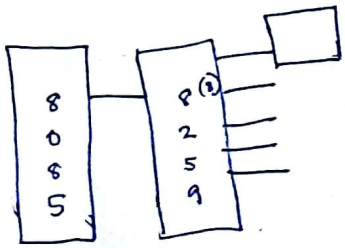
Programmable Interrupt Controller (PIC) 8259A → Peripheal to Processor

(Internal Work Procedure Required)
(For Short Notes on 8259A, ICW and OCW need not be described)



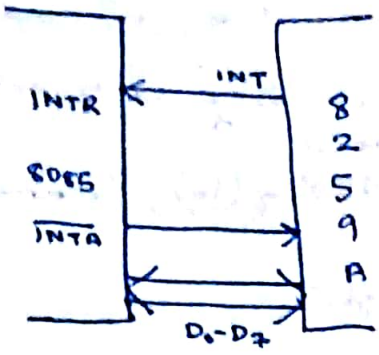
Block Diagram of 8259

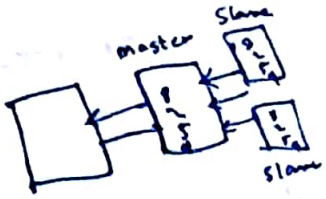
- IRR → Interrupt Request Register
- IMR → Interrupt Mask Register



ICW 1, ICW 2, ICW 3, ICW 4

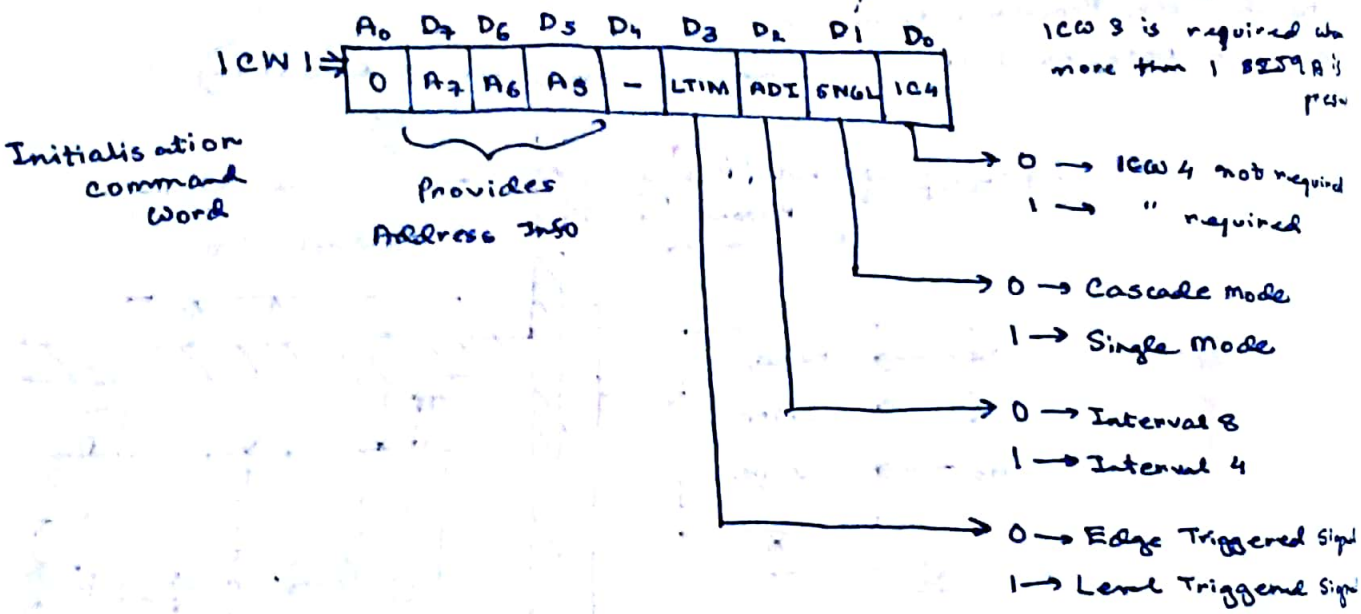
- 4 ICW
- 4 OCW



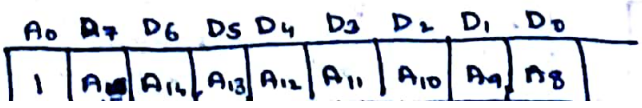


Set
using the
D2 bit (A
of IC

ICW 1, ICW 2



ICW 2



A7	A6	A5	A4	A3	A2	A1	A0
					1	1	0	0
9C$_H$ ⇒	1	0	0	1	1	0	1	0
98$_H$ ⇒	1	0	0	1	1	0	0	0
94$_H$ ⇒	1	0	0	1	0	1	0	0
90$_H$ ⇒	1	0	0	1	0	0	0	0

Set automatically using the D_2 bit (ADI) of ICW1

OCW 1,2,3 → Operational Command Word

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
M_7	M_6	M_5	M_4	M_3	M_2	M_1	M_0

→ Sent to IMR.

Port Address

80(icw1)

ICW1

0	0	1	1	0	0	1	1	0

7 6

MVI A,76H

OUT 80

MVI A,20H

OUT 81H

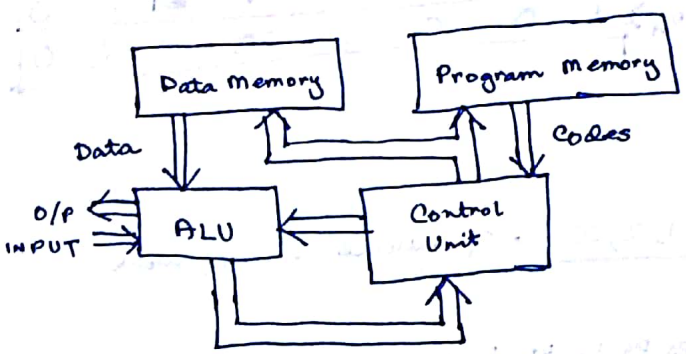
MVI A,( )

OUT (OCW1)

Microcontroller PIC 16F877

8 bit Mc

- Operand and opcode is present ~~together~~ separately.
- Follows ~~Von Neumann~~ Harvard Architecture
- ~~D~~ Faster



Harvard Architecture

- ALU → Accumulator Register (W Reg) (8 bit)
  → Flag/Status Register (PSW) (8 bit)

- Details not required of W and PSW, know the operations
- FSR Reg (8 bit) → Flag Selection Register
  ↓ Holds the Location
- INDF Reg (8 bit)
- 5 ports
- 35 instruction is maximum for all instructions here.

8251 → Prepare as Short Note