Subject Name: Computer Architecture

Paper Code: CSEN 2203

B.Tech 2nd Year 4th Semester SecA

Session 2016-2017

		9:00-9:55	9:55-10:50	10:50-11:45	Break	12:25:13:20	13:20-14:15	14:15-15:10	15:10-16:05	16:05-17:00	17:00-17:55
Mon	Gr-1	L /MATH2202 /JC /ICT304	L /CSEN2203 /AG /ICT304		L /HMTS2002 /NG, AL /CB514 (A+B)		L /MATH2201 /SD /ICT304	LAB /CSEN2213 /AG/ SHS+AS /ICT B10			
	Gr-2							T2 /PHYS2001 /AC /ICT305	LAB /MATH2212 /SD, SCK /ICT B11		
Tue	Gr-1	L /CSEN2201 /PBC /ICT304	T1 /CSEN2201 /PBC /ICT304	L /CSEN2203 /AG /ICT304		L /MATH2201 /SD /ICT304	L /PHYS2001 /AD /ICT304	T1 /PHYS2001 /HG /ICT304	LAB /HMTS2011 /ARD /CME005		
	Gr-2							LAB /CSEN2213 /AG/DS+ABS /ICT B11			
Wed	Gr-1	L /PHYS2001 /SS /ICT304	L /MATH2201 /SC /ICT304			L /MATH2202 /JC /ICT304					
	Gr-2										
Thu	Gr-1	L /CSEN2203 /AG /ICT304	L /CSEN2201 /SM /ICT304			LAB /MATH2212 /SD, SCK /ICT B11		Remedial			
	Gr-2					LAB /PHYS2011 /AD/CB108			LAB /HMTS2011 /ARD /A203		
Fri	Gr-1	LAB /PHYS2011 /AC /CB108				T1 /CSEN2203 /AG /ICT304	L /PHYS2001 /DM /ICT304	L /MATH2202 /AMB /ICT304			
	Gr-2	T2 /CSEN2201 /SM /ICT305	T2 /CSEN2203 /AG /ICT304			Remedial					

The even semester routine for the Session [illegible]-2017 will be **effective from 16th January 20[illegible]**

Books

1) **Kai Hwang:** Advanced Computer Architecture – Parallelism, etc.
2) **Hennessey & Patterson :** Computer Architecture – A Quantitative Approach
3) **Hamacher et el:** Computer Organization (5th Ed) & above
4) Kai Hwang & Briggs: Computer Architecture & Parallel Processing

Syllabus

Module 1: Introduction:

Review of basic computer architecture;

Pipelining: Basic concepts,

Instruction and arithmetic pipeline,

Scheduling in Pipeline;

Data hazards, control hazards and structural hazards, techniques for handling hazards.

Module 2:Instruction-level parallelism: Basic concepts,

Array and vector processors.

Superscalar, Superpipelined and VLIW processor architectures.

Interconnection networks:

Crossbar, Delta, Omega, Shuffle-Exchange, Banyan , Hypercube, Butterfly Networks.

Syllabus

Module 3:Measuring and reporting performance:

CPI,MIPS etc**.** Amdahl's Law & Gustafson's Law.

Hierarchical memory technology:

Inclusion, Coherence and locality properties;

Cache memory organizations, Techniques for reducing cache misses;

Virtual memory organization, mapping and management techniques, memory replacement policies.

Multiprocessor architecture: (6L)

Taxonomy of parallel architectures;

Centralized shared- memory architecture;

Distributed shared-memory architecture.

Cluster computers

Syllabus

Module 4:

Issues with Multiprocessor Architectures:

Synchronization, memory consistency; Cache Coherence protocols (brief discussion only);

Non von Neumann architectures:

Data flow computers, RISC architectures, Systolic architectures.

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Assessment

- 2 Internal Tests of 30 marks each – Average of them reduced to get ----------15 marks
- Attendance----------5 marks
- Quiz/assignments/

  Presentation on Architecture Related topics

  ----------10 marks

  Total-------30 marks

External Exam ----------70 marks