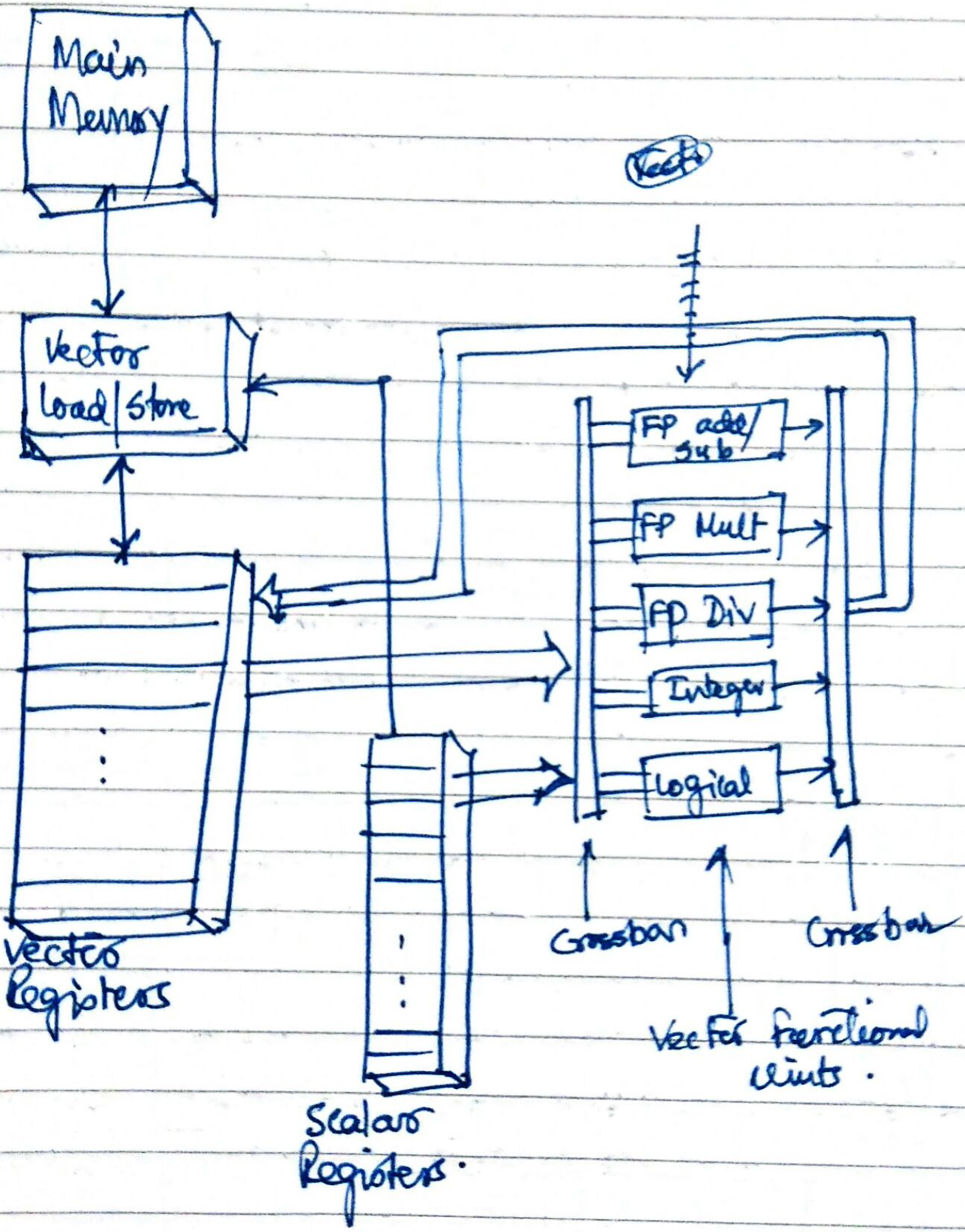
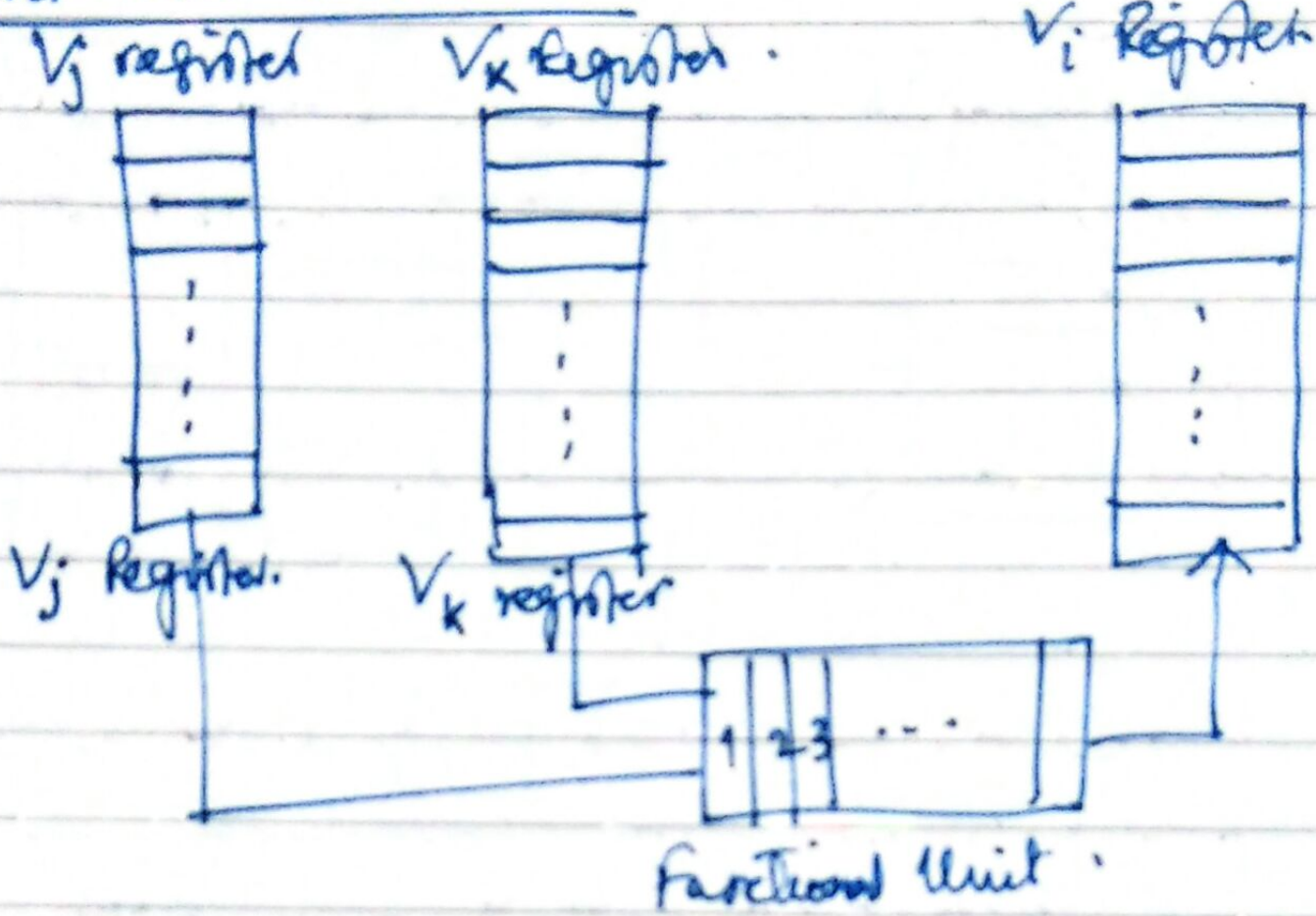
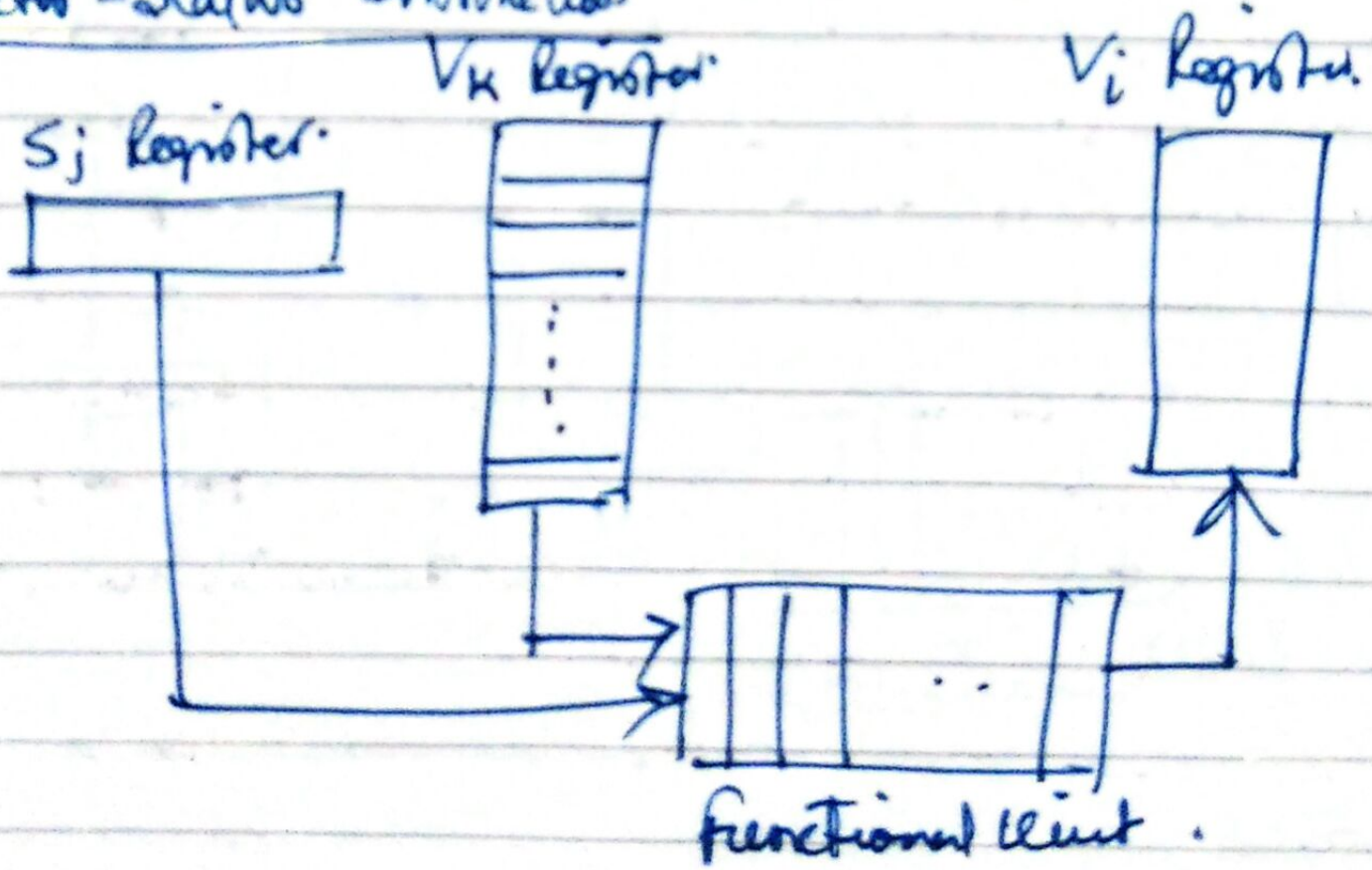


Basic Structure of a vector-register architecture

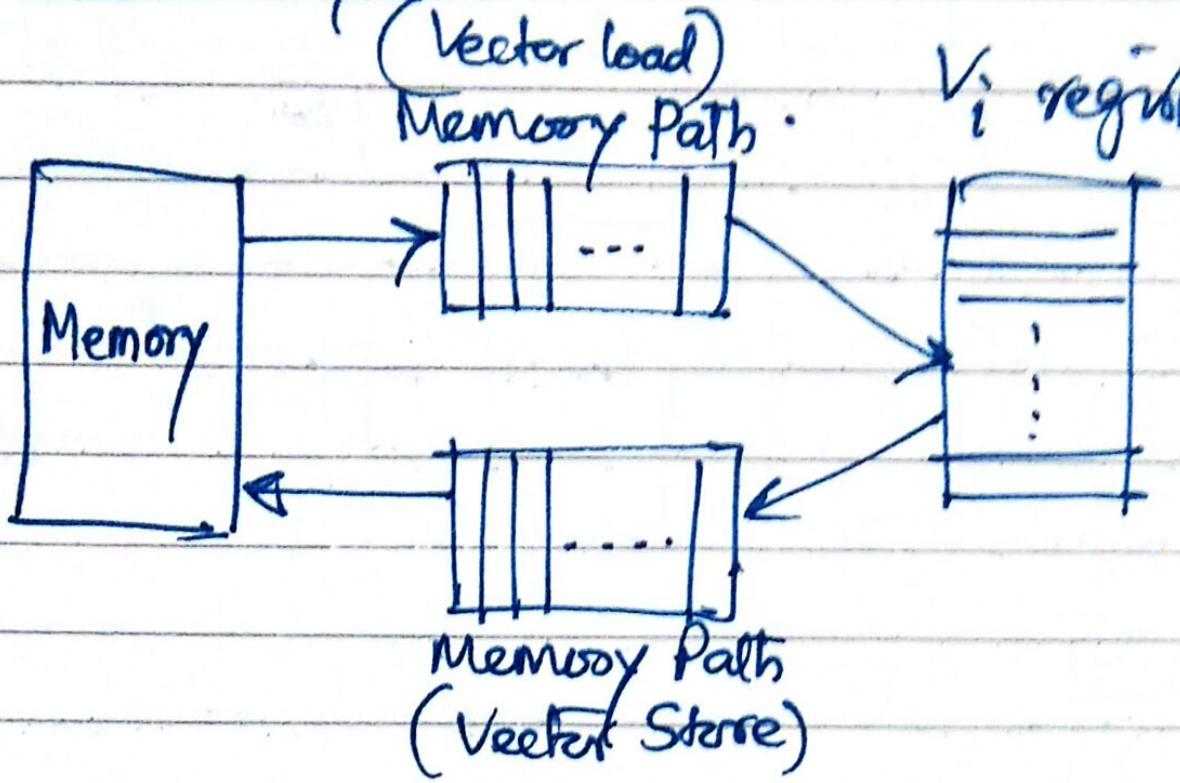
Vector-Vector Instruction



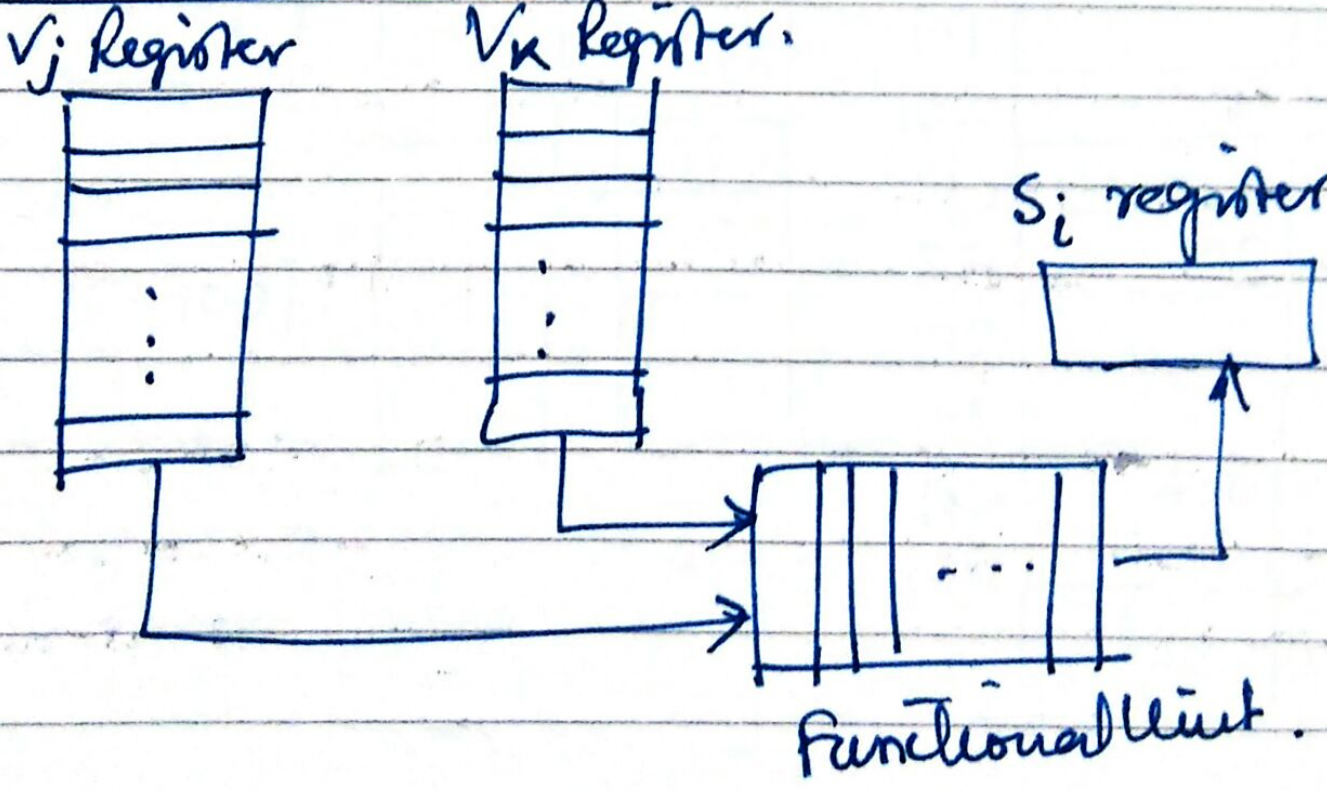
Vector-Scalar Instruction



Vector - memory instruction



Vector Reduction instruction



Gather Instruction

VL Register

4

A0

100

V0 Register

4
2
7
0

V1 Register

600 *
400 $
250 #
200 @

Memory

Addr	Content
100	@ 200
101	300
102	$ 400
103	500
104	* 600
105	700
106	100
107	# 250
108	350

Scatter Instruction

VL Register

4

A0

100

V0 Reg.

4
2
7
0

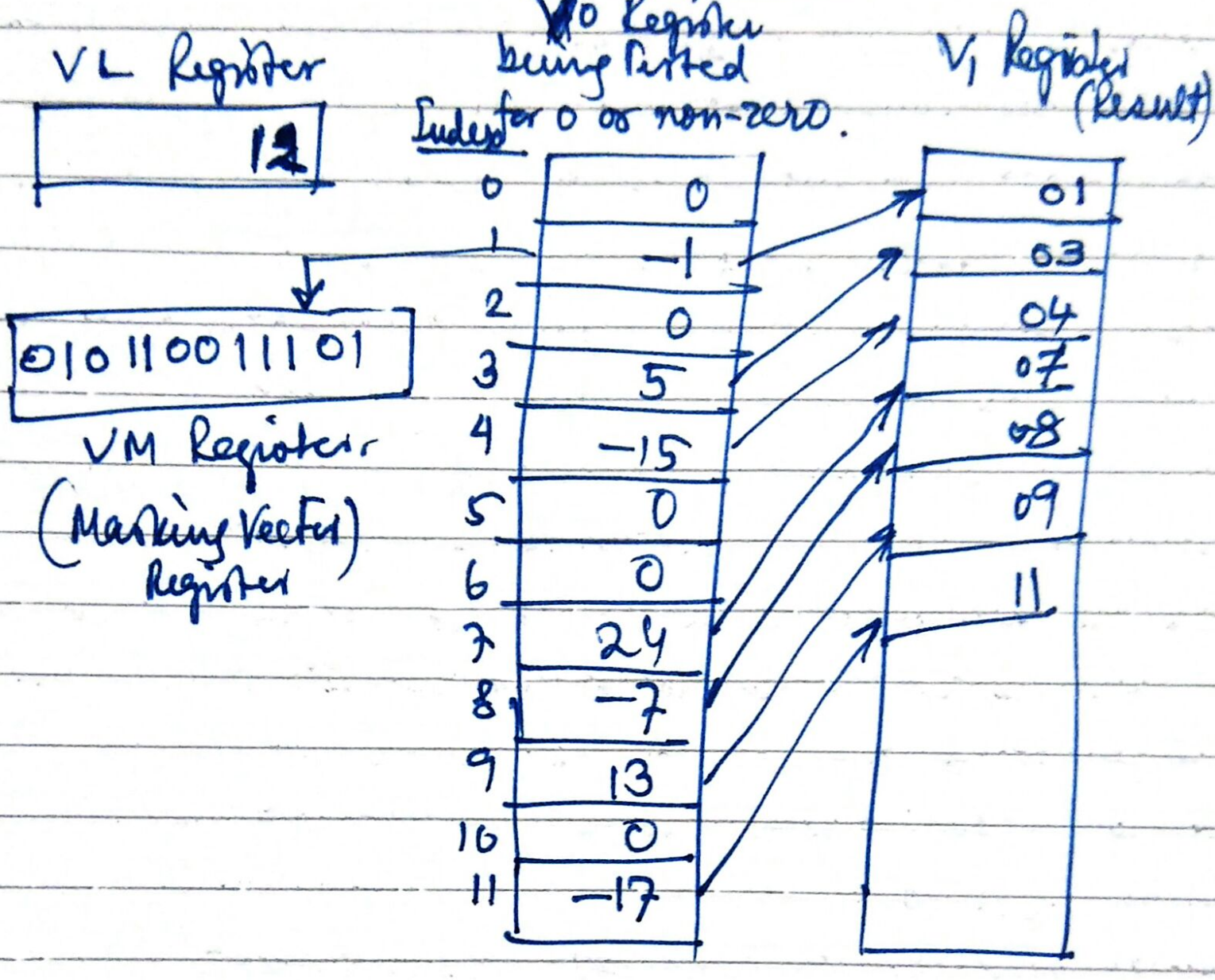
V1 Reg

200
300
401
500

Memory

100	500
101	
102	300
103	
104	200
105	
106	
107	400
108	

Masking Instructions



V_0 is tested for zero or non-zero element

VM → 0 indicates zero

1 indicates non-zero.

VL → Length of vector being tested.

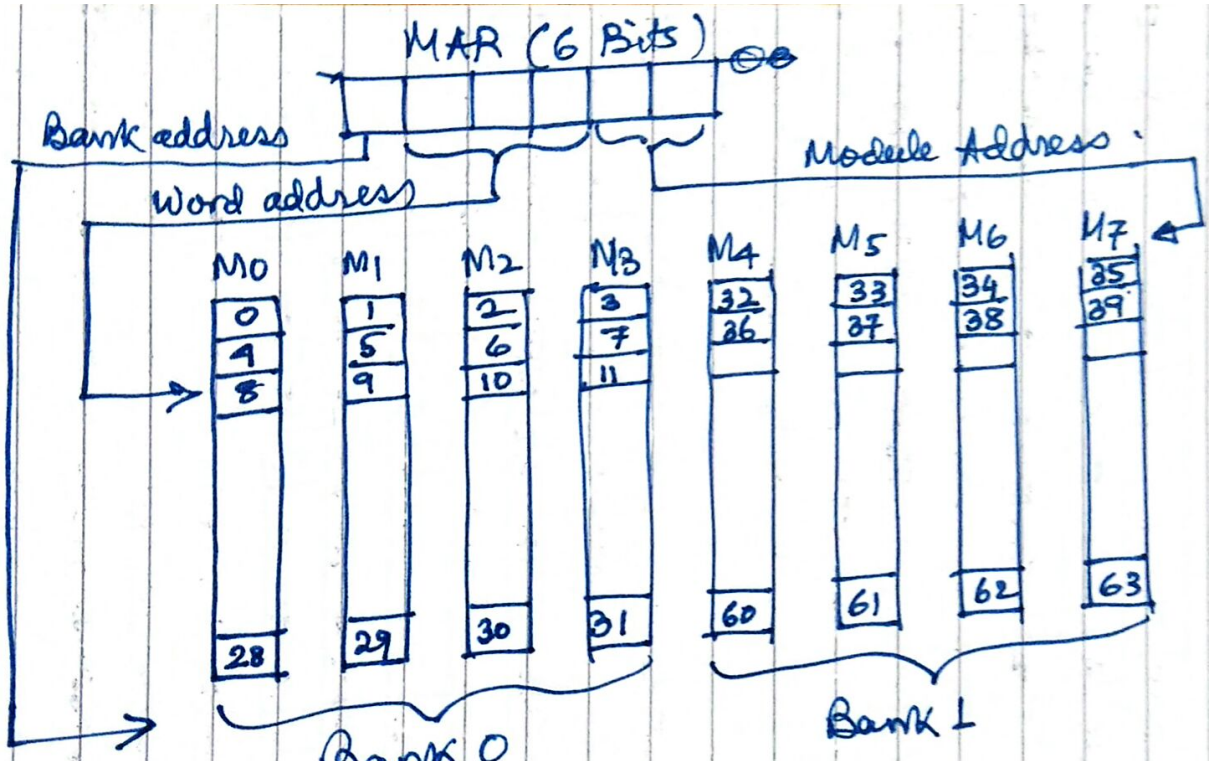
V_1 → Index of non-zero elements.

Vector Stride

$$\begin{bmatrix} 1 & 2 & 3 \\ 4 & 5 & 6 \\ 7 & 8 & 9 \end{bmatrix}$$

Row major order: 1 2 3 4 5 6 7 8 9

Column major order: 1 4 7 2 5 8 3 6 9.



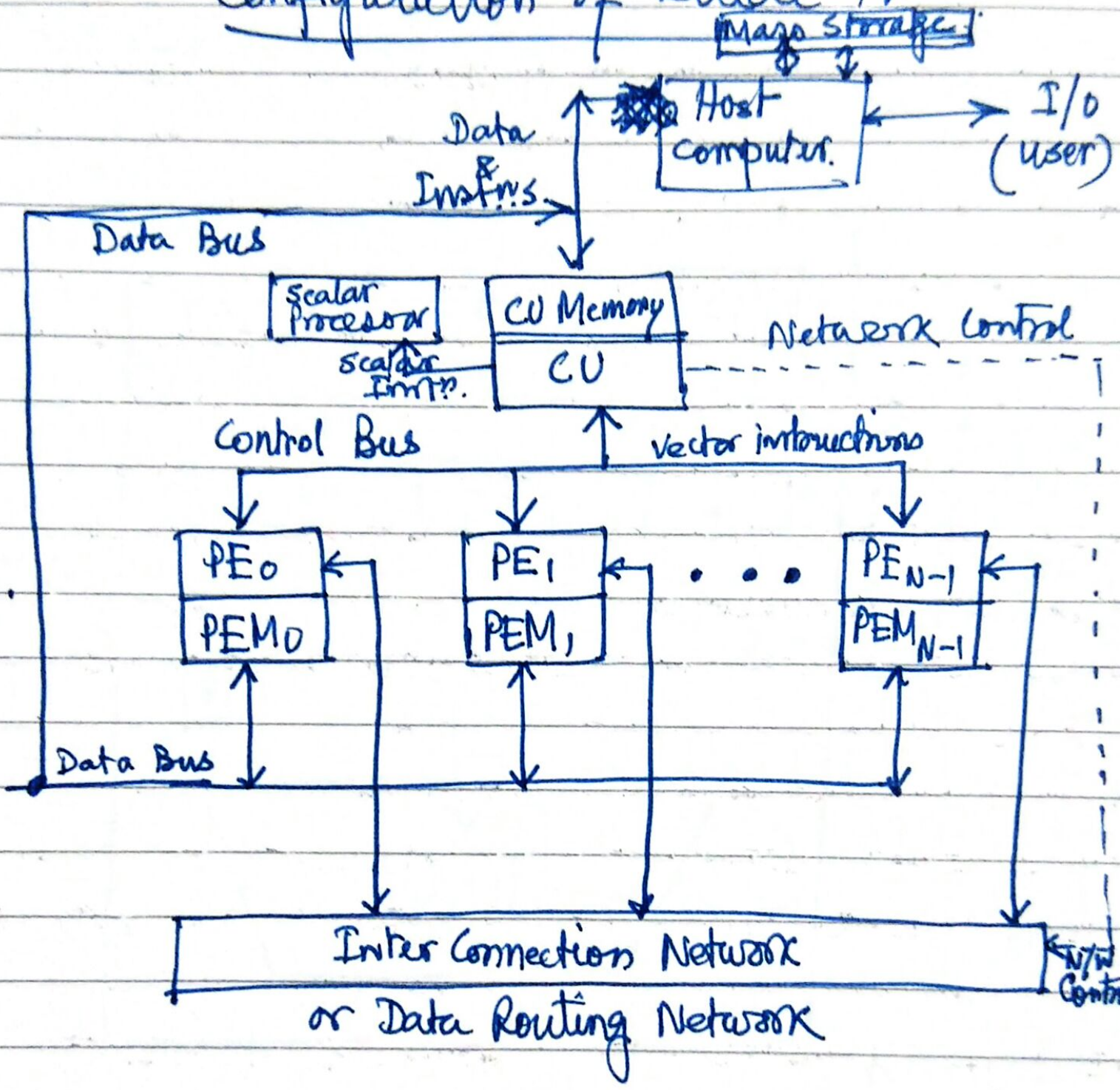
4-way interleaving within each memory bank

No. of banks = 2 (1 bit)
No. of modules per bank = 4 (2 bits)
No. of words per module = 8 (3 bits)
6 bits

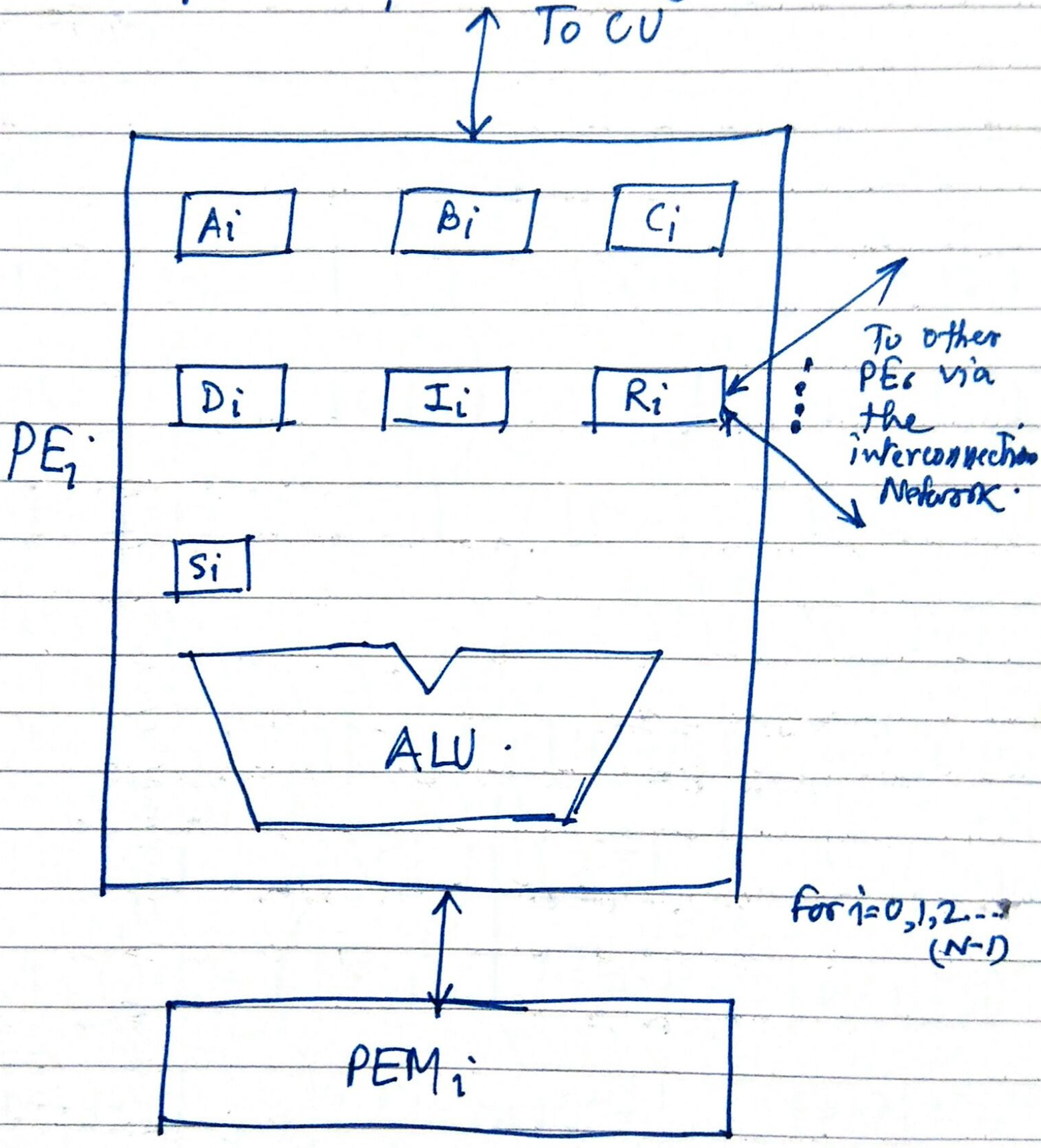
2-way interleaving within each memory bank.

No of banks = 4 (2 bits)
No of modules per bank = 2 (1 bit)
No of words per module = 8 (3 bits)
6 bits.

Configuration of Illiac IV



Components of a Processing Element



Calculation of $S(k) = \sum_{i=0}^{k} A_i$, $k = 0, 1, \ldots 7$

in an SIMD Machine