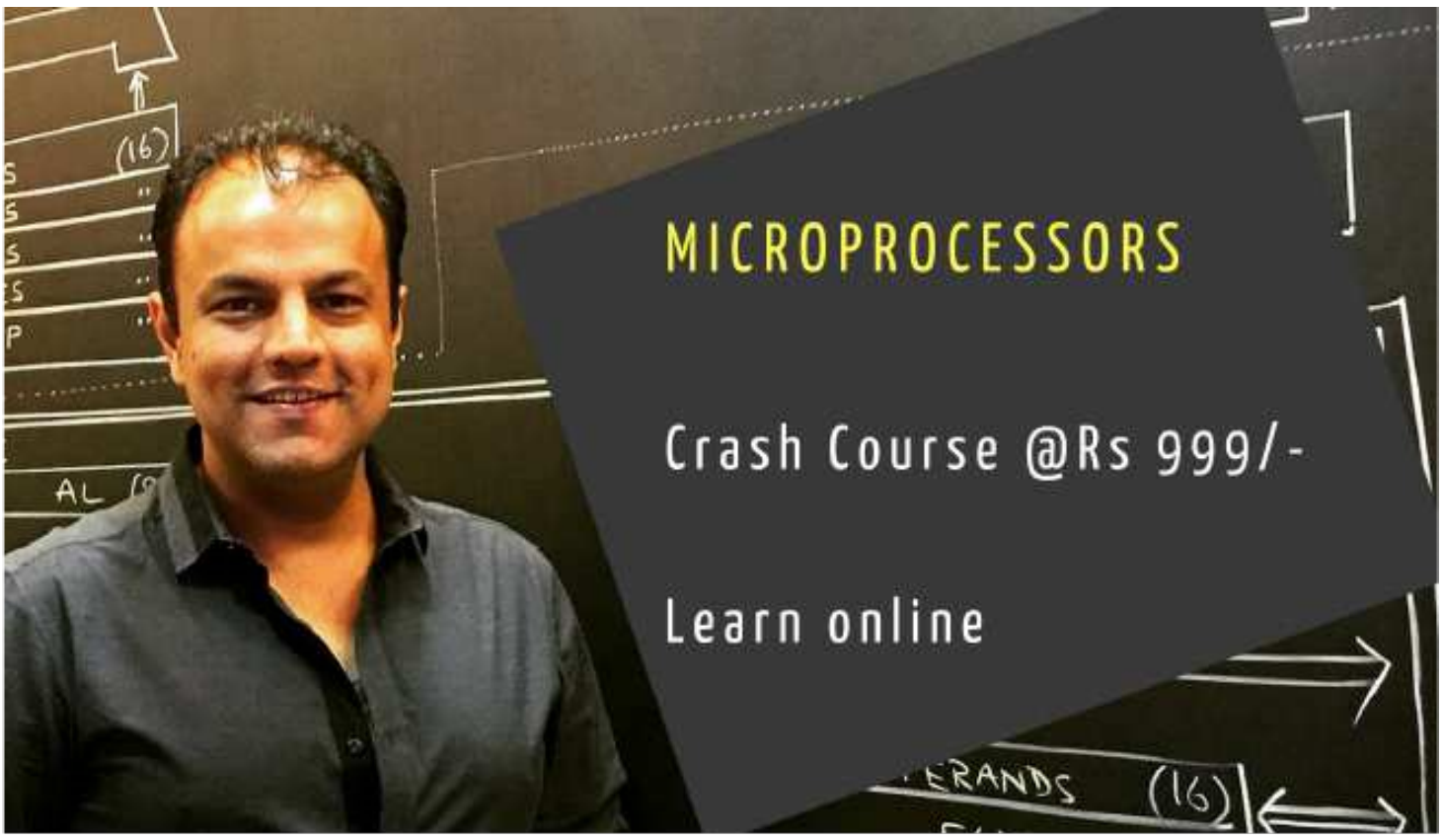
Mumbai University | 2018
Sem 5 | Computers | Extc | Microprocessors

Viva Questions – New Syllabus



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8086 Based Questions

External Examiner
How many pins does 8086 have?
Q: 1

You
8086 is a 40 pin IC.

Internal Examiner
8086 Address Bus and Memory?
Q: 2

You
8086 has a 20-bit address bus.
Therefore it can access 1 MB memory.

External Examiner
8086 Data Bus and ALU?
Q: 3

You
8086 has a 16-bit data bus and a 16-bit ALU.
This means it can transfer 16-bits in one cycle and also operate on 16-bits in 1 cycle. Therefore 8086 is called a 16-bit microprocessor.

Internal Examiner
Explain pipelining?
Q: 4

You
Fetching the next instruction while executing the current instruction is called pipelining. It saves time. It fails whenever there is a branch. The instruction fetched is no longer valid and hence has to be discarded.

Internal Examiner
Explain GPRs of 8086. Do they also have some special uses?
Q: 5

You ~ Bharat Sir's Student
There are 4 16-bit GPRs called AX, BX, CX & DX. They can also be used as 8 independent 8-bit GPRs: AL, AH; BL, BH…
They also have some special uses:
AX – Accumulator; BX – Memory pointer;
CX – Count Register; DX – 32-bit Accumulator along with AX.

External Examiner
How Many Segments are in 8086?
Q: 6

You ~ Bharat Sir's Student
There are 4 segments: Code, Stack, Data and Extra.

Internal Examiner
What is the max and min size of a segment and why?
Q: 7

You ~ Bharat Sir's Student
Max size: 64 KB. This is because offset addresses are of 16 bits. 16 Bytes. This is because formula of Physical address is segment address x 10h plus offset address. This puts a minimum gap of 10h bytes between two segments, which means 16 bytes.

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Good Going… Keep it up ☺
All the best!

External Examiner
What are the advantages of segmentation?
Q: 8

You ~ Bharat Sir's Student
We can access 1 MB memory using 16 bit addresses.
Moreover, the memory becomes more organized and overlaps are prevented between code, stack and data. www.BharatAcharyaEducation.com

External Examiner
Name Segment and offset registers?
What is the difference between SP and BP?
Q: 23 (Some questions were removed as SPARC is excluded from new syllabus)

You ~ Bharat Sir's Student
Segment registers: CS, SS, DS, ES. Offset Registers: IP, SP & BP, SI, DI.
SP and BP, both are for Stack Segment.
SP gives offset address of the top of stack. It is used for Push and Pop.
BP gives offset address of any location of the stack. It is used for random access of the stack.

External Examiner
Why is memory banking done?
How many banks are there?
Q: 24

You ~ Bharat Sir's Student
8086 has a 16-bit data bus.
Memory banking is done to access 16-bit data, which is stored in two consecutive locations. Hence memory is divided into 2 banks, Even bank and Odd Bank, also called Lower and Higher banks respectively.
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Internal Examiner
How are the memory banks selected?
Q: 25

You ~ Bharat Sir's Student
Draw A0 and BHE table from #BharatSir notes.

Internal Examiner
Can we access locations 24000H and 24001H simultaneously?
Q: 26

You ~ Bharat Sir's Student
Yes. By Ignoring A0, both these locations have the same bit pattern on A1-A19. Locations are selected on the basis of A1-A19, whereas A0 and BHE are used to select the banks.
Such data is called "Aligned Data".

Internal Examiner
Can we access locations 24001H and 24002H simultaneously?
Q: 27

You
No. Even after Ignoring A0, these two locations don't have the same address. So they will have to be accessed in two cycles.
Such data is called "Misaligned Data".

Bharat Sir
Shabbaash! I was sure you could answer that ☺
Keep it up!

External Examiner
Give advantages of 8086 ALU over 8085 ALU?
Q: 28

You ~ Bharat Sir's Student
8086 has a 16-bit ALU compared to 8085, which had an 8-bit ALU.
8086 ALU can perform MUL and DIV, which 8085 could not.
8086 ALU does not depend upon Accumulator for most of its operations, whereas 8085 had an Accumulator based ALU.

External Examiner
Explain Flag register of 8086?
Q: 29

You ~ Bharat Sir's Student
Please refer #BharatSir notes for diagram and answer.
Show examples from #BharatSir lecture notes if asked.

External Examiner
How is overflow determined?
Q: 30

You ~ Bharat Sir's Student
OF is determined by Ex-Or of C7 and C6.
It basically means that the result is out of range for a signed number.
Range for 8-bit signed number (-80h...00h...+7Fh).
Range for 16-bit signed number (-8000h...0000h...+7FFFh).

External Examiner
Why are DF, IF and TF called Control Flags?
Q: 31

You ~ Bharat Sir's Student
They are used by the programmer to control different operations.
DF: Controls direction for String Instructions.
IF: Controls enabling and disabling of interrupts.
TF: Controls Single Stepping used for debugging of programs.

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External Examiner
What is the size of the Prefetch queue? Why?
When is the Queue Refilled? Why?
Q: 32

You ~ Bharat Sir's Student
The Prefetch Queue is of 6-bytes as it is the max size of an instruction.
It is refilled whenever two bytes are empty as 8086 has a 16-bit data bus.

External Examiner
What is the advantage of using String Instructions?
Q: 33

You ~ Bharat Sir's Student
String instructions are fetched and decoded only once but executed repeatedly.
So they can perform large transfers very fast.

External Examiner
Difference between MUL and IMUL?
Q: 34

You ~ Bharat Sir's Student
MUL is used for unsigned numbers. IMUL for signed.

External Examiner
Difference between SUB and CMP?
Q: 35

You ~ Bharat Sir's Student
Both perform Subtraction. SUB will store the result and affect the flags.
CMP will not store the result. Will only affect the flags.

External Examiner
Where is TEST instruction used?
Q: 36

You ~ Bharat Sir's Student
To check a Semaphore in Multiprocessor Systems for principle of Mutual Exclusion.

External Examiner
How do you interchange the nibbles of a number?
Q: 37

You ~ Bharat Sir's Student
Rotate it 4 times: MOV CL, 04h, ROL AL, CL; This will Interchange nibbles of AL.

External Examiner
Where is ADC used?
Q: 38

You ~ Bharat Sir's Student
To add 2 large numbers.
Lower Bytes are added using ADD, higher Bytes using ADC.

External Examiner
Where is DAA used?
Q: 39

You ~ Bharat Sir's Student
To add two BCD numbers (Decimal Numbers). First enter the numbers, Add them, Perform DAA, by its adjustment logic, it gives the correct BCD answer.

External Examiner
MOV AL, 25H, DAA;
Show the working of DAA in this example?
Q: 40

You ~ Bharat Sir's Student
Won't work. DAA stands for Dec Adjust "After Addition"!

External Examiner
How can we make any bit of a register "0"?
Q: 41

You ~ Bharat Sir's Student
To make any bit 0: AND that bit with "0" & remaining bits with "1"
To make any bit 1: OR that bit with "1" & remaining bits with "0"
To complement a bit: XOR that bit with "1" & remaining bits with "0"

External Examiner
What is the use of various String Instructions?
Q: 42

You ~ Bharat Sir's Student
MOVS: To transfer a block as it is.
LODS & STOS: To Manipulate and Transfer a block
CMPS: To Compare two strings
SCAS: To Search for a number in a string.

External Examiner
Transfer block form 12345H to 54678H using MOVS?
Q: 43

You ~ Bharat Sir's Student
Initialize as follows: DS: 1000H, SI: 2345H, ES: 5000H & DI: 4678H

External Examiner
How do we perform NAND, NOR or XNOR?
Q: 44

You ~ Bharat Sir's Student
There are no direct instructions for these operations.
AND followed by NOT is a NAND.
OR followed by NOT is a NOR.
XOR followed by NOT is a XNOR.

External Examiner
When is CBW used?
Q: 45

You ~ Bharat Sir's Student
To expand an 8-bit signed number into 16 bits by retaining its MSB.

External Examiner
Can the binary number (1000 0011) can have two values?
Q: 46

You ~ Bharat Sir's Student
Yes. Depending upon whether we are working in signed or unsigned system. Unsigned: 83H. Signed: -7DH.

Bharat Sir ~ For Doubts Call Me @ 9820408217
Excellent answer… Most students get this one wrong!
Keep it up!

External Examiner
Difference between Control Flags and Status Flags?
Q: 47

You ~ Bharat Sir's Student
Status flags give status of Current result and are changed by the ALU.
Control flags are changed by the programmer & are used to control different operations.

External Examiner
Perform (-25H) + (-35H). Show effect on Flags?
Q: 48

You ~ Bharat Sir's Student
Answer: -5AH. Flags: OF = 0, SF = 1, ZF = 0, AC = 1, PF = 1, CF = 1.
In case of doubts please refer #BharatSir classroom examples.

External Examiner
What is the use of Control Flags?
Q: 49

You ~ Bharat Sir's Student
DF: Decides Direction for String Operations (0- decrement, 1-increment)
IF: Enables or Disables INTR interrupt (0 – disable, 1 - enable)
TF: Perform single stepping (1- perform, 0 – don't perform)

External Examiner
Why does IF affect only INTR interrupt?
Q: 50

You ~ Bharat Sir's Student
There are 256 interrupts. We can't disable software interrupts.
We can't disable NMI. That leaves only INTR interrupt.

External Examiner
What are Vectored and Non Vectored interrupts?
Q: 51

You ~ Bharat Sir's Student
Interrupts that have a Fixed Vector Number are called Vectored.
All Software interrupts and NMI are Vectored.
An interrupt whose Vector Number is Not Fixed is called Non-Vectored.
INTR is the only Non Vectored Interrupt of 8086.

External Examiner
Why does 8086 give INTA#?
Q: 52

You ~ Bharat Sir's Student
INTA# is given in response to INTR to obtain the Vector Number as INTR is Non Vectored. 8086 gives two INTA#. On first INTA# device generates the value of Vector Number. On 2nd INTA# device sends the value of Vector Number to 8086.
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External Examiner
What are INT 0… INT 4 called?
Q: 53

You ~ Bharat Sir's Student
These are called Dedicated Interrupts as their functions are dedicated.
INT 0: Divide Error.
INT 1: Single Stepping.
INT 2: NMI.
INT 3: Breakpoint.
INT 4: Interrupt on Overflow.

External Examiner
What are INT 5… INT 31 called?
Q: 54

You ~ Bharat Sir's Student
These are called Reserved Interrupts.
They are reserved by Intel, for Future Processors.

External Examiner
What are INT 32… INT 255 called?
Q: 55

You ~ Bharat Sir's Student
These are called User Defined Interrupts.
They are available to the programmer and can be used to service any user-defined condition.

External Examiner
Define an interrupt?
Q: 56

You ~ Bharat Sir's Student
An interrupt is a condition that can make the microprocessor execute an ISR

External Examiner
What are Assembler Directives?
Q: 57

You ~ Bharat Sir's Student
These are statements given to the assembler so that it can convert the program into machine language. They are not instructions so they don't have any opcode.

External Examiner
What .ASM file?
Q: 58

You ~ Bharat Sir's Student
It is an Assembly language file
The Assembler converts into .OBJ file, which is in machine language.
The Linker converts it into a .EXE file that can be executed..

External Examiner
What is the use of DB, DW, DD, DQ, DT directives?
Q: 59

You ~ Bharat Sir's Student
These are data types used for declaring variables.
DB: 8-bit. DW: 16-bit. DD: 32-bit. DQ: 64-bit. DT: 80-bits.

External Examiner
What is the use of Assume Directive?
Q: 60

You ~ Bharat Sir's Student
Informs the Assembler, which are the segments. E.g.:: Assume CS: Code, DS: Data.

External Examiner
What is the use of .model Small directive?
Q: 61

You ~ Bharat Sir's Student
It reduces the memory consumed by our program by allowing the Assembler to overlap the segments instead of reserving 64 KB space for every segment.

External Examiner
What is the use of .stack 100 directives?
Q: 62

You ~ Bharat Sir's Student
Allocates 100 bytes to stack. Can be increased if needed.

External Examiner
What is the use of INT 21H?
Q: 63

You ~ Bharat Sir's Student
It is a DOS Interrupt. It performs several functions depending upon the value in AH.

To Accept a Value from User
MOV AH, ***01H***
INT 21H; user given value comes in AL.

To Accept a String from User
LEA DX, String
MOV AH, ***0AH***
INT 21H; user given string stored at location pointed by DX.

To Display a the result on Screen
MOV DL, value
MOV AH, ***02H***
INT 21H; value in Dl will be displayed

To Display a message on Screen
Msg DB 'Hello World' --- do this in data segment
LEA DX, Msg
MOV AH, ***09H***
INT 21H; "Hello World" will be displayed on the screen.

To Terminate the Program
MOV AH, ***4CH***
INT 21H; Termination Code.

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External Examiner
What is the use 13, 10, (or 0DH, 0AH) while declaring a string?
Q: 64

You ~ Bharat Sir's Student
It is the ASCII for Carriage Return, Line Feed.
This simply means the string will be displayed on a new line, from the left most position.
This is the same as putting "\n" in C Programming.

External Examiner
Why do we put a $ at the end of a string?
Q: 65

You ~ Bharat Sir's Student
For the Assembler to understand that the string has ended.

External Examiner
Why do we write, "Start" at the beginning?
Q: 66

You ~ Bharat Sir's Student
This indicates the beginning of the first executable statement in the program. Its like "main" of a C program.

External Examiner
Why do we write, "Org" assembler directive?
Q: 67

You ~ Bharat Sir's Student
Org stands for Origin.
It gives the absolute location where the data (following Org) will be stored.

External Examiner
What is 8282? Where is it used?
Q: 68

Bharat Sir's Student
It is an 8-bit latch. It is used to latch the address from the multiplexed address – data bus. It captures address when ALE is 1.

External Examiner
What is 8286? Where is it used?
Q: 69

Bharat Sir's Student
It is an 8-bit data trans-receiver. It is a bi-directional buffer. It passes data. It is enabled by DEN# (DEN bar) and its direction is decided by DT/R# signal.

External Examiner
What is 8284? Where is it used?
Q: 70

Bharat Sir's Student
It is a clock generator. It is used to generate the system clock.
It is connected to a crystal oscillator.
The Crystal frequency is divided by 3, to produce a clock of 33 % duty cycle.
If 8086 operates at 6 MHz we connect a crystal of 18 MHz
8284 also synchronizes Reset and Ready for the entire system.

External Examiner
What is 8288? Where is it used?
Q: 71

Bharat Sir's Student
It is a Bus Controller. It is used to generate control signals in Max Mode.
It decodes S2#, S1#, S0# and generates all the control signals.

External Examiner
How do you Generate Control Signals in Min Mode?
Q: 72

You ~ Bharat Sir's Student
In Min Mode, 8086 Produces M/IO#, RD# and WR#. They Are decoded by a 3:8 decoder to produce MEMR#, MEMW#, IOR# and IOW#.

External Examiner
What is the difference between Min Mode and Max Mode?
Q: 73

You ~ Bharat Sir's Student
In Min Mode, there is only one processor that is 8086.
In Max Mode 8086 can work along-with other processors like 8087 and 8089.
8087 is called NDP (Numeric data processor), also called Math Co Processor.
8089 is called I/O Processor.

External Examiner
What is 8288? Where is it used?
Q: 74

You
It is a Bus Controller. It is used to generate control signals in Max Mode.
It decodes S2#, S1#, S0# and generates all the control signals.

External Examiner
What is a Machine Cycle/ Bus Cycle? Example?
Q: 75

You
One operation performed on the system bus is called a Machine Cycle.
Example: Memory Read, Memory Write etc.
In 8086 every Machine cycle requires 4 t-states.

External Examiner
In a Read Machine cycle, why is there a time gap between Address and Data?
Q: 76

You
It a Read Cycle, Data has to travel from Memory (or I/O) to the Microprocessor. This travel takes time. It is called propagation delay.
It is not required in a Write Cycle as data is sent by the microprocessor itself.

External Examiner
Why are Read or Write signals activated in T2?
Q: 77

You ~ Bharat Sir's Student
Because in T1, the multiplexed bus carries address.

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External Examiner
Instruction Cycles are Interrupt Breakpoints, Machine Cycles are DMA Breakpoints. Justify?
Q: 78

You ~ Bharat Sir's Student
When an Interrupt occurs microprocessor finishes the current instruction before executing the ISR. In case of doubts call #BharatSir on: 982040 08217.
When a Bus Request (DMA) occurs, microprocessor simply finishes the current machine cycle and releases the bus.

External Examiner
Why does 8086 have two GND pins?
Q: 79

You ~ Bharat Sir's Student
GND is the pin from where all the Current is drained out of the chip.
In order to avoid over-heating on a single ground pin, 8086 has 2 GNDs.

External Examiner
If RESET, HOLD, NMI and INTR occur simultaneously, what is their priority order of service?
Q: 80

You ~ Bharat Sir's Student
The strongest signal of microprocessor is RESET, and will be serviced first.
Then Bus Request Signals (Hold or RG#/GT#). Then NMI and Finally INTR.

External Examiner
When does 8086 check Ready Signal?
Q: 81

You ~ Bharat Sir's Student
Ready is checked during T3 of any machine cycle.
If it is "0", it means device is not ready. Refer #BharatSir lecture notes for more!
"Wait States" are inserted between T3 and T4 till Ready becomes "1"

External Examiner
What are Advanced Write signals?
Q: 82

You ~ Bharat Sir's Student
They get activated 1 T-state in advance. It gives slower devices more time to accept the data. Please refer #BharatSir printed notes for more on this!

External Examiner
What is the use of 8087 NDP?
Q: 83

You ~ Bharat Sir's Student
It is used to perform powerful arithmetic like Trigonometry, Log, Square-Root etc. It operates on Floating Point numbers up to 80 bits. It can perform multiprocessing with 8086 to give higher performance.

External Examiner
What are the data formats of 8087?
Q: 84

You ~ Bharat Sir's Student
Integers: Words Int (16). Short Int (32). Long Int (64 bits).
BCD: Packed BCD (80bits).
Floating Point: Short Real (32). Long Real (64). Temp Real (80) bits.
Draw Floating Point formats from Class Notes.

External Examiner
How does 8087 know if host is 8086 or 8088?
Q: 85

You ~ Bharat Sir's Student
By checking BHE# pin on reset. If it is 0, then it is 8086 else 8088.

External Examiner
What is Normalization of a Floating Point No?
Q: 86

You ~ Bharat Sir's Student
Normalization means converting a Floating Pt Number to Fixed Point.

External Examiner
What are the errors/ exceptions of 8087?
Q: 87

You ~ Bharat Sir's Student
8087 interrupts 8086 due to 6 different errors/ exceptions.
Precision: Mantissa is too large to be stored
Underflow: Exponent is too small to be stored
Overflow: Exponent is too large to be stored.
Zero Divide: When we divide by zero
De-Normal Operand: When operand is not normalized
Invalid Operation: When we perform an invalid operation

External Examiner
What are the types of multi processor systems?
Q: 88

You ~ Bharat Sir's Student
Closely Coupled: Multiple Processors use the same, SHARED Memory, I/O & Buses.
Loosely Coupled: Multiple Processors use their own LOCAL Memory, I/O & Buses, and are connected to each other by a SHARED bus.

External Examiner
What is the Role of 8289 Bus Arbiter?
Q: 89

You ~ Bharat Sir's Student
8289 is used in Loosely Coupled systems to resolve priorities when different modules request for the SHARED system bus.

External Examiner
What are different Arbitration Schemes?
Q: 90

You ~ Bharat Sir's Student
Daisy Chaining, Polling and Independent Requests.

External Examiner
What are the instruction prefixes used in 8086?
Q: 91

Bharat Sir's Student
REP: Used to repeat string instructions "CX" times.
LOCK: Prevents the microprocessor from releasing the bus during an instruction.
ESC: Used to identify an 8087 instruction. (ESC is "11011" in binary)

External Examiner
What is the role of WAIT instruction in 8086?
Q: 92

You ~ Bharat Sir's Student
WAIT makes 8086 check TEST# signal.
TEST# comes from BUSY signal of 8087. If 8087 is BUSY, TEST# will be "1".
Now 8086 enters Wait State, and will resume after TEST# becomes "0".

Bharat Sir ~ Winter is coming.
Well done… Keep it up!

External Examiner
What is the role of 8259 PIC?
Q: 93

You ~ Bharat Sir's Student
It is used to increase the number of interrupts.
8259 has 8 interrupt pins IR0 – IR7.
If cascaded, 8259 can provide up to 64 interrupts using 1 master and 8 slaves.

External Examiner
What are the priority modes of 8259?
Q: 94

Bharat Sir's Student
FNM: Default mode. IR0 Highest… IR7 Lowest. Used in Single 8259.
SFNM: IR0 Highest… IR7 Lowest. Used in Cascaded 8259.
Rotating Priority: After any interrupt is serviced it becomes lowest priority.

External Examiner
What is SMM in 8259?
Q: 95

Bharat Sir's Student
Any interrupt can interrupt the current ISR, irrespective of their priority, except the interrupt currently being serviced.

External Examiner
What are EOI modes in 8259?
Q: 96

Bharat Sir's Student
Normal EOI Mode: Programmer gives EOI command at the end if ISR to clear bit from in service register.
Auto EOI Mode: 8259 automatically clears bit from in service register after 2nd INTA# cycle.

External Examiner
What is the use of CAS lines in 8259?
Q: 97

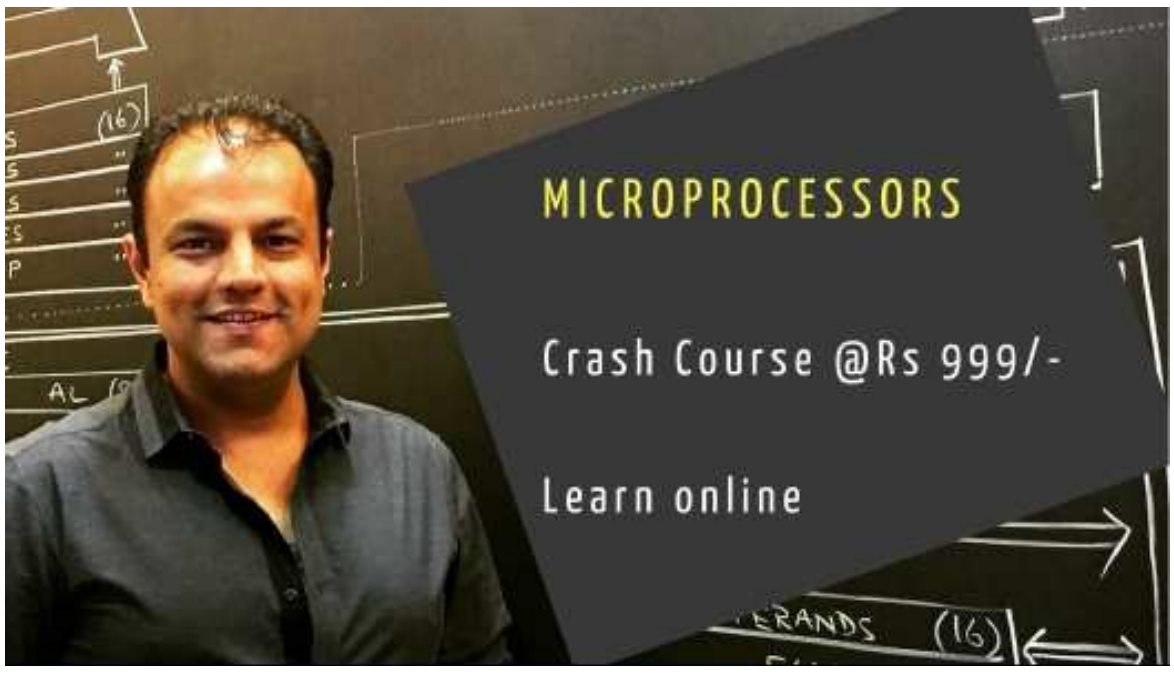
Bharat Sir's Student
$CAS_{0,1,2}$ are used by the master to select the slave during 1st INTA#.

External Examiner
What is Polling in 8259?
Q: 98

Bharat Sir's Student
In Poll Mode, instead of 8259 interrupting the microprocessor, 8086 will periodically POLL 8259 to know which interrupt has occurred.

External Examiner
What are the Commands of 8259?
Q: 99

Bharat Sir's Student
There are two types of Commands:
ICW1, ICW2, ICW3 and ICW4: Initialization Command Words.
OCW1, OCW2 and OCW3: Operational Command Words.
These are commands given by the programmer to 8259 to program various properties such an Vector Numbers, Triggering, Masking, Priority etc.



External Examiner
What is the Role of 8255 PPI?
Q: 100

Bharat Sir's Student
8255 provides 3, 8-bit bidirectional I/O ports for connection I/O devices to 8086. It can perform Handshake based data transfer to increase reliability.

External Examiner
What is data transfer Modes of 8255?
Q: 101

Bharat Sir's Student
Mode 0: Simple I/O. All ports transfer data but no handshaking.
Mode1: Handshake I/O. Port A, B transfer data, Port C does Handshaking.
Mode 2: Bidirectional Handshaking. Only Available for Port A.

External Examiner
What are the Commands of 8255 PPI?
Q: 102

Bharat Sir's Student
I/O Command: Used to select the Modes and Directions of all ports of 8255.
BSR Command; Used to set or reset a single line of Port C.

External Examiner
How can we generate a square wave using 8255?
Q: 103

Bharat Sir's Student
Using BSR Command, we can make any line of port C alternate between 1 and 0 (Set and Reset) with a delay after each. Connect this output to a CRO and we get a square wave. By manipulating delay we can also produce Rectangular wave.

Bharat Sir
Superb answer! Say the same thing if asked to blink an LED.
Keep it up!

External Examiner
What is the role of 8253/8254 PIT?
Q: 104

Bharat Sir's Student
It is used to produce hardware delays using three 16-bit Counters: C0, C1 & C2.

External Examiner
What are the 6 Counting Modes of 8254 PIT?
Q: 105

You ~ Bharat Sir's Student
Mode 0: Interrupt on Terminal Count
Mode 1: Mono-stable Multi-vibrator
Mode 2: Rate Generator
Mode 3: Square Wave Generator
Mode 4: Software Triggered Strobe
Mode 5: Hardware Triggered Strobe

External Examiner
What are the methods of reading the count?
Q: 106

Bharat Sir's Student
Ordinary Read: Counting has to be stopped.
Counter Latch Command: Can read the Count without stopping.
Read Back Command: Can read Count and Status without stopping.

External Examiner
What is the difference between 8253 & 8254?
Q: 107

Bharat Sir's Student
8253 does not have a Read Back Command

External Examiner
What if we give an ODD count for Mode 3 Sq. Wave Gen?
Q: 108

You ~ Bharat Sir's Student
The Extra pulse is always given on the HIGH side.
Count = 6: 3-High, 3-Low pulses. Count = 7: 4-High, 3-Low pulses

Bharat Sir
That was a tricky one… Well Done!
Call: 9820408217

External Examiner
What is DMA?
Q: 109

You ~ Bharat Sir's Student
Direct Memory Access means transferring data directly between Memory and I/O without involving the microprocessor. It is extremely fast due to two reasons: The transfer is direct and it is hardware based so no time is wasted in fetching and decoding instructions.

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External Examiner
Explain DMA operation in brief?
Q: 110

You ~ Bharat Sir's Student
DMA Controller (8237/ 8275) makes Hold = 1. 8086 Releases system bus and makes HLDA = 1. DMAC becomes bus master and transfers data directly between Memory and I/O. At the end DMAC makes Hold = 0. 8086 becomes bus master again.

External Examiner
What are DMA Data Transfer Modes?
Q: 111

You ~ Bharat Sir's Student
Block transfer also called Burst Mode: DMAC performs full data transfer and only then return the bus back to 8086.
Cycle Stealing also called Single Byte transfer: Both 8086 and DMAC perform Single Cycles alternately.
Demand transfer: Transfer stops whenever DREQ becomes low, and resumes when DREQ becomes high again (transfer happens only on demand)
Transparent Mode also called Hidden Mode: Transfer done only when 8086 is idle.

External Examiner
What is Cascaded mode of DMA?
Q: 112

You ~ Bharat Sir's Student
DMAC has 4 Channels.
If we want more devices then we can connect DMAC in a cascaded form.

External Examiner
What is DMA Read and DMA Write Cycle?
Q: 113

You ~ Bharat Sir's Student
DMA Read: When DMAC transfers data from Memory to I/O.
DMA Write: When DMAC transfers data from I/O to Memory.

External Examiner
Explain DMAC Priority Modes?
Q: 114

You ~ Bharat Sir's Student
Fixed Priority: Channel 0 Highest… Channel 3 Lowest.
Rotating Priority: When a channel is serviced it gets lowest priority and others come up in the order in a circular manner.

External Examiner
Give some features of 80586 - Pentium?
Q: 116

You ~ Bharat Sir's Student
Operating frequency: 66 - 99 MHz
Address Bus: 32 bits, Physical Memory: 4GB
Data Bus: 64 bits , Memory Banks: 8 banks
ALU: 32 bits, Classification: 32-bit microprocessor
Pipeline Stages: 5 stages – Fetch, Decode, Operand Addr Calc, Exec, Write Back

External Examiner
What are the different types of Non – Volatile Memories?
Q: 117

You ~ Bharat Sir's Student
***ROM**: Read Only Memory. This is the original type of ROM. Cannot be written.*
***PROM**: Programmable ROM. Can be written but only once. Also called OTPROM.*
***EPROM**: Erasable PROM. Can be erased by exposure to UV rays.*
***EEPROM**: Electrically EPROM. Can be erased by applying higher voltage.*
***Flash ROM**. Special type of EEPROM. Allows block-wise erasure so erasure is faster.*

External Examiner
What are the different types of Volatile Memories?
Q: 118

You ~ Bharat Sir's Student
***RAM**: Random Access Memory. It is of two types.*
***SRAM**: Static RAM. Uses Flip-Flops to store data so works faster. Very Expensive.*
***DRAM**: Dynamic RAM. Uses capacitors to store data. Slower. Cheaper.*
***SDRAM**: Synchronous Dynamic RAM. Uses common clock with CPU to synchronize.*
***RDRAM**: Rambus RAM. Uses dedicated bus with CPU to transfer data..*

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External Examiner
What memories are used in your mobile phone?
Q: 119

You ~ Bharat Sir's Student
It uses DRAM for primary memory, and Flash for secondary storage. Even the memory card is Flash ROM.

External Examiner
What memories are used in your computer?
Q: 120

You ~ Bharat Sir's Student
Primary Memory: DRAM ~ 4GB
Secondary Memory: Hard Disk ~ 1TB
Cache Memory: SRAM ~ 3MB
Portable Memory: CD – 700MB, DVD – 4.7GB. Pen Drives: Flash ROM of any size.

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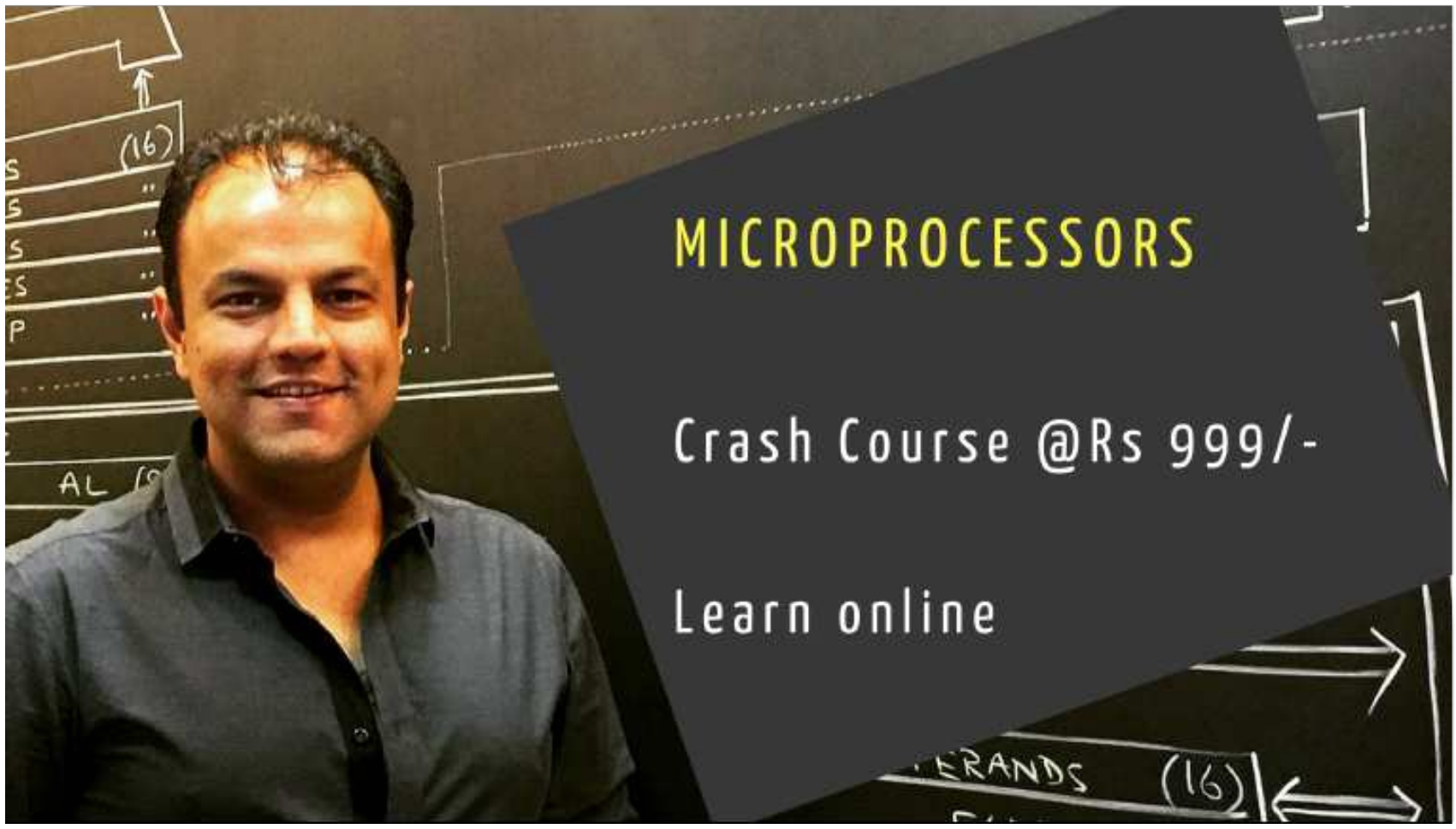

80386 Based Questions

External Examiner
What are the basic features of 80386?
Q: 121

You ~ Bharat Sir's Student
Address bus: 32 bits. Therefore total physical memory = 2^{32} = 4GB.
ALU: 32 bits. Hence called 32 bit µP.
Data bus: 32 bits hence 4 memory banks.
Operating frequency: 16MHz – 33 MHz

External Examiner
Difference between SX and DX version of 80386?
Q: 122

You ~ Bharat Sir's Student
SX: Single execution speed… 32 bit ALU but 16 bit data bus.
DX: Double execution speed… 32 bit ALU and 32 bit data bus.

External Examiner
What are the new flags added by 80386?
Q: 123

You ~ Bharat Sir's Student
VM: to enter Virtual 8086 mode
RF: Resume flag for debug breakpoints
NT: Nested task for multitasking environment
IOPL: Decides privilege level for I/O Devices

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External Examiner
Describe pipelining of 80386?
Q: 124

You ~ Bharat Sir's Student
3 - Stage pipeline.
Fetch, Decode and Execute.

External Examiner
What is the size of Virtual memory of 80386?
Q: 125

You ~ Bharat Sir's Student
Virtual address is 46 bits (14 bit selector and 32 bit offset)
This gives 2^{46} = 64TB of Virtual address space.
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External Examiner
What are the steps in address translation?
Q: 126

You ~ Bharat Sir's Student
46 bit Virtual address is converted into 32 bit linear address by segmentation.
This is further converted into 32 bit physical address by paging.
Segmentation is compulsory, Paging is optional.
If paging is not performed then the linear address is the physical address.

External Examiner
What is GDTR, LDTR, IDTR and TR?
Q: 127

You ~ Bharat Sir's Student

GDTR: Global Descriptor table register.
Gives base address of GDT.

LDTR: Local Descriptor table register.
Gives a selector to the LDT descriptor in GDT.

IDTR: Interrupt Descriptor table register.
Gives base address of IDT.

TR: Task register.
Gives a selector to the TSS descriptor in GDT.

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External Examiner
What are the operating modes of 80386?
Q: 128

You ~ Bharat Sir's Student
***Real mode**: Works like a fast 8086. Selected on reset.*
***Protected mode**: all new features of 386 are active in protected mode like protection mechanism, multitasking, advanced address translation and paging.*
***Virtual 8086 mode**: To invoke in a virtual 8086 environment once we have switched to protected mode.*

External Examiner
What are the sizes of the following?
Q: 129

You ~ Bharat Sir's Student
GDT: 64KB
LDT: 64 KB
IDT: 2KB
GDTR: 48 bit
LDTR: 16 bit
IDTR: 48 bit
TR: 16 bit
Segment registers: 16 bit
Offset registers: 32 bit
Virtual address: 46 bit
Linear address: 32 bit
Physical address: 32 bit
Page table: 4KB
Page Directory: 4KB
Page: 4KB
EFLAGS: 32 bits
Control registers: 32 bits
GPRs: 32 bit
All of this is applicable to protected mode.
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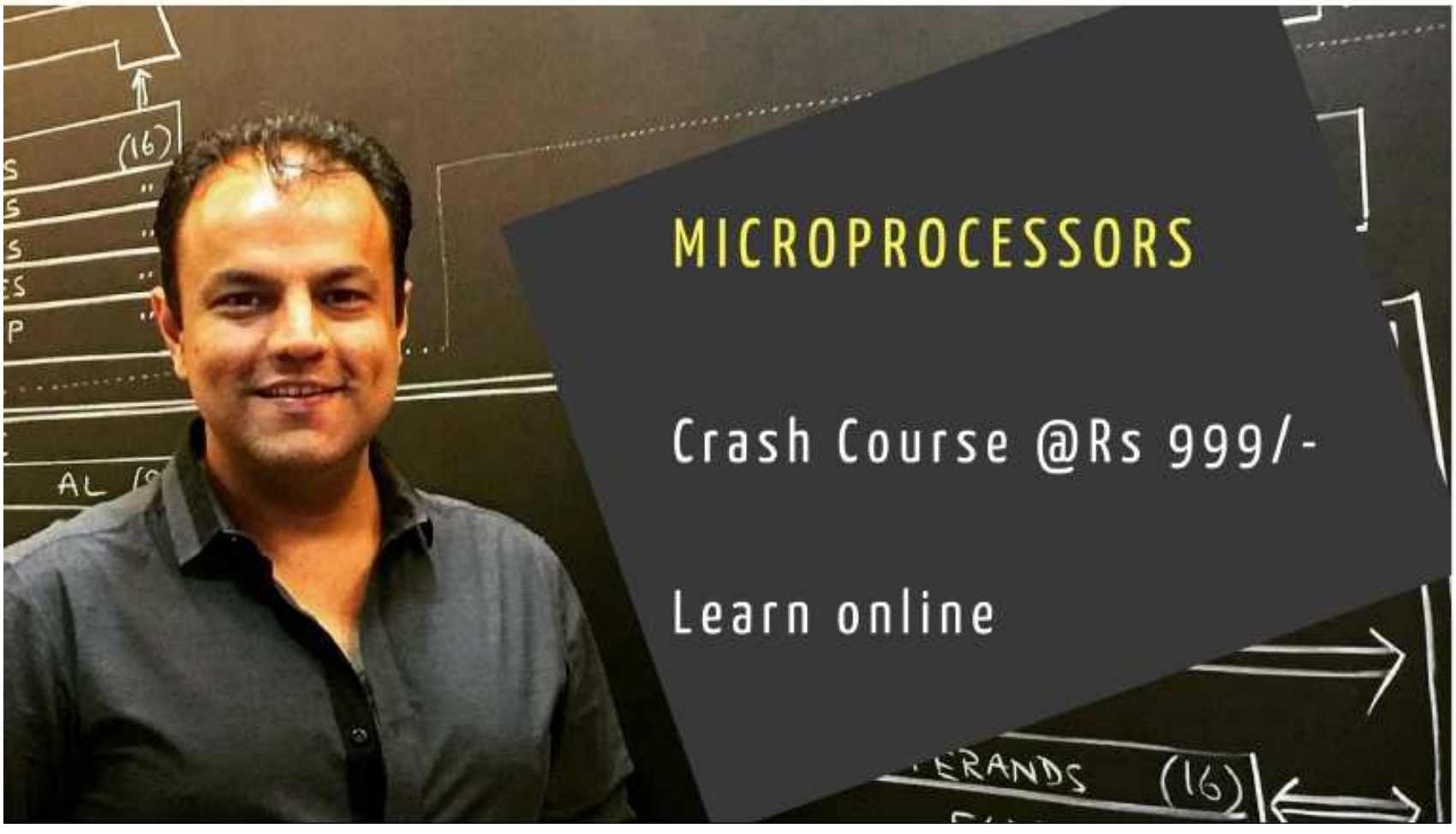

Pentium Based Questions

External Examiner
Give basic features of Pentium?
Q: 130

You ~ Bharat Sir's Student
Address bus: 32 bits. Therefore total physical memory = 2^{32} = 4GB.
ALU: 32 bits. Hence called 32 bit µP.
Data bus: 64 bits hence 8 memory banks.
Operating frequency: 66MHz – 100 MHz (Various versions were released)

External Examiner
What is the architecture of Pentium called?
Q: 131

You ~ Bharat Sir's Student
P5 Microarchitecture.
Several initial versions of Pentium were based on this microarchitecture.

External Examiner
What are the integer pipeline stages of Pentium?
Q: 132

You ~ Bharat Sir's Student
5 stage, 2 way superscalar
Prefetch, Decode1, Decode2, Execute, Write back.
The two pipes are called u and v pipes.
This is much easier than you think and wildly interesting.
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External Examiner
What are the floating point pipeline stages of Pentium?
Q: 133

You ~ Bharat Sir's Student
8 stage FP Pipeline
Prefetch, Decode1, Decode2, Execute, FPExec1, FPExec2, Write back, Error reporting.

External Examiner
What is the size of instruction queue?
Q: 134

You ~ Bharat Sir's Student
2 queues of 32 bytes each

External Examiner
What is the size of cache?
Q: 135

You ~ Bharat Sir's Student
Pentium has on-chip L1 Split cache.
8 KB on-chip L1 code cache.
8 KB on-chip L1 data cache.
Both are 2 way set associative.

If these words don't make any sense to you, that's only because you haven't tried understating these concepts.
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