Module-2
CSEN 3104
Lecture 14

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SIMD Architecture

Use of indexing to address the local memories in parallel at different local addresses

- Consider an array of n X n data elements:

$$A = \{A(i,j),\ 0 \le i,\ j \le (n-1)\}$$

- Elements of j^{th} column of A are stored in n consecutive locations of PEM_j [say from location 200 to location (200+n-1)] (assume $n \le N$)
- We want to access the principal diagonal elements A(j,j) for j=0, 1 , …, (n-1) of the array A
- The CU must generate and broadcast an effective memory address 200
- The local index registers must be set to be $I_j = j$ for j = 0, 1, …, (n-1) in order to convert the global address 200 to local address $200 + I_j = 200 + j$ for each PEM_j
- Within each PE, there is a separate memory address register for holding these local addresses

Data Routing Mechanisms

- Execution of the following vector instruction in an array of N processing elements (PEs)
- The sum S(k) of the first k components in a vector $A = (A_0, A_{1,} \ldots\ldots,\ A_{n-1})$ is desired for each k from 0 to (n-1)
- We need to compute the following n summations:

$$S(k) = \sum_{i=0}^{k} A_i \qquad \text{for } k = 0, 1, \ldots\ldots, (n-1)$$

Data Routing Mechanisms

- These n vector summations can be computed recursively by going through the following (n-1) iterations:

$$S(0) = A_0$$

$$S(k) = S(k-1) + A_k \qquad \text{for } k = 1, 2, \ldots\ldots, (n-1)$$

- For n = 8, the above recursive summation is implemented in an array processor with N = 8 processing elements (PEs)
- $Log_2 n = 3$ steps are required
- Both data routing and PE masking are used
- Show diagram
- Initially each A_i, residing in PEM_i is moved to the R_i register in PE_i for i = 0,1,2,…,7

Data Routing Mechanisms

- In the first step, A_i is routed from R_i to R_{i+1} and added to A_{i+1} with the resulting sum $A_i + A_{i+1}$ in R_{i+1} for $i = 0,1,2,\ldots,6$
- In step 2, the intermediate sums in R_i are routed to R_{i+2} for $i = 0$ to 5
- In step 3, the intermediate sums in R_i are routed to R_{i+4} for $i = 0$ to 3
- Thus, the final value of PE_k will be $S(k)$ for $k = 0,1,2,\ldots,7$

Data Routing Mechanisms

- In step 1, PE_7 is not involved in data routing (receiving but not transmitting)
- In step 2, PE_7 and PE_6 are not involved in data routing
- In step 3, PE_7, PE_6, PE_5 and PE_4 are not involved in data routing
- These unwanted PEs are masked off during the corresponding steps
- During the addition operations
  - PE_0 is disabled in step 1
  - PE_0 and PE_1 are made inactive in step 2
  - PE_0, PE_1, PE_2 and PE_3 are masked off in step 3
- The PEs that are masked off in each step depend on the operation (data-routing or addition)
- Thus the masking pattern keep changing in different operation cycles
- Masking and routing operation are much more complicated when the vector length $n > N$

Thank you