Module 1: **Introduction** Review of basic computer architecture;

Pipelining: Hwang Chapter 6
Basic concepts,
Instruction Pipeline and Scheduling in Pipeline page 265 to 279,
Data hazards, control hazards and structural hazards, techniques for handling hazards: page 283 to 288, page295-296 Hwang and Briggs Chapter 3 pages 200-203And
Problems:6.1, 6.6,6.9, 6.11, 6.13
Write short note on pipeline hazards and different techniques to handle them.

Arithmetic pipeline :Hwang page 297- 303, Hwang and Briggs Chapter 3- Floating Point Adder with four processing stages
Multiply-tree using CSA(Carry save adder) for n-bit x n-bit multiplication (n can be 4,5,6,7,8)
Describe the working of a Floating Point Adder using schematic diagram.

Module 2:

Instruction-level parallelism:,
Array processor-Hwang and Briggs Chapter 5.1, 5.1.1, 5.1.2
Explain masking and routing mechanism for an array processor (i.e SIMD)
Explain the working of a SIMD processor using a schematic diagram.

vector processors- Hwang and Briggs Chapter 3.4, 3.4.1, 3.4.3,
Pipeline chaining 4.4.2 and page 310
and presentation sent on 29/3/17
Hwang Chapter 8.1 pages 403 to 406
What are gather and scatter and masking instructions and how can they be used for sparse vectors or sparse matrices(page 406)?
Problem 8.5(b)
What is strip mining ? Hwang 8.3.2 page 437
What is pipeline chaining?
What is vectorising compiler?

Superscalar:-Hwang Chapter4 page 177-178
Superpipelined:- Hwang Chapter 6 page 316-318
VLIW processor architectures: -pages 182-184.
What are the CPIs and throughputs in case of linear pipeline ,superscalar pipeline, superpipeline and VLIW processor architectures?
Describe functioning of linear pipeline ,superscalar pipeline, superpipeline and VLIW processors.
Why isVLIW processor not as popular as Superscalar and superpipelined processor architecture?

Interconnection networks:
Crossbar, Delta, Omega, Shuffle-Exchange, Banyan , Hypercube, Butterfly Networks.
Hwang and Briggs Chapter 5.1.3, 5.2, 5.2.1 , 5.2.2, 5.2.3, 5.2.5,5.3.1 pages 355 to 358,5.3.4, 5.3.3 pages497 to502 and 2 presentation sent on 29/3/2017
Hwang 2.4 to 2.4.3,Tables on page 88 and 95.
Hwang and Briggs Problem 5.1,
Draw a 8x8 omega network.

Apply cube routing functions multistage network for N=8. Is cube network a blocking network?
Draw and explain a 9x16 delta network.
Draw a Shuffle exchange recirculating network for N=8.(Hwang and Briggs Figure 5.16)
What is bandwidth of a network?

Module 3:

Measuring and reporting performance:
CPI, MIPS: Reference:-Hwang 1.1.4
Hwang Exercise Problem 1.1 , 1.4,
Amdahl's Law & Gustafson's Law: Presentation sent on March23
State and explain Amdahl's law and Gustafson's Law.
How does Amdahl's Law & Gustafson's Law differ with respect to machine size and problem size?

Hierarchical memory technology:
Inclusion, Coherence Hwang 191-192
locality properties-Hwang page 193 :Question What is locality of reference? Differentiate between temporal and spatial locality;
Virtual memory organization , mapping and management techniques Hwang 194-204,
memory replacement policies hwang205-207.

Multiprocessor architecture:
Taxonomy of parallel architectures and Cluster computers: Reference Architecture Classification presentation sent on February 22.
Centralized shared- memory architecture:
Distributed shared-memory architecture
Hwang Chapter 1: 1.1.3, 1.2, 1.2.2
Hwang Problems: 1.7,1.8, 1.12(c)

What is the difference between loosely coupled and tightly coupled architecture?
What is meant by non-uniform memory access (NUMA).Explain with schematic diagram?
What is uniform memory access (UMA) Explain with schematic diagram?

What is cache coherence problem? Suggest methods used to solve cache coherence problem

Module 4:

Issues with Multiprocessor Architectures:
Synchronization, memory consistency; Cache Coherence protocols (brief discussion only);refer to presentation
Non von Neumann architectures: (3L)
Data flow computers Hwang Chapter 2.3.1 pages 71-72,presentation sent on March 23.
With simple diagram explain the data flow architecture. How does it differ from control flow architecture.
Advantage /Disadvantage of Data flow
Draw data flow graph for a given set of instructions (as shown in presentation).

RISC architectures: Hwang page 163to 165 Chapter 4.1.2,and presentation sent on March 15
Questions: Explain RISC architecture. Compare and contrast RISC and CISC architecture.

References:

1) **Kai Hwang:** Advanced Computer Architecture – Parallelism, etc.
2) **Hennessey & Patterson :** Computer Architecture – A Quantitative Approach
3) **Hamacher et el:** Computer Organization (5^{th} Ed) & above
4) Kai Hwang & Briggs: Computer Architecture & Parallel Processing