COURSE STRUCTURE OF B. TECH IN COMPUTER SCIENCE & ENGINEERING, HIT

Subject Name: Computer Architecture					
Paper Code: CSEN 3104					
Contact Hours per week	**L**	**T**	**P**	**Total**	**Credit Points**
	3	**0**	**0**	**3**	**3**

Module 1: **(9L)**

CPU Architecture: Instruction Execution Mechanism details;
Classification of Computer Architecture – Von Neumann and Harvard;
Basics of Pipelining;
Instruction Set Architecture details; Comparison between various types: Stack / Accumulator / Memory to Memory/ Load Store architecture;
CISC vs. RISC Architecture; MIPS Architecture & ISA as case study.
(4L)

Pipelined Architecture: Brief Introduction, Performance Measures - speed up,
Efficiency ,performance - cost ratio etc.
Static pipelines - reservation tables, scheduling of static pipelines, definitions - minimum average latency, minimum achievable latency, greedy strategy etc.,
Theoretical results on latency bounds without proof.
Dynamic pipelines - reservation tables, outline only.
(5L)

Module 2: **(9L)**

Vector Processing: Vector registers; Vector Functional Units; Vector Load / Store;
Vectorization; Vector operations: gather / scatter; Masking; Vector chaining;
(2L)

SIMD Architectures: brief introduction, various concepts illustrated by studying detailed
SIMD algorithms, viz., Matrix multiplication, Sorting on Linear array, Mesh;
Intel MMX operations; (4L)

Interconnection Networks: Detailed study of Interconnection Network - Boolean cube,
Mesh, Shuffle-exchange, Banyan, Omega, Butterfly, Generalized Hypercube,
Delta etc (3L)

Module 3: **(8L)**

Superscalar Architecture: Microarchitecture of a typical super scalar processor :
Instruction fetching, decoding and parallel execution; branch prediction;
Handling memory operations; (2L)

Branch Prediction: Handling Control Dependency; Delayed Branching; Branch
Prediction techniques; (2L)

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MIMD Architectures: Sorting and Matrix Multiplication algorithms (flavours only); (4L)

Module 4: **(8L)**

Data Flow Architecture: Data Flow Graphs; ISA; Nodes; Programs; Control flow vs. Data flow; Example Dataflow Processor; Advantages & Disadvantages; (2L)
VLIW Architecture; (2L)
Memory Consistency; (2L)
Cache Coherence; (2L)

Text Books:
1. Patterson & Hennessy: Computer Organization and Design: The Hardware/Software Interface (3rd Ed – 5th Ed)
2. Hennessey & Patterson : Computer Architecture – A Quantitative Approach

3. Hwang & Briggs: Advanced Computer Architecture and Parallel processing, MH.
4. Quinn: Designing Efficient Algorithms for Parallel Computers, MH.
5. Yale N. Patt, Sanjay J. Patel: Introduction to Computing Systems: From Bits & Gates to C & Beyond.

Reference Books & Materials:
1. NPTEL Materials on Computer Organization and Architecture;
2. Onur Mutlu's lecture materials on Computer Architecture from CMU web site: https://users.ece.cmu.edu/~omutlu/

Paper:

1. James E. Smith, and Gurindar S. Sohi, The Microarchitecture of Superscalar Processors, in Proceedings of the IEEE, vol. 83, no. 12, December 1995.