Pipelining in VLIW Processess Fetch Decode Execute

Execute

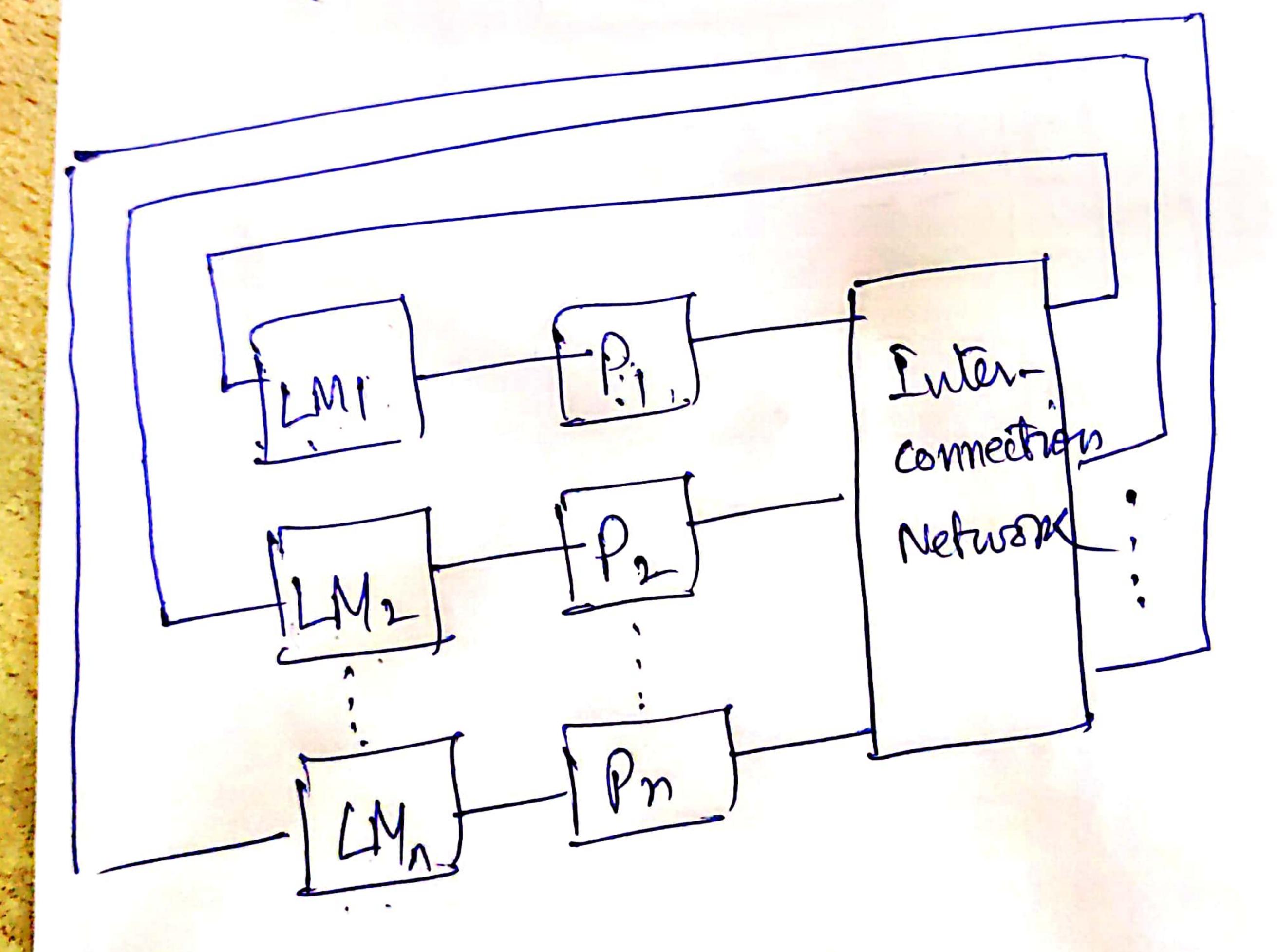
3 operations Veren 201 VLIW execution with degree 3

Multiprocesors Model ()MA Rocessoos, Bus, Crossbar Smitch, Hultistage NW) Shared Memosy

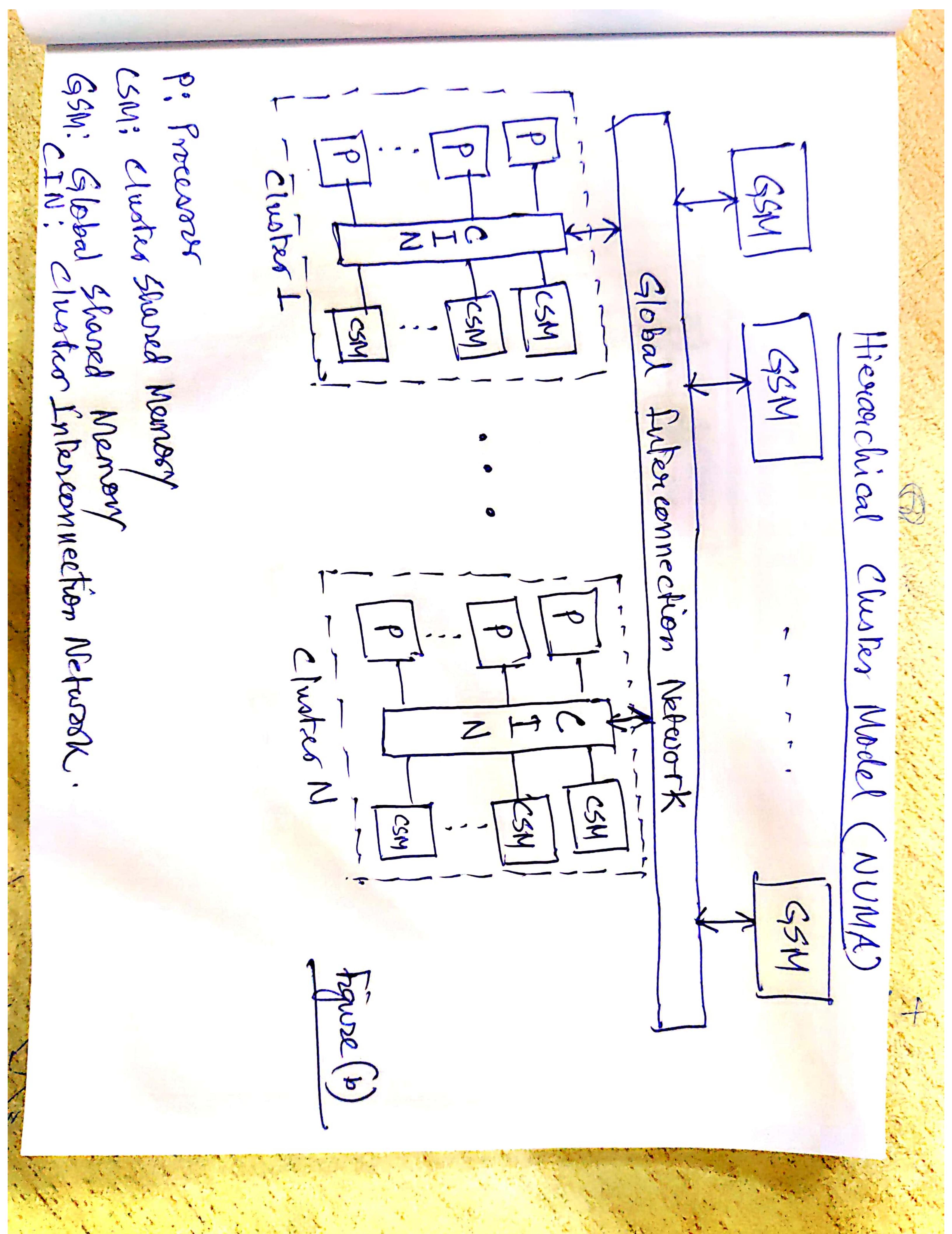
Scanned by CamScanner

Carion

MUMA model (shared total memories)

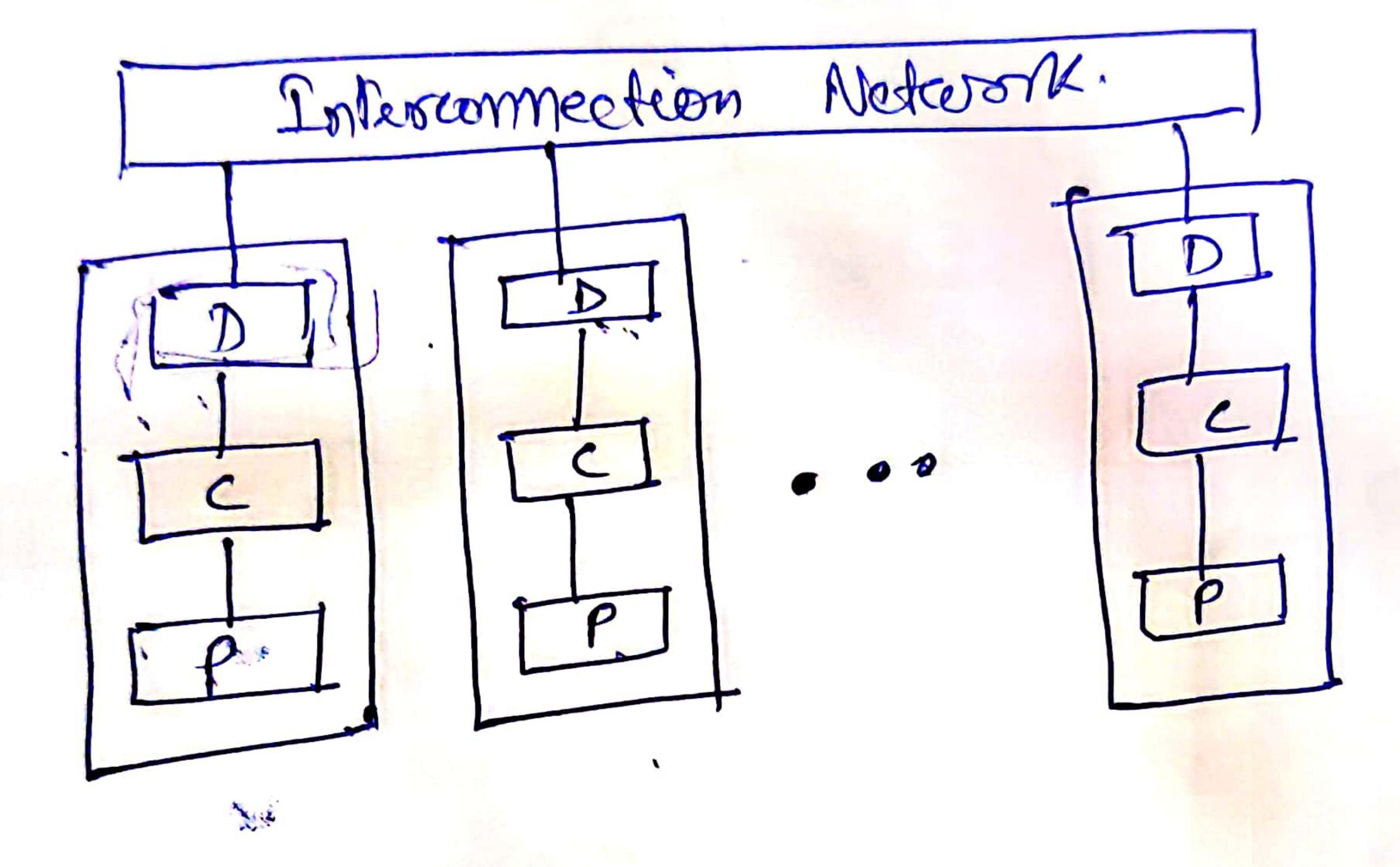


Feguere (a)



Scanned by CamScanner

COMA Model



Scanned by CamScanner

P: Processors Cache

· Directory.

CONT MINE

NORMA Architecture

