# OSOROM Instruction Set Reference

The Moroso Project

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# Contents

# Chapter 1

# CPU Architecture

## 1.1 Instructions

Each instruction is a 32-bit word, stored in little-endian order. The top 2 bits of the instruction select one of four predicate registers, and the third bit from the top optionally inverts it. The instruction is only executed if the resulting predicate is true.

## 1.2 VLIW

At each time step, the CPU fetches a "packet" of 4 instructions located contiguously in memory and executes them in parallel. These packets must be aligned to their 16-byte size, and branch targets must also be so aligned.

There are three types of instructions: Control, Memory, and ALU instructions. Only one control instruction may be executed in any given packet; it must occupy the first (lowest-address) slot in its packet. Likewise, only the first two slots in a packet may execute memory instructions. ALU instructions may be located in any slot.

ALU instructions in the first three slots may optionally specify a "long immediate" operand. In this case, the 32 bits following that instruction are interpreted as an operand, and a no-op is scheduled in the following slot of thatpacket.

## 1.3 Registers

There are 32 32-bit general-purpose registers, R0 through R31. R31 is used as the link register for BL instructions. The program counter is stored separately, and may only be modified through branch instructions and read through BL instructions.

There are three one-bit predicate registers that may be written to by compare instructions and used to conditionally execute any instruction.

## 1.4 Shifting

The ALU is preceded by a shifter for its second operand

## 1.5 Virtual Memory

Virtualmemory is accomplished through a hardware-filled TLB, with 4KB pages and a 2-level page-table structure that looks like x86's without any of the fancy bits. (more detail to come in this section; in particular, we want to boot with paging on but it's not clear how the world looks then)

## 1.6 Exceptions

# Chapter 2

# Instruction Listing

## 2.1 ADD

### 2.1.1 Encoding

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PRED | | | | 0 | CONSTANT | | | | | | | | | | | | | | ROTATE | | | 0 | 0 | 0 | 0 | RD | | | | RS | | |
| PRED | | | | 1 | 0 | 1 | SHIFTAMT | | | | | | | | | SHF | RT | | | | | 0 | 0 | 0 | 0 | RD | | | | RS | | |
| PRED | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RD | | | | RS | | |

### 2.1.2 Behavior

The first form adds the value `CONSTANT ROR 2*ROTATE` to `RS`, storing the result in `RD`. The second form shifts the value in `RT` in the manner specified by `SHF` and `SHIFTAMT`, then adds that to `RS` and stores the result in `RD`. The third form adds the long immediate stored in the next instruction slot to `RS` and stores the result in `RD`. A no-op is issued for the next instruction slot.

## 2.2 AND

### 2.2.1 Encoding

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PRED | | | 0 | CONSTANT | | | | | | | | | | | | | | ROTATE | | | | 0 | 0 | 0 | 1 | RD | | | | RS | | | |
| PRED | | | 1 | 0 | 1 | SHIFTAMT | | | | | | | | SHF | | RT | | | | | | 0 | 0 | 0 | 1 | RD | | | | RS | | | |
| PRED | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | RD | | | | RS | | | |

## 2.3 NOR

### 2.3.1 Encoding

| 31–29 | 28 | 27–20 | 19–15 | 14–10 | 9–5 | 4–0 |
|---|---|---|---|---|---|---|
| PRED | 0 | CONSTANT | ROTATE | 0010 | RD | RS |
| PRED | 101 | SHIFTAMT | SHF | RT | 0010 | RD | RS |
| PRED | 1000000000 | 00000 | 00000 | 0010 | RD | RS |

## 2.4 OR

### 2.4.1 Encoding

| 31–29 | 28 | 27–20 | 19–14 | 13–10 | 9–6 | 5–0 |
|---|---|---|---|---|---|---|
| PRED | 0 | CONSTANT | ROTATE | 0011 | RD | RS |
| PRED | 101 | SHIFTAMT | SHF | RT | 0011 | RD | RS |
| PRED | 1000000000000000 | 0011 | RD | RS |

## 2.5 SUB

### 2.5.1 Encoding

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PRED | | | | 0 | CONSTANT | | | | | | | | | | | | | ROTATE | | | | 0 | 1 | 0 | 0 | RD | | | | RS | | | |
| PRED | | | | 1 | 0 | 1 | SHIFTAMT | | | | | | | | SHF | RT | | | | | | 0 | 1 | 0 | 0 | RD | | | | RS | | | |
| PRED | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | RD | | | | RS | | | |

## 2.6 RSB

### 2.6.1 Encoding

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PRED | | | | 0 | CONSTANT | | | | | | | | | | | | | ROTATE | | | 0 | 1 | 0 | 1 | RD | | | | RS | | | |
| PRED | | | | 1 | 0 | 1 | SHIFTAMT | | | | | SHF | RT | | | | | | | | 0 | 1 | 0 | 1 | RD | | | | RS | | | |
| PRED | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | RD | | | | RS | | | |

## 2.7 XOR

### 2.7.1 Encoding

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PRED | | | 0 | CONSTANT | | | | | | | | | | | | | | ROTATE | | 0 | 1 | 1 | 0 | RD | | | | RS | | | |
| PRED | | | 1 | 0 | 1 | SHIFTAMT | | | | | SHF | RT | | | | | | | | 0 | 1 | 1 | 0 | RD | | | | RS | | | |
| PRED | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | RD | | | | RS | | | |

## 2.8 MOV

### 2.8.1 Encoding

| 31–29 | 28 | 27–20 | 19 | 18–14 | 13–9 | 8–5 | 4–0 |
|---|---|---|---|---|---|---|---|
| PRED | 0 | CONSTHIGH | R | 1000 | RD | CONSTLOW | |
| PRED | 101 | SHIFTAMT | SHF | XXXXX | 1000 | RD | RS |
| PRED | 1000001 | | SHF | RT | 1000 | RD | RS |
| PRED | 10000000000 | | | | 1000 | RD | RS |

## 2.9 MVN

### 2.9.1 Encoding

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PRED | | | 0 | CONSTHIGH | | | | | | | | | | | | | | | R | 1 | 0 | 0 | 1 | RD | | | | CONSTLOW | | | |
| PRED | | | 1 | 0 | 1 | SHIFTAMT | | | | | SHF | X | X | X | X | X | 1 | 0 | 0 | 1 | RD | | | | RS | | | | | | | |
| PRED | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | SHF | RT | | | | | 1 | 0 | 0 | 1 | RD | | | | RS | | | | | | | |
| PRED | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | RD | | | | RS | | | | | | | |

## 2.10 SXB

### 2.10.1 Encoding

| 31–29 | 28 | 27–24 | 23–20 | 19–16 | 15–12 | 11–10 | 9–8 | 7–4 | 3–0 |
|---|---|---|---|---|---|---|---|---|---|
| PRED | 0 | CONSTANT | | | | ROTATE | 1 0 | RD | RS |
| PRED | 1 0 | 1 | SHIFTAMT | | | SHF | RT | RD | RS |
| PRED | 1 0 | 0 0 0 0 0 0 0 0 0 0 | | | | | | RD | RS |

## 2.11 SXH

### 2.11.1 Encoding

| 31–29 | 28 | 27–24 | 23–20 | 19–16 | 15–12 | 11–8 | 7–4 | 3–0 |
|---|---|---|---|---|---|---|---|---|
| PRED | 0 | CONSTANT | | | ROTATE | 1011 | RD | RS |
| PRED | 101 | SHIFTAMT | | SHF | RT | 1011 | RD | RS |
| PRED | 1000 | 0000 | 0000 | 0000 | 0000 | 1011 | RD | RS |

## 2.12 CMP

### 2.12.1 Encoding

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PRED | | | 0 | CONSTANT | | | | | | | | | | | | ROTATE | | | | 0 | 1 | 1 | 1 | CMPTP | | PD | | RS | | | |
| PRED | | | 1 | 0 | 1 | SHIFTAMT | | | | | SHF | | RT | | | | | | | 0 | 1 | 1 | 1 | CMPTP | | PD | | RS | | | |
| PRED | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | CMPTP | | PD | | RS | | | |

## 2.13 B

### 2.13.1 Encoding

| 31–29 | 28 | 27 | 26 | 25 | 24–0 |
|---|---|---|---|---|---|
| PRED | 1 | 1 | 0 | 0 | OFFSET |
| PRED | 1 | 1 | 1 | 0 | OFFSET | RS |

## 2.14 BL

### 2.14.1 Encoding

| 31–29 | 28 | 27 | 26 | 25–0 |
|---|---|---|---|---|
| PRED | 1 | 1 | 0 | 1 | OFFSET | |
| PRED | 1 | 1 | 1 | 1 | OFFSET | RS |