

# OSOROM Instruction Set Reference

The Moroso Project

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# Chapter 1

## CPU Architecture

### 1.1 Instructions

Each instruction is a 32-bit word, stored in little-endian order. The top 2 bits of the instruction select a predicate register, and the third bit from the top optionally inverts it. The instruction is only executed if the resulting predicate is true.

### 1.2 Registers

There are 32 32-bit general-purpose registers, R0 through R31. R31 is used as the link register for BL instructions. The program counter is stored separately, and may only be modified through branch instructions and read through BL instructions.

There are three one-bit predicate registers, P0 through P2, that may be written to by compare instructions. A fourth predicate register, P3, is always true. Instructions predicated on P3 will always execute, and writes to P3 are ignored.

### 1.3 ALU Instruction Formats

ALU instructions may accept immediate values for one of their input operands, which come in two forms: Short immediates are embedded in the instruction and consist of a 10-bit constant and a 4-bit rotate amount. To achieve any even rotation between 0 and 30, the rotate amount is first multiplied by 2, and the constant is rotated right by the result. ALU instructions that accept a single operand use the portion of the instruction normally used for the other operand register to extend the constant to 15 bits. Long immediate operands are 32 bit values, and occupy the memory word following the instruction.

If a register is used as the last source operand of an ALU instruction, it may optionally be shifted by a 5-bit immediate value, as specified with the **SHF** and **SHIFTAMT** fields of the instruction. The **SHIFTAMT** field is the amount to shift, between 0 and 31, and the **SHF** field specifies the shift type, as follows:

Encoding	Mnemonic	Shift Type
0 0	LSL	Logical Shift Left
0 1	LSR	Logical Shift Right
1 0	ASR	Arithmetic Shift Right
1 1	ROR	Rotate Right

ALU instructions taking a single operand may also specify a register shifted by an unsigned value contained in another register *Rt*. In this case, the same SHF types are available. If the value of the shift register is greater than 31, the following behavior is used: Logical shifts zero the result, arithmetic right shift extends the sign bit of the operand register across the entire result, and rotate rotates the value by *Rt* % 32.

## 1.4 VLIW

At each time step, the CPU fetches a “packet” of 4 instructions located contiguously in memory and executes them in parallel. These packets must be aligned to their 16-byte size, and branch targets must also be so aligned.

There are three types of instructions: Control, Memory, and ALU instructions. Only one control instruction may be executed in any given packet; it must occupy the first (lowest-address) slot in its packet. Likewise, only the first two slots in a packet may execute memory instructions. ALU instructions may be located in any slot.

If a long immediate operand is specified for an ALU instruction, the following slot is interpreted as an operand and no operation is issued for that slot. The final slot in a packet may not specify a long immediate operand.

## 1.5 Virtual Memory

Virtual memory is accomplished through a hardware-filled TLB, with 4KB pages and a 2-level page-table structure. Page directories and page tables are one page in size, containing 1024 32-bit entries. Virtual addresses are 32 bits and are broken up into 3 parts: Page Directory Index, Page Table Index, and Page Offset, as follows:

3	2	2	1	1	
1	2	1	2	1	0
PD INDEX		PT INDEX		OFFSET	

The page directory base is stored in a coprocessor register, PTBR. Writes to this register will flush all entries not marked global from the TLB. Page table entries and page directory entries are each 32 bits and have the same format:

3	2	2				1	1					
1	9	8				2	1	4	3	2	1	0
RSV		PHYSICAL PAGE BASE					UNUSED		G	K	W	P

The four flags in each entry have the following meanings:

- **G**: Global page. Mappings with this bit set in either level will not be flushed from the TLB when the page table base register is modified.
- **K**: Kernel-only page. Mappings with this bit set in either level may only be read or written to while the processor is in kernel mode. Attempting to access such mappings from user mode will generate a page fault exception.
- **W**: Writeable page. Attempting to write to a page without this bit set in both levels will result in a page fault.

- P: Present. Attempting to access a page without this bit set in both levels will result in a page fault.

Since our FPGA has 512MB of physical memory, physical page bases are 17 bits, and offsets are 12 bits. The top bits of an entry are not used but should remain 0 in case we go to 32-bit physical addresses in the future. Bits 11 through 4 are free for programmer use.

## 1.6 Coprocessor Registers

The coprocessor registers are control registers accessible only in kernel mode via the MFC and MTC instructions. They provide information about exceptions to the kernel and are used to configure the processor. The following coprocessor registers are present:

Encoding	Mnemonic	Purpose
00000	PFLAGS	Processor control flags. Currently only one: Bit 0 is 1 for paging enabled, 0 for paging disabled.
00001	PTB	Page Table Base Register. Specifies the start of the page directory for virtual address translation. Writes to this register flush the TLB.
00010	EHA	Exception Handler Address. Specifies a virtual address to which to transfer control when an exception or interrupt is encountered.
00011	EPC	Error PC. The virtual address of the last instruction packet to cause an exception, or the first instruction not executed due to an interrupt.
00100	EC0	Error Cause 0. The cause of an exception occurring on lane 0, or the type of a received interrupt. See Section 1.7 for a list of causes.
00101	EC1	Error Cause 1. The cause of an exception occurring on lane 1.
00110	EC2	Error Cause 2. The cause of an exception occurring on lane 2.
00111	EC3	Error Cause 3. The cause of an exception occurring on lane 3.
01000	EA0	Error Address 0. If lane 0 makes an invalid memory access, the virtual address it attempted to access will be stored in this register.
01001	EA1	Error Address 1. If lane 1 makes an invalid memory access, the virtual address it attempted to access will be stored in this register.

## 1.7 Exceptions

## Chapter 2

# Instruction Listing











### 2.5.1 Encoding

[illegible]











## 2.10 CMPLEU - Compare Less Than or Equal (Unsigned)

### 2.10.1 Encoding

3 3 2 2 2 2 2 2 2 2 2 2 1																																
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0																																
PRED		0	CONSTANT										ROTATE				0	1	1	1	0	0	1	PD	RS							
PRED		1	0	1	SHIFTAMT				SHF	RT				0	1	1	1	0	0	1	PD	RS										
PRED		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	PD	RS				LIM				

### 2.10.2 Syntax

- CMPLEU[PN] Pd, Rs, #Imm
- CMPLEU[PN] Pd, Rs, Rt [SHF #Imm]

### 2.10.3 Type

CMPLEU is an ALU operation. It may be placed in any slot of a packet. If the long immediate form is used it must not be located in the last slot in a packet, and no instruction may be specified in the following slot.

### 2.10.4 Behavior

CMPLEU interprets its operands as 32-bit unsigned integers, and writes 1 into the specified predicate register if the value of Rs is less than or equal to the value of the second operand, and 0 otherwise.

P3 is pinned to 1. Writes into P3 from compare instructions are ignored.







## 2.14 ERET - Return from Exception

### 2.14.1 Encoding

[illegible]

### 2.14.2 Syntax

- ERET [PN]

### 2.14.3 Type

RET is a Control operation. It may only be placed as the first instruction in a packet. It may only be used when the processor is in kernel mode.

#### 2.14.4 Behavior

ERET returns the processor to user mode from kernel mode, and branches to the memory address contained in the Error PC control register. Other instructions in the same packet as the ERET instruction are executed in kernel mode before control is transferred. This instruction also clears the memory link bit.



## 2.16 FLUSH - Flush L1 Caches

### 2.16.1 Encoding

3 3 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 1																												
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0																												
PRED	1	0	0	0	1	0	1	0	1	C	X	X	X	X	X	X	X	TYPE	X	X	X	X	X	RS				

### 2.16.2 Syntax

- FLUSH[PN] TYPE,  $R_s$

### 2.16.3 Type

FLUSH is a Control operation. It may only be placed as the first instruction in a packet.

### 2.16.4 Behavior

FLUSH invalidates the line in the specified L1 cache corresponding to the virtual address contained in **Rs**. For instruction or data cache flushes, attempting to flush a virtual address whose access would cause a page fault will also cause a page fault. If a dirty data cache line is flushed, the new value is immediately written out to the L2 cache, where it will be visible to DMA peripherals.

Values for the TYPE field are as follows:

Value	Mnemonic	Type
0 0	DATA	L1 Data Cache
0 1	INST	L1 Instruction Cache
1 0	DTLB	Data TLB
1 1	ITLB	Instruction TLB









## 2.20 LW - Load Word

### 2.20.1 Encoding

3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																														</
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### 2.20.2 Syntax

- LW[PN] Rd, (Rs [+ OFFSET])

### 2.20.3 Type

LW is a Memory operation. It may only be placed in the first or second slot in an instruction packet.

### 2.20.4 Behavior

LW loads a word from the specified address into Rd. The address is computed by sign-extending the **OFFSET** field to 32 bits and adding it to the value of **Rs**. Only 4-byte aligned addresses may be accessed - the low 2 bits of the address are ignored.

## 2.21 MFC - Move From Coprocessor Register

### 2.21.1 Encoding

[illegible]

### 2.21.2 Syntax

- MFC [PN] Rd, CPRs

### 2.21.3 Type

MFC is a Control operation. It may only be placed as the first instruction in a packet. It may only be used when the processor is in kernel mode.

### 2.21.4 Behavior

MFC moves the contents of the specified coprocessor register into the specified general-purpose register. See [TODO XXX Link](#) for a description of the available coprocessor registers and their mnemonics.





## 2.24 MTC - Move To Coprocessor Register

### 2.24.1 Encoding

[illegible]

### 2.24.2 Syntax

- MTC [PN] CPRd, Rs

### 2.24.3 Type

MTC is a Control operation. It may only be placed as the first instruction in a packet. It may only be used when the processor is in kernel mode.

### 2.24.4 Behavior

MTC moves the contents of the selected general-purpose register into the specified coprocessor register. See [TODO XXX Link](#) for a description of the available coprocessor registers and their mnemonics.







## 2.27 MULT - Integer Multiplication

### 2.27.1 Encoding

PRED	1	0	0	0	1	1	0	0	0	S	RT	X	X	X	X	RD	RS
------	---	---	---	---	---	---	---	---	---	---	----	---	---	---	---	----	----

### 2.27.2 Syntax

- MULT[PN] Rd, Rs, Rt
- MULTS[PN] Rd, Rs, Rt

### 2.27.3 Type

MULT is a Control operation. It may only be placed as the first instruction in a packet.

### 2.27.4 Behavior

MULT performs an integer multiplication on its two register operands. If the S bit is set, the operands are interpreted as two's complement signed integers; otherwise they are interpreted as unsigned. The low 32 bits of the 64 bit result are placed in the specified destination register, and the high 32 bits are placed in the special-purpose multiply/division overflow register, where they are accessible via the MFHI instruction.

## 2.28 NOR - Bitwise Logical NOR

### 2.28.1 Encoding

3 3 2 2 2 2 2 2 2 2 2 2 1																											
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0																											
PRED	0	CONSTANT										ROTATE					0 0 1 0			RD			RS			LIM	
PRED	1 0 1	SHIFTAMT					SHF	RT					0 0 1 0			RD			RS								
PRED	1 0 0	0 0 0 0 0	0 0 0 0 0 0					0 0 0 0 0 0					0 0 1 0			RD			RS								

### 2.28.2 Syntax

- NOR[PN] Rd, Rs, #Imm
- NOR[PN] Rd, Rs, Rt [SHF #Imm]

### 2.28.3 Type

NOR is an ALU operation. It may be placed in any slot of a packet. If the long immediate form is used it must not be located in the last slot in a packet, and no instruction may be specified in the following slot.

#### 2.28.4 Behavior

Computes the bitwise logical NOR of the two operands, storing the result in the destination register. If two register operands are specified, the second may optionally be shifted by an immediate value before the computation is performed.

## 2.29 OR - Bitwise Logical OR

### 2.29.1 Encoding

3 3 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1																													
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0																													
PRED		0	CONSTANT										ROTATE				0 0 1 1				RD				RS				
PRED		1	0	1	SHIFTAMT					SHF		RT				0 0 1 1				RD				RS					
PRED		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	RD				RS				LIM

### 2.29.2 Syntax

- OR[PN] Rd, Rs, #Imm
- OR[PN] Rd, Rs, Rt [SHF #Imm]

### 2.29.3 Type

OR is an ALU operation. It may be placed in any slot of a packet. If the long immediate form is used it must not be located in the last slot in a packet, and no instruction may be specified in the following slot.

### 2.29.4 Behavior

Computes the bitwise logical OR of the two operands, storing the result in the destination register. If two register operands are specified, the second may optionally be shifted by an immediate value before the computation is performed.





## 2.32 SC - Store Conditional

### 2.32.1 Encoding

3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1																											
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0																											
PRED	1	0	0	1	OFFSETHIGH					RT					M	1	1	1	OFFSETLOW					RS			

### 2.32.2 Syntax

- SC[PN] Rt, (Rs [+ OFFSET])

### 2.32.3 Type

SC is a Memory operation. It may only be placed in the first or second slot in an instruction packet.

### 2.32.4 Behavior

SC stores the value in **Rt** at the provided address, if the processor's link bit is set. The address is computed by sign-extending the **OFFSET** field to 32 bits and adding it to the value of **Rs**. Only 4-byte aligned addresses may be accessed - the low 2 bits of the address are ignored.

The link bit is set by executing the LL instruction, and is cleared by the SC or ERET instructions, or any time an exception or interrupt is dispatched. SC only completes if the link bit is set when it is executed - thus, if it completes, all instructions since the last LL instruction are known to have been executed atomically. The SC instruction writes a 1 into predicate register 0 if the store completes successfully, or a 0 if it fails.

The **OFFSET** field for stores is broken up into 3 parts: {inst[24:19], inst[13], inst[9:5]}.

### 2.33 SH - Store Half-Word

### 2.33.1 Encoding

[illegible]

### 2.33.2 Syntax

- SH[PN] Rt, (Rs [+ OFFSET])

### 2.33.3 Type

SH is a Memory operation. It may only be placed in the first or second slot in an instruction packet.

#### 2.33.4 Behavior

SH stores the low two bytes of **Rt** at the provided address. The address is computed by sign-extending the **OFFSET** field to 32 bits and adding it to the value of **Rs**. The address must be aligned to a multiple of 2; the low bit of the address is ignored.

The **OFFSET** field for stores is broken up into 3 parts: {inst[24:19], inst[13], inst[9:5]}.







## 2.36 SXB - Sign-Extend Byte

### 2.36.1 Encoding

3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 1 1																														
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0																														
PRED	0	CONSTLOW										ROTATE					1	0	1	0	RD					CONSTHI				
PRED	1	0	1	SHIFTAMT					SHF	X	X	X	X	X	1	0	0	1	RD					RS						
PRED	1	0	0	0	0	0	0	1	SHF	RT					1	0	1	0	RD					RS						
PRED	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	RD					RS					LIM	

### 2.36.2 Syntax

- SXB[PN] Rd, #Imm
- SXB[PN] Rd, Rs [SHF #Imm]
- SXB[PN] Rd, Rs SHF Rt

### 2.36.3 Type

SXB is an ALU operation. It may be placed in any slot of a packet. If the long immediate form is used it must not be located in the last slot in a packet, and no instruction may be specified in the following slot.

### 2.36.4 Behavior

SXB moves the low byte of its source operand into the specified destination register, sign-extending it across the rest of the register. If the second operand is a register, it may be shifted by an immediate value or by the contents of a register before being stored.





## 2.39 XOR - Bitwise Exclusive OR

### 2.39.1 Encoding

3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
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### 2.39.2 Syntax

- XOR[PN] Rd, Rs, #Imm
- XOR[PN] Rd, Rs, Rt [SHF #Imm]

### 2.39.3 Type

XOR is an ALU operation. It may be placed in any slot of a packet. If the long immediate form is used it must not be located in the last slot in a packet, and no instruction may be specified in the following slot.

### 2.39.4 Behavior

Computes the bitwise logical XOR of the two operands, storing the result in the destination register. If two register operands are specified, the second may optionally be shifted by an immediate value before the computation is performed.