

OSOROM Instruction Set Reference

The Moroso Project

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Chapter 1

CPU Architecture

1.1 Instructions

Each instruction is a 32-bit word, stored in little-endian order. The top 2 bits of the instruction select a predicate register, and the third bit from the top optionally inverts it. The instruction is only executed if the resulting predicate is true.

1.2 Registers

There are 32 32-bit general-purpose registers, R0 through R31. R31 is used as the link register for BL instructions. The program counter is stored separately, and may only be modified through branch instructions and read through BL instructions.

There are three one-bit predicate registers, P0 through P2, that may be written to by compare instructions. A fourth predicate register, P3, is always true. Instructions predicated on P3 will always execute, and writes to P3 are ignored.

1.3 ALU Instruction Formats

ALU instructions may accept immediate values for one of their input operands, which come in two forms: Short immediates are embedded in the instruction and consist of a 10-bit constant and a 4-bit rotate amount. To achieve any even rotation between 0 and 30, the rotate amount is first multiplied by 2, and the constant is rotated right by the result. ALU instructions that accept a single operand use the portion of the instruction normally used for the other operand register to extend the constant to 15 bits. Long immediate operands are 32 bit values, and occupy the memory word following the instruction.

If a register is used as the last source operand of an ALU instruction, it may optionally be shifted by a 5-bit immediate value, as specified with the **SHF** and **SHIFTAMT** fields of the instruction. The **SHIFTAMT** field is the amount to shift, between 0 and 31, and the **SHF** field specifies the shift type, as follows:

Encoding	Mnemonic	Shift Type
0 0	LSL	Logical Shift Left
0 1	LSR	Logical Shift Right
1 0	ASR	Arithmetic Shift Right
1 1	ROR	Rotate Right

ALU instructions taking a single operand may also specify a register shifted by an unsigned value contained in another register *Rt*. In this case, the same SHF types are available. If the value of the shift register is greater than 31, the following behavior is used: Logical shifts zero the result, arithmetic right shift extends the sign bit of the operand register across the entire result, and rotate rotates the value by *Rt* % 32.

1.4 VLIW

At each time step, the CPU fetches a “packet” of 4 instructions located contiguously in memory and executes them in parallel. These packets must be aligned to their 16-byte size, and branch targets must also be so aligned.

There are three types of instructions: Control, Memory, and ALU instructions. Only one control instruction may be executed in any given packet; it must occupy the first (lowest-address) slot in its packet. Likewise, only the first two slots in a packet may execute memory instructions. ALU instructions may be located in any slot.

If a long immediate operand is specified for an ALU instruction, the following slot is interpreted as an operand and no operation is issued for that slot. The final slot in a packet may not specify a long immediate operand.

1.5 Virtual Memory

Virtual memory is accomplished through a hardware-filled TLB, with 4KB pages and a 2-level page-table structure. Page directories and page tables are one page in size, containing 1024 32-bit entries. Virtual addresses are 32 bits and are broken up into 3 parts: Page Directory Index, Page Table Index, and Page Offset, as follows:

3	2 2	1 1	
1	2 1	2 1	0
PD INDEX		PT INDEX	OFFSET

The page directory base is stored in a coprocessor register, *PTBR*. Writes to this register will flush all entries not marked global from the TLB. Page table entries and page directory entries are each 32 bits and have the same format:

3	2 2	1 1					
1	9 8	2 1	4	3	2	1	0
RSV	PHYSICAL PAGE BASE		UNUSED	G	K	W	P

The four flags in each entry have the following meanings:

- **G**: Global page. Mappings with this bit set in either level will not be flushed from the TLB when the page table base register is modified.
- **K**: Kernel-only page. Mappings with this bit set in either level may only be read or written to while the processor is in kernel mode. Attempting to access such mappings from user mode will generate a page fault exception.
- **W**: Writeable page. Attempting to write to a page without this bit set in both levels will result in a page fault.

- P: Present. Attempting to access a page without this bit set in both levels will result in a page fault.

Since our FPGA has 512MB of physical memory, physical page bases are 17 bits, and offsets are 12 bits. The top bits of an entry are not used but should remain 0 in case we go to 32-bit physical addresses in the future. Bits 11 through 4 are free for programmer use.

1.6 Coprocessor Registers

The coprocessor registers are control registers accessible only in kernel mode via the MFC and MTC instructions. They provide information about exceptions to the kernel and are used to configure the processor.

1.6.1 List of Coprocessor Registers

Encoding	Mnemonic	Purpose
00000	PFLAGS	Processor control flags. See below.
00001	PTB	Page Table Base Register. Specifies the start of the page directory for virtual address translation. Writes to this register flush the TLB.
00010	EHA	Exception Handler Address. Specifies a virtual address to which to transfer control when an exception or interrupt is encountered.
00011	EPC	Error PC. The virtual address of the last instruction packet to cause an exception, or the first instruction not executed due to an interrupt.
00100	EC0	Error Cause 0. The cause of an exception occurring on lane 0, or the type of a received interrupt. See Section 1.7 for a list of causes.
00101	EC1	Error Cause 1. The cause of an exception occurring on lane 1.
00110	EC2	Error Cause 2. The cause of an exception occurring on lane 2.
00111	EC3	Error Cause 3. The cause of an exception occurring on lane 3.
01000	EA0	Error Address 0. If lane 0 makes an invalid memory access, the virtual address it attempted to access will be stored in this register.
01001	EA1	Error Address 1. If lane 1 makes an invalid memory access, the virtual address it attempted to access will be stored in this register.

1.6.2 The PFLAGS Register

At present, the PFLAGS register contains 2 flags: Bit 0 is 1 if interrupts are enabled, and bit 1 is 1 if paging is enabled. More control flags may be added here if needed.

1.7 Exceptions and Interrupts

Exceptions and interrupts cause the processor to enter kernel mode and transfer control to the virtual address specified in the EHA register. If an interrupt occurs, the code corresponding to that interrupt will be written into the EC0 register. If one or more instructions in a packet cause exceptions, a code corresponding to the exception type will be written into the EC register corresponding to that instruction's location in the packet. If an instruction on lane 0 or 1 attempts to access an invalid memory address, the address will be written into the EA register for that lane.

In all cases, the virtual address of the program counter where the exception occurred is written into the EPC register. For exceptions, this is the address of the instruction packet that caused the exception. For interrupts, this is the address of the first instruction packet not executed due to the interrupt. In all cases, interrupts are disabled. This is necessary in order to ensure the kernel can save the coprocessor registers before they are overwritten by another interrupt.

1.7.1 Error Code Format

3																	
1				8				7		6		5		1		0	
RESERVED								INT		EXNTYPE		M					

- **M** is 1 if the processor was in kernel mode when the exception or interrupt occurred, or 0 otherwise.
- **EXNTYPE** corresponds to a value in Table 1.1 and indicates the type of exception that occurred.
- If **EXNTYPE** indicates that an interrupt occurred, **INT** will correspond to a value in Table 1.2 and signify the type of interrupt.

Error Code	Type
00000	No Error
00001	Page Fault on Instruction Fetch
00010	Illegal Instruction
00011	Duplicate Destination
00100	Page Fault on Data Access
00101	Invalid Physical Address
00110	Divide by Zero (TODO are we doing other arithmetic exceptions??)
00111	Interrupt
01000	SYSCALL
01001	BREAK

Table 1.1: Exception Codes

Interrupt Code	Type
00	Timer
01	USB
10	Framebuffer
11	SD Card

Table 1.2: Interrupt Codes

Chapter 2

Instruction Set Summary

2.1 Instruction Set Encoding

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALU 1-Op Short	Pred	0	Immediate Low 10										Rotate			ALU Opcode				Rd		Imm High 5										
ALU 2-Op Short	Pred	0	Immediate 10										Rotate			ALU Opcode				Rd		Rs										
Compare Short	Pred	0	Immediate 10										Rotate			0	1	1	1	Ctype		Pn	Rs									
ALU Register	Pred	1	0	1	Shift amount				Stype		Rt			ALU Opcode				Rd		Rs												
Compare Register	Pred	1	0	1	Shift amount				Stype		Rt			0	1	1	1	Ctype		Pn	Rs											
Load	Pred	1	0	0	1	Offset 12										LSU Opcode			Rd		Rs											
Store	Pred	1	0	0	1	Offset High 6					Rt			M	LSU Opcode			Offset Low 5			Rs											
Branch immediate	Pred	1	1	0	L	Offset 25																										
Branch register	Pred	1	1	0	L	Offset 20																			Rs							
Control	Pred	1	0	0	0	1	Ctrl Opcode High					Rt			Ctrl Opcode Low				Rd		Rs											
ALU 1-Op Regsh	Pred	1	0	0	0	0	0	0	1	Stype		Rt			ALU Opcode				Rd		Rs											
ALU Long	Pred	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ALU Opcode				Rd		Rs			Imm 32						
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Chapter 3

Instruction Listing

3.2 AND - Bitwise And

3.2.1 Encoding

3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
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3.2.2 Syntax

- AND[PN] Rd, Rs, #Imm
- AND[PN] Rd, Rs, Rt [SHF #Imm]

3.2.3 Type

AND is an ALU operation. It may be placed in any slot of a packet. If the long immediate form is used it must not be located in the last slot in a packet, and no instruction may be specified in the following slot.

3.2.4 Behavior

Computes the bitwise logical AND of the two operands, storing the result in the destination register. If two register operands are specified, the second may optionally be shifted by an immediate value before the computation is performed.

3.5 BREAK - TODO XXX

3.5.1 Encoding

[illegible]

3.6 CMPBC - Compare Bits Clear

3.6.1 Encoding

3 3 2 2 2 2 2 2 2 2 2 2 1																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																		
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																		
PRED		0	CONSTANT										ROTATE					0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

3.6.2 Syntax

- CMPBC[PN] Pd, Rs, #Imm
- CMPBC[PN] Pd, Rs, Rt [SHF #Imm]

3.6.3 Type

CMPBC is an ALU operation. It may be placed in any slot of a packet. If the long immediate form is used it must not be located in the last slot in a packet, and no instruction may be specified in the following slot.

3.6.4 Behavior

CMPBC checks each bit of Rs corresponding to a 1 bit in the second operand, writing 1 into the destination predicate if all such bits are 0, and writing 0 otherwise – that is, it computes the unary OR of the bits in ($\sim Rs \ \& \ OP2$) and stores the result in the desired predicate.

P3 is pinned to 1. Writes into P3 from compare instructions are ignored.

3.7 CMPBS - Compare Bits Set

3.7.1 Encoding

3 3 2 2 2 2 2 2 2 2 2 2 1																													
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0																													
PRED		0	CONSTANT										ROTATE					0 1 1 1				1 1 0			PD		RS		
PRED		1 0 1			SHIFTAMT					SHF		RT					0 1 1 1				1 1 0			PD		RS			
PRED		1 0 0			0 0 0 0 0					0 0 0		0 0 0 0 0					0 1 1 1				1 1 0			PD		RS			LONG

3.7.2 Syntax

- CMPBS[PN] Pd, Rs, #Imm
- CMPBS[PN] Pd, Rs, Rt [SHF #Imm]

3.7.3 Type

CMPBS is an ALU operation. It may be placed in any slot of a packet. If the long immediate form is used it must not be located in the last slot in a packet, and no instruction may be specified in the following slot.

3.7.4 Behavior

CMPBS checks each bit of Rs corresponding to a 1 bit in the second operand, writing 1 into the destination predicate if any such bit is 1, and writing 0 otherwise – that is, it computes the unary OR of the bits in (Rs & OP2) and stores the result in the desired predicate. P3 is pinned to 1. Writes into P3 from compare instructions are ignored.

3.8 CMPEQ - Compare Equal

3.8.1 Encoding

3 3 2 2 2 2 2 2 2 2 2 2 1																															
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0																															
PRED		0	CONSTANT										ROTATE					0 1 1 1				0 1 0			PD		RS				
PRED		1 0 1			SHIFTAMT					SHF		RT					0 1 1 1				0 1 0			PD		RS					
PRED		1 0 0			0 0 0 0 0 0					0 0 0		0 0 0 0 0					0 1 1 1				0 1 0			PD		RS				LONG	

3.8.2 Syntax

- CMPEQ[PN] Pd, Rs, #Imm
- CMPEQ[PN] Pd, Rs, Rt [SHF #Imm]

3.8.3 Type

CMPEQ is an ALU operation. It may be placed in any slot of a packet. If the long immediate form is used it must not be located in the last slot in a packet, and no instruction may be specified in the following slot.

3.8.4 Behavior

CMPEQ tests whether its two operands are equal, writing 1 into the destination predicate if they are and 0 otherwise.

P3 is pinned to 1. Writes into P3 from compare instructions are ignored.

3.10 CMPLEU - Compare Less Than or Equal (Unsigned)

3.10.1 Encoding

3 3 2 2 2 2 2 2 2 2 2 2 1																													
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0																													
PRED		0	CONSTANT										ROTATE					0 1 1 1				0 0 1			PD		RS		
PRED		1 0 1			SHIFTAMT					SHF		RT					0 1 1 1				0 0 1			PD		RS			
PRED		1 0 0			0 0 0 0 0					0 0		0 0 0 0 0					0 1 1 1				0 0 1			PD		RS			LONG

3.10.2 Syntax

- CMPLEU[PN] Pd, Rs, #Imm
- CMPLEU[PN] Pd, Rs, Rt [SHF #Imm]

3.10.3 Type

CMPLEU is an ALU operation. It may be placed in any slot of a packet. If the long immediate form is used it must not be located in the last slot in a packet, and no instruction may be specified in the following slot.

3.10.4 Behavior

CMPLEU interprets its operands as 32-bit unsigned integers, and writes 1 into the specified predicate register if the value of Rs is less than or equal to the value of the second operand, and 0 otherwise.

P3 is pinned to 1. Writes into P3 from compare instructions are ignored.

3.12 CMPLTU - Compare Less Than (Unsigned)

3.12.1 Encoding

3 3 2 2 2 2 2 2 2 2 2 2 1																													
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0																													
PRED		0	CONSTANT										ROTATE				0	1	1	1	0	0	0	PD	RS				
PRED		1	0	1	SHIFTAMT				SHF	RT				0	1	1	1	0	0	0	PD	RS							
PRED		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	PD	RS				LONG

3.12.2 Syntax

- CMPLTU[PN] Pd, Rs, #Imm
- CMPLTU[PN] Pd, Rs, Rt [SHF #Imm]

3.12.3 Type

CMPLTU is an ALU operation. It may be placed in any slot of a packet. If the long immediate form is used it must not be located in the last slot in a packet, and no instruction may be specified in the following slot.

3.12.4 Behavior

CMPLTU interprets its operands as 32-bit unsigned integers, and writes 1 into the specified predicate register if the value of **Rs** is less than to the value of the second operand, and 0 otherwise. P3 is pinned to 1. Writes into P3 from compare instructions are ignored.

3.13 DIV - Integer Division

3.13.1 Encoding

PRED	1	0	0	0	1	1	0	0	1	X	RT	X	X	X	X	RD	RS
------	---	---	---	---	---	---	---	---	---	---	----	---	---	---	---	----	----

3.13.2 Syntax

- DIV[PN] Rd, Rs, Rt

3.13.3 Type

DIV is a Control operation. It may only be placed as the first instruction in a packet.

3.13.4 Behavior

Performs the integer division **R**s / **R**t, writing the quotient into **R**d and the remainder into the multiply/divide overflow register.

3.14 ERET - Return from Exception

3.14.1 Encoding

[illegible]

3.14.2 Syntax

- ERET [PN]

3.14.3 Type

RET is a Control operation. It may only be placed as the first instruction in a packet. It may only be used when the processor is in kernel mode.

3.14.4 Behavior

ERET returns the processor to user mode from kernel mode, and branches to the memory address contained in the Error PC control register. Other instructions in the same packet as the ERET instruction are executed in kernel mode before control is transferred. This instruction also clears the memory link bit.

3.15 FENCE

3.15.1 Encoding

[illegible]

3.15.2 Syntax

- FENCE [PN]

3.15.3 Type

FENCE is a Control operation. It may only be placed as the first instruction in a packet.

3.15.4 Behavior

Our architecture doesn't reorder requests, so right now FENCE is a no-op. If we have to add behavior to it in the future, memory instructions in the same packet as the FENCE will probably go after it, but please don't count on that right now.

3.16 FLUSH - Flush L1 Caches

3.16.1 Encoding

3 3 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1																												
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0																												
PRED	1	0	0	0	1	0	1	0	1	C	X	X	X	X	X	X	X	TYPE	X	X	X	X	X	RS				

3.16.2 Syntax

- FLUSH[PN] TYPE, R_s

3.16.3 Type

FLUSH is a Control operation. It may only be placed as the first instruction in a packet.

3.16.4 Behavior

FLUSH invalidates the line in the specified L1 cache corresponding to the virtual address contained in **Rs**. For instruction or data cache flushes, attempting to flush a virtual address whose access would cause a page fault will also cause a page fault. If a dirty data cache line is flushed, the new value is immediately written out to the L2 cache, where it will be visible to DMA peripherals.

Values for the TYPE field are as follows:

Value	Mnemonic	Type
0 0	DATA	L1 Data Cache
0 1	INST	L1 Instruction Cache
1 0	DTLB	Data TLB
1 1	ITLB	Instruction TLB

3.17 LB - Load Byte

3.17.1 Encoding

3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																														
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3.17.2 Syntax

- LB[PN] Rd, (Rs [+ OFFSET])

3.17.3 Type

LB is a Memory operation. It may only be placed in the first or second slot in an instruction packet.

3.17.4 Behavior

LB loads a byte from the specified address into **Rd**. The address is computed by sign-extending the **OFFSET** field to 32 bits and adding it to the value of **Rs**. The high 24 bits of **Rd** are zeroed.

3.18 LH - Load Half-Word

3.18.1 Encoding

[illegible]

3.18.2 Syntax

- LH[PN] Rd, (Rs [+ OFFSET])

3.18.3 Type

LH is a Memory operation. It may only be placed in the first or second slot in an instruction packet.

3.18.4 Behavior

LH loads two bytes from the specified address into **Rd**. The address is computed by sign-extending the **OFFSET** field to 32 bits and adding it to the value of **Rs**. Only 2-byte aligned addresses may be accessed - the low bit of the address is ignored. The high 16 bits of **Rd** are zeroed.

3.19 LL - Load Linked

3.19.1 Encoding

[illegible]

3.19.2 Syntax

- $LL[PN] \text{ Rd}, (Rs [+ \text{OFFSET}])$

3.19.3 Type

LL is a Memory operation. It may only be placed in the first or second slot in an instruction packet.

3.19.4 Behavior

LL loads a word from the specified address into **Rd**. The address is computed by sign-extending the **OFFSET** field to 32 bits and adding it to the value of **Rs**. Only 4-byte aligned addresses may be accessed - the low 2 bits of the address are ignored.

Additionally, LL sets the link bit. A future SC operation will only complete if no interrupt, exception, or ERET clears the link bit in the intervening period.

3.20 LW - Load Word

3.20.1 Encoding

[illegible]

3.20.2 Syntax

- LW[PN] Rd, (Rs [+ OFFSET])

3.20.3 Type

LW is a Memory operation. It may only be placed in the first or second slot in an instruction packet.

3.20.4 Behavior

LW loads a word from the specified address into Rd. The address is computed by sign-extending the **OFFSET** field to 32 bits and adding it to the value of **Rs**. Only 4-byte aligned addresses may be accessed - the low 2 bits of the address are ignored.

3.23 MOV - Move

3.23.1 Encoding

3 3 2 2 2 2 2 2 2 2 2 2 1																														
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0																														
PRED		0	CONSTLOW								ROTATE				1 0 0 0				RD				CONSTHI							
PRED		1	0	1	SHIFTAMT				SHF	RT				1 0 0 0				RD				X X X X X								
PRED		1	0	0	0	0	0	0	1	SHF	RT				1 0 0 0				RD				X X X X X							
PRED		1	0	0	0	0	0	0	0	0	0	0	0	0	0	1 0 0 0				RD				X X X X X						LONG

3.23.2 Syntax

- MOV[PN] Rd, #Imm
- MOV[PN] Rd, Rt [SHF #Imm]
- MOV[PN] Rd, Rt SHF Rs

3.23.3 Type

MOV is an ALU operation. It may be placed in any slot of a packet. If the long immediate form is used it must not be located in the last slot in a packet, and no instruction may be specified in the following slot.

3.23.4 Behavior

MOV moves the value of its source operand into the specified destination register. If the second operand is a register, it may be shifted by an immediate value or by the contents of a register before being stored.

3.24 MTC - Move To Coprocessor Register

3.24.1 Encoding

[illegible]

3.24.2 Syntax

- MTC [PN] CPRd, Rs

3.24.3 Type

MTC is a Control operation. It may only be placed as the first instruction in a packet. It may only be used when the processor is in kernel mode.

3.24.4 Behavior

MTC moves the contents of the selected general-purpose register into the specified coprocessor register. See Section 1.6 for a description of the available coprocessor registers and their mnemonics.

3.30 RSB - Reverse Subtraction

3.30.1 Encoding

3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0

PRED	0	CONSTANT				ROTATE				0 1 0 1	RD	RS	
PRED	1 0 1	SHIFTAMT		SHF	RT				0 1 0 1	RD	RS		
PRED	1 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 1 0 1	RD	RS	LONG	

3.30.2 Syntax

- RSB[PN] Rd, Rs, #Imm
- RSB[PN] Rd, Rs, Rt [SHF #Imm]

3.30.3 Type

RSB is an ALU operation. It may be placed in any slot of a packet. If the long immediate form is used it must not be located in the last slot in a packet, and no instruction may be specified in the following slot.

3.30.4 Behavior

Subtracts the value stored in RS from the value of the second operand, storing the result in the destination register. If two register operands are specified, the second may optionally be shifted by an immediate value before the computation is performed.

3.31 SB - Store Byte

3.31.1 Encoding

[illegible]

3.31.2 Syntax

- SB[PN] Rt, (Rs [+ OFFSET])

3.31.3 Type

SB is a Memory operation. It may only be placed in the first or second slot in an instruction packet.

3.31.4 Behavior

SB stores the low byte of **Rt** at the provided address. The address is computed by sign-extending the **OFFSET** field to 32 bits and adding it to the value of **Rs**.

The **OFFSET** field for stores is broken up into 3 parts: {inst[24:19], inst[13], inst[9:5]}.

3.34 SUB - Subtraction

3.34.1 Encoding

3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
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3.34.2 Syntax

- SUB[PN] Rd, Rs, #Imm
- SUB[PN] Rd, Rs, Rt [SHF #Imm]

3.34.3 Type

SUB is an ALU operation. It may be placed in any slot of a packet. If the long immediate form is used it must not be located in the last slot in a packet, and no instruction may be specified in the following slot.

3.34.4 Behavior

Subtracts the value of the second operand from the value in **Rs**, storing the result in the destination register. If two register operands are specified, the second may optionally be shifted by an immediate value before the computation is performed.

3.38 SYSCALL - TODO XXX

3.38.1 Encoding

[illegible]

3.39 XOR - Bitwise Exclusive OR

3.39.1 Encoding

[illegible]

3.39.2 Syntax

- XOR[PN] Rd, Rs, #Imm
- XOR[PN] Rd, Rs, Rt [SHF #Imm]

3.39.3 Type

XOR is an ALU operation. It may be placed in any slot of a packet. If the long immediate form is used it must not be located in the last slot in a packet, and no instruction may be specified in the following slot.

3.39.4 Behavior

Computes the bitwise logical XOR of the two operands, storing the result in the destination register. If two register operands are specified, the second may optionally be shifted by an immediate value before the computation is performed.