WEBER STATE UNIVERSITY
Engineering, Applied Science & Technology

— DEPARTMENT OF —
ELECTRICAL & COMPUTER
ENGINEERING

VDD

SW1
CHS-08B

1	1	16	16	B-7
2	2	15	15	A-7
3	3	14	14	C-6
4	4	13	13	B-6
5	5	12	12	A-6
6	6	11	11	C-5
7	7	10	10	B-5
8	8	9	9	A-5

U1.2
C8051F020-GQR

62	P0.0	P1.0/AIN1.0/A8	36
61	P0.1	P1.1/AIN1.1/A9	35
60	P0.2	P1.2/AIN1.2/A10	34
59	P0.3	P1.3/AIN1.3/A11	33
58	P0.4	P1.4/AIN1.4/A12	32
57	P0.5/ALE	P1.5/AIN1.5/A13	31
56	P0.6/RD	P1.6/AIN1.6/A14	30
55	P0.7/WR	P1.7/AIN1.7/A15	29

46	A8m/A0/P2.0	P3.0/AD0/D0	54
45	A9m/A1/P2.1	P3.1/AD1/D1	53
44	A10m/A2/P2.2	P3.2/AD2/D2	52
43	A11m/A3/P2.3	P3.3/AD3/D3	51
42	A12m/A4/P2.4	P3.4/AD4/D4	50
41	A13m/A5/P2.5	P3.5/AD5/D5	49
40	A14m/A6/P2.6	P3.6/AD6/D6/IE6	48
39	A15m/A7/P2.7	P3.7/AD7/D7/IE7	47

98	P4.0	P5.0/A8	88
97	P4.1	P5.1/A9	87
96	P4.2	P5.2/A10	86
95	P4.3	P5.3/A11	85
94	P4.4	P5.4/A12	84
93	P4.5/ALE	P5.5/A13	83
92	P4.6/RD	P5.6/A14	82
91	P4.7/WR	P5.7/A15	81

80	A8m/A0/P6.0	AD0/D0/P7.0	72
79	A9m/A1/P6.1	AD1/D1/P7.1	71
78	A10m/A2/P6.2	AD2/D2/P7.2	70
77	A11m/A3/P6.3	AD3/D3/P7.3	69
76	A12m/A4/P6.4	AD4/D4/P7.4	68
75	A13m/A5/P6.5	AD5/D5/P7.5	67
74	A14m/A6/P6.6	AD6/D6/P7.6	66
73	A15m/A7/P6.7	AD7/D7/P7.7	65

SW1
1 2
3 4   C-4

SW2
1 2
3 4   B-4

GND

C-20   LED1   R1 1k
B-20   LED2   R2 1k
A-20   LED3   R3 1k
C-19   LED4   R4 1k
B-19   LED5   R5 1k
A-19   LED6   R6 1k
C-18   LED7   R7 1k
B-18   LED8   R8 1k
A-10   LED9   R9 1k
C-9   LED10   R10 1k

NOTES:

1) AVOID PORT 0 (BITS 0 AND 1 WILL BE USED FOR THE SERIAL PORT)
   AND AVOID PORTS 4, 6 AND 7 (THESE WILL BE USED FOR BUS EXPANSION LATER).
   MAKE THE LEDS TURN ON WHEN THE CORRESPONDING PORT LINES ARE LOW.
2) BOTH LED COM PORTS NEED TO BE CONNECTED TO VDD (A1)

TITLE:
Lab02 Input/Output

REV: 1.1

Company: ECE3710

Sheet: 1/1

Date: 2023-01-23   Drawn By: Jacob Watts