1. Why can’t you use both pins PA0 and PC0 for external interrupts at the same time?

   The EXTI0 multiplexer can only have one go through at a time

2. What software priority level gives the highest priority? What level gives the lowest?

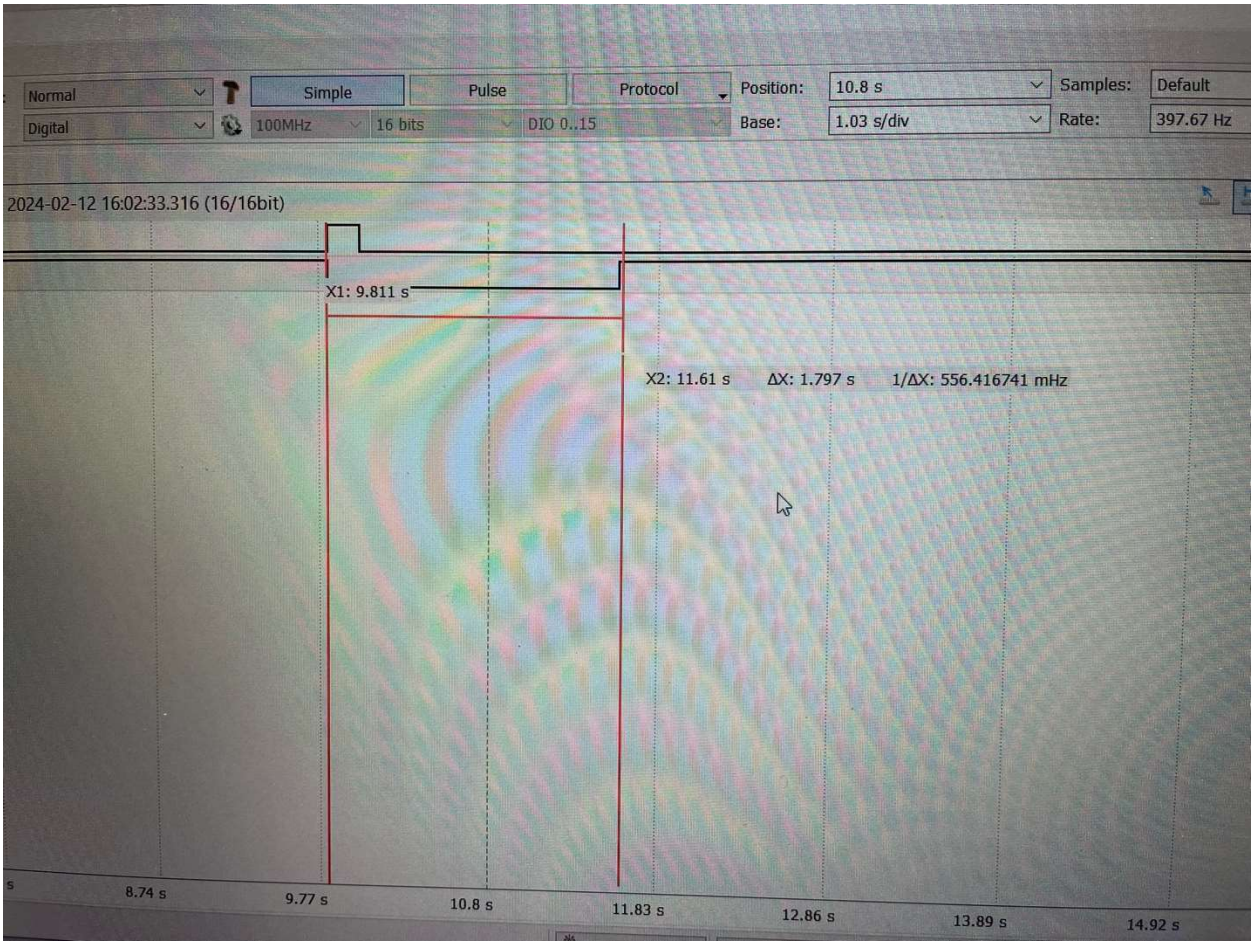
   0 is the highest priority, 3 is the lowest priority

3. How many bits does the NVIC have reserved in its priority (IPR) registers for each interrupt (including non-implemented bits)? Which bits in the group are implemented?

   2 bits

4. What was the latency between pushing the Discovery board button and the LED change (interrupt handler start) that you measured with the logic analyzer? Make sure to include a screenshot in the post-lab submission.

   About 1.8 seconds



5. Why do you need to clear status flag bits in peripherals when servicing their interrupts?

   To signal that the interrupt is handled