6.2 — Postlab 6. Please answer the following questions about the ADC and DAC, and submit your source code.

1. Consider a system where the DAC is updated every 4us (250 kHz) with a value from a 200- element wave table containing a single cycle of a waveform. What would be the frequency of the output wave?

250 kHz / 200 samples = 1.25 kHz

2. Consider that the ADC in 12-bit mode divides the input voltage range (0-3V) into 4096 steps (where 0V is 0, and 3V is 4095).

• What is the voltage/measurement resolution (how much does the voltage change per bit) of the ADC?

3V / 4095 steps = 3/4095 v/steps

• What would be the ADC output value (nearest integer) if the input voltage was 1.75V?

1.75V * 4095/3 steps/V = 2388.75 or 2389 steps