Jack Payne

thejackpayne@gmail.com • (352)-942-4648 • jackpayne.space • https://www.linkedin.com/in/jack-lpayne/

Education

University of Florida – BS Computer Engineering (3.75 GPA) May 2024 - Present

- **Relevant coursework:** Microprocessor Applications, Signals & Systems, Data Structures & Algorithms, OS
- **Current coursework:** Real-Time DSP, VLSI, Digital Design, Neural Interfaces & Systems

Santa Fe College – AA (3.8 GPA) April 2024

Projects

Adaptive Narrowband Interference Suppressor for SDRs https://github.com/jacklpayne/anis-sdr

- Developed adaptive multi-notch IIR filter in C++ as GNU Radio block, combining intermittent FFT-based spike detection with time-domain tracking of drifting interferers via gradient descent at up to 50MHz sample rates
- Achieved signal power recovery >99% across test harnesses using synthetic noise, satellite data, and EEG data

RTOS-Based Sensor Monitoring and Telemetry System https://github.com/jacklpayne/rtos-telem

- Created producer-consumer pipeline on STM32 (C) with acquisition, analysis, and transmission RTOS tasks to communicate signal metrics via UART across test ADC injections at 1kHz sampling rates
- Leveraged priority-based scheduling with FreeRTOS queues to synchronize tasks and minimize dropped samples

EEG Data Acquisition Pipeline https://github.com/jacklpayne/Gh05t

- Integrated ATMega MCU and biosignal ADC for real-time 8-channel capture of <5µV biosignals
- Wrote ADC library API (C) and designed SPI/I2C communication flows, reducing signal noise by over 90%
- Integrating system with OpenBCI headset and electrodes, developing affordable alternative to their board

Embedded Real-Time Music Creation System https://github.com/jacklpayne/Brizachord

- Designed STM32-based embedded instrument with concurrent I2C and GPIO peripherals orchestrated in C++
- Brought up PCB with LTSpice and KiCad integrating sensors and Class-D audio output, achieving <50ms I/O latency

Work Experience

Research Assistant, Hybrid Photonics (CHIP) Lab, University of Florida August 2023 – July 2025

- Developed signal pipeline with Python and MATLAB to load RF-encoded image data through Zynq FPGA RFSoC and stream to photonic chip via optical cable for AI acceleration
- Wrote RF test signals in MATLAB to validate edge cases, improving coverage by 100%

Teaching Assistant, Electronic Circuits I, University of Florida July 2025 – Present

- Train 20+ lab students in circuit analysis and use of oscilloscopes, function generators, and multimeters
- Streamlined lab documents for 200+ students, maintaining 100% positive student evaluation score

Leadership

Chief of Research, IEEE Signal Processing Society, University of Florida August 2025 – Present

- Lead 6 research groups towards publication by managing biosignals, audio ML, and wearables projects

Hardware/Software Lead, Audio Engineering Society, University of Florida May 2025 – Present

- Develop embedded workshops teaching both DSP principles and electronic design to 80+ attendees

Skills

Languages: C/C++, VHDL/Verilog, Python, Rust
Software: STM32CubeIDE, MATLAB, FreeRTOS, GNURadio, Vivado/Vitis, Quartus, KiCad, LTSpice, Git, Linux