

Introduction to Digital Logic

EECS/CSE 31L

Assignment 1: 1-Bit Full Adder/Subtractor

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1 Block Description

Take in two 1-bit inputs and perform addition or subtraction

2 Input/Output Port Description

Port name	Port size	Port Type	Description
Input0	1	IN	Value of first input
Input1	1	IN	Value of second input
CarryIn	1	IN	Carry in value
AddORSub	1	IN	Determine which operation to perform
Sum	1	IN	The operation result
CarryOut	1	IN	The carry out value

3 Design Schematics

Truth Tables:

Original Full Adder

In_0	In_1	Cin	Cout	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Two's Complement Adder/Subtractor

AddOrSub	Function	Operation
0	$In_0 + In_1$	Addition
1	$In_0 + In_1' + 1$	Subtraction

In_1 XOR AddOrSub

In_1	AddOrSub	
0	0	0
0	1	1
1	0	1
1	1	0

Full Adder/Subtractor

In_0	In_1	Cin	Cout	Sum
0	0	0	0	0
0	1	0	0	1
1	0	0	0	1
1	1	0	1	0
0	0	1	1	0
0	1	1	0	1
1	0	1	1	1
1	1	1	1	0

Boolean Expressions:

$$In_1 = In_1 \oplus AddOrSub$$

$$Cin = AddOrSub$$

$$Sum = (In_0')(In_1')(Cin) + (In_0')(In_1)(Cin') + (In_0)(In_1')(Cin') + (In_0)(In_1)(Cin)$$

$$Cout = (In_0')(In_1)(Cin) + (In_0)(In_1')(Cin) + (In_0)(In_1)(Cin') + (In_0)(In_1)(Cin)$$

$$In_1 = In_1 \oplus AddOrSub$$

$$Cin = AddOrSub$$

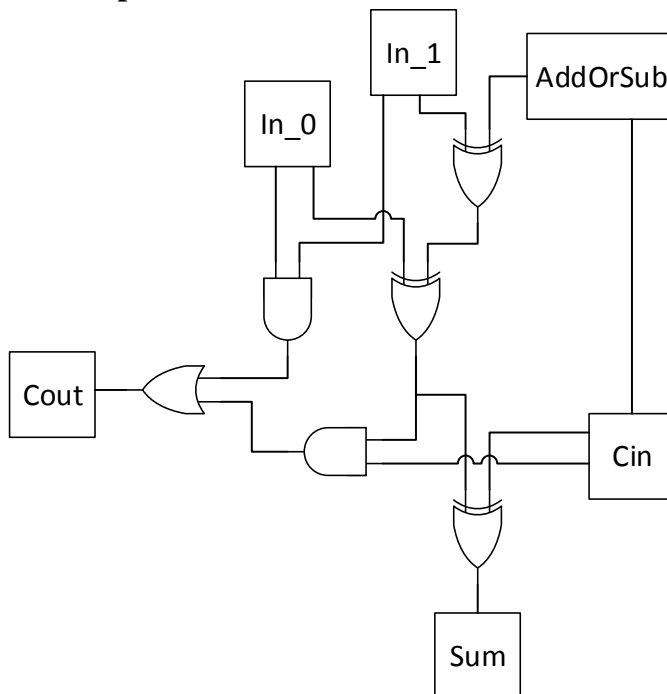
$$Sum = (In_0 \oplus In_1) \oplus Cin$$

$$Cout = (In_0)(In_1) + (Cin)(In_0 \oplus In_1)$$

$$Sum = (In_0 \oplus (In_1 \oplus AddOrSub)) \oplus Cin$$

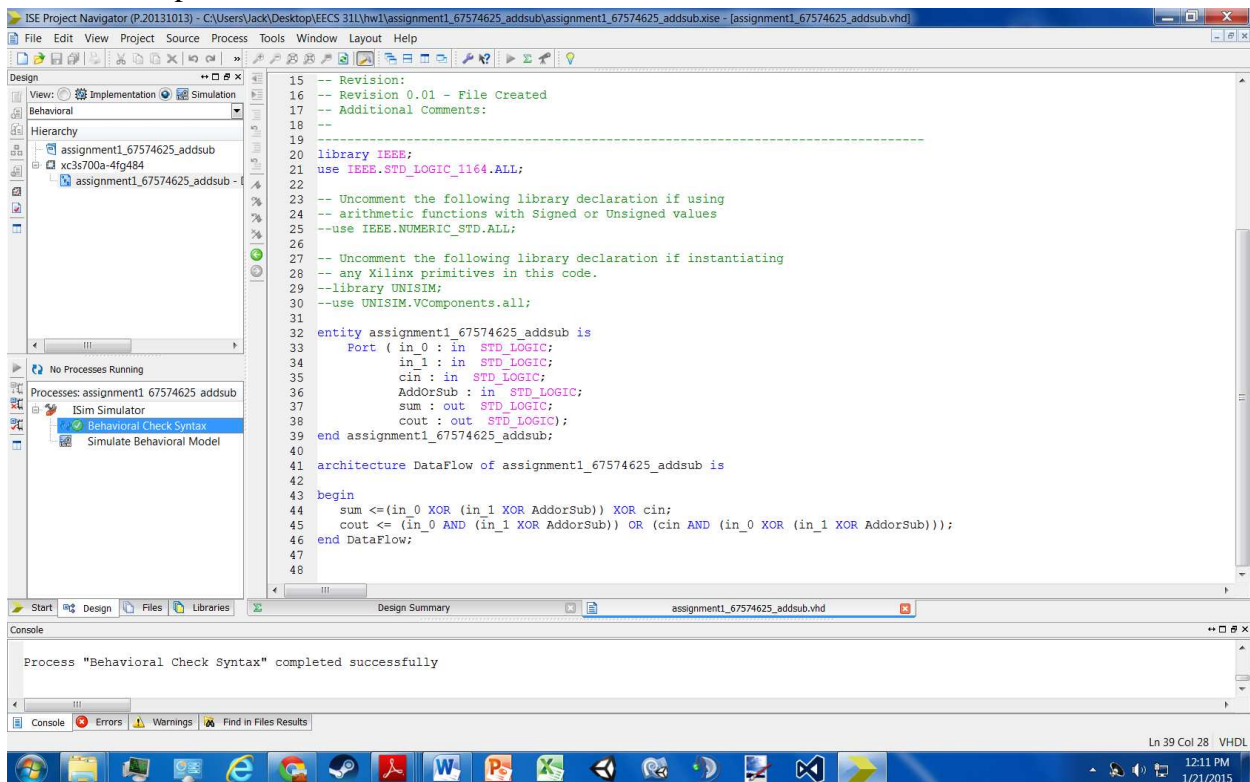
$$Cout = (In_0)(In_1 \oplus AddOrSub) + ((Cin)(In_0 (In_1 \oplus AddOrSub)))$$

Gate Representation:

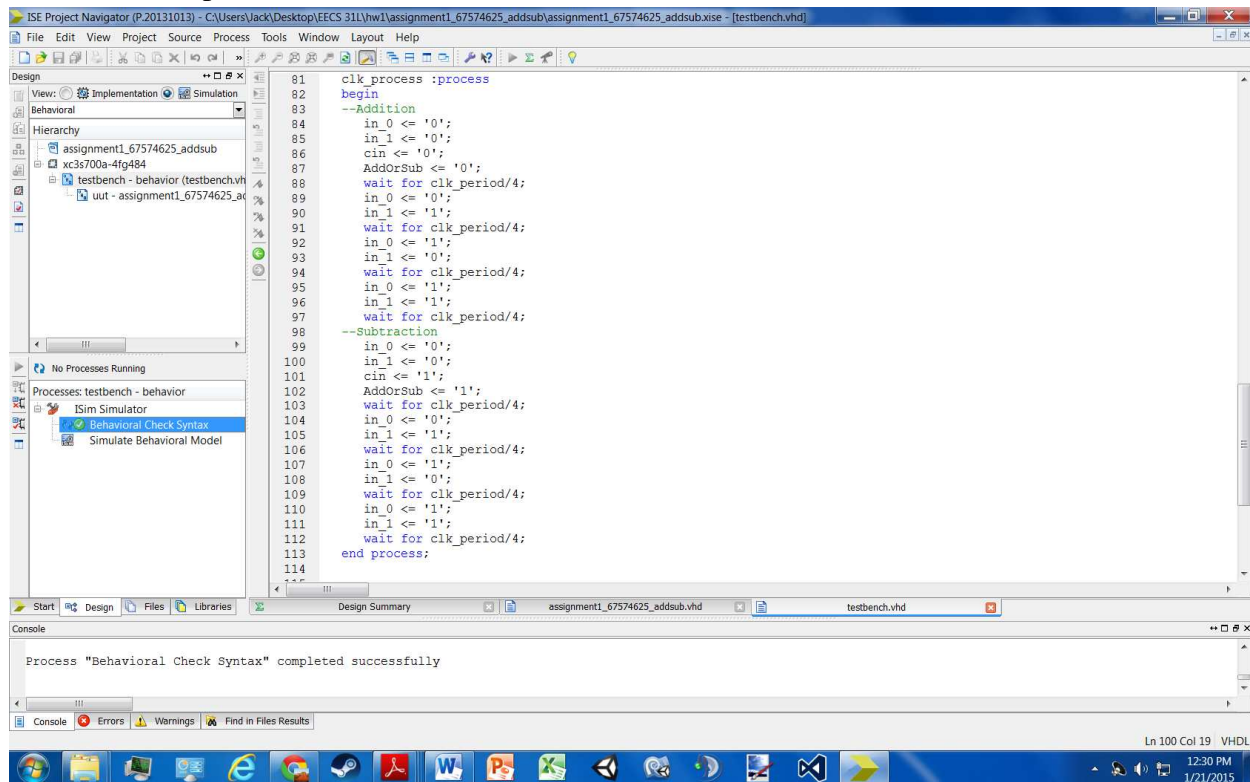


4 Compilation

AddSub compiled



Testbench compiled



5 Elaboration

Assumptions:

- in_0, in_1, cin, AddorSub, sum, and cout are all 1-Bit
- cin and Add or Sub are essentially same and are given the same value. If cin = '0', then AddorSub = '0'. If cin = '1', then AddorSub = '1'.

Errors:

- I tried making an input variable behave like an output variable
- I resolved it by inserting that equation into the output equations

Simulation Log:

Started : "Simulate Behavioral Model".

Determining files marked for global include in the design...

Running fuse...

Command Line: fuse -intstyle ise -incremental -o {C:/Users/Jack/Desktop/EECS

31L/hw1/assignment1_67574625_addsub/testbench_isim_beh.exe} -prj

{C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_addsub/testbench_beh.prj}

work.testbench { }

Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -intstyle ise -incremental -o C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_addsub/testbench_isim_beh.exe -prj C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_addsub/testbench_beh.prj work.testbench

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 4

Turning on mult-threading, number of parallel sub-compilation jobs: 8

Determining compilation order of HDL files

Parsing VHDL file "C:/Users/Jack/Desktop/EECS

31L/hw1/assignment1_67574625_addsub/assignment1_67574625_addsub.vhd" into library work

Parsing VHDL file "C:/Users/Jack/Desktop/EECS

31L/hw1/assignment1_67574625_addsub/testbench.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std_logic_1164

Compiling architecture dataflow of entity assignment1_67574625_addsub

[assignment1_67574625_addsub_defa...]

Compiling architecture behavior of entity testbench

Time Resolution for simulation is 1ps.

Waiting for 1 sub-compilation(s) to finish...

Compiled 5 VHDL Units

Built simulation executable C:/Users/Jack/Desktop/EECS

31L/hw1/assignment1_67574625_addsub/testbench_isim_beh.exe

Fuse Memory Usage: 29836 KB

Fuse CPU Usage: 389 ms

Launching ISim simulation engine GUI...

"C:/Users/Jack/Desktop/EECS

31L/hw1/assignment1_67574625_addsub/testbench_isim_beh.exe" -intstyle ise -gui -tclbatch

isim.cmd -wdb "C:/Users/Jack/Desktop/EECS

31L/hw1/assignment1_67574625_addsub/testbench_isim_beh.wdb"

ISim simulation engine GUI launched successfully

Process "Simulate Behavioral Model" completed successfully

6 Waveform

