Introduction to Digital Logic
EECS/CSE 31L

Assignment 1: 4-Input Multiplexer

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1 Block Description

This block is designed to take in 2 inputs in order to select between another 4 inputs

2 Input/Output Port Description

Port name	Port size	Port Type	Description
Input0	1	IN	Value of first input
Input1	1	IN	Value of second input
Input2	1	IN	Value of third input
Input3	1	IN	Value of fourth input
Select0	1	IN	Gets the first select operand
Select1	1	IN	Gets the second select operand
output	1	OUT	The operation result

3 Design Schematics

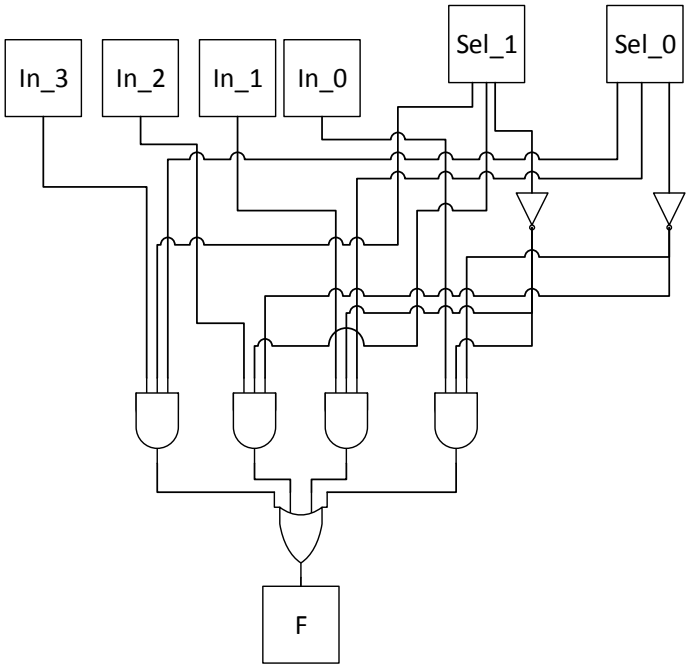
Truth Table:

Sel_1	Sel_0	F
0	0	In_0
0	1	In_1
1	0	In_2
1	1	In_3

Boolean Expression:

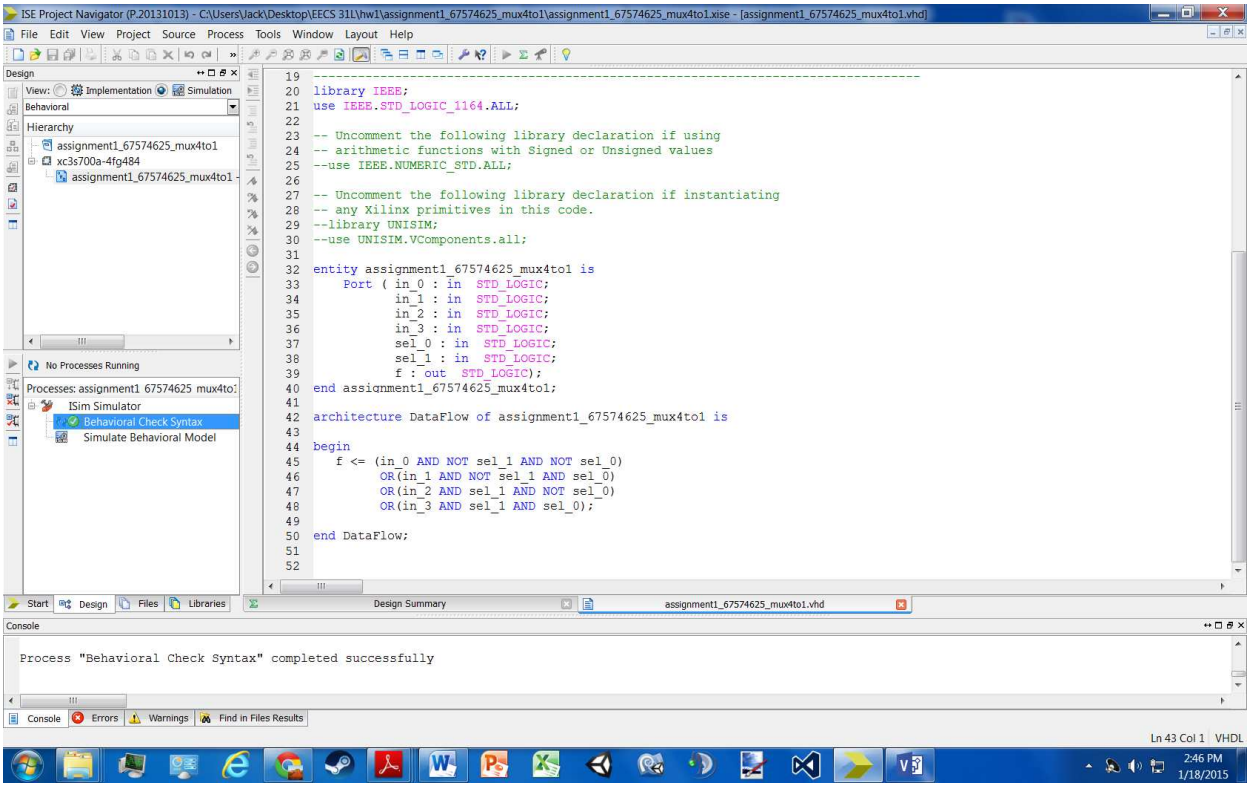
F = (Sel_1')(Sel_0')(In_0) + (Sel_1')(Sel_0)(In_1) + (Sel_1)(Sel_0')(In_2) + (Sel_1)(Sel_0)(In_3)

Gate Representation:

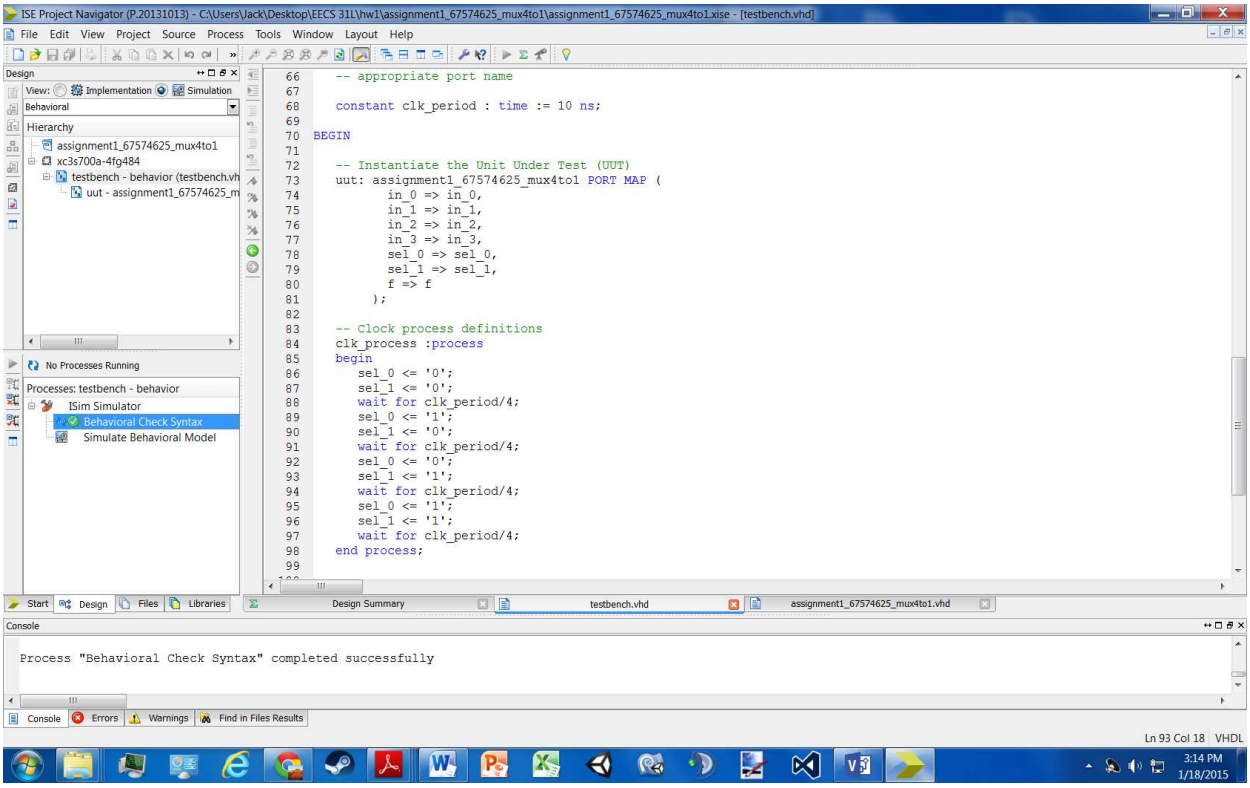


4 Compilation

4 to 1 mux code compiled



Testbench compiled



5 Elaboration

Assumptions:

- in_0, in_1, in_2, in_3 are only 1-bit
- f becomes ‘0’ when either in_0 or in_2 are selected because in_0 and in_2 = ‘0’
- f becomes ‘1’ when either in_1 or in_3 are selected because in_1 and in_3 = ‘1’
- Truth table above shows selection method.

Errors:

- No errors occurred while coding

Simulation Log:

Started : "Simulate Behavioral Model".

Determining files marked for global include in the design...
Running fuse...
Command Line: fuse -intstyle ise -incremental -o {C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_mux4to1/testbench_isim_beh.exe} -prj {C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_mux4to1/testbench_beh.prj} work.testbench {}

Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -intstyle ise -incremental -o C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_mux4to1/testbench_isim_beh.exe -prj C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_mux4to1/testbench_beh.prj work.testbench
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 4
Turning on mult-threading, number of parallel sub-compilation jobs: 8
Determining compilation order of HDL files
Parsing VHDL file "C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_mux4to1/assignment1_67574625_mux4to1.vhd" into library work
Parsing VHDL file "C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_mux4to1/testbench.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling architecture dataflow of entity assignment1_67574625_mux4to1 [assignment1_67574625_mux4to1_def...]
Compiling architecture behavior of entity testbench
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 5 VHDL Units
Built simulation executable C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_mux4to1/testbench_isim_beh.exe
Fuse Memory Usage: 29848 KB
Fuse CPU Usage: 420 ms
Launching ISim simulation engine GUI...
"C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_mux4to1/testbench_isim_beh.exe" -intstyle ise -gui -tclbatch isim.cmd -wdb "C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_mux4to1/testbench_isim_beh.wdb"
ISim simulation engine GUI launched successfully

Process "Simulate Behavioral Model" completed successfully

6 Waveform

Note: inputs and outputs are all 1-Bit