

# Introduction to Digital Logic

## EECS/CSE 31L

### Assignment 1: 4-Input Multiplexer

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January 14, 2015

## 1 Block Description

This block is designed to take in 2 inputs in order to select between another 4 inputs

## 2 Input/Output Port Description

Port name	Port size	Port Type	Description
Input0	1	IN	Value of first input
Input1	1	IN	Value of second input
Input2	1	IN	Value of third input
Input3	1	IN	Value of fourth input
Select0	1	IN	Gets the first select operand
Select1	1	IN	Gets the second select operand
output	1	OUT	The operation result

## 3 Design Schematics

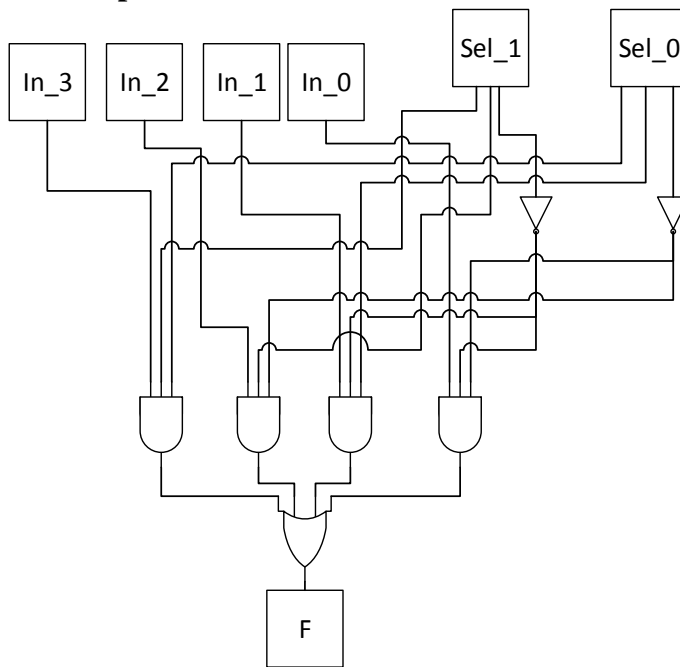
Truth Table:

Sel_1	Sel_0	F
0	0	In_0
0	1	In_1
1	0	In_2
1	1	In_3

**Boolean Expression:**

$$F = (\text{Sel}_1')(\text{Sel}_0')(\text{In}_0) + (\text{Sel}_1')(\text{Sel}_0)(\text{In}_1) + (\text{Sel}_1)(\text{Sel}_0')(\text{In}_2) + (\text{Sel}_1)(\text{Sel}_0)(\text{In}_3)$$

## Gate Representation:



## 4 Compilation

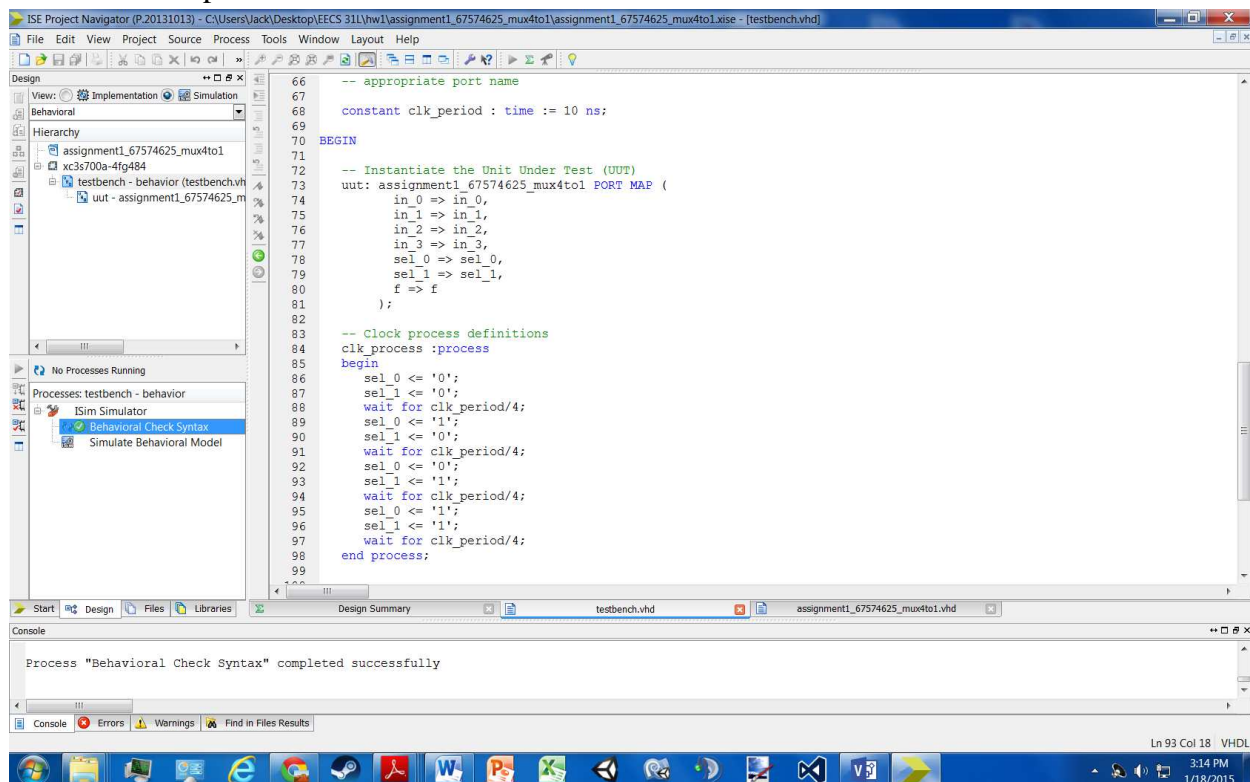
4 to 1 mux code compiled

The screenshot shows the ISE Project Navigator interface. The main window displays the VHDL code for a 4-to-1 multiplexer. The code is as follows:

```
19 library IEEE;
20 use IEEE.STD_LOGIC_1164.ALL;
21
22 -- Uncomment the following library declaration if using
23 -- arithmetic functions with Signed or Unsigned values
24 --use IEEE.NUMERIC_STD.ALL;
25
26 -- Uncomment the following library declaration if instantiating
27 -- any Xilinx primitives in this code.
28 --library UNISIM;
29 --use UNISIM.VComponents.all;
30
31 entity assignment1_67574625_mux4to1 is
32     Port ( in_0 : in STD_LOGIC;
33           in_1 : in STD_LOGIC;
34           in_2 : in STD_LOGIC;
35           in_3 : in STD_LOGIC;
36           sel_0 : in STD_LOGIC;
37           sel_1 : in STD_LOGIC;
38           f : out STD_LOGIC);
39 end assignment1_67574625_mux4to1;
40
41 architecture DataFlow of assignment1_67574625_mux4to1 is
42 begin
43     f <= (in_0 AND NOT sel_1 AND NOT sel_0)
44         OR (in_1 AND NOT sel_1 AND sel_0)
45         OR (in_2 AND sel_1 AND NOT sel_0)
46         OR (in_3 AND sel_1 AND sel_0);
47 end DataFlow;
48
49
50
51
52
```

The left pane shows the project hierarchy with the file 'assignment1\_67574625\_mux4to1.vhd' selected. The bottom pane shows the console output: 'Process "Behavioral Check Syntax" completed successfully'. The status bar at the bottom indicates 'Ln 43 Col 1 VHDL'.

## Testbench compiled



## 5 Elaboration

### Assumptions:

- in\_0, in\_1, in\_2, in\_3 are only 1-bit
- f becomes '0' when either in\_0 or in\_2 are selected because in\_0 and in\_2 = '0'
- f becomes '1' when either in\_1 or in\_3 are selected because in\_1 and in\_3 = '1'
- Truth table above shows selection method.

### Errors:

- No errors occurred while coding

### Simulation Log:

Started : "Simulate Behavioral Model".

Determining files marked for global include in the design...

Running fuse...

Command Line: fuse -intstyle ise -incremental -o {C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_mux4to1/testbench\_isim\_beh.exe} -prj {C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_mux4to1/testbench\_beh.prj} work.testbench { }

Running: C:\Xilinx\14.7\ISE\_DS\ISE\bin\nt64\unwrapped\fuse.exe -intstyle ise -incremental -o  
C:/Users/Jack/Desktop/EECS  
31L/hw1/assignment1\_67574625\_mux4to1/testbench\_isim\_beh.exe -prj  
C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1\_67574625\_mux4to1/testbench\_beh.prj  
work.testbench  
ISim P.20131013 (signature 0x7708f090)  
Number of CPUs detected in this system: 4  
Turning on mult-threading, number of parallel sub-compilation jobs: 8  
Determining compilation order of HDL files  
Parsing VHDL file "C:/Users/Jack/Desktop/EECS  
31L/hw1/assignment1\_67574625\_mux4to1/assignment1\_67574625\_mux4to1.vhd" into library  
work  
Parsing VHDL file "C:/Users/Jack/Desktop/EECS  
31L/hw1/assignment1\_67574625\_mux4to1/testbench.vhd" into library work  
Starting static elaboration  
Completed static elaboration  
Compiling package standard  
Compiling package std\_logic\_1164  
Compiling architecture dataflow of entity assignment1\_67574625\_mux4to1  
[assignment1\_67574625\_mux4to1\_def...]  
Compiling architecture behavior of entity testbench  
Time Resolution for simulation is 1ps.  
Waiting for 1 sub-compilation(s) to finish...  
Compiled 5 VHDL Units  
Built simulation executable C:/Users/Jack/Desktop/EECS  
31L/hw1/assignment1\_67574625\_mux4to1/testbench\_isim\_beh.exe  
Fuse Memory Usage: 29848 KB  
Fuse CPU Usage: 420 ms  
Launching ISim simulation engine GUI...  
"C:/Users/Jack/Desktop/EECS  
31L/hw1/assignment1\_67574625\_mux4to1/testbench\_isim\_beh.exe" -intstyle ise -gui -tclbatch  
isim.cmd -wdb "C:/Users/Jack/Desktop/EECS  
31L/hw1/assignment1\_67574625\_mux4to1/testbench\_isim\_beh.wdb"  
ISim simulation engine GUI launched successfully  
  
Process "Simulate Behavioral Model" completed successfully

## 6 Waveform

Note: inputs and outputs are all 1-Bit

