Introduction to Digital Logic
EECS/CSE 31L

Assignment 1: 1-Bit Comparator

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1 Block Description

This block is designed to take in 2 inputs in order to select between another 4 inputs

2 Input/Output Port Description

Port name	Port size	Port Type	Description
Input0	1	IN	Value of first input
Input1	1	IN	Value of second input
Greater	1	OUT	First operation result
Equal	1	OUT	Second operation result
Less	1	OUT	Third operation result

3 Design Schematics

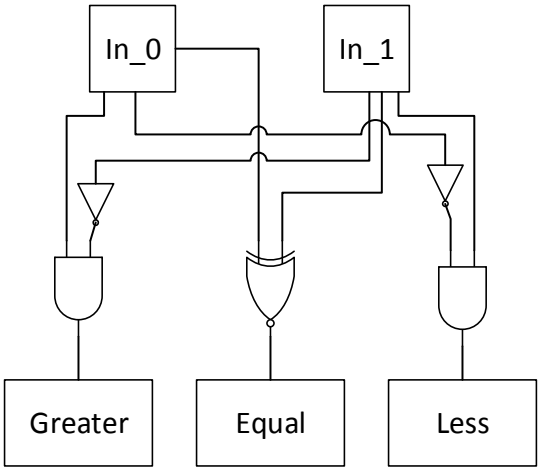
Truth Table:

In_0	In_1	Greater	Equal	Less
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

Boolean Expressions:

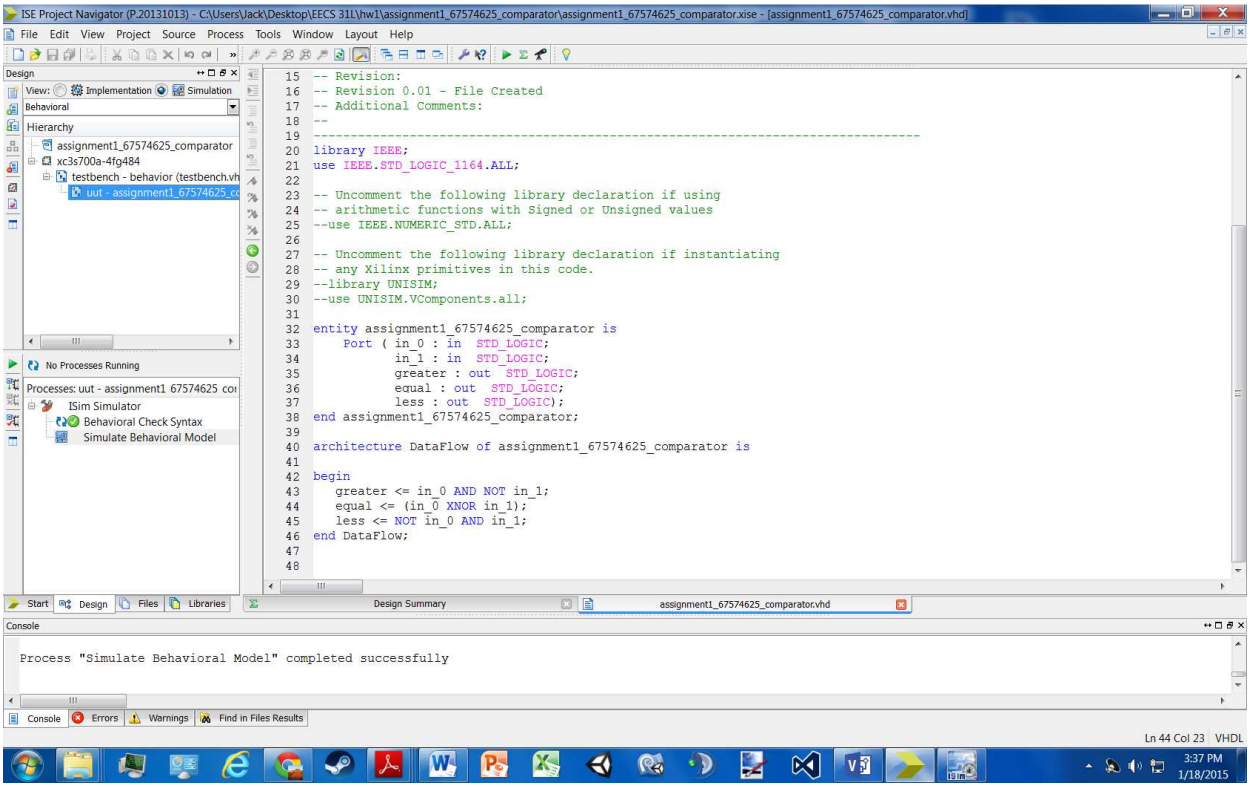
Greater = (In_0)(In_1')
Equal = (In_0')(In_1') + (In_0)(In_1) = In_0 $\odot$ In_1
Less = (In_0')(In_1)

Gate Representation:

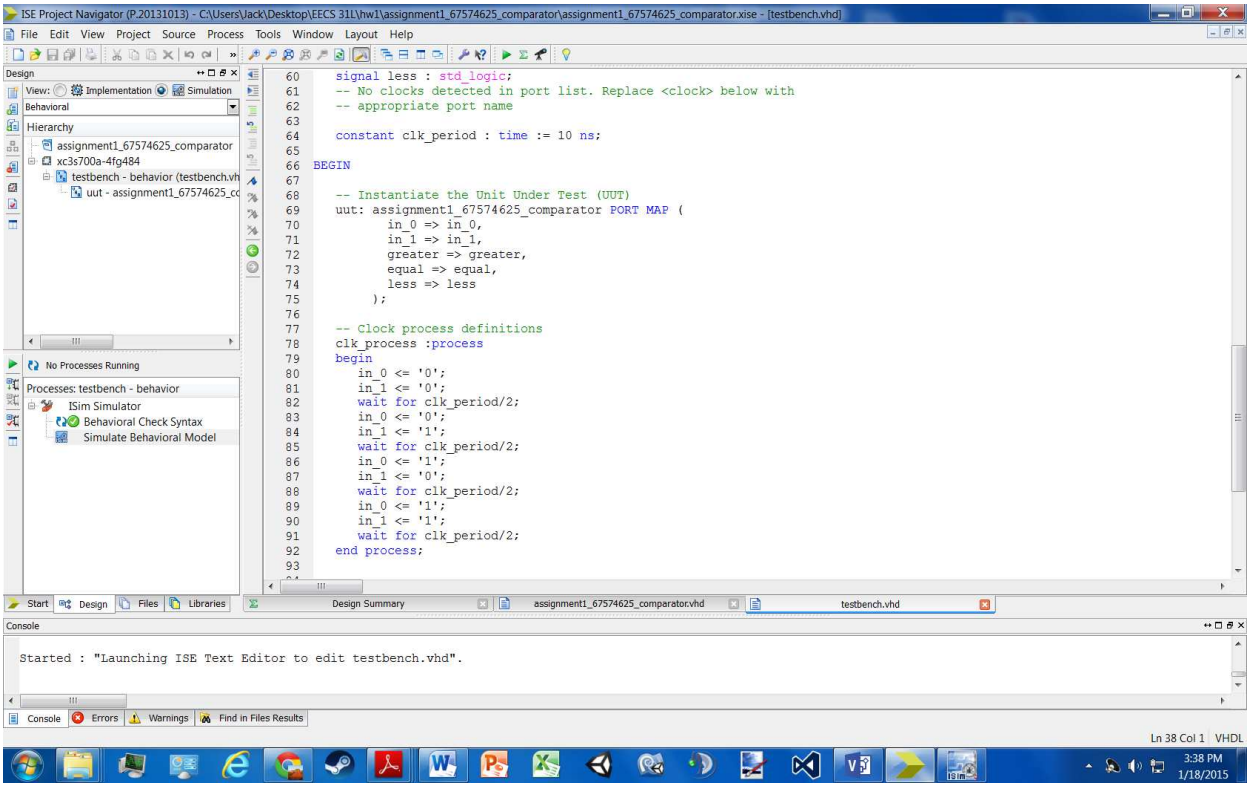


4 Compilation

Comparator compiled



Testbench compiled



5 Elaboration

Assumptions:

- All inputs and outputs are 1-Bit
- Less = 1 when in_0 < in_1 (‘0’ < ‘1’)
- Greater = 1 when in_0 > in_1 (‘1’ > ‘0’)
- Equal = 1 when in_0 = in_1 (‘0’ = ‘0’ or ‘1’ = ‘1’)

Errors:

- No errors occurred while coding

Simulation Log:

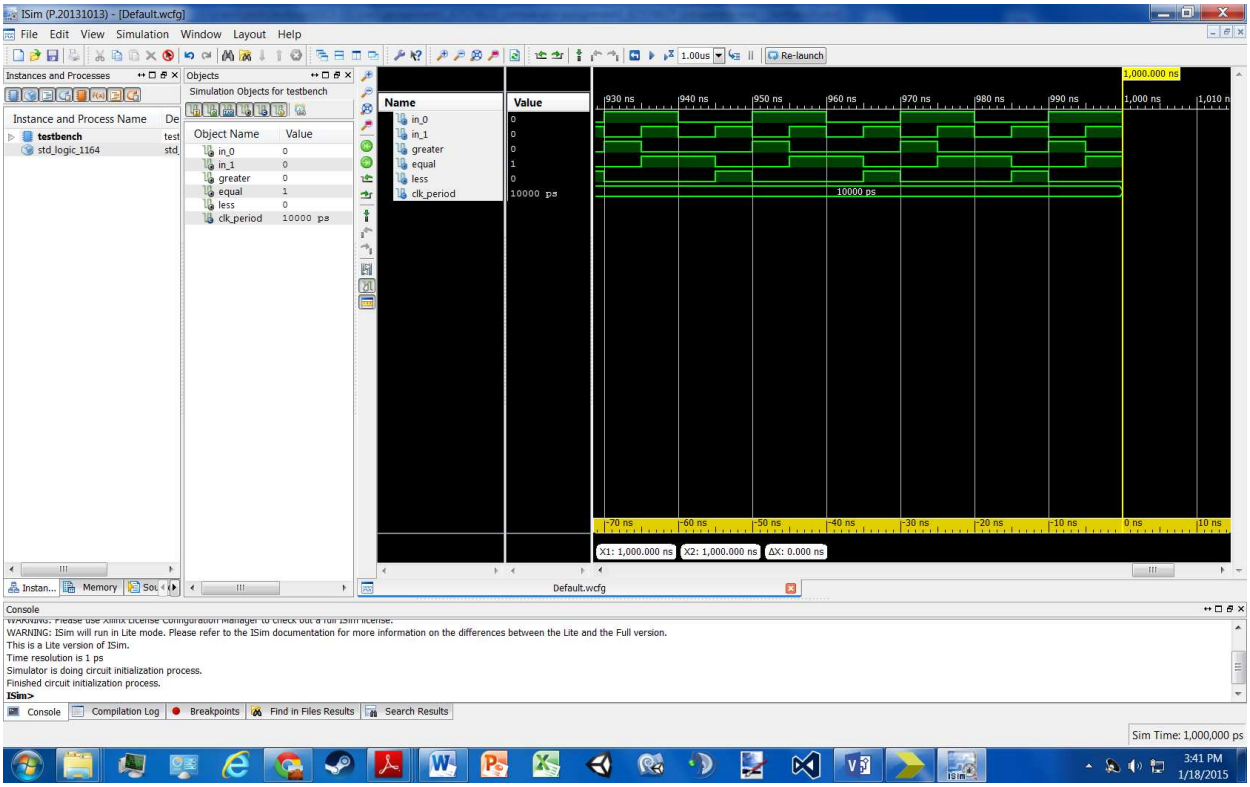
Started : "Simulate Behavioral Model".

Determining files marked for global include in the design...
Running fuse...
Command Line: fuse -intstyle ise -incremental -o {C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_comparator/testbench_isim_beh.exe} -prj {C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_comparator/testbench_beh.prj} work.testbench {}

Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -intstyle ise -incremental -o C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_comparator/testbench_isim_beh.exe -prj C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_comparator/testbench_beh.prj work.testbench
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 4
Turning on mult-threading, number of parallel sub-compilation jobs: 8
Determining compilation order of HDL files
Parsing VHDL file "C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_comparator/assignment1_67574625_comparator.vhd" into library work
Parsing VHDL file "C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_comparator/testbench.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling architecture dataflow of entity assignment1_67574625_comparator [assignment1_67574625_comparator_...]
Compiling architecture behavior of entity testbench
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 5 VHDL Units
Built simulation executable C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_comparator/testbench_isim_beh.exe
Fuse Memory Usage: 29860 KB
Fuse CPU Usage: 389 ms
Launching ISim simulation engine GUI...
"C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_comparator/testbench_isim_beh.exe" -intstyle ise -gui -tclbatch isim.cmd -wdb "C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_comparator/testbench_isim_beh.wdb"
ISim simulation engine GUI launched successfully

Process "Simulate Behavioral Model" completed successfully

6 Waveform


ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Instance and Process Name
testbench
std_logic_1164
Objects
Simulation Objects for testbench
Object Name Value
in_0 0
in_1 0
greater 0
equal 1
less 0
clk_period 10000 ps
Name
Value
in_0
in_1
greater
equal
less
clk_period
10000 ps
930 ns
940 ns
950 ns
960 ns
970 ns
980 ns
990 ns
1,000 ns
1,010 n
1,000.000 ns
-70 ns
-60 ns
-50 ns
-40 ns
-30 ns
-20 ns
-10 ns
0 ns
10 ns
X1: 1,000.000 ns
X2: 1,000.000 ns
ΔX: 0.000 ns
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps
3:41 PM
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