Introduction to Digital Logic
EECS/CSE 31L

Assignment 1

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1.1 Assignment Description

Follow the instructions in the tutorial for each tool appended to this text. CAD tools you will work with in this assignment are:

Tool 1: Questasim® MentorGraphics

Tool 2: Incisive Enterprise Simulator from Cadence

1.2 Assignment Deliverable

Tool 1: Questasim® MentorGraphics

• A short report on what you have learned
What I learned:

- Questasim can only be used on zuma or crystalcove Unix servers
- How to setup a project that uses Questasim
- Install Questasim for my use on the server for the project
- Compile the VHDL(.vhd) design files and the System Verilog(.sv) testbench files
- Optimize the VHDL design
- Simulate the design
- View the waveform

Questasim installation

```
zuma% source setup.csh
zuma% source pre_compile.csh
QuestaSim-64 vmap 10.4c Lib Mapping Utility 2015.07 Jul 19 2015
vmap work questa/work
Copying /home/linware/mentor/questa/questasim/linux_x86_64/../modelsim.ini to modelsim.ini
Modifying modelsim.ini
** Warning: (vlib-34) Library already exists at "questa/work".
QuestaSim-64 vmap 10.4c Lib Mapping Utility 2015.07 Jul 19 2015
vmap -c mtiUvm questa/work
Modifying modelsim.ini
** Warning: vmap will not overwrite local modelsim.ini.
QuestaSim-64 vmap 10.4c Lib Mapping Utility 2015.07 Jul 19 2015
vmap work questa/work
Modifying modelsim.ini
```

• Compilation, Elaboration, and Simulation logs

VHDL Design Compilation

```
zuma% vcom -64 -f rtl.cfg
QuestaSim-64 vcom 10.4c Compiler 2015.07 Jul 19 2015
Start time: 13:03:32 on Jan 06,2016
vcom -64 -f rtl.cfg
-- Loading package STANDARD
-- Loading package TEXTIO
-- Loading package std_logic_1164
-- Loading package NUMERIC_STD
-- Compiling entity ALU_32
-- Compiling architecture Behavioral of ALU_32
End time: 13:03:32 on Jan 06,2016, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
```

System Verilog Testbench Compilation

```
zuma% vlog -64 -sv -f tb.cfg
QuestaSim-64 vlog 10.4c Compiler 2015.07 Jul 19 2015
Start time: 13:03:44 on Jan 06,2016
vlog -64 -sv -f tb.cfg
-- Compiling module alu_32_tb

Top level modules:
        alu_32_tb
End time: 13:03:44 on Jan 06,2016, Elapsed time: 0:00:00
```

VHDL Design Optimization

```
zuma% vopt -64 alu_32_tb +acc=mpr -o alu_32_tb_opt
QuestaSim-64 vopt 10.4c Compiler 2015.07 Jul 19 2015
Start time: 13:04:01 on Jan 06,2016
vopt alu_32_tb "+acc=mpr" -o alu_32_tb_opt

Top level modules:
        alu_32_tb

Analyzing design...
-- Loading module alu_32_tb
-- Loading package STANDARD
-- Loading package TEXTIO
-- Loading package std_logic_1164
-- Loading package NUMERIC_STD
-- Loading entity ALU_32
-- Loading architecture Behavioral of ALU_32
Optimizing 2 design-units (inlining 0/1 module instances, 0/0 UDP instances):
-- Optimizing module alu_32_tb(fast)
-- Optimizing architecture Behavioral of ALU_32
Optimized design name is alu_32_tb_opt
End time: 13:04:01 on Jan 06,2016, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
```

Simulation Log

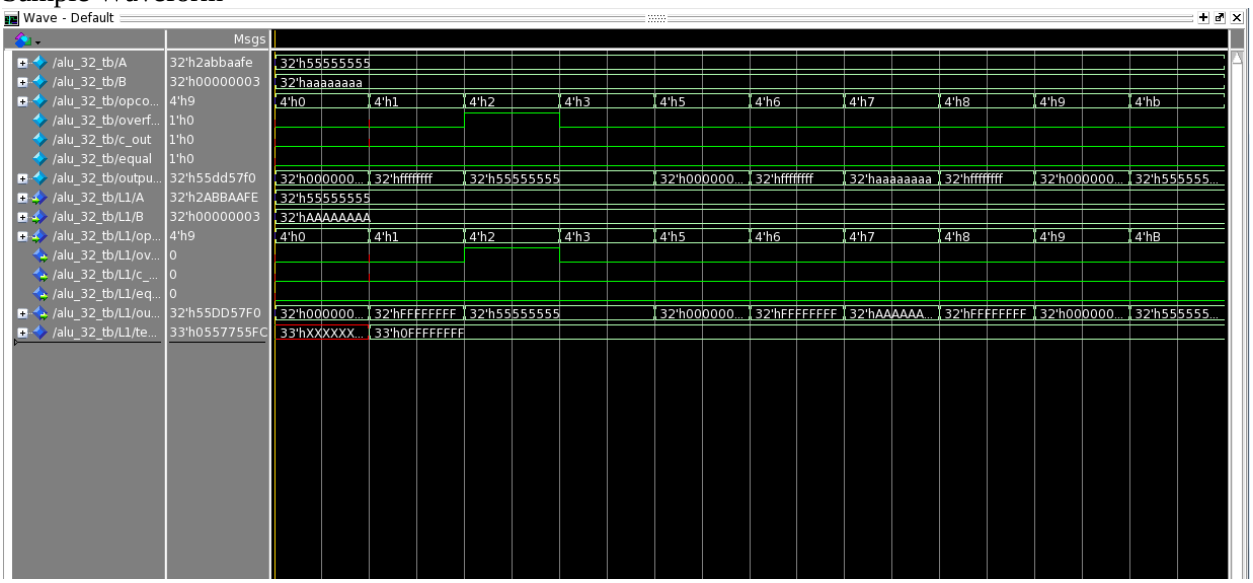
```
zuma% vsim -64 -l simulation.log -do sim.do -c alu_32_tb_opt
Reading pref.tcl

# 10.4c

# vsim -l simulation.log -do "sim.do" -c alu_32_tb_opt
# Start time: 13:04:18 on Jan 06,2016
# //  Questa Sim-64
# //  Version 10.4c linux_x86_64 Jul 19 2015
# //
# //  Copyright 1991-2015 Mentor Graphics Corporation
# //  All Rights Reserved.
# //
# //  THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
# //  WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION OR ITS
# //  LICENSORS AND IS SUBJECT TO LICENSE TERMS.
# //  THIS DOCUMENT CONTAINS TRADE SECRETS AND COMMERCIAL OR FINANCIAL
# //  INFORMATION THAT ARE PRIVILEGED, CONFIDENTIAL, AND EXEMPT FROM
# //  DISCLOSURE UNDER THE FREEDOM OF INFORMATION ACT, 5 U.S.C. SECTION 552.
# //  FURTHERMORE, THIS INFORMATION IS PROHIBITED FROM DISCLOSURE UNDER
# //  THE TRADE SECRETS ACT, 18 U.S.C. SECTION 1905.
# //
# Loading sv_std.std
# Loading work.alu_32_tb(fast)
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading ieee.numeric_std(body)
# Loading work.alu_32(behavioral)#1
# do sim.do
# .
# waveform.wlf
# ** Warning: (vsim-151) NUMERIC_STD.TO_INTEGER: Value -1431655766 is not in bounds of subtype NATURAL.
#    Time: 800 ns  Iteration: 1  Instance: .alu_32_tb.L1
# End time: 13:04:18 on Jan 06,2016, Elapsed time: 0:00:00
# Errors: 0, Warnings: 1
```

• Waveform snapshot from each tool

Opening waveform

```
zuma% vsim -view waveform.wlf
Reading pref.tcl
```

Sample Waveform



Tool 2: Incisive Enterprise Simulator from Cadence

• A short report on what you have learned
What I learned:

- Cadence can only be used on malibu or vivian Unix servers
- Enable Cadence for use on my account
- How to setup a project that uses Cadence
- Compile the VHDL(.vhd) design files and the System Verilog(.sv) testbench files
- Elaborate the VHDL design
- Simulate the design
- View the waveform

Cadence Installation

```
malibu% source /usr/skel/syswide.cshrc
malibu% source /ecelib/eceware/profile/cadence.linux
malibu% source /ecelib/eceware/profile/cadence61
malibu% source /ecelib/eceware/profile/mentor09
malibu% setenv T_DIR/ecelib/eceware/cadence61/tk_2011
```

• Compilation, Elaboration, and Simulation logs
VHDL Design Compilation

```
malibu% ncvhdl -messages orgate.vhd
ncvhdl: 06.20-s015: (c) Copyright 1995-2009 Cadence Design Systems, Inc.
orgate.vhd:
        errors: 0, warnings: 0
WORK.ORGATE (entity):
        streams: 4, words: 18
WORK.ORGATE:BEHAVIORAL (architecture):
        streams: 1, words: 23
```

System Verilog Testbench Compilation

```
malibu% ncvlog -sv -work work orgatetb.sv
ncvlog: 06.20-s015: (c) Copyright 1995-2009 Cadence Design Systems, Inc.
```

VHDL Design Elaboration

```
malibu% ncelab work.orgatetb -access +R+W -UPDATE -timescale 1ns/10ps -work work
ncelab: 06.20-s015: (c) Copyright 1995-2009 Cadence Design Systems, Inc.
```

Simulation Log

```
malibu% ncsim work.orgatetb -input run.cmd
ncsim: 06.20-s015: (c) Copyright 1995-2009 Cadence Design Systems, Inc.
ncsim> database -open waves -into waves.shm -default
Created default SHM database waves
ncsim> probe -create -shm -all -variables -depth all
Created probe 1
ncsim> run 50ns
Ran until 50 NS + 0
```

• Waveform snapshot from each tool

Open Waveform

```
ncsim> simvision &
simvision: 06.20-s015: (c) Copyright 1995-2009 Cadence Design Systems, Inc.

------------------------------------
Relinquished control to SimVision...
txe: 06.20-s015: (c) Copyright 1995-2007 Cadence Design Systems, Inc.
```

Waveform Snapshot