Introduction to Digital Logic
EECS/CSE 31L

Assignment 4: Register

Prepared by: Jack Melcher
Student ID: 67574625

EECS Department
Henry Samueli School of Engineering
University of California, Irvine

February 15, 2015

1 Block Description

- Construct a register that can be parameterized
- Can load a given input value
- Increment the value stored in the register
- Has an asynchronous reset and synchronous reset

2 Input/Output Port Description

Generic Name	Data Type	Default Value	Description
NBIT	INTEGER	32	Size of register

Port name	Port size	Port Type	Description
Clk	1	IN	Triggers the register process
Rst_a	1	IN	Will reset the register when active
Rst_s	1	IN	Will reset the register when active and clock rises
We	1	IN	Enables writing to the register
din	NBIT-1 downto 0	IN	The input value
dout	NBIT-1 downto 0	OUT	The register’s stored value

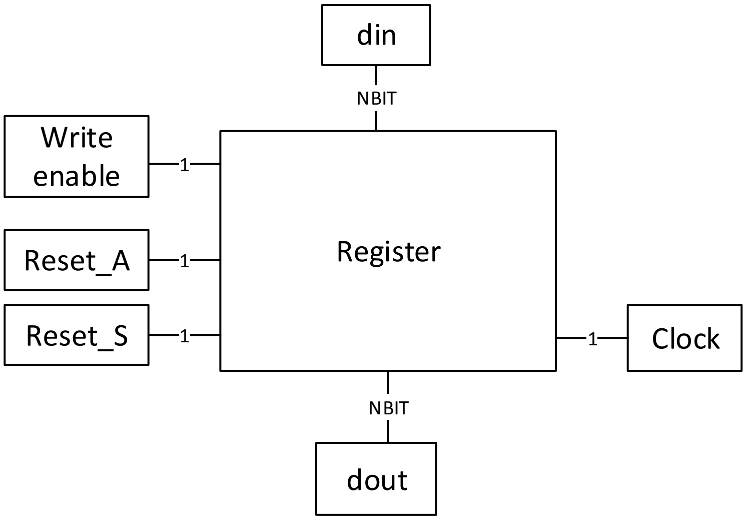
Variable Name	Data Type	Port size	Description
temp	INTEGER	NBIT-1 downto 0	Aids in register process

3 Design Schematics

Truth Table:

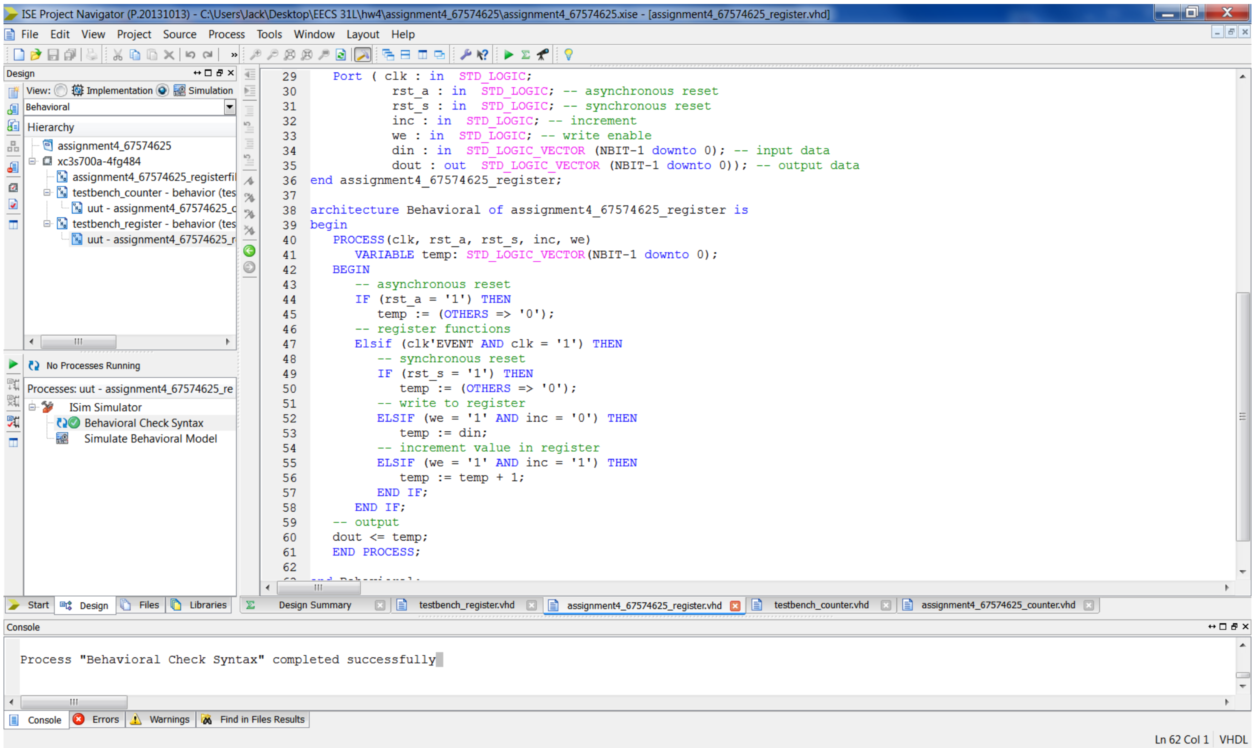
Clk (Rising edge)	Rst_a	Rst_s	inc	we	Function
X	1	X	X	X	Asynchronous Reset
1	0	1	X	X	Synchronous Reset
1	0	0	0	1	Load Input
1	0	0	1	1	Increment Value Stored in Register

Design:



4 Compilation

Register



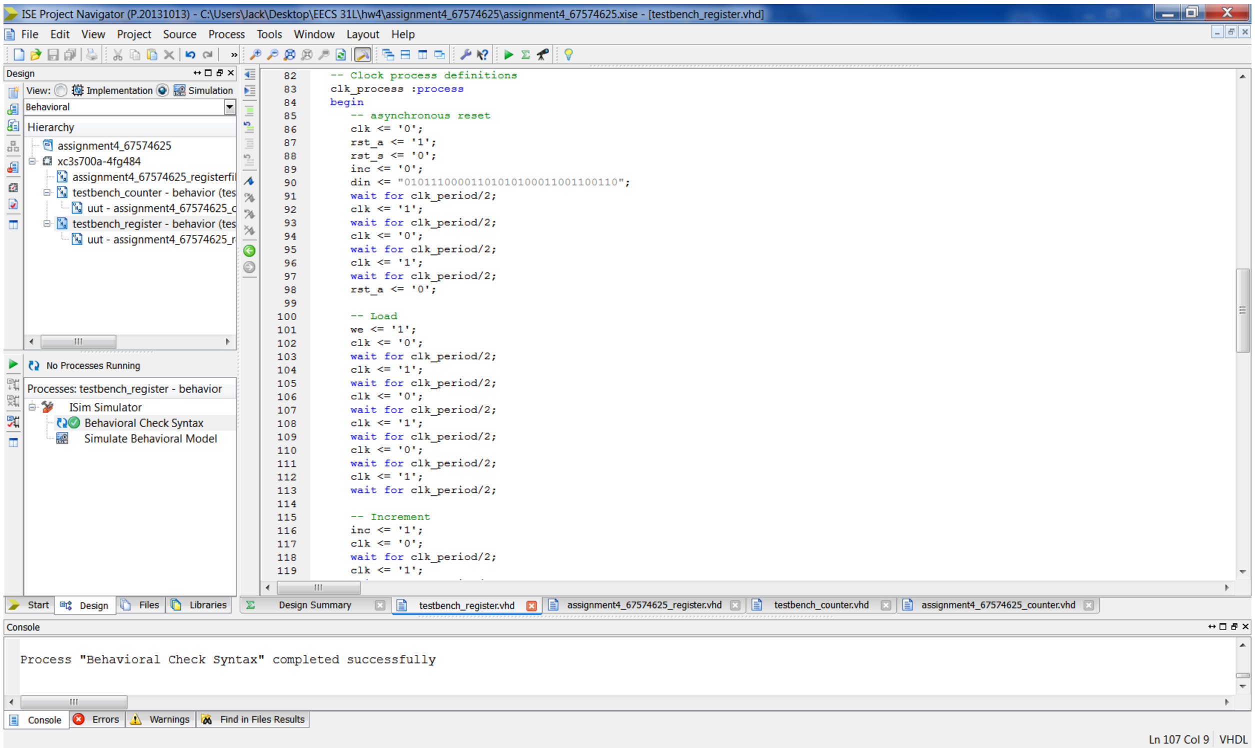
ISE Project Navigator (P.20131013) - C:\Users\Jack\Desktop\EECS 31L\hw4\assignment4_67574625\assignment4_67574625.xise - [assignment4_67574625_register.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
assignment4_67574625
xc3s700a-4fg484
assignment4_67574625_registerfi
testbench_counter - behavior (tes
uut - assignment4_67574625_c
testbench_register - behavior (tes
uut - assignment4_67574625_r
No Processes Running
Processes: uut - assignment4_67574625_re
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
Start Design Files Libraries
Design Summary
testbench_register.vhd
assignment4_67574625_register.vhd
testbench_counter.vhd
assignment4_67574625_counter.vhd
Console
Console Errors Warnings Find in Files Results
Ln 62 Col 1 VHDL

```
    Port ( clk : in  STD_LOGIC;
           rst_a : in  STD_LOGIC; -- asynchronous reset
           rst_s : in  STD_LOGIC; -- synchronous reset
           inc : in  STD_LOGIC; -- increment
           we : in  STD_LOGIC; -- write enable
           din : in  STD_LOGIC_VECTOR (NBIT-1 downto 0); -- input data
           dout : out  STD_LOGIC_VECTOR (NBIT-1 downto 0)); -- output data
end assignment4_67574625_register;

architecture Behavioral of assignment4_67574625_register is
begin
   PROCESS(clk, rst_a, rst_s, inc, we)
      VARIABLE temp: STD_LOGIC_VECTOR(NBIT-1 downto 0);
   BEGIN
      -- asynchronous reset
      IF (rst_a = '1') THEN
         temp := (OTHERS => '0');
      -- register functions
      Elsif (clk'EVENT AND clk = '1') THEN
         -- synchronous reset
         IF (rst_s = '1') THEN
            temp := (OTHERS => '0');
         -- write to register
         ELSIF (we = '1' AND inc = '0') THEN
            temp := din;
         -- increment value in register
         ELSIF (we = '1' AND inc = '1') THEN
            temp := temp + 1;
         END IF;
      END IF;
   -- output
   dout <= temp;
   END PROCESS;
```

```
Process "Behavioral Check Syntax" completed successfully
```

Testbench



ISE Project Navigator (P.20131013) - C:\Users\Jack\Desktop\EECS 31L\hw4\assignment4_67574625\assignment4_67574625.xise - [testbench_register.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
assignment4_67574625
xc3s700a-4fg484
assignment4_67574625_registerfi
testbench_counter - behavior (tes
uut - assignment4_67574625_c
testbench_register - behavior (tes
uut - assignment4_67574625_r
No Processes Running
Processes: testbench_register - behavior
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
Start Design Files Libraries
Design Summary
testbench_register.vhd
assignment4_67574625_register.vhd
testbench_counter.vhd
assignment4_67574625_counter.vhd
Console
Console Errors Warnings Find in Files Results
Ln 107 Col 9 VHDL

```
   -- Clock process definitions
   clk_process :process
   begin
      -- asynchronous reset
      clk <= '0';
      rst_a <= '1';
      rst_s <= '0';
      inc <= '0';
      din <= "01011100001101010100011001100110";
      wait for clk_period/2;
      clk <= '1';
      wait for clk_period/2;
      clk <= '0';
      wait for clk_period/2;
      clk <= '1';
      wait for clk_period/2;
      rst_a <= '0';

      -- Load
      we <= '1';
      clk <= '0';
      wait for clk_period/2;
      clk <= '1';
      wait for clk_period/2;
      clk <= '0';
      wait for clk_period/2;
      clk <= '1';
      wait for clk_period/2;
      clk <= '0';
      wait for clk_period/2;
      clk <= '1';
      wait for clk_period/2;

      -- Increment
      inc <= '1';
      clk <= '0';
      wait for clk_period/2;
      clk <= '1';
```

```
Process "Behavioral Check Syntax" completed successfully
```

5 Elaboration

Assumptions:

- Register can store any NBIT value

Regarding how I wrote my vhdl code

- I used a process with a variable called temp
- Used sequential if and elsif statements

Errors and Challenges:

- I was having issues early on with the process statement. I didn't realize "else if" id "elsif" in VHDL
- Misusing assignment operators; tried using signal assignment operator on a variable

Simulation Log:

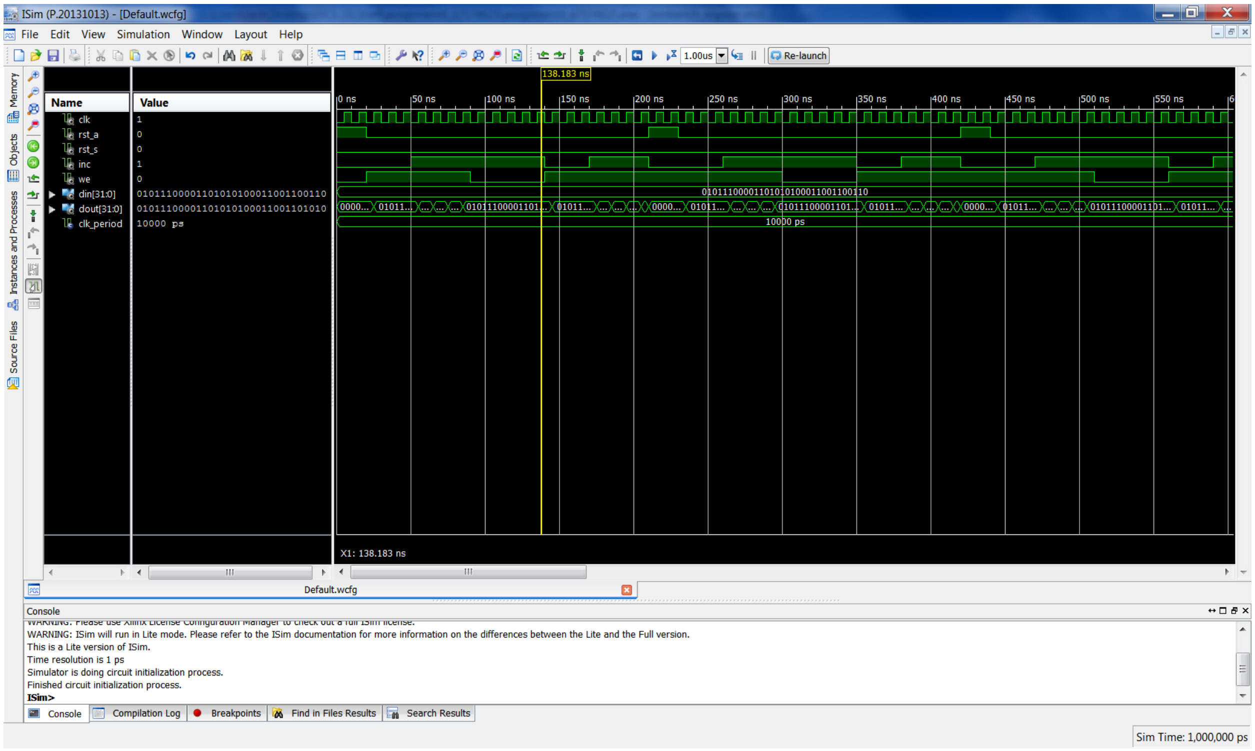
```
Started : "Simulate Behavioral Model".

Determining files marked for global include in the design...
Running fuse...
Command Line: fuse -intstyle ise -incremental -o {C:/Users/Jack/Desktop/EECS
31L/hw4/assignment4_67574625/testbench_register_isim_beh.exe} -prj
{C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4_67574625/testbench_register_beh.prj}
work.testbench_register {}
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -intstyle ise -incremental -o
C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4_67574625/testbench_register_isim_beh.exe
-prj C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4_67574625/testbench_register_beh.prj
work.testbench_register
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 4
Turning on mult-threading, number of parallel sub-compilation jobs: 8
Determining compilation order of HDL files
Parsing VHDL file "C:/Users/Jack/Desktop/EECS
31L/hw4/assignment4_67574625/assignment4_67574625_register.vhd" into library work
Parsing VHDL file "C:/Users/Jack/Desktop/EECS
31L/hw4/assignment4_67574625/testbench_register.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package std_logic_arith
Compiling package std_logic_unsigned
Compiling package numeric_std
Compiling architecture behavioral of entity assignment4_67574625_register
[\assignment4_67574625_register(3...]
Compiling architecture behavior of entity testbench_register
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 8 VHDL Units
Built simulation executable C:/Users/Jack/Desktop/EECS
31L/hw4/assignment4_67574625/testbench_register_isim_beh.exe
Fuse Memory Usage: 37152 KB
Fuse CPU Usage: 529 ms
Launching ISim simulation engine GUI...
"C:/Users/Jack/Desktop/EECS
31L/hw4/assignment4_67574625/testbench_register_isim_beh.exe" -intstyle ise -gui -tclbatch
isim.cmd  -wdb "C:/Users/Jack/Desktop/EECS
31L/hw4/assignment4_67574625/testbench_register_isim_beh.wdb"
ISim simulation engine GUI launched successfully

Process "Simulate Behavioral Model" completed successfully
```

6 Waveforms

Full Waveform Snapshot

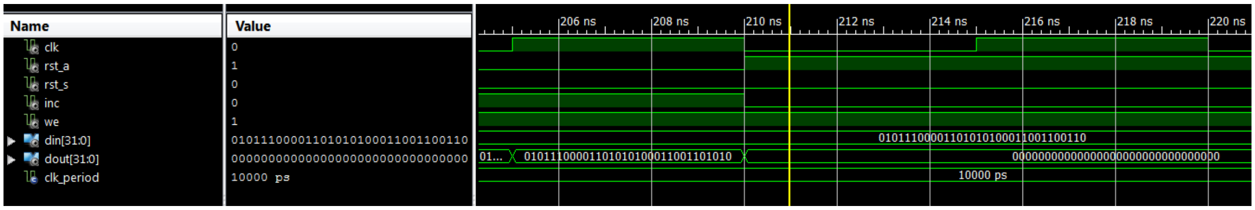


Name	Value
clk	1
rst_a	0
rst_s	0
inc	1
we	0
din[31:0]	01011100001101010100011001100110
dout[31:0]	01011100001101010100011001101010
clk_period	10000 ps

```
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
```

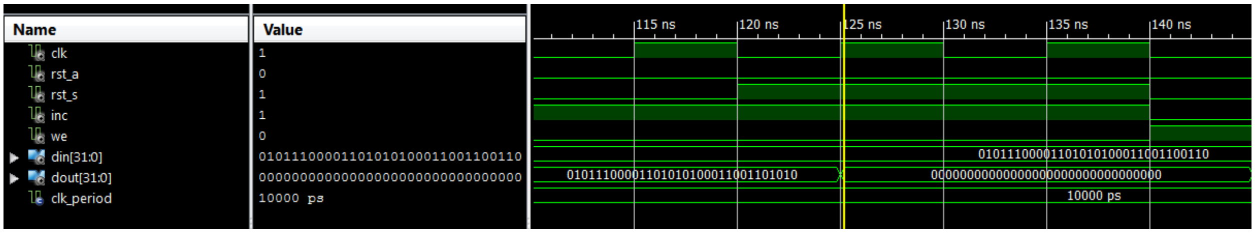
Snapshots of Waveform

Reset (asynchronous)



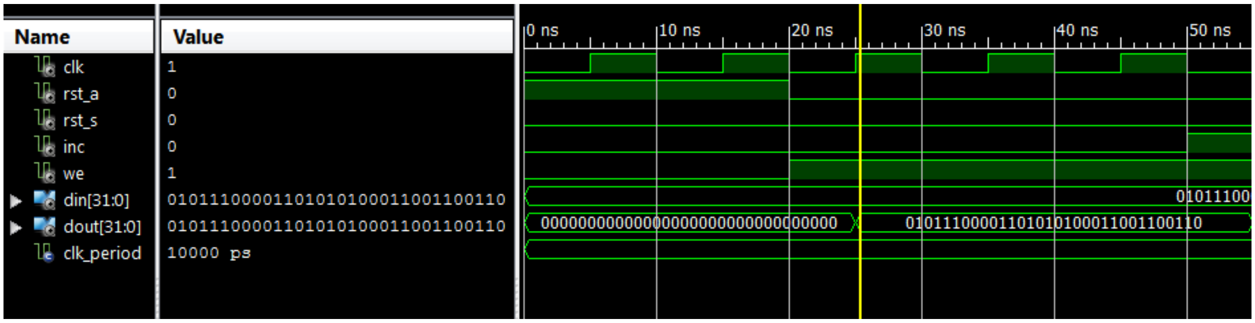
Name	Value
clk	0
rst_a	1
rst_s	0
inc	0
we	1
din[31:0]	01011100001101010100011001100110
dout[31:0]	00000000000000000000000000000000
clk_period	10000 ps

Reset (synchronous)



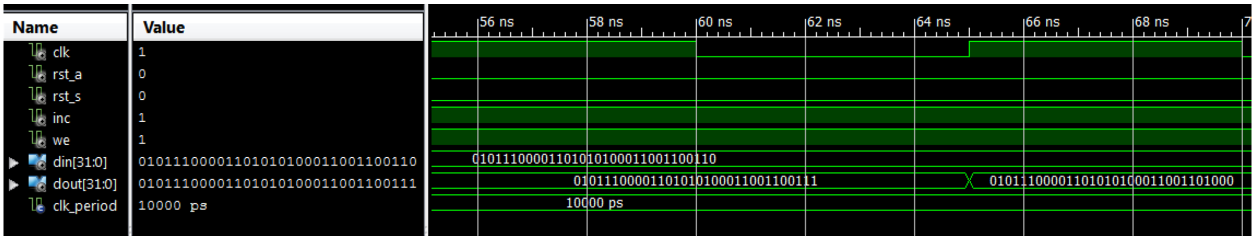
Name	Value
clk	1
rst_a	0
rst_s	1
inc	1
we	0
din[31:0]	01011100001101010100011001100110
dout[31:0]	00000000000000000000000000000000
clk_period	10000 ps

Load input



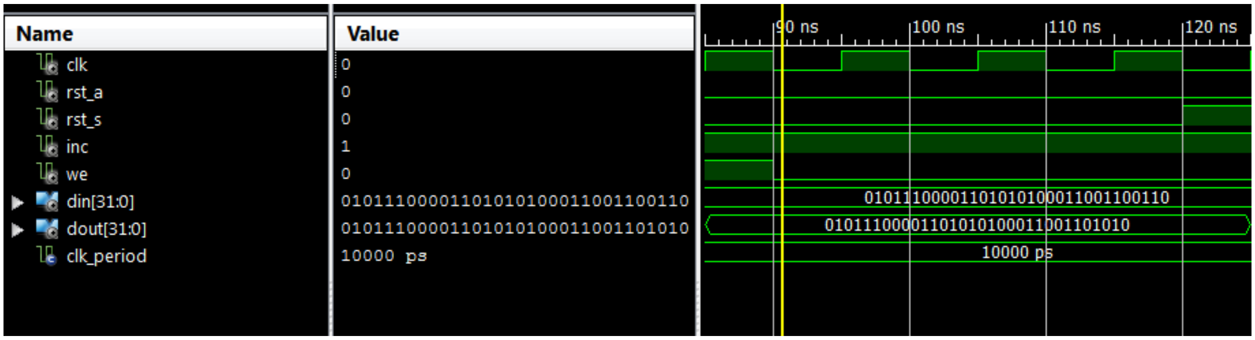
Name	Value
clk	1
rst_a	0
rst_s	0
inc	0
we	1
din[31:0]	01011100001101010100011001100110
dout[31:0]	01011100001101010100011001100110
clk_period	10000 ps

Increment



Name	Value
clk	1
rst_a	0
rst_s	0
inc	1
we	1
din[31:0]	01011100001101010100011001100110
dout[31:0]	01011100001101010100011001100111
clk_period	10000 ps

Hold (write enable off)



Name	Value
clk	0
rst_a	0
rst_s	0
inc	1
we	0
din[31:0]	01011100001101010100011001100110
dout[31:0]	01011100001101010100011001101010
clk_period	10000 ps