Introduction to Digital Logic
EECS/CSE 31L

Assignment 4: Counter

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1 Block Description

- Construct a counter that can be parameterized
- Can either increment or decrement
- Load the counter with a desired value
- Has a synchronous reset

2 Input/Output Port Description

Generic Name	Data Type	Default Value	Description
NBIT	INTEGER	32	Size of counter
STEP	INTEGER	1	How much the counter increments/decrements

Port name	Port size	Port Type	Description
Clk	1	IN	Triggers the counting
Rst_s	1	IN	Will reset the counter to zero when active
asc	1	IN	Increments when ‘1’ and decrements when ‘0’
preload	1	IN	Trigger the counter to load a given value
din	NBIT-1 downto 0	IN	The input value
dout	NBIT-1 downto 0	OUT	The counter’s value after counting

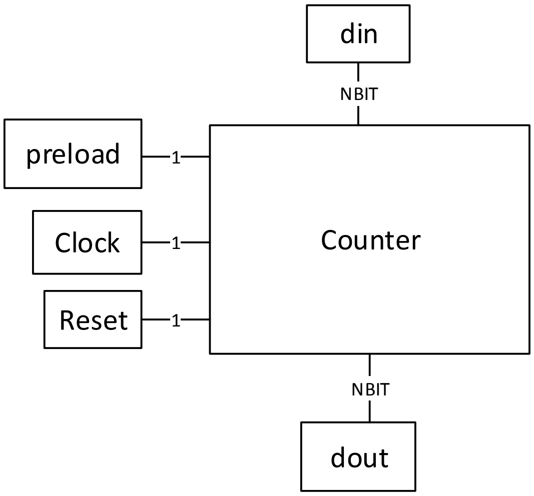
Variable Name	Data Type	Port size	Description
count	INTEGER	NBIT-1 downto 0	Aids in the counting process

3 Design Schematics

Truth Table:

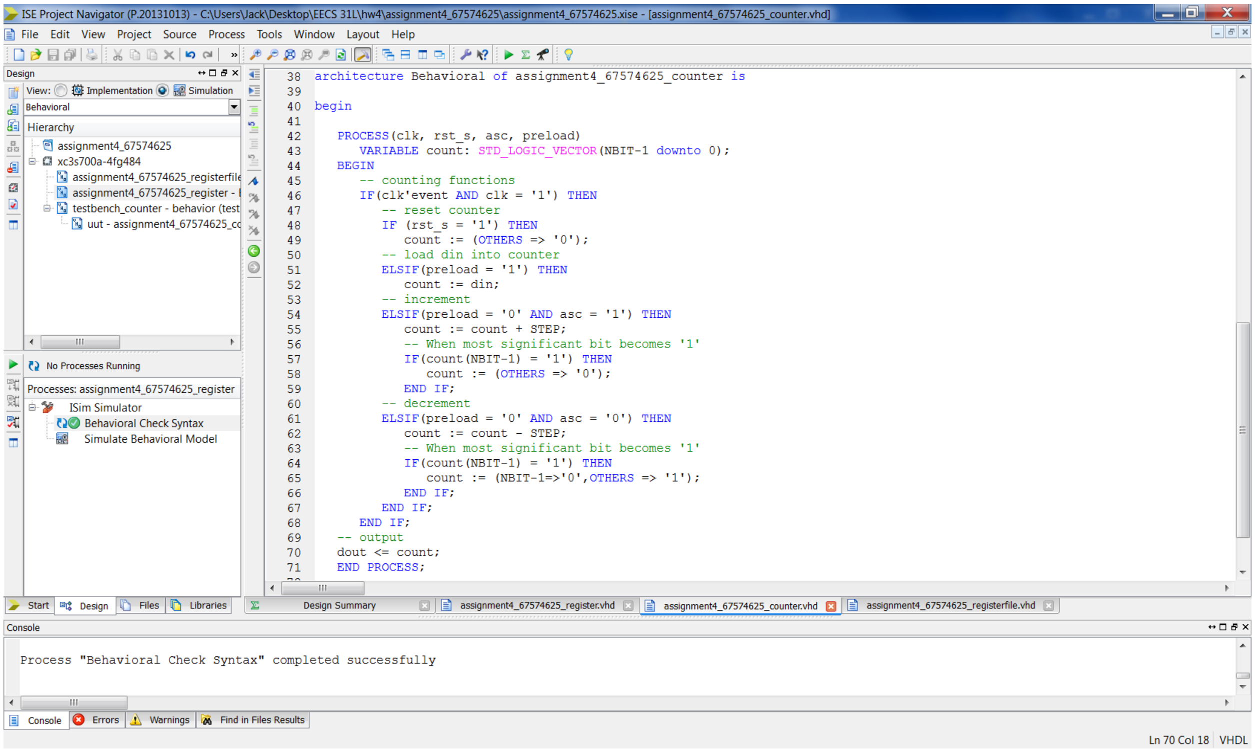
Clk (Rising edge)	Rst_s	asc	preload	Function
1	1	X	X	Reset counter to zero
1	0	1	0	increment
1	0	0	0	decrement
1	0	X	1	Load din into counter

Design:



4 Compilation

Counter


ISE Project Navigator (P.20131013) - C:\Users\Jack\Desktop\EECS 31L\hw4\assignment4_67574625\assignment4_67574625.xise - [assignment4_67574625_counter.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
assignment4_67574625
xc3s700a-4fg484
assignment4_67574625_registerfile
assignment4_67574625_register - I
testbench_counter - behavior (test
uut - assignment4_67574625_cc
No Processes Running
Processes: assignment4_67574625_register
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
Start
Design
Files
Libraries
Design Summary
assignment4_67574625_register.vhd
assignment4_67574625_counter.vhd
assignment4_67574625_registerfile.vhd
Console
Console
Errors
Warnings
Find in Files Results
Ln 70 Col 18
VHDL

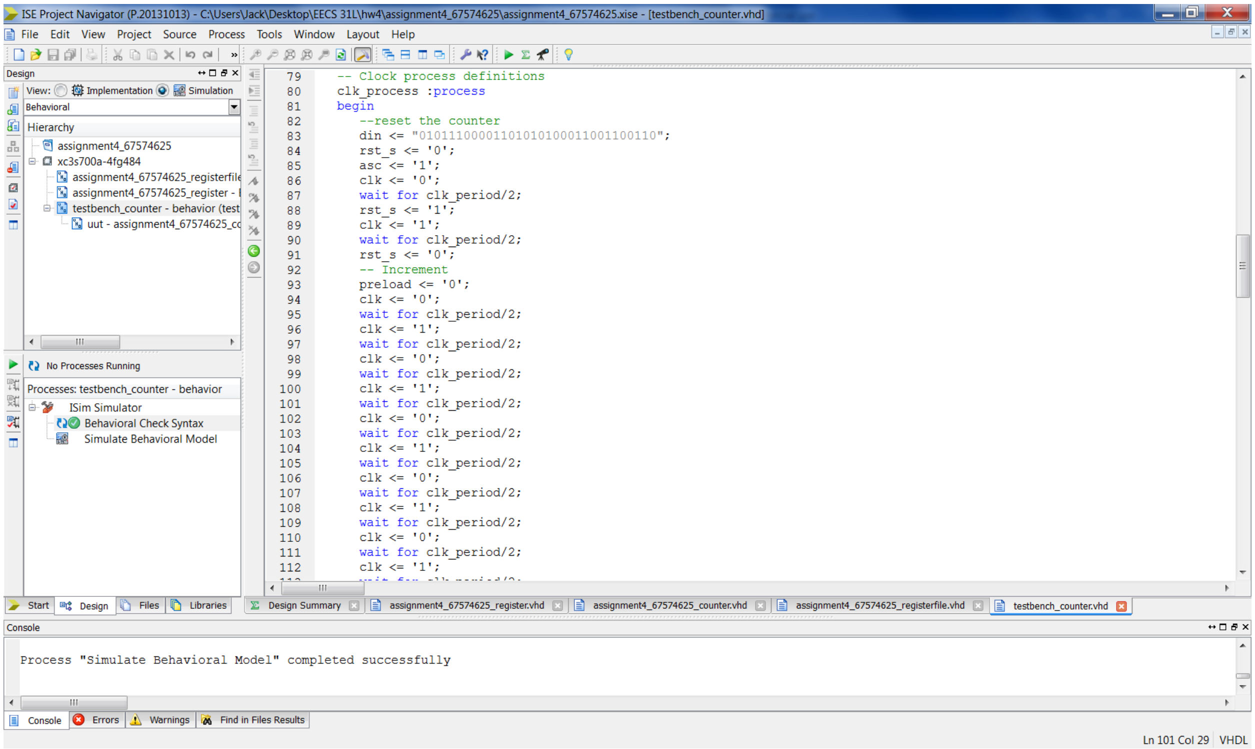
```
architecture Behavioral of assignment4_67574625_counter is

begin

   PROCESS(clk, rst_s, asc, preload)
      VARIABLE count: STD_LOGIC_VECTOR(NBIT-1 downto 0);
   BEGIN
      -- counting functions
      IF(clk'event AND clk = '1') THEN
         -- reset counter
         IF (rst_s = '1') THEN
            count := (OTHERS => '0');
         -- load din into counter
         ELSIF(preload = '1') THEN
            count := din;
         -- increment
         ELSIF(preload = '0' AND asc = '1') THEN
            count := count + STEP;
            -- When most significant bit becomes '1'
            IF(count(NBIT-1) = '1') THEN
               count := (OTHERS => '0');
            END IF;
         -- decrement
         ELSIF(preload = '0' AND asc = '0') THEN
            count := count - STEP;
            -- When most significant bit becomes '1'
            IF(count(NBIT-1) = '1') THEN
               count := (NBIT-1=>'0',OTHERS => '1');
            END IF;
         END IF;
      END IF;
   -- output
   dout <= count;
   END PROCESS;
```

```
Process "Behavioral Check Syntax" completed successfully
```

Testbench


ISE Project Navigator (P.20131013) - C:\Users\Jack\Desktop\EECS 31L\hw4\assignment4_67574625\assignment4_67574625.xise - [testbench_counter.vhd]
File
Edit
View
Project
Source
Process
Tools
Window
Layout
Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
assignment4_67574625
xc3s700a-4fg484
assignment4_67574625_registerfile
assignment4_67574625_register - I
testbench_counter - behavior (test
uut - assignment4_67574625_cc
No Processes Running
Processes: testbench_counter - behavior
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
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assignment4_67574625_register.vhd
assignment4_67574625_counter.vhd
assignment4_67574625_registerfile.vhd
testbench_counter.vhd
Console
Errors
Warnings
Find in Files Results
Ln 101 Col 29
VHDL

```
-- Clock process definitions
clk_process :process
begin
   --reset the counter
   din <= "01011100001101010100011001100110";
   rst_s <= '0';
   asc <= '1';
   clk <= '0';
   wait for clk_period/2;
   rst_s <= '1';
   clk <= '1';
   wait for clk_period/2;
   rst_s <= '0';
   -- Increment
   preload <= '0';
   clk <= '0';
   wait for clk_period/2;
   clk <= '1';
   wait for clk_period/2;
   clk <= '0';
   wait for clk_period/2;
   clk <= '1';
   wait for clk_period/2;
   clk <= '0';
   wait for clk_period/2;
   clk <= '1';
   wait for clk_period/2;
   clk <= '0';
   wait for clk_period/2;
   clk <= '1';
   wait for clk_period/2;
   clk <= '0';
   wait for clk_period/2;
   clk <= '1';
```

```
Process "Simulate Behavioral Model" completed successfully
```

5 Elaboration

Assumptions:

- The counter cannot output a negative value
- The most significant bit will result in the negative value
  - Counter loops back to zero if incrementing
  - Counter loops back to the greatest positive value it can take

Regarding how I wrote my vhdl code

- I used a process with a variable called count
- Used sequential if and elsif statements

Errors and Challenges:

- I was having issues early on with the process statement. I didn't realize "else if" id "elsif" in VHDL
- Misusing assignment operators; tried using signal assignment operator on a variable

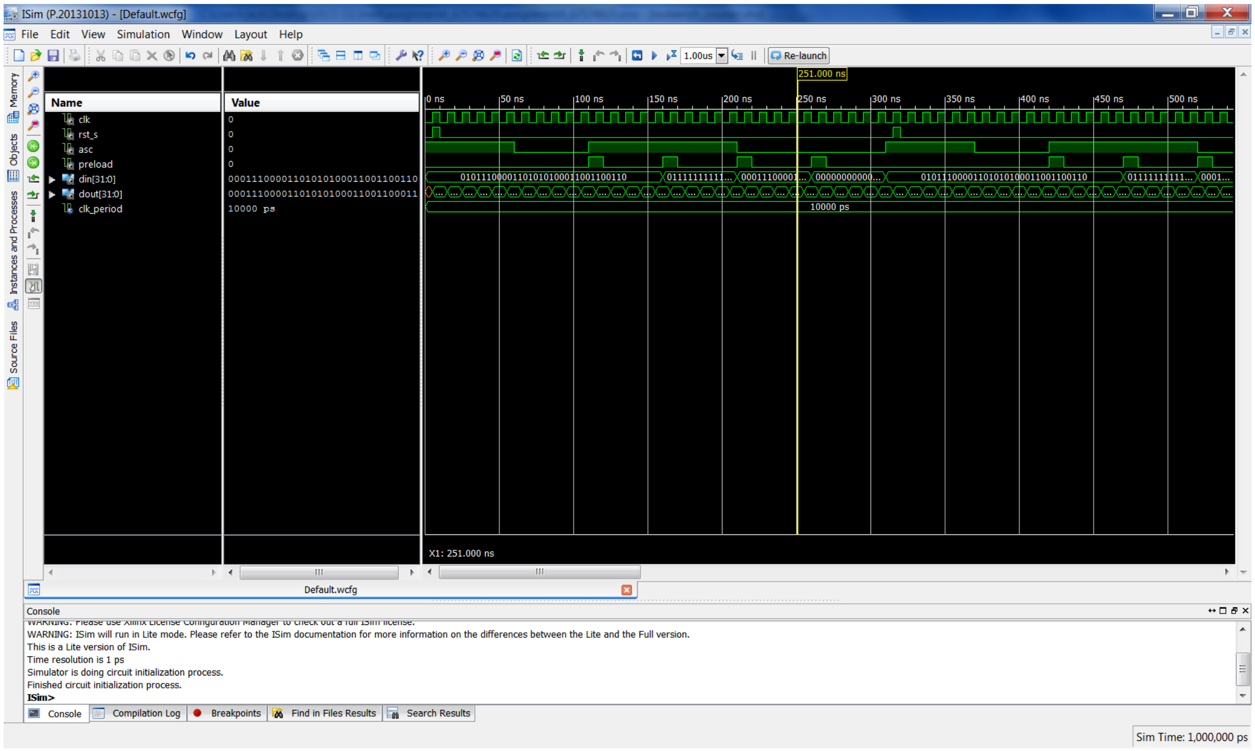
Simulation Log:

```
Started : "Simulate Behavioral Model".

Determining files marked for global include in the design...
Running fuse...
Command Line: fuse -intstyle ise -incremental -o {C:/Users/Jack/Desktop/EECS
31L/hw4/assignment4_67574625/testbench_counter_isim_beh.exe} -prj
{C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4_67574625/testbench_counter_beh.prj}
work.testbench_counter {}
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -intstyle ise -incremental -o
C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4_67574625/testbench_counter_isim_beh.exe
-prj C:/Users/Jack/Desktop/EECS 31L/hw4/assignment4_67574625/testbench_counter_beh.prj
work.testbench_counter
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 4
Turning on mult-threading, number of parallel sub-compilation jobs: 8
Determining compilation order of HDL files
Parsing VHDL file "C:/Users/Jack/Desktop/EECS
31L/hw4/assignment4_67574625/assignment4_67574625_counter.vhd" into library work
Parsing VHDL file "C:/Users/Jack/Desktop/EECS
31L/hw4/assignment4_67574625/testbench_counter.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling package std_logic_arith
Compiling package std_logic_unsigned
Compiling package numeric_std
Compiling architecture behavioral of entity assignment4_67574625_counter
[\assignment4_67574625_counter(32...]
Compiling architecture behavior of entity testbench_counter
Time Resolution for simulation is 1ps.
Compiled 8 VHDL Units
Built simulation executable C:/Users/Jack/Desktop/EECS
31L/hw4/assignment4_67574625/testbench_counter_isim_beh.exe
Fuse Memory Usage: 37152 KB
Fuse CPU Usage: 561 ms
Launching ISim simulation engine GUI...
"C:/Users/Jack/Desktop/EECS
31L/hw4/assignment4_67574625/testbench_counter_isim_beh.exe" -intstyle ise -gui -tclbatch
```

```
isim.cmd  -wdb "C:/Users/Jack/Desktop/EECS
31L/hw4/assignment4_67574625/testbench_counter_isim_beh.wdb"
ISim simulation engine GUI launched successfully

Process "Simulate Behavioral Model" completed successfully
```

6 Waveforms

Full Waveform Snapshot



ISim (P.20131013) - [Default.wcfg]

Name	Value
clk	0
rst_s	0
asc	0
preload	0
din[31:0]	00011100001101010100011001100110
dout[31:0]	00011100001101010100011001100011
clk_period	10000 ps

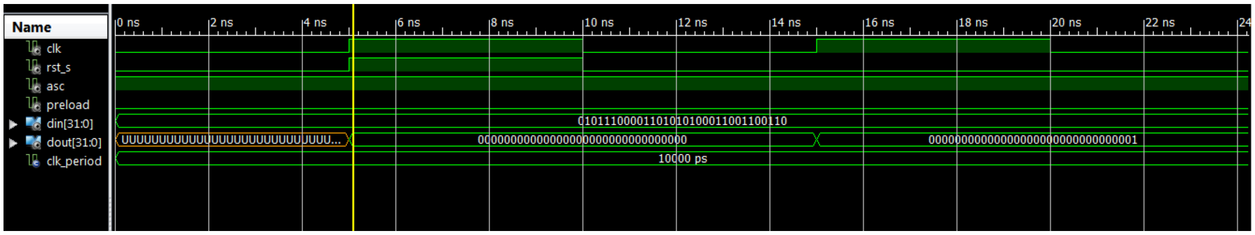
X1: 251.000 ns

```
Console
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
```

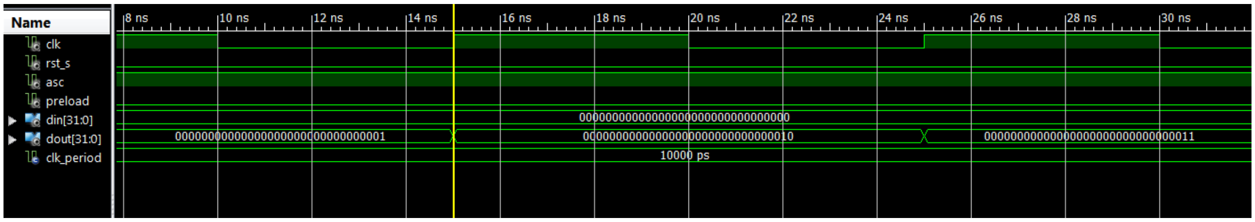
Sim Time: 1,000,000 ps

Snapshots of Waveform

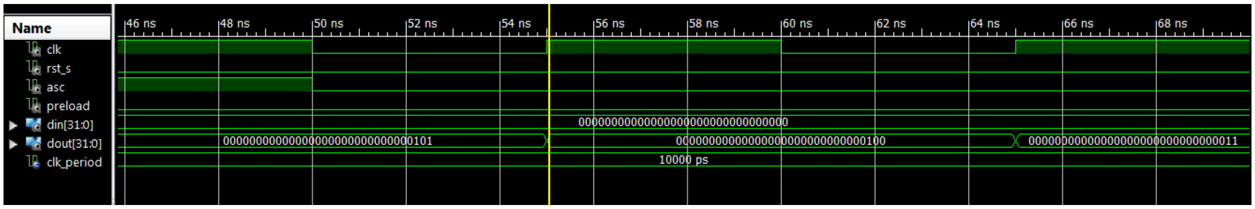
Reset Counter



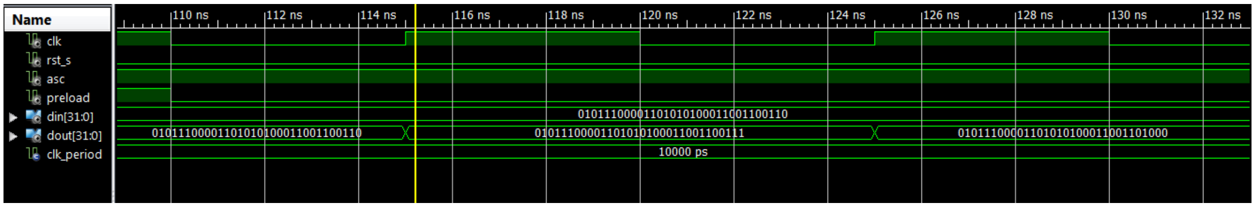
Increment



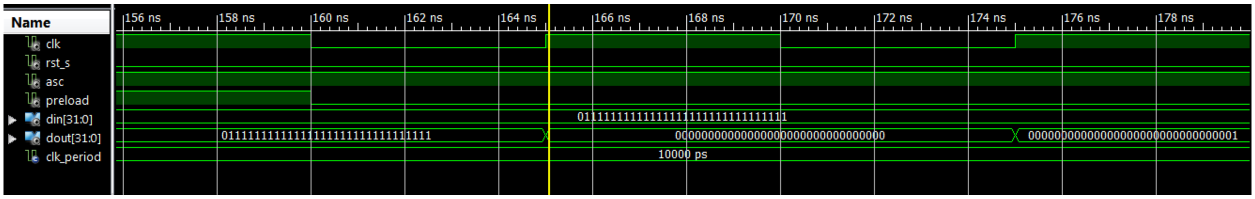
Decrement



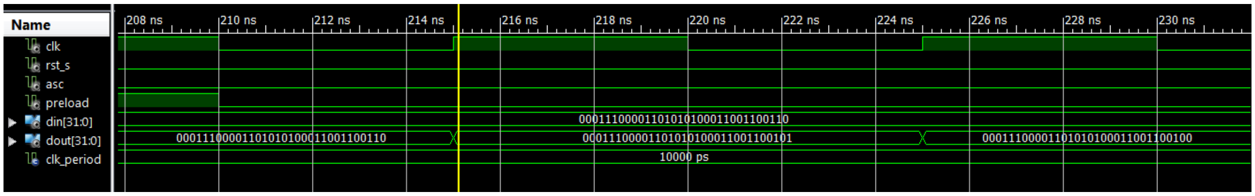
Load random value and start Incrementing



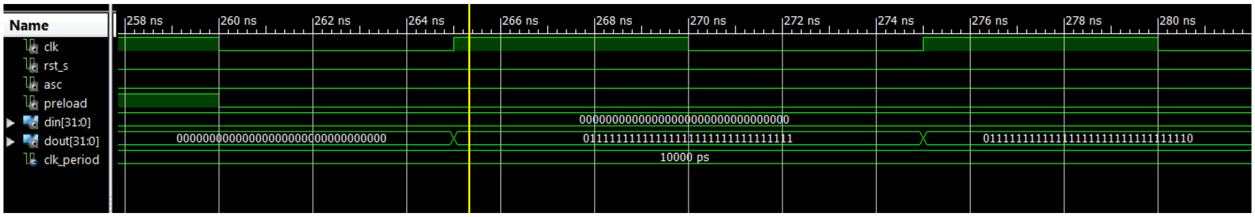
Load greatest positive value and loop back to zero and continue incrementing



Load random value and start Decrementing



Load zero and loop back to greatest positive value and continue decrementing


Name
clk
rst_s
asc
preload
din[31:0]
dout[31:0]
clk_period
258 ns
260 ns
262 ns
264 ns
266 ns
268 ns
270 ns
272 ns
274 ns
276 ns
278 ns
280 ns
00000000000000000000000000000000
00000000000000000000000000000000
01111111111111111111111111111111
01111111111111111111111111111110
10000 ps