Introduction to Digital Logic
EECS/CSE 31L

Assignment 1: 2-Bit Encoder

Prepared by: Jack Melcher
Student ID: 67574625

EECS Department
Henry Samueli School of Engineering
University of California, Irvine

January 14, 2015

1 Block Description

This block is deigned to take in an enable and 2 inputs and encode it into 1 output

2 Input/Output Port Description

Port name	Port size	Port Type	Description
Enable	1	IN	Enable the operation to occur
Input0	1	IN	Gets the first operand
Input1	1	IN	Gets the second operand
output	1	OUT	The operation result

3 Design Schematics

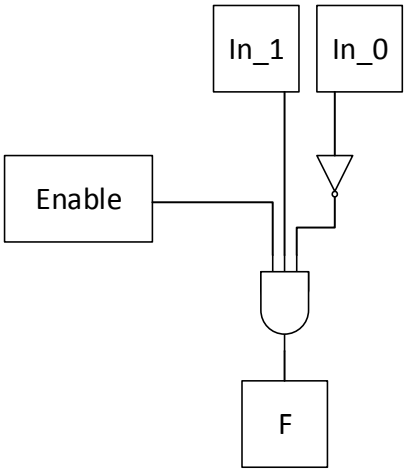
Truth Table:

Enable	In_1	In_0	F
0	X	X	0
1	0	1	0
1	1	0	1

Boolean Expressions:

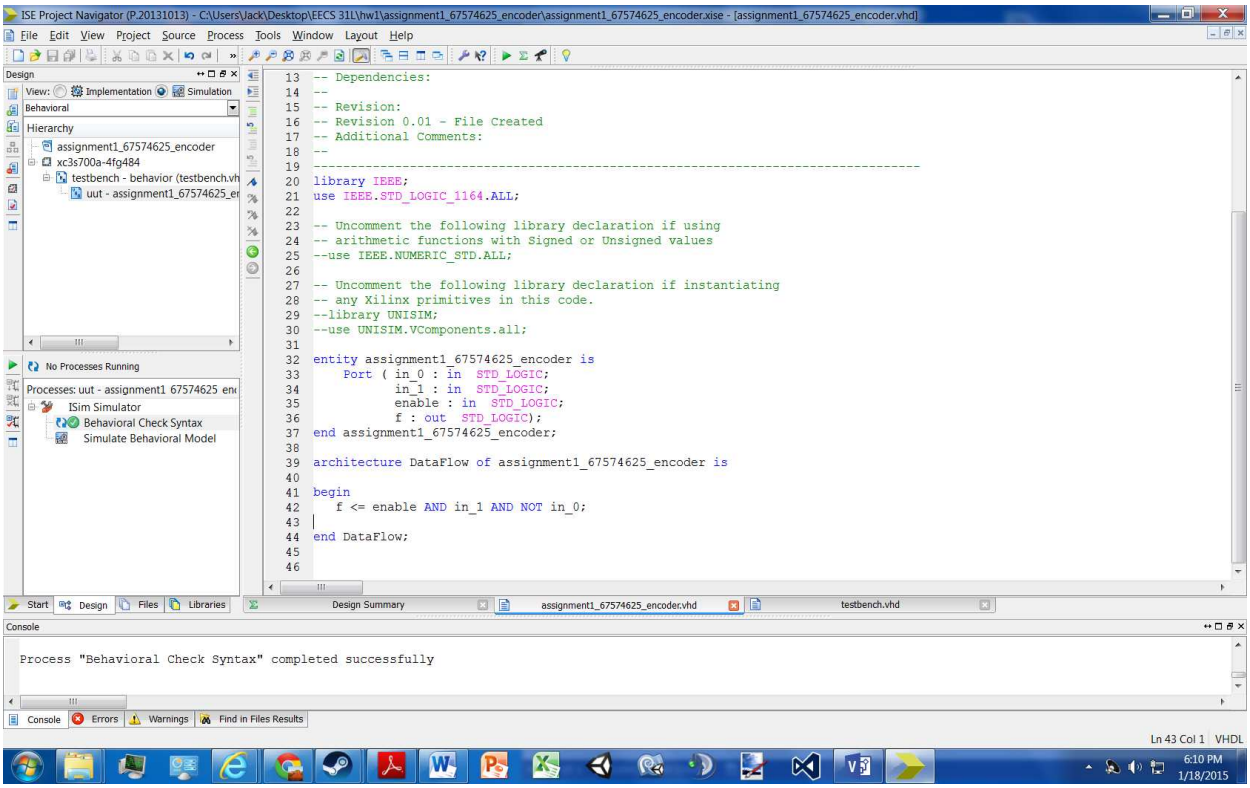
F = (Enable)(In_1)(In_0’)

Gate Representation:

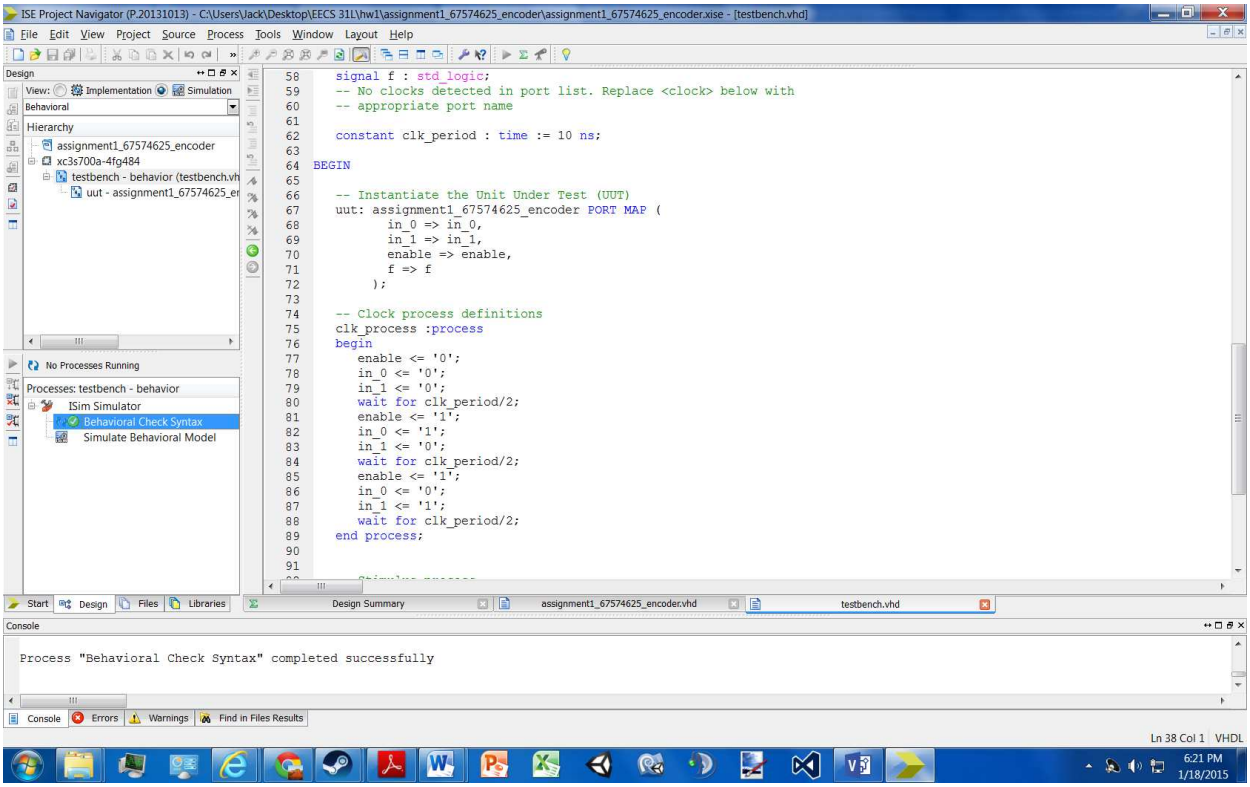


4 Compilation

Encoder compiled



Testbench compiled



5 Elaboration

Assumptions:

- while enable = ‘0’ , in_0 and in_1 can be either ‘0’ or ‘1’ (not shown in waveform)
- encoders do not use input combinations “00” or “11” while enabled

Errors:

- No errors occurred while coding

Simulation Log:

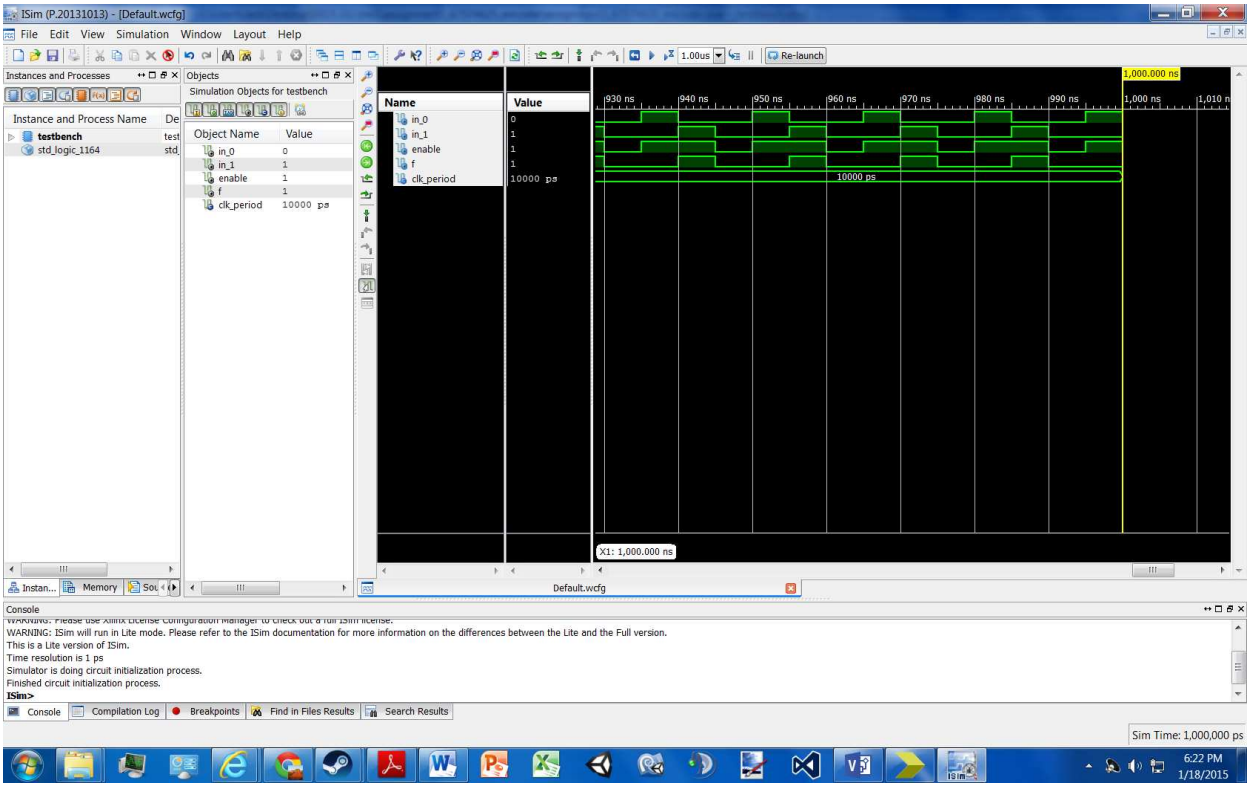
Started : "Simulate Behavioral Model".

Determining files marked for global include in the design...
Running fuse...
Command Line: fuse -intstyle ise -incremental -o {C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_encoder/testbench_isim_beh.exe} -prj {C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_encoder/testbench_beh.prj} work.testbench {}
Running: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\fuse.exe -intstyle ise -incremental -o C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_encoder/testbench_isim_beh.exe -prj

```
C:/Users/Jack/Desktop/EECS 31L/hw1/assignment1_67574625_encoder/testbench_beh.prj
work.testbench
ISim P.20131013 (signature 0x7708f090)
Number of CPUs detected in this system: 4
Turning on mult-threading, number of parallel sub-compilation jobs: 8
Determining compilation order of HDL files
Parsing VHDL file "C:/Users/Jack/Desktop/EECS
31L/hw1/assignment1_67574625_encoder/assignment1_67574625_encoder.vhd" into library
work
Parsing VHDL file "C:/Users/Jack/Desktop/EECS
31L/hw1/assignment1_67574625_encoder/testbench.vhd" into library work
Starting static elaboration
Completed static elaboration
Compiling package standard
Compiling package std_logic_1164
Compiling architecture dataflow of entity assignment1_67574625_encoder
[assignment1_67574625_encoder_def...]
Compiling architecture behavior of entity testbench
Time Resolution for simulation is 1ps.
Compiled 5 VHDL Units
Built simulation executable C:/Users/Jack/Desktop/EECS
31L/hw1/assignment1_67574625_encoder/testbench_isim_beh.exe
Fuse Memory Usage: 29820 KB
Fuse CPU Usage: 420 ms
Launching ISim simulation engine GUI...
"C:/Users/Jack/Desktop/EECS
31L/hw1/assignment1_67574625_encoder/testbench_isim_beh.exe" -intstyle ise -gui -tclbatch
isim.cmd  -wdb "C:/Users/Jack/Desktop/EECS
31L/hw1/assignment1_67574625_encoder/testbench_isim_beh.wdb"
ISim simulation engine GUI launched successfully

Process "Simulate Behavioral Model" completed successfully
```

6 Waveform


ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Instance and Process Name
testbench
std_logic_1164
Objects
Simulation Objects for testbench
Object Name Value
in_0 0
in_1 1
enable 1
f 1
clk_period 10000 ps
Name
Value
930 ns
940 ns
950 ns
960 ns
970 ns
980 ns
990 ns
1,000 ns
1,010 n
1,000.000 ns
10000 ps
X1: 1,000.000 ns
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps
6:22 PM
1/18/2015