

ANALOG CIRCUIT DESIGN NOTES

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November 23, 2016

As you know from elementary school...

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Chapter 1

MOS Overview

1.1 Current with modulation effect

$$I_{DS} = \frac{1}{2} \mu C'_{ox} \frac{W}{L} (V_{GS} - V_t)^2 \left(1 + \frac{V_D - V_S}{V_A}\right) \quad (1.1)$$

1.2 Weak inversion regime

Taxonomy	IC values	Bias range
Weak inversion	$IC \leq 0.1$	$V_{GS} \leq V_T - 0.1V$
Moderate inversion	$0.1 \leq IC \leq 10$	$V_T - 0.1V < V_{GS} < V_T + 0.2V$
Strong inversion	$IC \geq 10$	$V_{GS} \geq V_T + 0.2V$

1.2.1 Inversion Coefficient IC

$$IC = \frac{I}{2n\mu C'_{ox} V_{th}^2 W/L} \quad (1.2)$$

With $n=1.5$ subthreshold coefficient.

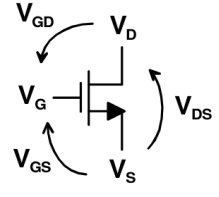
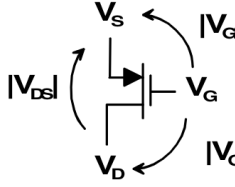
1.2.2 Transconductance

$$g_m = \frac{I}{nV_{th}} \frac{2}{1 + \sqrt{1 + 4IC}} \quad (1.3)$$

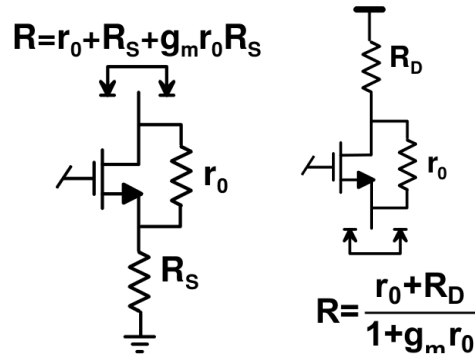
1.3 Cut-off frequency

$$f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad (1.4)$$

1.4 Saturation conditions

<p>Saturation condition for a NMOS:</p> $\begin{cases} V_{GS} > V_T \\ V_{DS} > V_{OV} = V_{GS} - V_T \end{cases}$ <p>The first condition assures that the transistor is on. The second condition corresponds to $V_{GD} < V_T$, and assures to be in the saturation region.</p>	
<p>Saturation condition for a PMOS:</p> $\begin{cases} V_{SG} > V_T \\ V_{SD} > V_{OV} = V_{GS} - V_T \end{cases}$	

1.5 Input and output resistance in MOS circuits



1.6 Pelgrom constants

1.6.1 For resistors

$$\frac{\Delta R}{R} = \frac{K_{\Delta R/R}}{\sqrt{WL}} \quad (1.5)$$

1.6.2 For transistors

Threshold voltage

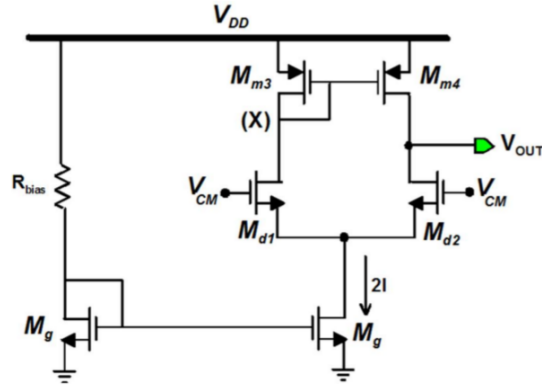
$$\sigma(\Delta V_t) = \frac{K_{\Delta V_t/V_t}}{\sqrt{WL}} \quad (1.6)$$

Parameter k

$$\sigma\left(\frac{\Delta k}{k}\right) = \frac{K_{\Delta V_t/V_t}}{\sqrt{WL}} \quad (1.7)$$

Chapter 2

One stage OTA



2.1 Differential gain

$$G_d = g_{m1} r_{0,2} // r_{0,4} \quad (2.1)$$

2.2 Common mode gain

$$G_{CM} = \frac{\varepsilon(r_{0,2} // r_{0,4})}{r_{0,g}} \quad (2.2)$$

The variable ε has 2 dependance on deterministic and non deterministic effects.

2.2.1 Deterministic contributions

Mirror error

Current read from M3 is a partition ,caused by r_{03} , of the total current.

$$\varepsilon_{det,mirror} = \frac{1/g_{mM}}{1/g_{mM} + r_{03}} = \frac{1}{1 + 1/g_{mM} \cdot r_{03}} \simeq \frac{1}{1/g_{mM} \cdot r_{03}} \quad (2.3)$$

Unballace of the stage

The impedance seen from the source of the input generators if the two branches is not the same.

$$\varepsilon_{det,unbalance} \simeq \frac{1}{r_{01} \cdot 1/g_{mM}} \quad (2.4)$$

2.2.2 Statistical contributions

Statistical mismatch of the mirror

Taking $\Delta g_m = g_{m3} - g_{m4}$

$$\varepsilon_{stat,mirror} = \frac{\Delta g_m}{g_m} \quad (2.5)$$

Statistical mismatch of the input mos

Taking $\Delta g_m = g_{m1} - g_{m2}$ and $g_m = (g_{m1} + g_{m2})/2$

$$\varepsilon_{stat,input} = -\frac{\Delta g_m}{g_m} \left(1 + \frac{2r_{0G}}{r_{01}}\right) \quad (2.6)$$

2.3 CMRR

$$CMRR = G_d/G_{CM} = \frac{2g_{m1}r_{0g}}{\varepsilon} \quad (2.7)$$

2.3.1 Deterministic CMRR

Common mode rejection ratio due to deterministic effect

$$CMRR_{det} \simeq \frac{2g_{m1}r_{0g}}{\frac{1}{1/g_{mM} \cdot r_{03}} + \frac{1}{r_{01} \cdot 1/g_{mM}}} \quad (2.8)$$

2.3.2 Statistical CMRR

Common mode rejection ratio due to statistical effect with very bit r_g approaches to

$$CMRR = G_d/G_{CM} = \frac{2g_{m1}r_{0g}}{\varepsilon_{stat}} \rightarrow \frac{g_{mM} \cdot r_{01}}{\frac{\Delta g_{m1}}{g_{m1}}} \quad (2.9)$$

2.4 Input voltage offset

Input voltage offset caused due to statistical unbalance of the transistors.

2.4.1 Input mismatch

Offset caused by k variations

$$V_{OS}^{in,k} = \frac{V_{ov1}}{2} \cdot \frac{\Delta k}{k} \quad (2.10)$$

Offset caused by V_t variations

$$V_{OS}^{in,V_t} = \Delta V_t \quad (2.11)$$

So the total offset due to input transistors is

$$V_{OS}^{in} = \frac{V_{ov1}}{2} \cdot \frac{\Delta k}{k} + \Delta V_t \quad (2.12)$$

2.4.2 Mirror mismatch

Offset caused by k variations

$$V_{OS}^{mirror,k} = \frac{V_{ov,g}}{2} \cdot \frac{\Delta k_M}{k_M} \quad (2.13)$$

Offset caused by V_t variations

$$V_{OS}^{mirror,V_t} = \frac{V_{ov,g}}{V_{ov,m}} \Delta V_{t,M} \quad (2.14)$$

2.4.3 Total offset

$$V_{OV} = \Delta V_{t,in} + \Delta V_{t,M} \cdot \frac{V_{ov,in}}{V_{ov,M}} + \frac{V_{ov,in}}{2} \left[\left(\frac{\Delta k}{k} \right)_{in} + \left(\frac{\Delta k}{k} \right)_M \right] \quad (2.15)$$

2.5 Dynamics

2.5.1 Output voltage swing

$$V_{out}^{min} = V_{CM} - V_{Td} \quad (2.16)$$

$$V_{out}^{max} = V_{dd} - |V_{ov}^m| \quad (2.17)$$

2.5.2 CM voltage dynamic

$$V_{CM}^{max} = V_{dd} - V_{GSm} + V_{Td} \quad (2.18)$$

$$V_{CM}^{min} = V_{OVg} + V_{GS1} \quad (2.19)$$

2.6 Input equivalent noise

Voltage noise:

$$S_v^{in} = \frac{8kT\gamma}{g_{m1}} \left(1 + \frac{g_{mM}}{g_{m1}} \right) = \frac{8kT\gamma}{g_{m1}} \left(1 + \frac{V_{ov,in}}{V_{ov,m}} \right) \quad (2.20)$$

Current noise:

$$S_i^{in} = kT\gamma(4g_{m,in} + 2g_{m,M} + g_{m,G}) \left(\frac{\omega}{\omega_T} \right)^2 \quad (2.21)$$

With $\omega_T = \frac{1}{C_{gs1}/g_m}$ cut off radial frequency. This noise has a quadratic dependence with frequency.

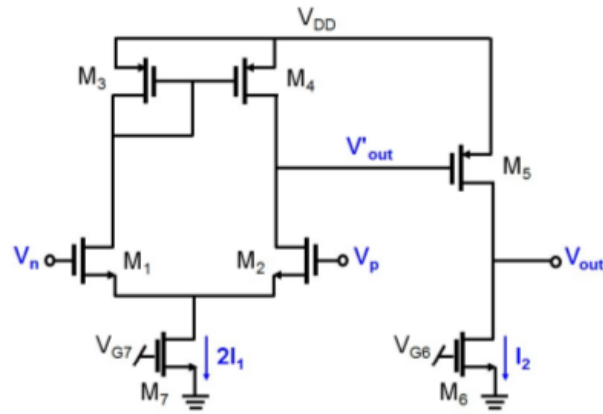
The voltage noise is dominant over the current one until the crossover frequency

$$f \simeq \frac{f_t}{g_m R_s} \quad (2.22)$$

with R_s input resistance of the circuit. In practice we will current noise is considered only in RF applications.

Chapter 3

Two stage OTA

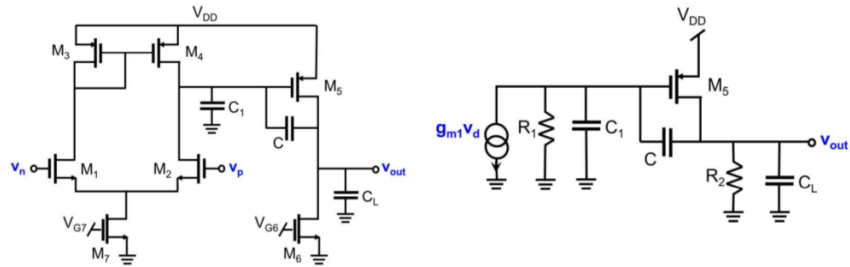


3.1 Differential gain

$$G_d = G_1 G_2 = g_{m,1}(r_{0,2} // r_{0,4}) g_{m,5}(r_{0,5} // r_{0,6}) \quad (3.1)$$

$$G_d = \frac{4V_a^2}{L_{min}^2 V_{ov}^{m5} V_{ov}^{m1}} \left(\frac{L_2 L_4}{L_2 + L_4} \right) \left(\frac{L_5 L_6}{L_5 + L_6} \right) \quad (3.2)$$

3.2 Compensation capacitance



GBWP:

$$GBWP = \frac{g_{m1}}{2\pi C} \quad (3.3)$$

Poles:

$$f_L = \frac{1}{2\pi(R_1 C_1 + R_1 C_1(1 + g_{m5} R_2) + (C + C_L) R_2)} \simeq \frac{1}{2\pi(R_1 C(1 + g_{m5} R_2))} \quad (3.4)$$

$$f_H = \frac{C R_1 g_{m5} R_2}{2\pi(R_1 C_1 R_2 (C_L + C) + R_2 C_L C R_1)} \simeq \frac{C g_{m5}}{2\pi(C(C_1 + C_L) + C_1 C_L)} \quad (3.5)$$

Increasing the compensation capacitance C the low frequency pole decrease while the high frequency pole approaches his asymptotic value

$$f_H \rightarrow \frac{g_{m5}}{2\pi(C_1 + C_L)} \quad (3.6)$$

To find this poles it's useful to use the time constant method.

To find the first pole we have to compute what resistance is seen by a capacitor while the others are open in order to compute the τ^0 :

$$\tau_{C_1}^0 = R_1 C_1 \quad (3.7)$$

$$\tau_{C_L}^0 = R_2 C_L \quad (3.8)$$

$$\tau_C^0 = C(R_2 + R_1(1 + g_{m5} R_2)) \quad (3.9)$$

Doing so we get the first pole

$$f_L = \frac{1}{\tau_{C_1}^0 + \tau_{C_L}^0 + \tau_C^0} \quad (3.10)$$

To estimate the second pole ,since the 3 capacitors are not independent, we may consider the C as a short and doing so we find that C_1 and C_2 are in parallel and they see an impedance of $1/g_{m5}$ that is the asymptotic value.

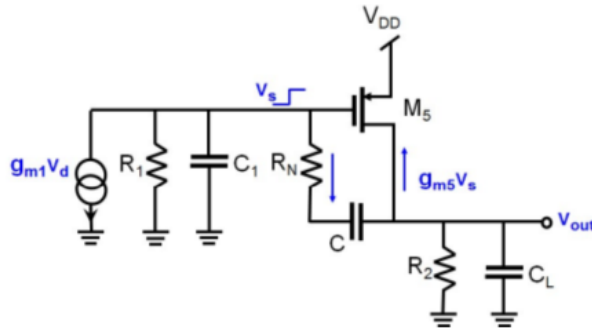
Zero:

$$f_z = \frac{g_{m5}}{2\pi C} \quad (3.11)$$

It's a positive zero that add a -90 shift on the phase.

3.3 Frequency compensation

3.3.1 Nulling resistor



Zero:

The circuit has still a zero in

$$f_z = \frac{1}{2\pi C(R_n - 1/g_{m5})} \quad (3.12)$$

so depending on the value of R_n the zero can be negative or at infinite frequency.

Poles:

We will consider $R_n \simeq 2/g_{m5} \ll R_1, R_2$

Low frequency pole estimated with time constants

$$f_L = \frac{1}{2\pi(R_1C_1 + R_1C_1(1 + g_{m5}R_2) + (C + C_L)R_2) + R_nC} \simeq \frac{1}{2\pi(R_1C(1 + g_{m5}R_2))} \quad (3.13)$$

Middle frequency pole estimated considering C a short

$$f_M \simeq \frac{g_{m5}}{2\pi(C_1 + C_L)} \quad (3.14)$$

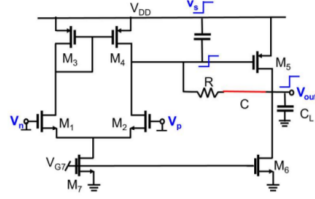
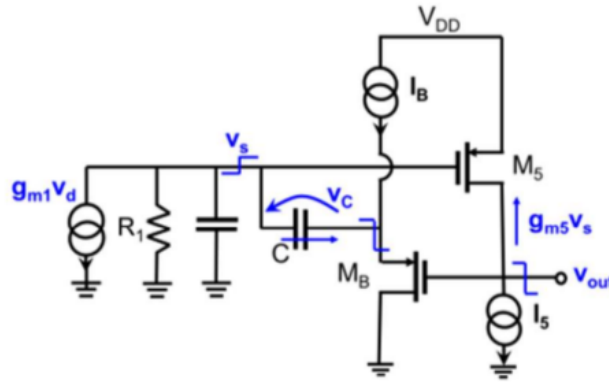
High frequency pole estimated with time constants

$$f_H = \frac{1}{2\pi(C_1 // C_L // C)R_n} \quad (3.15)$$

GBWP:

$$GBWP = \frac{g_{m1}}{2\pi C} \quad (3.16)$$

Remember: this circuit has a bad power supply rejection ration (PSRR) at middle frequency

**3.3.2 Voltage buffer****Zero:**

$$f_z = \frac{1}{2\pi(C/g_{mB})} \quad [LHP] \quad (3.17)$$

Poles:

$$f_L \simeq \frac{1}{2\pi C R_1 (1 + g_{m5} R_2)} \quad (3.18)$$

The high frequency poles are complex conjugate with

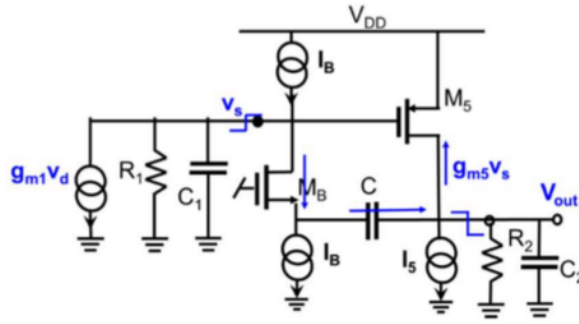
$$\omega_0 = \sqrt{\frac{g_{m5} g_{mB}}{C_1 C_L}} \quad (3.19)$$

$$Q = \sqrt{\frac{g_{m5} C_1}{g_{mB} C_L}} \quad (3.20)$$

GBWP:

$$GBWP = \frac{g_{m1}}{2\pi C} \quad (3.21)$$

3.3.3 Ahuja compensation



Zero:

$$f_z = \frac{1}{2\pi(C/g_{mB})} \quad [LHP] \quad (3.22)$$

Poles:

$$f_L \simeq \frac{1}{2\pi C R_1 (g_{m5} R_2)} \quad (3.23)$$

The high frequency poles are complex conjugate so we get

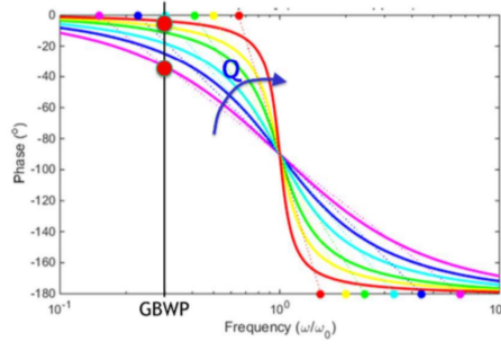
$$\omega_0 = \sqrt{\frac{g_{m5} g_{mB}}{C_1 C_L}} \quad (3.24)$$

$$Q = \sqrt{\frac{g_{m5} C_L}{g_{mB} C_1}} \quad (3.25)$$

GBWP:

$$GBWP = \frac{g_{m1}}{2\pi C} \quad (3.26)$$

Remember the lower the Q factor of the pole pair, the higher the phase shift at the GBWP



3.3.4 Simple cascode

No additional current needed and better PSRR.

Poles:

Same pole of the Ahuja structure so

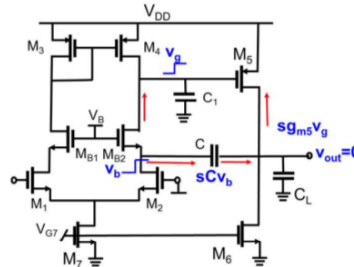
$$f_L \simeq \frac{1}{2\pi C R_1 (g_{m5} R_2)} \quad (3.27)$$

The high frequency poles are complex conjugate so we get

$$\omega_0 = \sqrt{\frac{g_{m5} g_{mB}}{C_1 C_L}} \quad (3.28)$$

$$Q = \sqrt{\frac{g_{m5} C_L}{g_{mB} C_1}} \quad (3.29)$$

Zeros:



To find the zeros we have to derive the following equation

$$i_5 = \frac{g_{m5} g_{mB}}{s C_1} v_b = s C v_b \quad (3.30)$$

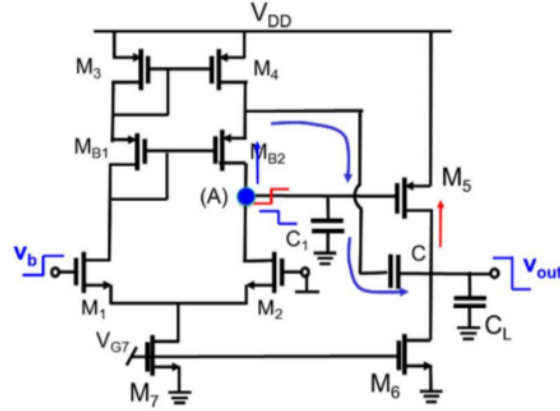
that gives us the 2 zeros one positive and one negative

$$s = \pm \sqrt{\frac{g_{m5} g_{mB}}{C C_L}} \quad (3.31)$$

Taking into account all parassitic terms the 2 zeros are not equal but the positive one is a little bit at lower frequency but provided that $g_{mB}/C_1 \gg g_{m5}/C$ this has a limited impact on the phase margin.

3.3.5 Cascoded mirror

To avoid the RHP zero we can use this configuration



The miller effect is retained and we remove the RHP zero.

3.4 Slew Rate SR

3.4.1 Internal SR

For this we don't have to take into account the load capacitance so

$$SR_{int} = \frac{2I_1}{g_{m1}}(2\pi GBWP) = \frac{2I_1}{C} \quad (3.32)$$

3.4.2 Power Bandwith

The maximum frequency that can be reached by full swing armonic signals without suffering from slew-rate distortion

$$f_{PBW} = \frac{SR}{2\pi A_{max}} \quad (3.33)$$

where A_{max} is the maximum value allowed to the voltage dynamics at the output node.

3.4.3 External SR

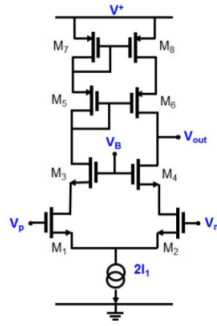
$$SR_{ext} = \frac{I_5}{C + C_L} \quad (3.34)$$

Chapter 4

High gain one stage OTA

4.1 Telescopic cascode

4.1.1 Gain



Considering all transistors with the same r_0

$$G_d = \frac{(g_{m1}r_0)^2}{2} \quad (4.1)$$

If the r_0 are different we get

$$r_{down} = \frac{r_{04} + 2r_{02} + 2g_{m4}r_{04}r_{02}}{2} \simeq \frac{2g_{m4}r_{04}r_{02}}{2} = g_{m4}r_{04}r_{02} \quad (4.2)$$

$$r_{up} = r_{06} + r_{08} + g_{m6}r_{06}r_{08} \simeq g_{m6}r_{06}r_{08} \quad (4.3)$$

so for Norton theorem

$$G_d = g_{m1} \cdot r_{down} / r_{up} \quad (4.4)$$

4.1.2 Dynamics

Output voltage swing

Upper voltage limited by M6 saturation

$$V_{out}^{max} = V_{dd} - V_{gs8} + V_{ov6} \quad (4.5)$$

Lower voltage limited by M4 saturation

$$V_{out}^{min} = V_B - V_t \quad (4.6)$$

Input common mode range

Upper voltage limited by saturation of M1-M2

$$V_{CM}^{max} = V_B - V_{gs4} + V_t \quad (4.7)$$

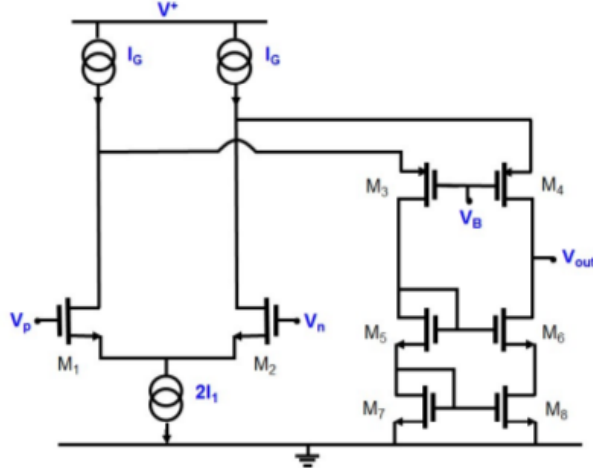
Lower voltage limited by saturation of the tail current generator

$$V_{CM}^{min} = V_{ovG} + V_{gs1} \quad (4.8)$$

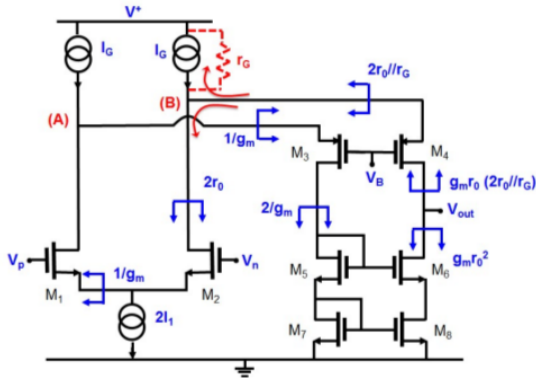
The setting of V_B is quite critical. By decreasing V_B , the output swing increases, but reducing the common-mode swing.

$$V_B^{max} = V_{dd} - V_{gs7} - V_{ov6} \quad V_B^{min} = V_{ovG} + V_{ov2} + V_{gs3} \quad (4.9)$$

4.2 Folded cascode



4.2.1 Gain



Using Norton theorem

$$r_{down} = r_{06} + r_{08} + g_{m6}r_{06}r_{08} \simeq g_{m6}r_{06}r_{08} \quad (4.10)$$

The upper resistance

without taking into account the loop is

$$r_{up}^{no-loop} = r_{04} + r_{0g} // 2r_{02} + g_{m4}r_{04}(r_{0g} // 2r_{02}) \simeq g_{m4}r_{04}(r_{0g} // 2r_{02}) \quad (4.11)$$

The G_{loop} is now

$$G_{loop} = -\frac{r_{0g}}{r_{0g} + 2r_{02}} \quad (4.12)$$

Therefore we have

$$r_{up} \simeq g_{m4}r_{04}(r_{04} // r_{0g}) \quad (4.13)$$

and a differential gain of

$$G_d = g_{m1}g_{m4} \cdot r_{up} // r_{down} \simeq \frac{(g_m r_0)^2}{3} \quad (4.14)$$

4.2.2 Dynamics

Output voltage swing

Upper voltage limited by the saturation of M4

$$V_{out}^{max} = V_B + V_t \quad (4.15)$$

Lower voltage limited by the voltage drop across the mirror

$$V_{out}^{min} = V_{gs7} + V_{ov6} \quad (4.16)$$

Input common mode range

Upper limit is the saturation of M1 and M2

$$V_{CM}^{max} = V_B + V_{gs4} + V_t \quad (4.17)$$

Lower limit is the current source saturation

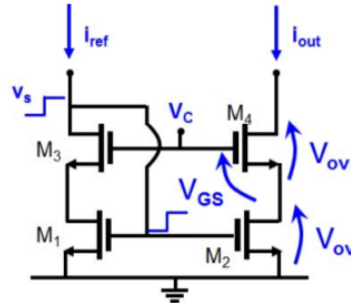
$$V_{CM}^{min} = V_{ovG} + V_{gs1} \quad (4.18)$$

By increasing the V_B value both the output swing and the common-mode range increases.

The upper limit for V_B is set by the saturation of the 2 generators

$$V_B^{max} = V^+ - V_{ovG} - |V_{gs4}| \quad (4.19)$$

To further increase the voltage dynamic is possible to use this topology instead of the mirror-load.



Remember to prevent the degradation of the amplifier time response I_G must be $> 2I_1$

Chapter 5

Output buffers