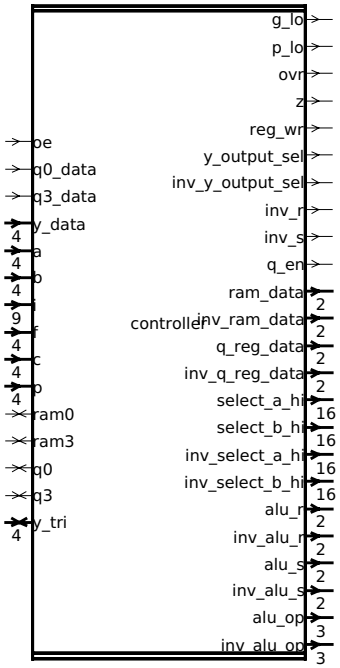
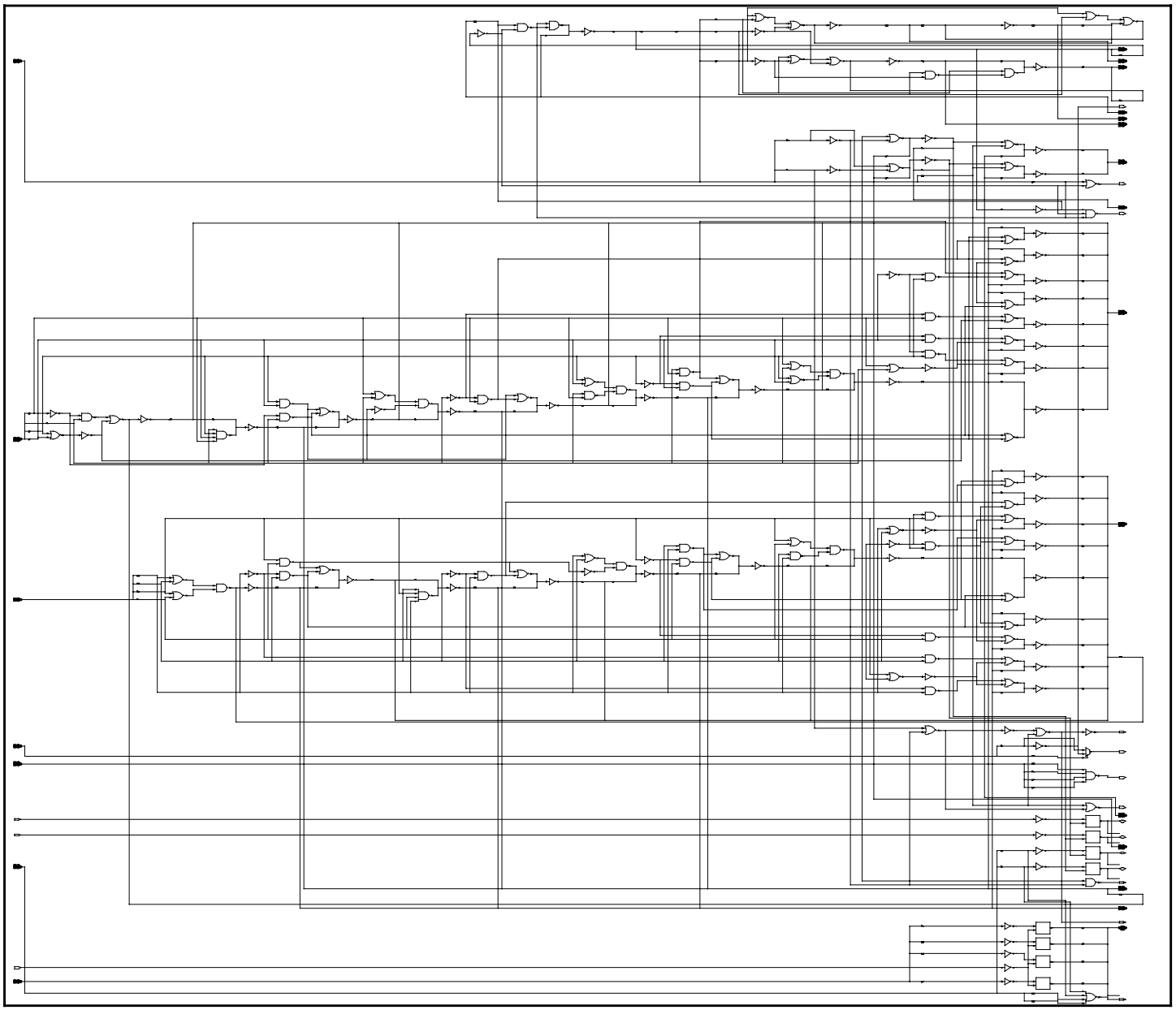
1. **Synthesis (rise/fall constraints = 275 and 325 respectively):**

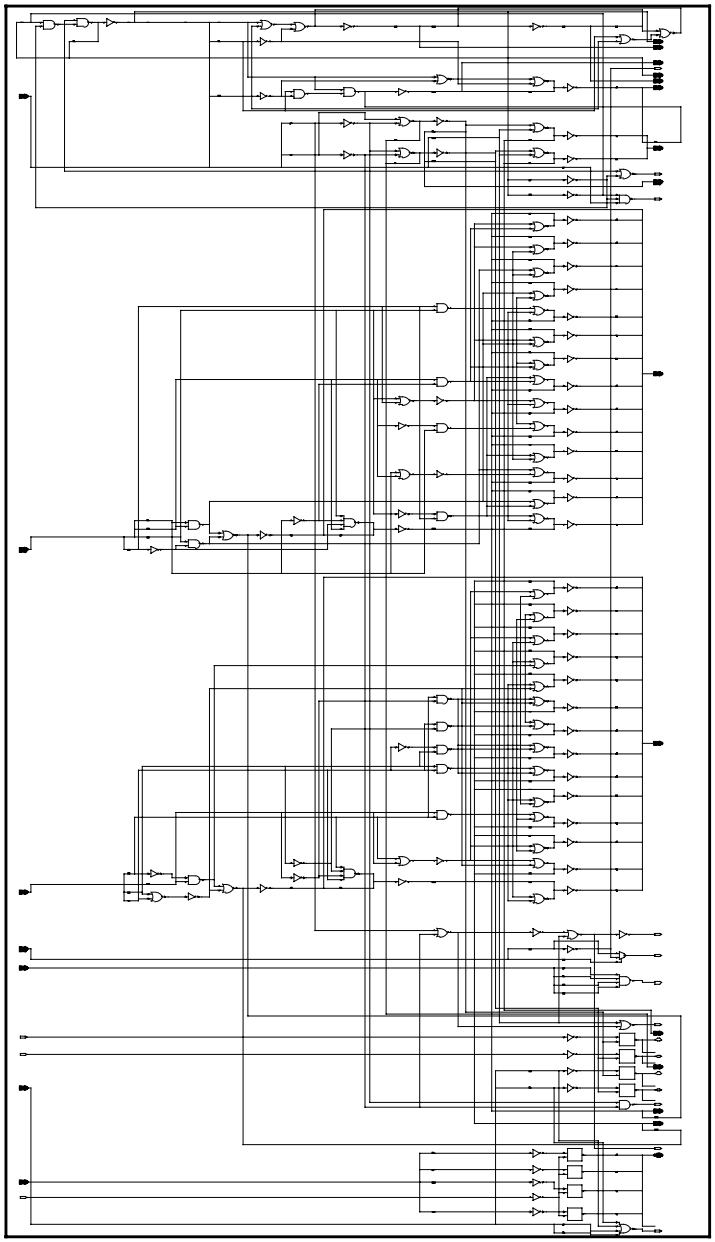
   Max rise/fall time = 275ps
   Capacitive load = 5pF
   Total cell area = 9928.396774um^2

   Max rise/fall time = 325ps
   Capacitive load = 5pF
   Total cell area = 8393.414383um^2

   Note: Capacitive load = 5pF instead of 10pF because our design utilizes *select_a_hi[15:0]* and *select_b_hi[15:0]* along with their complementary signals (i.e. *inv_select_a_hi[15:0]* and *inv_select_b_hi[15:0])* as opposed to using inverters to generate these signals in the *regbit* cell.


g_lo
p_lo
ovr
z
reg_wr
y_output_sel
inv_y_output_sel
inv_r
inv_s
q_en
ram_data
inv_ram_data
q_reg_data
inv_q_reg_data
select_a_hi
select_b_hi
inv_select_a_hi
inv_select_b_hi
alu_r
inv_alu_r
alu_s
inv_alu_s
alu_op
inv_alu_op
controller
oe
q0_data
q3_data
y_data
a
b
i
f
c
p
ram0
ram3
q0
q3
y_tri
4
9
2
16
3





```
#################################################################
#  Generated by:      Cadence Encounter 14.28-s033_1
#  OS:                Linux x86_64(Host ID linux-32.ews.illinois.edu)
#  Generated on:      Tue May 10 13:54:04 2022
#  Design:            controller
#  Command:           summaryReport -noHtml -outfile summaryReport.rpt
#################################################################


==============================
General Design Information
==============================
Design Status: Routed
Design Name: controller
# Instances: 150
# Hard Macros: 0
# Std Cells: 150
    ------------------------------
    Standard Cells in Netlist
    ------------------------------
              Cell Type   Instance Count  Area (um^2)
                 and3_1                1          97.9776
                  inv_1               59        2890.3392
                  inv_2                6         293.9328
                  inv_4                6         293.9328
                invzp_1                8         653.1840
                 mux2_1                1         114.3072
                nand2_1                5         326.5920
                nand2_2               12         783.8208
                nand4_1                3         244.9440
                 nor2_1               44        2155.5072
                 nor2_4                4         457.2288
                 nor4_1                1          81.6480
# Pads: 0
# Net: 195
# Special Net: 2
# IO Pins:
    ------------------------------
    Issued IO Information
    ------------------------------
    # Unplaced IO Pin  0
    # Floating IO
        ------------------------------
        Floating IO
        ------------------------------
            Floating IO Name
               inv_alu_op[2]
                        c[0]
                        c[1]  3
    # IO Connected to Non-IO Inst
        ------------------------------
        IO Connected to Non-IO Inst
        ------------------------------
                     IO Name      Non-IO Inst Name
                        q_en                 U406
                      inv_s                  U408
                      inv_r                  U407
            inv_y_output_sel                 U338
                y_output_sel                 U337
               inv_alu_op[0]                 U333
               inv_alu_op[1]                 U310
                   alu_op[0]                 U334
                   alu_op[1]                 U310
```

alu_op[2]	U307
inv_alu_s[0]	U331
inv_alu_s[1]	U327
alu_s[0]	U330
alu_s[1]	U328
inv_alu_r[0]	U321
inv_alu_r[1]	U325
alu_r[0]	U322
alu_r[1]	U324
inv_q_reg_data[0]	U319
inv_q_reg_data[1]	U315
q_reg_data[0]	U318
q_reg_data[1]	U314
inv_ram_data[0]	drvqshl
inv_ram_data[1]	drvqshr
ram_data[0]	U316
ram_data[1]	U312
reg_wr	U405
q3_data	U350
q0_data	U356
q3	drvqshl
q0	drvqshr
ram3	drvraml
ram0	drvramr
oe	U309
y_data[0]	U354
y_data[1]	U353
y_data[2]	U352
y_data[3]	U351
y_tri[0]	drvy0
y_tri[1]	drvy1
y_tri[2]	drvy2
y_tri[3]	drvy3
z	U311
ovr	U358
p_lo	U357
g_lo	U279
p[0]	U357
p[1]	U357
p[2]	U357
p[3]	U357
c[2]	U358
c[3]	U279
f[0]	U311
f[1]	U311
f[2]	U311
f[3]	U311
inv_select_b_hi[0]	U348
inv_select_b_hi[1]	U392
inv_select_b_hi[2]	U394
inv_select_b_hi[3]	U376
inv_select_b_hi[4]	U359
inv_select_b_hi[5]	U380
inv_select_b_hi[6]	U280
inv_select_b_hi[7]	U367
inv_select_b_hi[8]	U360
inv_select_b_hi[9]	U382
inv_select_b_hi[10]	U384
inv_select_b_hi[11]	U368
inv_select_b_hi[12]	U364
inv_select_b_hi[13]	U395
inv_select_b_hi[14]	U397
inv_select_b_hi[15]	U370

inv_select_a_hi[0]	U343
inv_select_a_hi[1]	U399
inv_select_a_hi[2]	U401
inv_select_a_hi[3]	U378
inv_select_a_hi[4]	U361
inv_select_a_hi[5]	U386
inv_select_a_hi[6]	U281
inv_select_a_hi[7]	U371
inv_select_a_hi[8]	U362
inv_select_a_hi[9]	U388
inv_select_a_hi[10]	U390
inv_select_a_hi[11]	U372
inv_select_a_hi[12]	U366
inv_select_a_hi[13]	U402
inv_select_a_hi[14]	U404
inv_select_a_hi[15]	U374
select_b_hi[0]	U347
select_b_hi[1]	U391
select_b_hi[2]	U393
select_b_hi[3]	U375
select_b_hi[4]	U282
select_b_hi[5]	U379
select_b_hi[6]	U283
select_b_hi[7]	U284
select_b_hi[8]	U285
select_b_hi[9]	U381
select_b_hi[10]	U383
select_b_hi[11]	U286
select_b_hi[12]	U363
select_b_hi[13]	U287
select_b_hi[14]	U396
select_b_hi[15]	U369
select_a_hi[0]	U342
select_a_hi[1]	U398
select_a_hi[2]	U400
select_a_hi[3]	U377
select_a_hi[4]	U288
select_a_hi[5]	U385
select_a_hi[6]	U289
select_a_hi[7]	U290
select_a_hi[8]	U291
select_a_hi[9]	U387
select_a_hi[10]	U389
select_a_hi[11]	U292
select_a_hi[12]	U365
select_a_hi[13]	U293
select_a_hi[14]	U403
select_a_hi[15]	U373
b[0]	U269
b[1]	U269
b[2]	U267
b[3]	U267
a[0]	U270
a[1]	U270
a[2]	U268
a[3]	U268
i[0]	U320
i[1]	U306
i[2]	U308
i[3]	U307
i[4]	U333
i[5]	U310
i[6]	U314

```
                        i[7]                  U275
                        i[8]                  U276  137  140
# Pins:
    ------------------------------
    Correctness of Pin Connectivity for All Instances
    ------------------------------
    # Floating Terms  0
    # Output Term Marked Tie Hi/Lo  0
    # Output Term Shorted to PG Net  0  389
# PG Pins:
    ------------------------------
    Correctness of PG Pin Connectivity for All Instances
    ------------------------------
    # Instances that No Net Defined for Any PG Pin
        ------------------------------
        The Instances that No Net Defined for any PG Pin
        ------------------------------
               Instance Name
                        U408
                        U407
                        U406
                        U405
                        U404
                        U403
                        U402
                        U401
                        U400
                        U399
                        U398
                        U397
                        U396
                        U395
                        U394
                        U393
                        U392
                        U391
                        U390
                        U389
                        U388
                        U387
                        U386
                        U385
                        U384
                        U383
                        U382
                        U381
                        U380
                        U379
                        U378
                        U377
                        U376
                        U375
                        U374
                        U373
                        U372
                        U371
                        U370
                        U369
                        U368
                        U367
                        U366
                        U365
                        U364
```

U363
U362
U361
U360
U359
U358
U357
U356
U355
U354
U353
U352
U351
U350
U349
U348
U347
U346
U345
U344
U343
U342
U341
U340
U339
U338
U337
U336
U335
U334
U333
U332
U331
U330
U329
U328
U327
U326
U325
U324
U323
U322
U321
U320
U319
U318
U317
U316
U315
U314
U313
U312
U311
U310
U309
U308
U307
U306
U305
U304
U303
U302
U301

```
                        U300
                        U299
                        U298
                        U297
                        U296
                        U295
                        U294
                        U293
                        U292
                        U291
                        U290
                        U289
                        U288
                        U287
                        U286
                        U285
                        U284
                        U283
                        U282
                        U281
                        U280
                        U279
                        U278
                        U277
                        U276
                        U275
                        U274
                        U273
                        U272
                        U271
                        U270
                        U269
                        U268
                        U267
                      drvy3
                      drvy2
                      drvy1
                      drvy0
                    drvraml
                    drvramr
                    drvqshl
                    drvqshr  150
    # Floating PG Terms  0
    # PG Pins Connect to Non-PG Net  0
    # Power Pins Connect Ground Net  0
    # Ground Pins Connect Power Net  0  300
Average Pins Per Net(Signal): 1.995

==============================
General Library Information
==============================
# Routing Layers: 5
# Masterslice Layers: 12
# Pin Layers:
    General Caution:
        1) Library have metal1, metal2, metal3, metal4 and metal5 pins, you should setP
reRouteAsObs {1 2 3}                                    to ensure these pins are accessibl
e after placement

    ------------------------------
    Pin Layers
    ------------------------------
    metal5
```

```
    metal4
    metal3
    metal2
    metal1  5
# Layers:
    ------------------------------
    Layer metal5 Information
    ------------------------------
    Type  Routing
    Wire Pitch X  2.160 um
    Wire Pitch Y  2.160 um
    Wire Width  0.480 um
    Spacing  0.480 um
    ------------------------------
    Layer via4 Information
    ------------------------------
    Type  Cut
    Vias
        ------------------------------
        Via list in layer via4
        ------------------------------
                Vias in via4  Default
                       M5_M4      Yes  For complete list click here
    Multiple Orientation Vias  CAUTION: There is only one default via in this layer
    ------------------------------
    Layer metal4 Information
    ------------------------------
    Type  Routing
    Wire Pitch X  1.080 um
    Wire Pitch Y  1.080 um
    Wire Width  0.360 um
    Spacing  0.480 um
    ------------------------------
    Layer via3 Information
    ------------------------------
    Type  Cut
    Vias
        ------------------------------
        Via list in layer via3
        ------------------------------
                Vias in via3  Default
                       M4_M3      Yes  For complete list click here
    Multiple Orientation Vias  CAUTION: There is only one default via in this layer
    ------------------------------
    Layer metal3 Information
    ------------------------------
    Type  Routing
    Wire Pitch X  1.080 um
    Wire Pitch Y  1.080 um
    Wire Width  0.360 um
    Spacing  0.480 um
    ------------------------------
    Layer via2 Information
    ------------------------------
    Type  Cut
    Vias
        ------------------------------
        Via list in layer via2
        ------------------------------
                Vias in via2  Default
                       M3_M2      Yes  For complete list click here
    Multiple Orientation Vias  CAUTION: There is only one default via in this layer
    ------------------------------
```

```
Layer metal2 Information
------------------------------
Type  Routing
Wire Pitch X  1.080 um
Wire Pitch Y  1.080 um
Wire Width  0.360 um
Spacing  0.480 um
------------------------------
Layer via Information
------------------------------
Type  Cut
Vias
    ------------------------------
    Via list in layer via
    ------------------------------
             Vias in via  Default
                  M2_M1      Yes  For complete list click here
Multiple Orientation Vias  CAUTION: There is only one default via in this layer
------------------------------
Layer metal1 Information
------------------------------
Type  Routing
Wire Pitch X  1.080 um
Wire Pitch Y  1.080 um
Wire Width  0.360 um
Spacing  0.360 um
------------------------------
Layer cc Information
------------------------------
Type  Cut
Vias
    ------------------------------
    Via list in layer cc
    ------------------------------
              Vias in cc  Default
                 M1_POLY       No
                    NTAP       No
                    M1_N       No
                    M1_P       No  For complete list click here
------------------------------
Layer nodrc Information
------------------------------
Type  Masterslice
------------------------------
Layer metalcap Information
------------------------------
Type  Masterslice
------------------------------
Layer cap_id Information
------------------------------
Type  Masterslice
------------------------------
Layer res_id Information
------------------------------
Type  Masterslice
------------------------------
Layer text Information
------------------------------
Type  Masterslice
------------------------------
Layer sblock Information
------------------------------
Type  Masterslice
```

```
    ------------------------------
    Layer pad Information
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer glass Information
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer poly Information
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer pactive Information
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer nactive Information
    ------------------------------
    Type  Masterslice
    ------------------------------
    Layer nwell Information
    ------------------------------
    Type  Masterslice  22
# Pins without Physical Port: 0
# Pins in Library without Timing Lib:
    ------------------------------
    Pins in Library without timing lib
    ------------------------------
               Cell Name      List of Pin Name
                  ABnorC                   ip1
                  ABnorC                   ip2
                  ABnorC                   ip3
                  ABnorC                    op
                   ABorC                   ip1
                   ABorC                   ip2
                   ABorC                   ip3
                   ABorC                    op
            ab_or_c_or_d                   ip1
            ab_or_c_or_d                   ip2
            ab_or_c_or_d                   ip3
            ab_or_c_or_d                   ip4
            ab_or_c_or_d                    op
                  and2_1                   ip1
                  and2_1                   ip2
                  and2_1                    op
                  and2_2                   ip1
                  and2_2                   ip2
                  and2_2                    op
                  and2_4                   ip1
                  and2_4                   ip2
                  and2_4                    op
                  and3_1                   ip1
                  and3_1                   ip2
                  and3_1                   ip3
                  and3_1                    op
                  and3_2                   ip1
                  and3_2                   ip2
                  and3_2                   ip3
                  and3_2                    op
                  and3_4                   ip1
                  and3_4                   ip2
                  and3_4                   ip3
```

and3_4	op
and4_1	ip1
and4_1	ip2
and4_1	ip3
and4_1	ip4
and4_1	op
and4_2	ip1
and4_2	ip2
and4_2	ip3
and4_2	ip4
and4_2	op
and4_4	ip1
and4_4	ip2
and4_4	ip3
and4_4	ip4
and4_4	op
buf_1	ip
buf_1	op
buf_2	ip
buf_2	op
buf_4	ip
buf_4	op
bufzp_2	c
bufzp_2	ip
bufzp_2	op
cd_12	ip
cd_12	op
cd_16	ip
cd_16	op
cd_8	ip
cd_8	op
dksp_1	ck
dksp_1	ip
dksp_1	q
dksp_1	qb
dksp_1	sb
dp_1	ck
dp_1	ip
dp_1	q
dp_2	ck
dp_2	ip
dp_2	q
dp_4	ck
dp_4	ip
dp_4	q
drp_1	ck
drp_1	ip
drp_1	q
drp_1	rb
drp_2	ck
drp_2	ip
drp_2	q
drp_2	rb
drp_4	ck
drp_4	ip
drp_4	q
drp_4	rb
drsp_1	ck
drsp_1	ip
drsp_1	q
drsp_1	rb
drsp_1	s
drsp_2	ck

drsp_2	ip
drsp_2	q
drsp_2	rb
drsp_2	s
drsp_4	ck
drsp_4	ip
drsp_4	q
drsp_4	rb
drsp_4	s
dtrsp_2	ck
dtrsp_2	ip
dtrsp_2	q
dtrsp_2	rb
dtrsp_2	s
dtrsp_2	sip
dtrsp_2	sm
fulladder	a
fulladder	b
fulladder	ci
fulladder	co
fulladder	s
inv_1	ip
inv_1	op
inv_2	ip
inv_2	op
inv_4	ip
inv_4	op
invzp_1	c
invzp_1	ip
invzp_1	op
invzp_2	c
invzp_2	ip
invzp_2	op
invzp_4	c
invzp_4	ip
invzp_4	op
jkrp_2	ck
jkrp_2	j
jkrp_2	k
jkrp_2	q
jkrp_2	qb
jkrp_2	rb
lp_1	ck
lp_1	ip
lp_1	q
lp_2	ck
lp_2	ip
lp_2	q
lrp_1	ck
lrp_1	ip
lrp_1	q
lrp_1	rb
lrp_2	ck
lrp_2	ip
lrp_2	q
lrp_2	rb
lrp_4	ck
lrp_4	ip
lrp_4	q
lrp_4	rb
lrsp_1	ck
lrsp_1	ip
lrsp_1	q

lrsp_1	rb
lrsp_1	s
lrsp_2	ck
lrsp_2	ip
lrsp_2	q
lrsp_2	rb
lrsp_2	s
lrsp_4	ck
lrsp_4	ip
lrsp_4	q
lrsp_4	rb
lrsp_4	s
mux2_1	ip1
mux2_1	ip2
mux2_1	op
mux2_1	s
mux2_2	ip1
mux2_2	ip2
mux2_2	op
mux2_2	s
mux2_4	ip1
mux2_4	ip2
mux2_4	op
mux2_4	s
mux3_2	ip1
mux3_2	ip2
mux3_2	ip3
mux3_2	op
mux3_2	s0
mux3_2	s1
mux4_2	ip1
mux4_2	ip2
mux4_2	ip3
mux4_2	ip4
mux4_2	op
mux4_2	s0
mux4_2	s1
nand2_1	ip1
nand2_1	ip2
nand2_1	op
nand2_2	ip1
nand2_2	ip2
nand2_2	op
nand2_4	ip1
nand2_4	ip2
nand2_4	op
nand3_1	ip1
nand3_1	ip2
nand3_1	ip3
nand3_1	op
nand3_2	ip1
nand3_2	ip2
nand3_2	ip3
nand3_2	op
nand3_4	ip1
nand3_4	ip2
nand3_4	ip3
nand3_4	op
nand4_1	ip1
nand4_1	ip2
nand4_1	ip3
nand4_1	ip4
nand4_1	op

nand4_2	ip1
nand4_2	ip2
nand4_2	ip3
nand4_2	ip4
nand4_2	op
nand4_4	ip1
nand4_4	ip2
nand4_4	ip3
nand4_4	ip4
nand4_4	op
nor2_1	ip1
nor2_1	ip2
nor2_1	op
nor2_2	ip1
nor2_2	ip2
nor2_2	op
nor2_4	ip1
nor2_4	ip2
nor2_4	op
nor3_1	ip1
nor3_1	ip2
nor3_1	ip3
nor3_1	op
nor3_2	ip1
nor3_2	ip2
nor3_2	ip3
nor3_2	op
nor3_4	ip1
nor3_4	ip2
nor3_4	ip3
nor3_4	op
nor4_1	ip1
nor4_1	ip2
nor4_1	ip3
nor4_1	ip4
nor4_1	op
nor4_2	ip1
nor4_2	ip2
nor4_2	ip3
nor4_2	ip4
nor4_2	op
nor4_4	ip1
nor4_4	ip2
nor4_4	ip3
nor4_4	ip4
nor4_4	op
not_ab_or_c_or_d	ip1
not_ab_or_c_or_d	ip2
not_ab_or_c_or_d	ip3
not_ab_or_c_or_d	ip4
not_ab_or_c_or_d	op
or2_1	ip1
or2_1	ip2
or2_1	op
or2_2	ip1
or2_2	ip2
or2_2	op
or2_4	ip1
or2_4	ip2
or2_4	op
or3_1	ip1
or3_1	ip2
or3_1	ip3

```
                  or3_1                    op
                  or3_2                   ip1
                  or3_2                   ip2
                  or3_2                   ip3
                  or3_2                    op
                  or3_4                   ip1
                  or3_4                   ip2
                  or3_4                   ip3
                  or3_4                    op
                  or4_1                   ip1
                  or4_1                   ip2
                  or4_1                   ip3
                  or4_1                   ip4
                  or4_1                    op
                  or4_2                   ip1
                  or4_2                   ip2
                  or4_2                   ip3
                  or4_2                   ip4
                  or4_2                    op
                  or4_4                   ip1
                  or4_4                   ip2
                  or4_4                   ip3
                  or4_4                   ip4
                  or4_4                    op
                xnor2_1                   ip1
                xnor2_1                   ip2
                xnor2_1                    op
                xnor2_2                   ip1
                xnor2_2                   ip2
                xnor2_2                    op
                 xor2_1                   ip1
                 xor2_1                   ip2
                 xor2_1                    op
                 xor2_2                   ip1
                 xor2_2                   ip2
                 xor2_2                    op
                 padgnd                  pad
          padbidirhe_025                   di
          padbidirhe_025                  dib
          padbidirhe_025                   do
          padbidirhe_025                  oeb
          padbidirhe_025                  pad
                 padinc                   di
                 padinc                  dib
                 padinc                  pad
                  padio                 data
                  padio                  pad
                 padout                   di
                 padout                  dib
                 padout                   do
                 padout                  pad
                 padvdd                  pad
            padnoconnect                 pad  338
# Pins Missing Direction: 0
Antenna Summary Report:
    General Caution:
        1) All Antenna Constructs are absent for the layer section of LEF.
        2) All Antenna Constructs are absent for the macro section of LEF.For more info
rmation click here
# Cells Missing LEF Info: 0
# Cells with Dimension Errors: 0

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Netlist Information
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# HFO (>200) Nets: 0
# No-driven Nets: 7
    General Caution:
        1) TODO
    No-driven Nets
    i_0
    i_1
    i_2
    i_4
    inv_alu_op[2]
    i[3]
    i[5]
# Multi-driven Nets: 0
# Assign Statements: 6
    General Caution:
        1) The assignment statements can impact CTS and IPO.
        2) You can use "setDoAssign" properly to slove the problem.

    Verilog File Name: controller_synth.v
    Module Name: controller
    alu_op[1] = i[5]
    alu_op[2] = i[3]
    i_0 = i[0]
    i_1 = i[1]
    i_2 = i[2]
    i_4 = i[4]
Is Design Uniquified: YES
# Pins in Netlist without timing lib:
    ------------------------------
    Pins in Netlist without timing lib
    ------------------------------
    Cell Name  List of Pin Name
    and3_1  ip1
    and3_1  ip2
    and3_1  ip3
    and3_1  op
    inv_1  ip
    inv_1  op
    inv_2  ip
    inv_2  op
    inv_4  ip
    inv_4  op
    invzp_1  c
    invzp_1  ip
    invzp_1  op
    mux2_1  ip1
    mux2_1  ip2
    mux2_1  op
    mux2_1  s
    nand2_1  ip1
    nand2_1  ip2
    nand2_1  op
    nand2_2  ip1
    nand2_2  ip2
    nand2_2  op
    nand4_1  ip1
    nand4_1  ip2
    nand4_1  ip3
    nand4_1  ip4
    nand4_1  op
    nor2_1  ip1
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    nor2_1  ip2
    nor2_1  op
    nor2_4  ip1
    nor2_4  ip2
    nor2_4  op
    nor4_1  ip1
    nor4_1  ip2
    nor4_1  ip3
    nor4_1  ip4
    nor4_1  op  39

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: Internal  External
No of Nets:        184           0
No of Connections:        342           0
Total Net Length (X): 3.2780e+03  0.0000e+00
Total Net Length (Y): 3.5082e+03  0.0000e+00
Total Net Length: 6.7862e+03  0.0000e+00

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Timing Information
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# Clocks in design: 0
# Generated clocks: 0
# "dont_use" cells from .libs: 0
# "dont_touch" cells from .libs: 0
# Cells in .lib with max_tran: 0
# Cells in .lib with max_cap: 0
# Cells in .lib with max_fanout: 0
SDC max_cap: N/A
SDC max_tran: N/A
SDC max_fanout: N/A
Default Ext. Scale Factor: 1.000
Detail Ext. Scale Factor: 1.000

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Floorplan/Placement Information
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Total area of Standard cells: 8393.414 um^2
Total area of Standard cells(Subtracting Physical Cells): 8393.414 um^2
Total area of Macros: 0.000 um^2
Total area of Blockages: 0.000 um^2
Total area of Pad cells: 0.000 um^2
Total area of Core: 10336.637 um^2
Total area of Chip: 10336.637 um^2
Effective Utilization: 8.5240e-01
Number of Cell Rows: 3
% Pure Gate Density #1 (Subtracting BLOCKAGES): 81.201%
% Pure Gate Density #2 (Subtracting BLOCKAGES and Physical Cells): 81.201%
% Pure Gate Density #3 (Subtracting MACROS): 81.201%
% Pure Gate Density #4 (Subtracting MACROS and Physical Cells): 81.201%
% Pure Gate Density #5 (Subtracting MACROS and BLOCKAGES): 81.201%
% Pure Gate Density #6 (Subtracting MACROS and BLOCKAGES and Physical Cells): 81.201%
% Core Density (Counting Std Cells and MACROs): 81.201%
% Core Density #2(Subtracting Physical Cells): 81.201%
% Chip Density (Counting Std Cells and MACROs and IOs): 81.201%
% Chip Density #2(Subtracting Physical Cells): 81.201%
# Macros within 5 sites of IO pad: No
Macro halo defined?: No

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Wire Length Distribution
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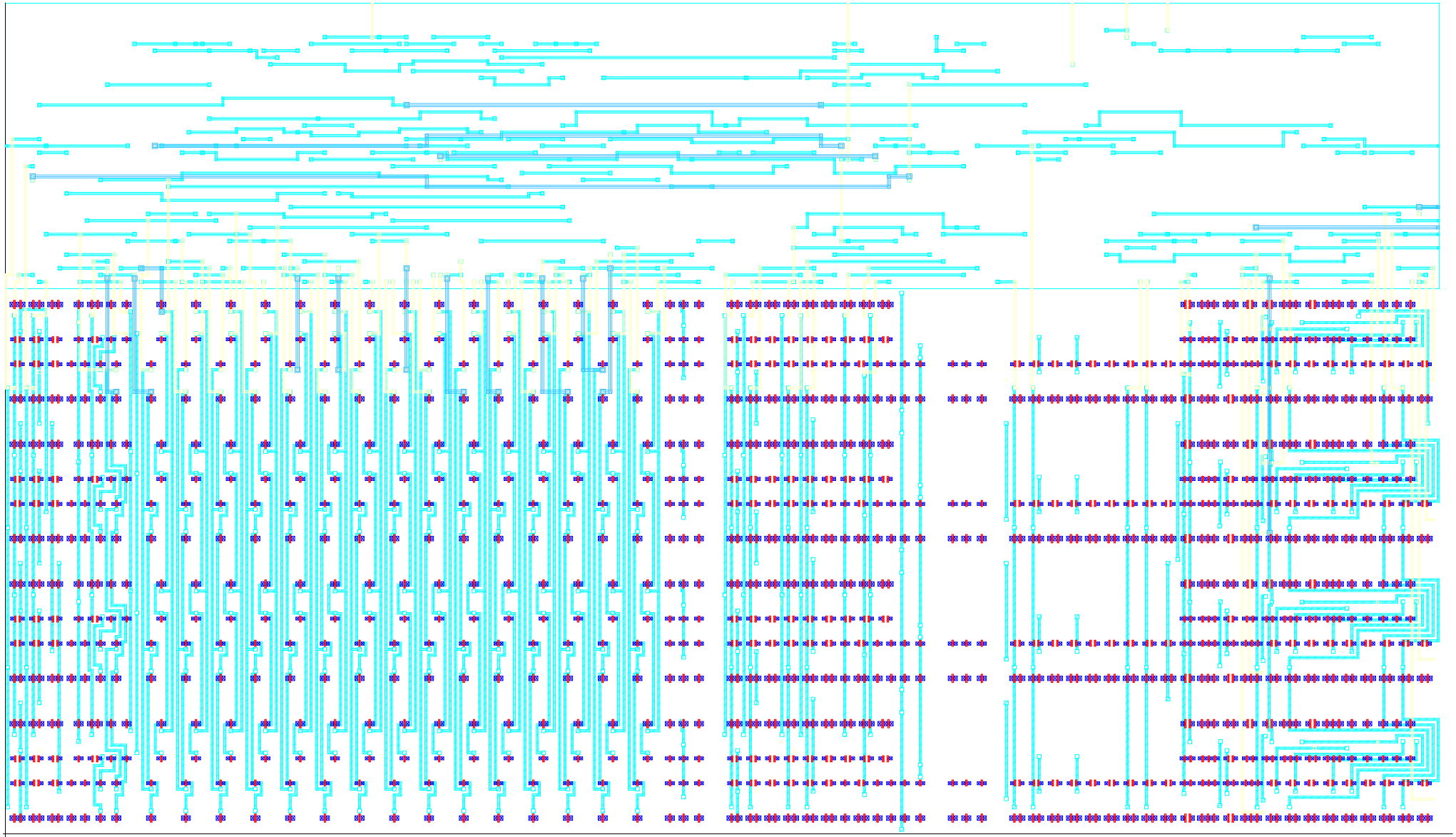
Total metal1 wire length: 358.5600 um
Total metal2 wire length: 1709.8200 um
Total metal3 wire length: 2439.8400 um
Total metal4 wire length: 1786.5600 um
Total metal5 wire length: 658.5000 um
Total wire length: 6953.2800 um
Average wire length/net: 35.6578 um
Area of Power Net Distribution:

Area of Power Net Distribution

Layer Name	Area of Power Net	Routable Area	Percentage
metal1	902.4048	10336.6368	8.7302%
metal2	146.9664	10336.6368	1.4218%
metal3	0.0000	10331.9420	0.0000%
metal4	0.0000	10336.6368	0.0000%
metal5	0.0000	10336.6368	0.0000%

For more information click here



Total Layout Area for ‘am2901’ = 228.72 [um] * 132 [um] = 30,191.04 [um²]