Rev. 1.0, Feb. 2014

K9ACGD8S0C
K9CFGD8SXC
K9OHGD8SXC

64Gb C-die Toggle NAND Flash

Multi-Level-Cell (3bit/cell)

datasheet ***WF biz Only***

Revision History

Revision No.	History	Draft Date	Remark	Edited by
1.0	1. Customer Sample	Feb. 06, 2014	Final	S.M.Lee

Table Of Contents

1.0 INTRODUCTION

1.1 Features

- Voltage Supply :
  - VCC : 3.3V (2.7V ~ 3.6V)
  - VccQ : 3.3V (2.7V ~ 3.6V)
- Organization
  - Page Size : (8K + 1024) x 8bit
  - Data Register : (8K + 1024) x 8bit
  - Block Size : (2M + 256K) bytes
  - Unit Device capacity : (2M + 256K) x 4281
- Products
  - K9ACGD8S0C : Unit device x 1

- Automatic Program and Erase
  - Page Program : (8K + 1024)Byte
  - Block Erase : (2M + 256K)Byte
- Page Read Operation
  - Random Read : TLC part : 90μs(Max.)
    SLC part : 50μs(Max.)
  - Data Transfer rate : up to 400Mbps or 200Mhz
- Write Cycle Time
  - Page Program time : TLC part : 1.65ms(Typ.)
    SLC part : 0.35ms(Typ.)
  - Block Erase Time : TLC part : 5ms(Typ.)
    SLC part : 10ms(Typ.)
- Command/Address/Data Multiplexed DQ Port
- Toggle Mode DDR Data Interface
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - ECC Requirement : 70bit/BCH
- Command Driven Operation
- Scalable DQ Driver

- Package :

1.2 Product List

Part Number	Density	Interface	Organization	Vcc Range	VccQ Range	PKG Type
K9ACGD8S0C	64Gb	Toggle DDR	x8	2.7V ~ 3.6V	2.7V ~ 3.6V	Wafer

1.3 General Description

Toggle DDR is a NAND interface for high performance applications which support data read and write operations using bidirectional DQS.

Toggle DDR NAND has implemented 'Double Data Rate' without a clock. It is compatible with functions and command which have been supported in conventional type NAND(i.e. SDR NAND) while providing high data transfer rate based on the high-speed Toggle DDR Interface and saving power with separated DQ voltage. For applications that require high capacity and high performance NAND, Toggle DDR NAND is the most appropriate.

Toggle DDR2.0 NAND supports the interface speed of up to 200 MHz(400 Mbps), which is more than 10 times faster than the data transfer rate offered by SDR NAND (40Mbps). Toggle DDR NAND transfers data at high speed using DQS signal that behaves as a clock, and DQS shall be used only when data is transferred for optimal power consumption.

1.4 Toggle DDR Interface according to Data Transfer Rate

Feature		up to 200Mbps (100Mhz)
VccQ		3.3V
I/O Type	CMOS	Support
	Vref Support	Not support
	Differential signaling for DQS and $\overline{RE}$ 1)	Not support

NOTE :
1) Vref shall be used for DQx when differential signaling is used.

1.5 Definitions and Abbreviations

DDR
Acronym for double data rate.

Address
The address is comprised of a column address with 2 cycles and a row address with 3 cycles. The row address identifies the page, block and LUN to be accessed. The column address identifies the byte within a page to access. The least significant bit of the column address shall always be zero.

Column
The byte location within the page register.

Row
Refer to the block and page to be accessed.

Page
The smallest addressable unit for the Read and the Program operations.

Block
Consists of multiple pages and is the smallest addressable unit for the Erase operation.

Page register
Register used to transfer data to and from the Flash Array.

Defect area
The defect area is where factory defects are marked by the manufacturer. Refer to the section 3.2

Device
The packaged NAND unit. A device may contain more than a target.

LUN (Logical Unit Number)
The minimum unit that can independently execute commands and report status. There are one or more LUNs per $\overline{CE}$.

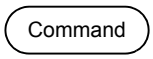
Target
An independent NAND Flash component with its own $\overline{CE}$ signal.

SR[x] (Read Status)
SR refers to the status register contained within a particular LUN. SR[x] refers to bit x in the status register for the associated LUN. Refer to Chapter 5.2.14 for the definition of bit meanings within the status register.

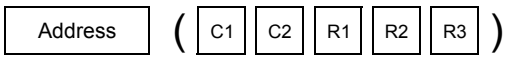
1.6 Diagram Legend

Diagrams in the Toggle DDR2.0 datasheet use the following legend:

This legend shows the command data. Refer to the Table 27 for more information about the command data.

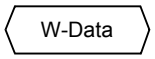


This legend shows the Address data. The address are comprised of 2 cycles column address and 3 cycles row address

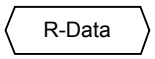


C1 : Column address 1
C2 : Column address 2
R1 : Row address 1
R2 : Row address 2
R3 : Row address 3

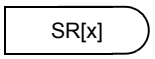
This legend shows Host writing data(data input) to the device.



This legend shows Host reading data(data output) from the device.



This legend shows Host reading the status register within a particular LUN.



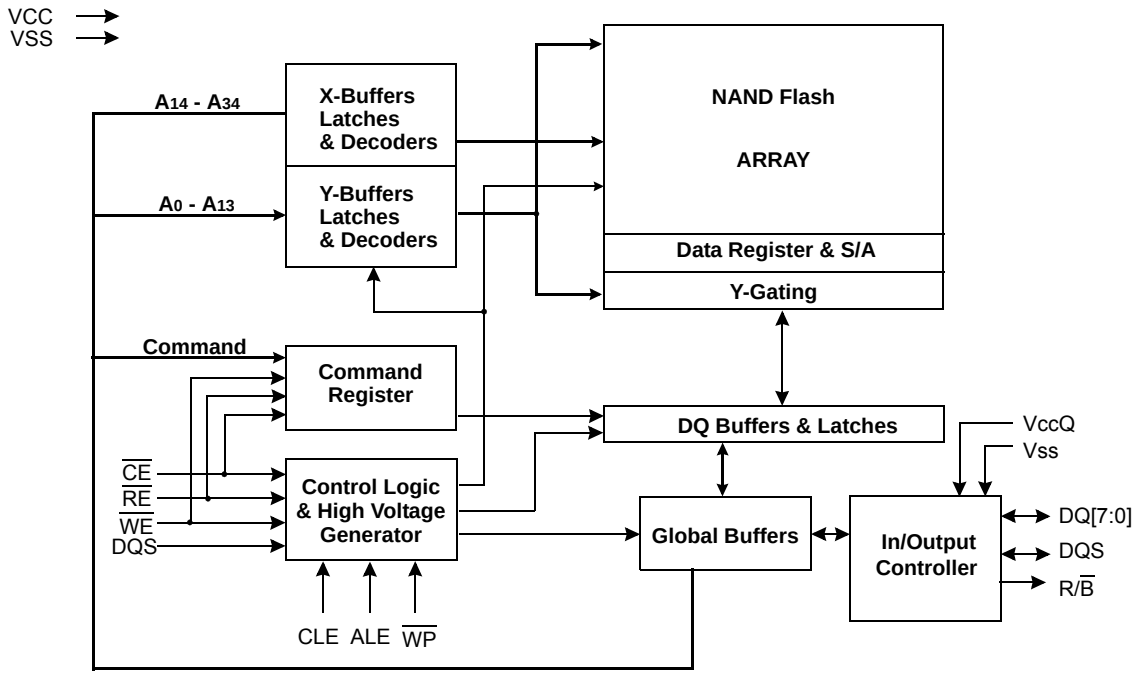
2.0 PHYSICAL INTERFACE

2.1 Pin Description

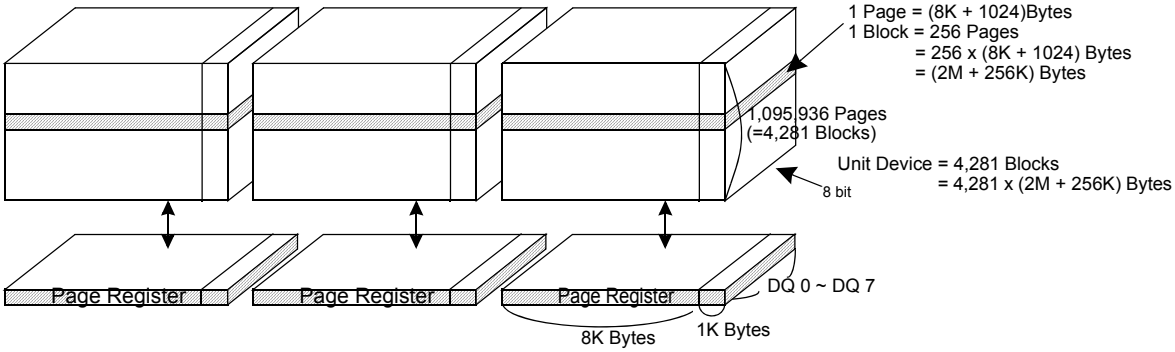
Pin Name	Pin Function
DQ[7:0]	**DATA INPUTS/OUTPUTS** The DQ pins are used to input command, address and data, and to output data during read operations. The DQ pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the DQ ports on the rising edge of the $\overline{WE}$ signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.
$\overline{CE}$	**CHIP ENABLE** The $\overline{CE}$ input is the device selection control. When the device is in the Busy state, $\overline{CE}$ high is ignored, and the device does not return to standby mode in program or erase operation.
$\overline{RE}$, (RE) or RE_t, (RE_c)	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active, drives the data onto the DQ bus. Data is valid after t_{DQSRE} of rising edge & falling edge of $\overline{RE}$, which also increments the internal column address counter by each one. The Read Enable $\overline{RE}$ is paired with differential signal RE to provide differential pair signaling to the system during reads.
$\overline{WE}$	**WRITE ENABLE** The $\overline{WE}$ input controls writes to the DQ port. Commands, addresses are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.
R/$\overline{B}$	**READY/BUSY OUTPUT** The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled. R/$\overline{B}$ shall be tied to VccQ
DQS, ($\overline{DQS}$) or DQS_t, (DQS_c)	**DATA STROBE** Data output is aligned with DQS falling/rising edge, and data inputs at DQS falling/rising. The data strobe DQS is paired with differential signal $\overline{DQS}$ to provide differential pair signaling to the system during reads and writes.
Vcc	**POWER** V_{CC} is the power supply for device.
VccQ	**DQ POWER** The VccQ is the power supply for input and/or output signals.
Vss	**GROUND**
V_{REF}	**REFERENCE VOLTAGE**
V_{PP}	**EXTERNAL HIGH VOLTAGE**
N/C	**NO CONNECTION** Lead is not internally connected.
RFU	**RESERVED FOR USE** Nothing should be connected with it.

NOTE :
Connect all VCC and VSS pins of each device to common power supply outputs.
Do not leave VCC or VSS disconnected.

Functional Block Diagram



Array Organization of Unit Device



	DQ 0	DQ 1	DQ 2	DQ 3	DQ 4	DQ 5	DQ 6	DQ 7	
1st Cycle	A_0[1)]	A_1	A_2	A_3	A_4	A_5	A_6	A_7	**Column Address**
2nd Cycle	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	*L	*L	
3rd Cycle	A_{14}	A_{15}	A_{16}	A_{17}	A_{18}	A_{19}	A_{20}	A_{21}	**Row Address;**
4th Cycle	A_{22}	A_{23}	A_{24}	A_{25}	A_{26}	A_{27}	A_{28}	A_{29}	**Page Address : A_{14} - A_{21}**
5th Cycle	A_{30}	A_{31}	A_{32}	A_{33}	A_{34}	**A_{35}	*L	*L	**Plane Address : A_{22} - A_{23}**[3)] **Block Address : A_{24} - A_{34}**

NOTE :

1) A0 must be set to "Low"
2) Data input/output unit should be 2-byte(16bit).
Column Address : Starting Address of the Register.
* When unused address bits shall be set to "Low".
* The device ignores any additional input of address cycles than required.
** A_{35} is used for DDP with a single CE
3) "11" is invalid address.

2.2 Valid Block

[Table 1] The number of valid block per a $\overline{CE}$

Part No.	Symbol	Min	Typ.	Max	Unit
K9ACGD8S0C	N_{VB}.	4,174	-	4,281	Blocks

NOTE :
1) The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of initial invalid blocks.
2) The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.

2.3 Absolute Maximum DC Rating

Stresses greater than those listing in Table 2 may cause permanent damage to the device. This is a stress rating only. Operation beyond the operating conditions specified in Table 2 is not recommended. Extended exposure beyond these conditions may affect device reliability.

[Table 2] Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{CC}	-0.6 to +4.6	V
	VccQ	-0.6 to +4.6	
	V_{IN}	-0.6 to VccQ + 0.3(<4.6)	
	$V_{I/O}$		
Storage Temperature	T_{STG}	-65 to +100	°C

NOTE :
Maximum DC voltage on input and I/O pins is VCCQ+0.3V which, during transition, may have overshoot that is defined in Table 6.

2.4 Operating Temperature Condition

[Table 3] Operating Temperature Condition

Symbol	Parameter	Rating	Unit
T_{OPER}	Operating Temperature Range for Commercial	0 to +70	°C

NOTE :
1) Operating Temperature(T_{OPER}) is the case surface temperature on the center/top side of the NAND.
2) The Normal Temperature Range specifies the temperatures where all NAND specifications will be supported. During operation, the NAND case temperature must be maintained between 0-70°C for commercial under all operating conditions.

2.5 Recommended Operating Conditions

[Table 4] Recommended Operating Condition

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	Vcc	2.7	3.3	3.6	V
Ground Voltage	Vss	0	0	0	V
Supply Voltage for 3.3V I/O signaling	VccQ	2.7	3.3	3.6	V
External high Voltage	V_{PP}	11.5	12	12.5	V

NOTE :
1) Vcc and VccQ may be distinct and unique voltages. The device shall support one of the following Vcc/VccQ combinations,
Vcc = 3.3V, VccQ = 3.3V
All parameters, timing modes and other characteristics are related to the supported voltage combination.
2) The maximum external Vpp supply current per LUN is 5mA

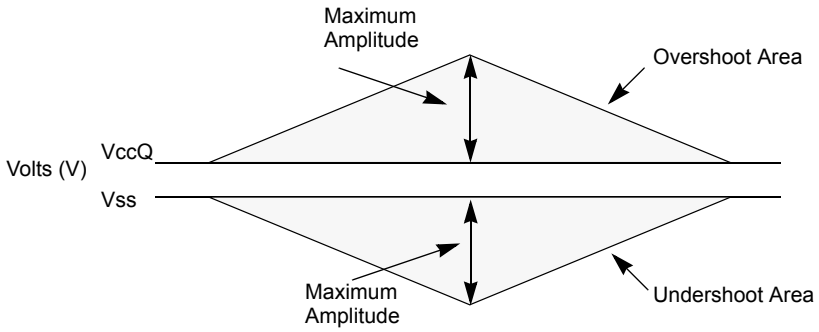
2.6 AC Overshoot/Undershoot Requirements

TThe device may have AC overshoot or undershoot from VccQ and Vss levels. Table 5 defines the maximum values that the AC overshoot or undershoot may attain. These values apply for both 3.3V Vss levels.

[Table 5] AC Overshoot/Undershoot Specification

Parameter	Maximum Value				Unit
	~50Mhz	51~66Mhz	67~83Mhz	84~100Mhz	
Max. peak amplitude allowed for overshoot area	1	1	1	1	V
Max. peak amplitude allowed for undershoot area	1	1	1	1	V
Max. overshoot area above VccQ	3	2.25	1.8	1.5	V*ns
Max. undershoot area above Vss	3	2.25	1.8	1.5	V*ns

NOTE :
1) This specification is intended for devices with no clamp protection and is guaranteed by design.



[Figure 1] Overshoot/Mndershoot Diagram

2.7 DC Operating Characteristics

[Table 6] DC & Operating Characteristics for VccQ=3.3V

Parameter	Symbol	Test Conditions	2-Plane			3-Plane			Unit
			Min	Typ	Max	Min	Typ	Max	
Page Read Operation Current	I_{CC1}	-	-	-	45	-	-	50	mA
Page Program Operation Current	I_{CC2}	-	-	-	45	-	-		
Erase Operation Current	I_{CC3}	-	-	-	45	-	-		
DQ Burst Read Current	I_{CC4R}	C_{LOAD}=0pF (I_{OUT}=0mA) $\overline{CE}$=V_{IL}, Half data switching tRC=10ns(100Mhz)	-	-	-	-	-	80	
	I_{CCQ4R}		-	-	-	-	-	50	
DQ Burst Write Current	I_{CC4W}	$\overline{CE}$=V_{IL}, Half data switching tDSC=10ns(100Mhz)	-	-	-	-	-	80	
	I_{CCQ4W}		-	-	-	-	-	10	
Bus Idle Current	I_{CC5}	-	-	-	-	-	-	10	
Stand-by Current(CMOS)	I_{SB}(3)	$\overline{CE}$=VccQ-0.2, $\overline{WP}$=0V/VccQ	-	-	-	-	15	50	µA
Input Leakage Current	I_{LI}(4)	V_{IN}=0 to VccQ(max)	-	-	±10	-	-	±10	
Output Leakage Current	I_{LO}(4)	V_{OUT}=0 to VccQ(max)	-	-	±10	-	-	±10	
Output High Voltage Level	V_{OH}	I_{OH}=-400µA	2.4	-	-	2.4	-	-	V
Output Low Voltage Level	V_{OL}	I_{OL}= 2.1mA	-	-	0.4	-	-	0.4	
Output Low Current(R/$\overline{B}$)	I_{OL}(R/$\overline{B}$)	V_{OL}=0.4V	8	10	-	8	10	-	mA

NOTE :
1) Typical value is measured at Vcc=3.3V, T_A=25°C. Not 100% tested.
2) VOH and VOL should be available on these two conditions; Output Strength is nominal and VccQ=3.3V, Rpd/Rpu are all VccQx0.5. If the driver strength settings are supported, Table 10 shall be used to derive the output driver impedence values.

2.8 AC & DC Input Measurement Levels

[Table 7] Single Ended without V_{REF} AC & DC input level

Parameter	Symbol	Min	Max	Unit
DC input logic high	$V_{IH(DC)}$	0.7 x V_{CCQ}	V_{CCQ} + 0.3	V
DC input logic low	$V_{IL(DC)}$	- 0.3	0.3 x V_{CCQ}	
AC input logic high	$V_{IH(AC)}$	0.8 x V_{CCQ}	-	
AC input logic low	$V_{IL(AC)}$	-	0.2 x V_{CCQ}	

NOTE :
1) VIL can undershoot to -0.3V and VIH can overshoot to VCCQ +0.3V for durations of 20 ns or less.
2) Vref shall be used at high interface speed above 200Mbps

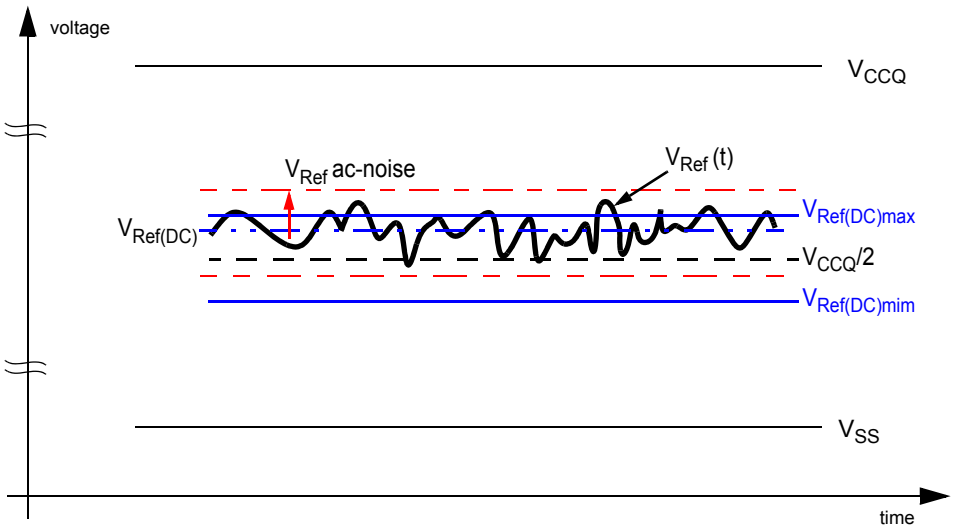
[Table 8] Single Ended with V_{REF} AC & DC input level

Parameter	Symbol	Min	Max	Unit
DC input logic high	$V_{IH(DC)}$	V_{REF} + 0.15	V_{CCQ} + 0.3	V
DC input logic low	$V_{IL(DC)}$	- 0.3	V_{REF} - 0.15	
AC input logic high	$V_{IH(AC)}$	V_{REF} + 0.3	-	
AC input logic low	$V_{IL(AC)}$	-	V_{REF} - 0.3	
Reference Voltage	$V_{REF(DC)}$	0.49 xVccQ	0.51 xVccQ	

NOTE :
V_{REF} is used only for 1.8VccQ

2.9 V_{REF} Tolerances

The DC-tolerance and AC-noise limits for the reference voltages. Figure 2 shows a valid reference voltage $V_{REF}(t)$ as a function of time.
$V_{REF}(DC)$ is the linear average of $V_{REF}(t)$ over a very long period of time (e.g. 1sec). This average has to meet the min/max requirements in Table 8.
$V_{REF}(t)$ may temporarily deviate from $V_{REF}(DC)$ by no more than +/- 1% V_{CCQ}
The voltage levels for setup and hold time measurements $V_{IH}(AC)$, $V_{IH}(DC)$, $V_{IL}(AC)$ and $V_{IL}(DC)$ are dependent on V_{REF}.
"V_{REF}" shall be understood as $V_{REF}(DC)$, as defined in Figure 2.



[Figure 2] $V_{REF}(DC)$ tolerance and V_{REF} AC-noise limits

2.10 Input/Output Capacitance(T_A=25°C, VCC=3.3V, f=100MHz)

[Table 9] Input/ Output capacitance

Item	Symbol	Test Condition	K9ACGD8S0C		Unit
			Min	Max	
Input/Output Capacitance	C_{DQ}	V_{IL}=0V	-	TBD	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	TBD	pF

NOTE :
1) Capacitance is periodically sampled and not 100% tested.

2.11 DQ Driver Strength

The device may be configured with multiple driver strengths with 'SET FEATURE' command. There are Underdrive, Nominal options. The Toggle DDR supports all four driver strength settings. Devices that support driver strength settings shall comply with the output driver requirements in this section. A device is only required to meet driver strength values for either 3.3V VccQ or 1.8V VccQ, and is not required to meet driver strength values for both 3.3V VccQ and 1.8V VccQ.

[Table 10] DQ Driver Strength Settings

Setting	Driver Strength	VccQ
Nominal	1.0x = 35 Ohms	3.3 V
Underdrive1	0.7x = 50 Ohms	
Nominal	1.0x = 35 Ohms	1.8 V
Underdrive1	0.7x = 50 Ohms	

The impedance values corresponding to several different VccQ values are defined in Table 12 for 3.3V and 1.8V VccQ. The test conditions that shall be used to verify the impedance values are specified in Table 11. The terms T_{OPER}(Min) and T_{OPER}(Max) are in reference to the minimum and maximum operating temperature defined for the device.

[Table 11] Testing Conditions for Impedance Values

Condition	Temperature	VccQ (3.3V)	VccQ (1.8V)	Process
Minimum Impedance	T_{OPER} (Min) degrees Celsius	3.6 V	1.95 V	Fast - fast
Nominal Impedance	25 degrees Celsius	3.3 V	1.8 V	Typical
Maximum Impedance	T_{OPER} (Max) degrees Celsius	2.7 V	1.7 V	Slow-slow

[Table 12] Output Driver Strength Impedance Values

Output Strength	Rpd/Rpu	VOUT to Vss	Minimum		Nominal		Maximum		Units
			VccQ(3.3V)	VccQ(1.8V)	VccQ(3.3V)	VccQ(1.8V)	VccQ(3.3V)	VccQ(1.8V)	
Nominal	Rpd	VccQ × 0.2	6.0	4.0	33.0	32.0	48.0	47.0	ohms
		VccQ × 0.5	16.0	17.0	35.0	35.0	51.0	53.0	ohms
		VccQ × 0.8	31.0	29.0	40.0	45.0	61.0	74.0	ohms
	Rpu	VccQ × 0.2	31.0	29.0	40.0	45.0	61.0	74.0	ohms
		VccQ × 0.5	16.0	17.0	35.0	35.0	51.0	53.0	ohms
		VccQ × 0.8	6.0	4.0	33.0	32.0	48.0	47.0	ohms
Underdrive 1	Rpd	VccQ × 0.2	16.0	12.0	47.0	45.0	64.0	64.0	ohms
		VccQ × 0.5	29.0	31.0	50.0	50.0	70.0	74.0	ohms
		VccQ × 0.8	43.0	41.0	56.0	63.0	83.0	102.0	ohms
	Rpu	VccQ × 0.2	43.0	41.0	56.0	63.0	83.0	102.0	ohms
		VccQ × 0.5	29.0	31.0	50.0	50.0	70.0	74.0	ohms
		VccQ × 0.8	16.0	12.0	47.0	45.0	64.0	64.0	ohms

[Table 13] Pull-up and Pull-down Output Impedance Mismatch

Driver Strength	1.8V		3.3V		Unit
	Minimum	Maximum	Minimum	Maximum	
Nominal	0	8	0	9	ohms
Underdrive 1	0	11	0	12	ohms

NOTE :
1) Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.
2) Test conditions: VccQ = VccQ(min), Vout = VccQ × 0.5, $T_A = T_{OPER}$

2.12 Input/Output Slew rate

The input slew rate requirements that the device shall comply with are defined in Table 14 and Table 15. The output slew rate requirements that the device shall comply with are defined in Table 17. The testing conditions that shall be used to verify the input slew rate are listed in Table 16 and Table 18.

[Table 14] Derating factor

Input slew rate	200Mbps	Unit
2.0V/ns	-	ps
1.5V/ns	-	
1.0V/ns	0	
0.8V/ns	150	
0.6V/ns	350	

NOTE :
1) Derating factor is required when DQ slew rate is lower than minimum slew rate while the slew rate of DQS meets the minimum slew rate.

[Table 15] Input Slew rate

Vccq	V_{IL}	V_{IH}	Min
			200Mbps
3.3V	0.2 x Vccq	0.8 x Vccq	1.0V/ns
Small swing	V_{REF} -300mV	V_{REF} +300mV	1.0V/ns

[Table 16] Testing Conditions for Input Slew Rate

Parameter	Value
Positive Input Transition	VIL (DC) to VIH (AC)
Negative Input Transition	VIH (DC) to VIL (AC)

[Table 17] Output Slew Rate Requirements

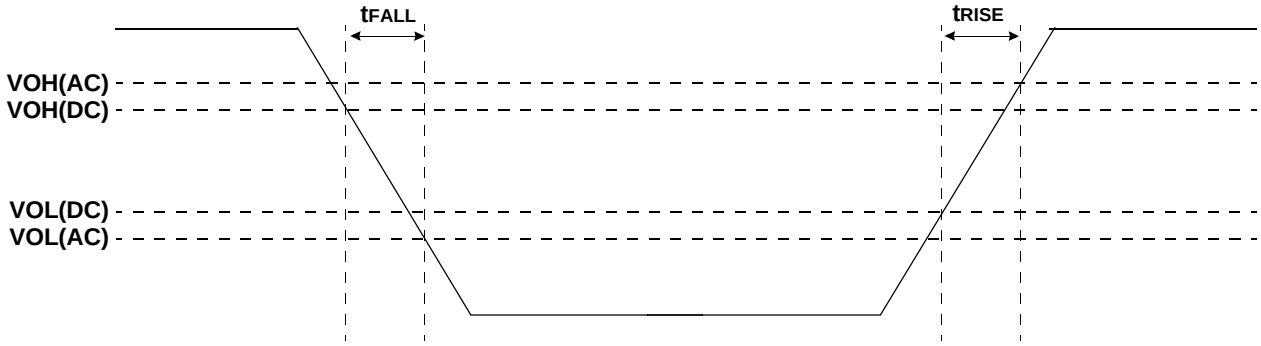
Parameter	VccQ=3.3V		Unit
	Minimum	Maximum	
Nominal	1.2	7.0	ohms
Underdrive 1	1.0	5.5	ohms

NOTE :
1) Measured with a test load of 5pF connected to Vss.
2) The ratio of pull-up slew rate to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maxiumum difference between pull-up and pull-down drivers due to process variation.

[Table 18] Testing Conditions for Output Slew Rate

Parameter	Value
VOL (DC)	0.3 * VccQ
VOH (DC)	0.7 * VccQ
VOL (AC)	0.2 * VccQ
VOH (AC)	0.8 * VccQ
Positive Output Transition	VOL (DC) to VOH (AC)
Negative Output Transition	VOH (DC) to VOL (AC)
tRISE[1)]	Time during Rising Edge from VOL (DC) to VOH (AC)
tFALL[1)]	Time during Falling Edge from VOH (DC) to VOL (AC)
Output Slew Rate Rising Edge	(VOH (AC) - VOL (DC)) / tRISE
Output Slew Rate Falling Edge	(VOH (DC) - VOL (AC)) / tFALL
Output Capacitive load	C_L = 5pF

NOTE :
1) Refer to Figure 3.
2) Output slew rate is verified by design and characterization. It may not be subject to production test.
3) The minimum slew rate is the minimum of the rising edge and the falling edge slew rate. The maximum slew rate is the maximum of the rising edge and the falling edge slew rate.



[Figure 3] tRISE and tFALL Definition for Output Slew Rate

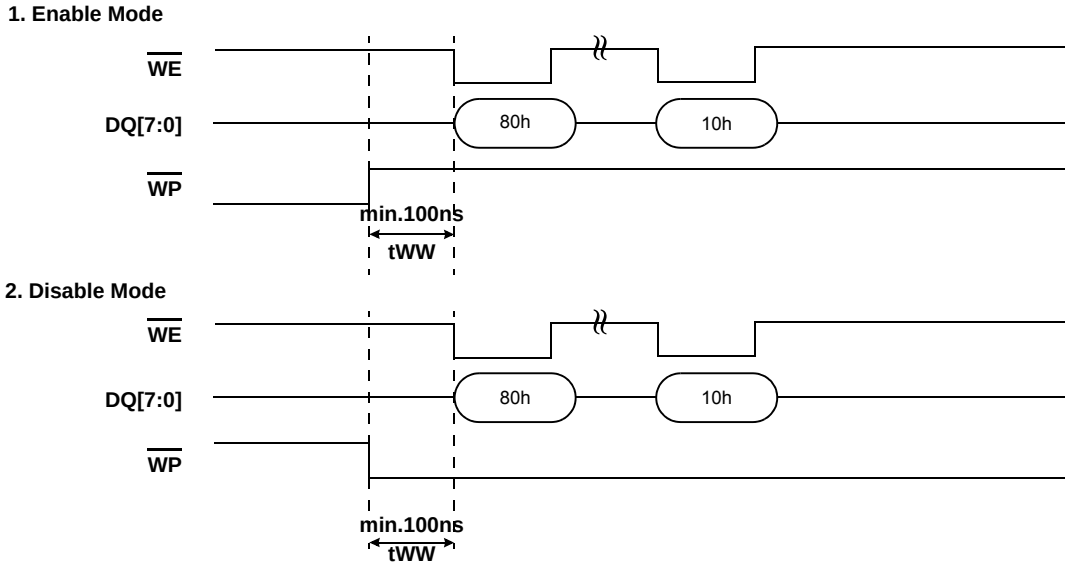
2.13 R/$\overline{B}$ and SR[6] Relationship

R/$\overline{B}$ represents the status of the selected target. R/$\overline{B}$ goes busy when only a single LUN is busy while rest of LUNs on the same target are idle.

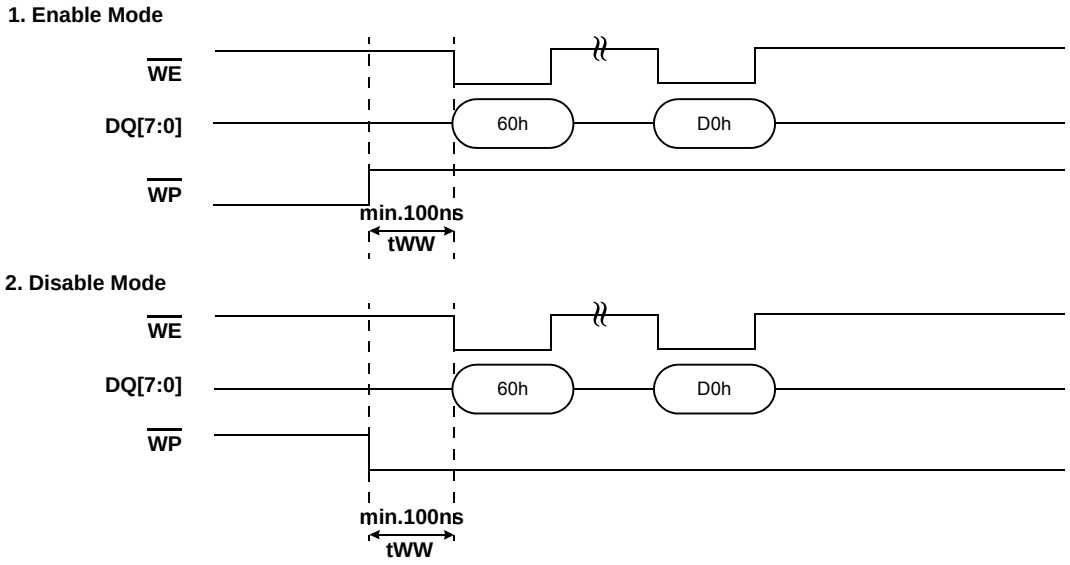
2.14 Write Protect

When $\overline{WP}$ is enabled, Flash array is blocked from any program and erase operations. This signal shall only be transitioned when a target is idle. The host shall be allowed to issue a new command after tWW once $\overline{WP}$ is enabled.

Figure 4 describes the tWW timing requirement, shown with the start of a Program command. And Figure 5 shows with the start of a Erase command.



[Figure 4] Write Protect Sequence requirements of the Program operation



[Figure 5] Write Protect Sequence requirements of the Erase operation

3.0 MEMORY ORGANIZATION

A device contains one or more targets. A target is controlled by one $\overline{CE}$ signal. A target is organized into one or more logical units (LUNs).

A logical unit (LUN) is the minimum unit that can independently execute commands and report status. Specifically, separate LUNs may operate on arbitrary command sequences in parallel. For example, it is permissible to start a Page Program operation on LUN 0 and then prior to the operation's completion to start a Read command on LUN 1. A LUN contains at least one page register and a Flash array. The number of page registers is dependent on the number of plane operations supported for the LUN. The Flash array contains a number of blocks.

A block is the smallest erasable unit of data within the Flash array of a LUN. There is no restriction on the number of blocks within the LUN. A block contains a number of pages.

A page is the smallest addressable unit for read and program operations.

Each LUN shall have at least one page register. A page register is used for the temporary storage of data before it is moved to a page within the Flash array or after it is moved from a page within the Flash array.

The byte location within the page register is referred to as the column.

There are two mechanisms to achieve parallelism within this architecture. There may be multiple commands outstanding to different LUNs at the same time. To get further parallelism within a LUN, plane addressing may be used to execute additional dependent operations in parallel.

3.1 Addressing

There are two address types used: the column address and the row address. The column address is used to access bytes within a page, i.e. the column address is the byte offset into the page. The least significant bit of the column address shall always be zero for a DDR interface, i.e. an even number of bytes is always transferred. The row address is used to address pages, blocks, and LUNs.

When both the column and row addresses are required to be issued, the column address is always issued first in one or more 8-bit address cycles. The row addresses follow in one or more 8-bit address cycles. There are some functions that may require only row addresses, such as Block Erase. In this case the column addresses shall not be issued.

For both column and row addresses the first address cycle always contains the least significant address bits and the last address cycle always contains the most significant address bits. If there are bits in the most significant cycles of the column and row addresses that are not used then they are required to be cleared to zero.

The row address structure is shown in Figure 6 with the least significant row address bit to the right and the most significant row address bit to the left.

[Figure 6] Row Address Layout

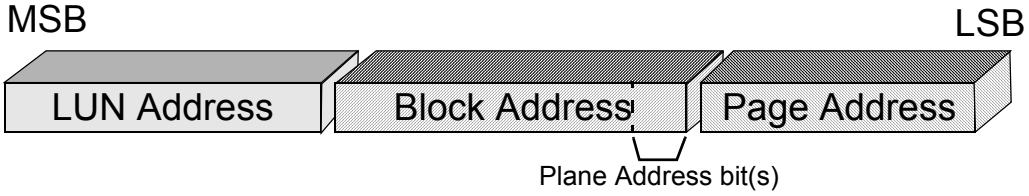
The page address is set by the least significant row address bits, and the LUN address is set by the most significant row address bit(s). The block address is between a page address and a LUN address.

A host shall not access an address of a page or block beyond maximum page address or block address.

3.1.1 Plane Addressing

The plane address comprises the lowest order bits of the block address as shown in Figure 7. The plane address is used when performing a multi-plane command sequence on a particular LUN:Multi-plane

The plane address bit(s) shall be different within address setting sequences for the Multi-plane-related operation, while the page address shall stay the same within address setting sequences for the Multi-plane-related operation.



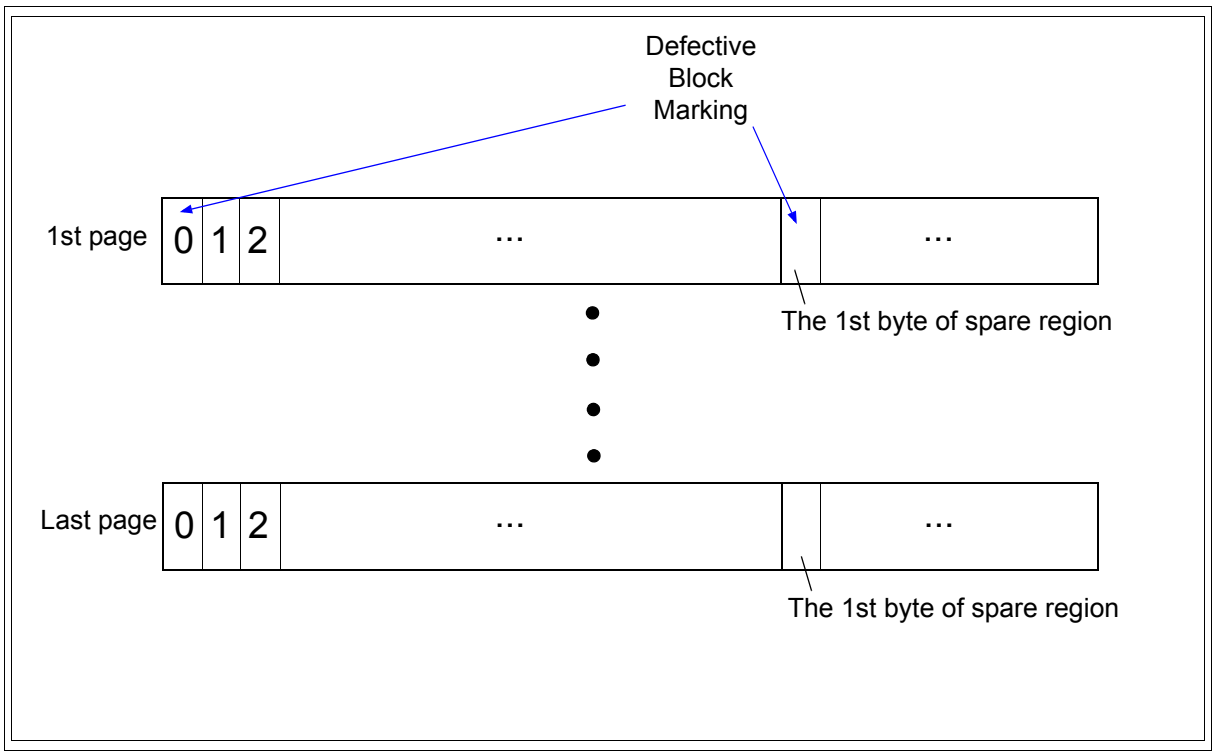
[Figure 7] Position of Plane Address

3.2 Factory Defect Mapping

The Flash array is not presumed to be pristine, and a number of defects that makes the blocks unusable may be present. Invalid blocks shall be sorted out from normal blocks by software.

3.2.1 Device Requirements

If a block is defective, the manufacturer shall mark the block as defective at SLC mode by setting the Defective Block Marking, as shown in Figure 8, of the 1st of the defective block to a value of non-FFh. The Defective Block Marking is located on the first byte of user data area or the first byte of spare data area in the pages within a block.



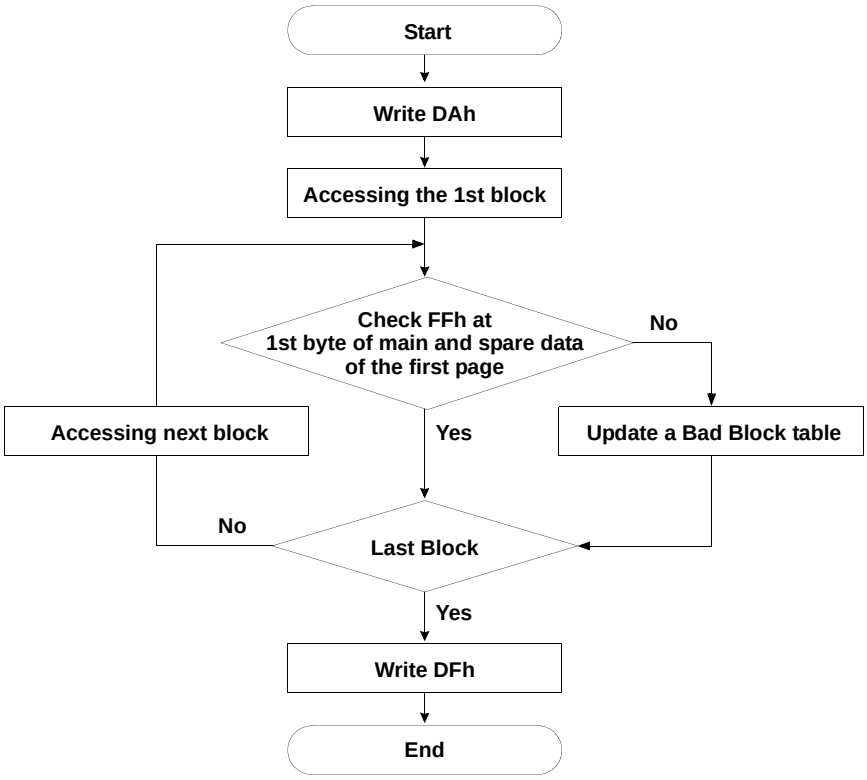
[Figure 8] Area marked in first of block indicating defect

3.2.2 Host Requirements

The host shall not erase or program blocks marked as defective by the manufacturer, and any attempt to do so yields indeterminate results.

Figure 9 outlines the flow chart how to create an initial invalid block table. It should be performed at SLC mode by the host to create the initial bad block table prior to performing any erase or programming operations on the target. The 1st byte of main or spare region in non-defective blocks are read FFh. A defective block is indicated by the majority of bits being read non-FFh in the Defective Block Marking location of the first page of the block. The host shall check the Defective Block Marking location of the first page of each block to verify the block is valid prior to any erase or program operations on that block.

NOTE :
Over the lifetime use of a NAND device, the Defective Block Marking of defective blocks may encounter read disturbs that cause bit changes. The initial defect marks by the manufacturer may change value over the lifetime of the device, and are expected to be read by the host and used to create a bad block table during initial use of the part.



[Figure 9] Flow chart to create initial invalid block table

3.3 Error In Write or Read Operation

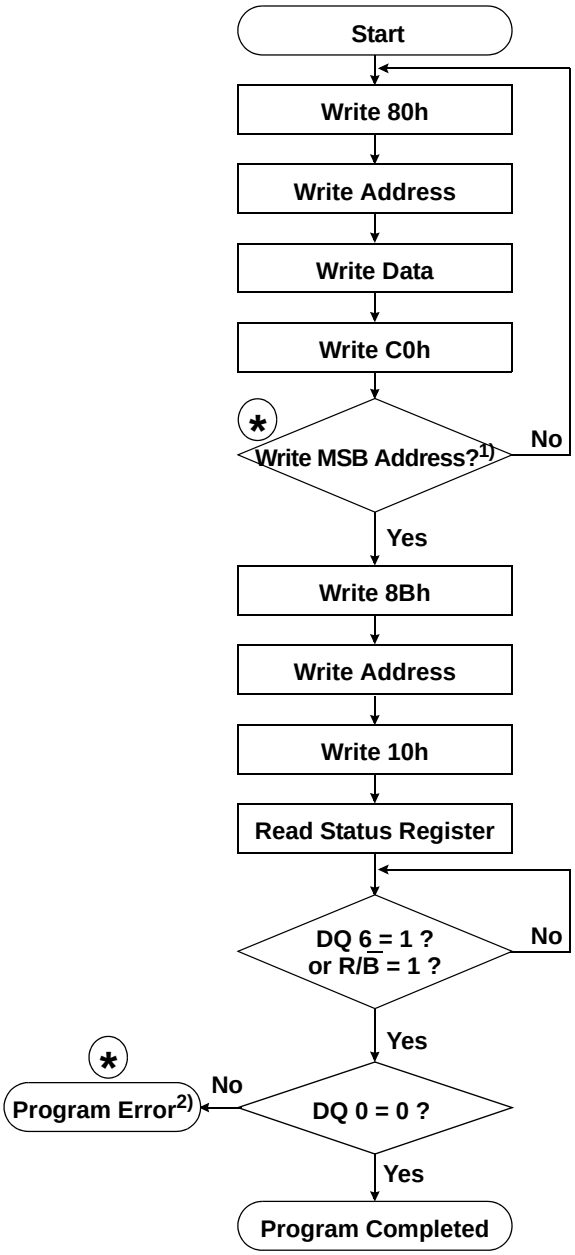
Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. Block replacement should be done upon erase or program error.

[Table 19] Failure cases

Failure Mode		Detection and Countermeasure sequence
Write	Program Failure	Read Status after Program --> Block Replacement
Erase	Erase Failure	Status Read after Erase --> Block Replacement
Read	LDPC	Verify ECC -> ECC Correction

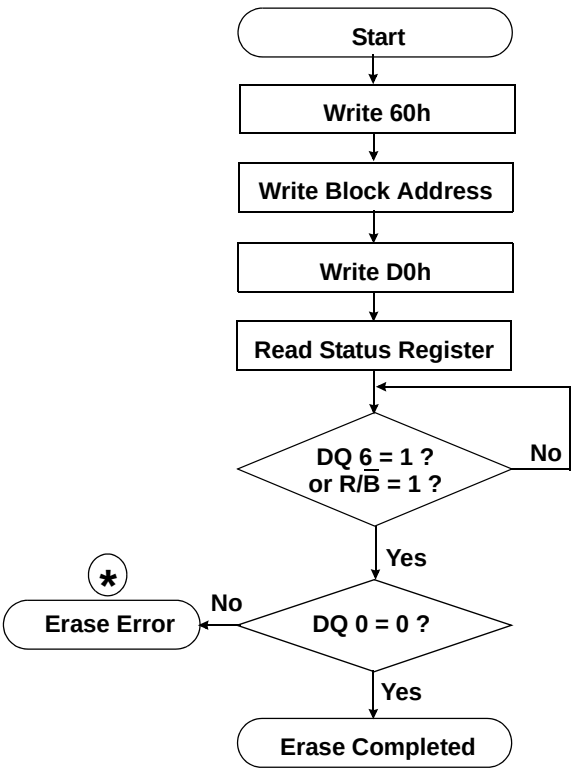
ECC : Error correcting code such as LDPC code.

Program Flow Chart

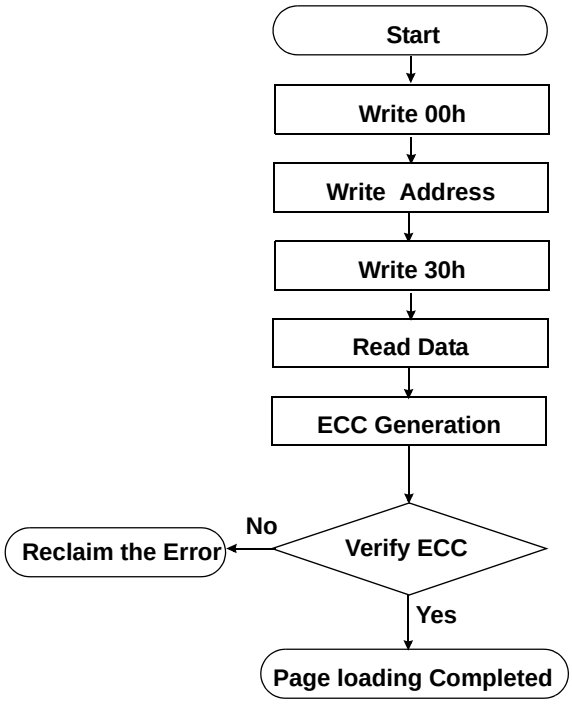


(*) 1) Buffer address after C0h command must be issued from LSB to MSB.
2) If program operation results in an error, map out the block including the page in error and copy the target data to another block.

Erase Flow Chart

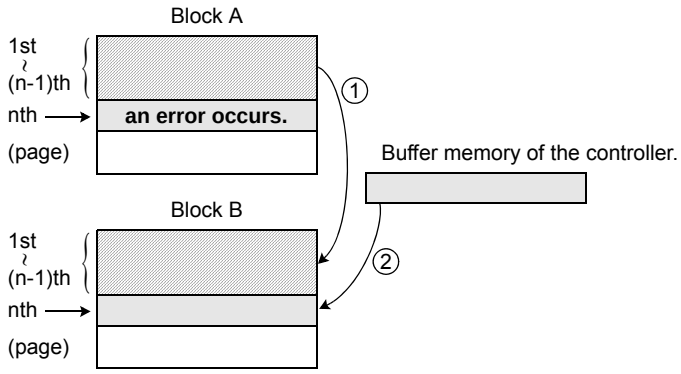


Read Flow Chart



(*) : If erase operation results in an error, map out the failing block and replace it with another block.

Block Replacement



* Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
* Step4
Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

3.4 Addressing For Program Operation

3bit/cell NAND has the following programming characteristics. The fine programming to one WL consists of 3 steps of program operation. 3 pages' data, LSB, CSB and MSB, has to be stored for each program operation to make 8 program states at the same time.

Each programming step has its own program order address which is not same as physical page address. The following is the program order address to minimize the coupling. The Program operation shall be followed in below sequence.
1st Program operation at WL0 -> 1st Program operation at WL1 -> 2nd Program operation at WL0 -> 1st Program operation at WL2 -> 2nd Program operation at WL1 -> 3rd Program operation at WL0 etc. The programmed data of each page can be read out only if 3rd program is completed.

Paired Program/Read Address Information

[Table 20] Program/Read Address

Grouped Page Address		
Group A	Group B	Group C
00h		
01h		02h
03h		04h
05h	06h	07h
08h	09h	0Ah
0Bh	0Ch	0Dh
0Eh	0Fh	10h
11h	12h	13h
14h	15h	16h
17h	18h	19h
1Ah	1Bh	1Ch
1Dh	1Eh	1Fh
20h	21h	22h
23h	24h	25h
26h	27h	28h
29h	2Ah	2Bh
2Ch	2Dh	2Eh
2Fh	30h	31h
32h	33h	34h
35h	36h	37h
38h	39h	3Ah
3Bh	3Ch	3Dh
3Eh	3Fh	40h
41h	42h	43h
44h	45h	46h
47h	48h	49h
4Ah	4Bh	4Ch
4Dh	4Eh	4Fh
50h	51h	52h
53h	54h	55h
56h	57h	58h
59h	5Ah	5Bh
5Ch	5Dh	5Eh
5Fh	60h	61h
62h	63h	64h
65h	66h	67h
68h	69h	6Ah
6Bh	6Ch	6Dh
6Eh	6Fh	70h
71h	72h	73h
74h	75h	76h
77h	78h	79h
7Ah	7Bh	7Ch
7Dh	7Eh	7Fh

Grouped Page Address		
Group A	Group B	Group C
80h	81h	82h
83h	84h	85h
86h	87h	88h
89h	8Ah	8Bh
8Ch	8Dh	8Eh
8Fh	90h	91h
92h	93h	94h
95h	96h	97h
98h	99h	9Ah
9Bh	9Ch	9Dh
9Eh	9Fh	A0h
A1h	A2h	A3h
A4h	A5h	A6h
A7h	A8h	A9h
AAh	ABh	ACh
ADh	AEh	AFh
B0h	B1h	B2h
B3h	B4h	B5h
B6h	B7h	B8h
B9h	BAh	BBh
BCh	BDh	BEh
BFh	C0h	C1h
C2h	C3h	C4h
C5h	C6h	C7h
C8h	C9h	CAh
CBh	CCh	CDh
CEh	CFh	D0h
D1h	D2h	D3h
D4h	D5h	D6h
D7h	D8h	D9h
DAh	DBh	DCh
DDh	DEh	DFh
E0h	E1h	E2h
E3h	E4h	E5h
E6h	E7h	E8h
E9h	EAh	EBh
ECh	EDh	EEh
EFh	F0h	F1h
F2h	F3h	F4h
F5h	F6h	F7h
F8h	F9h	FAh
FBh		FCh
FDh		FEh
FFh		

Program Order Address Information

[Table 21] Order Address

Program Order Address		
1st Program	2nd Program	3rd Program
00h		
01h		03h
02h		07h
04h	06h	0Ah
05h	09h	0Dh
08h	0Ch	10h
0Bh	0Fh	13h
0Eh	12h	16h
11h	15h	19h
14h	18h	1Ch
17h	1Bh	1Fh
1Ah	1Eh	22h
1Dh	21h	25h
20h	24h	28h
23h	27h	2Bh
26h	2Ah	2Eh
29h	2Dh	31h
2Ch	30h	34h
2Fh	33h	37h
32h	36h	3Ah
35h	39h	3Dh
38h	3Ch	40h
3Bh	3Fh	43h
3Eh	42h	46h
41h	45h	49h
44h	48h	4Ch
47h	4Bh	4Fh
4Ah	4Eh	52h
4Dh	51h	55h
50h	54h	58h
53h	57h	5Bh
56h	5Ah	5Eh
59h	5Dh	61h
5Ch	60h	64h
5Fh	63h	67h
62h	66h	6Ah
65h	69h	6Dh
68h	6Ch	70h
6Bh	6Fh	73h
6Eh	72h	76h
71h	75h	79h
74h	78h	7Ch
77h	7Bh	7Fh
7Ah	7Eh	82h

Program Order Address		
1st Program	2nd Program	3rd Program
7Dh	81h	85h
80h	84h	88h
83h	87h	8Bh
86h	8Ah	8Eh
89h	8Dh	91h
8Ch	90h	94h
8Fh	93h	97h
92h	96h	9Ah
95h	99h	9Dh
98h	9Ch	A0h
9Bh	9Fh	A3h
9Eh	A2h	A6h
A1h	A5h	A9h
A4h	A8h	ACh
A7h	ABh	AFh
AAh	AEh	B2h
ADh	B1h	B5h
B0h	B4h	B8h
B3h	B7h	BBh
B6h	BAh	BEh
B9h	BDh	C1h
BCh	C0h	C4h
BFh	C3h	C7h
C2h	C6h	CAh
C5h	C9h	CDh
C8h	CCh	D0h
CBh	CFh	D3h
CEh	D2h	D6h
D1h	D5h	D9h
D4h	D8h	DCh
D7h	DBh	DFh
DAh	DEh	E2h
DDh	E1h	E5h
E0h	E4h	E8h
E3h	E7h	EBh
E6h	EAh	EEh
E9h	EDh	F1h
ECh	F0h	F4h
EFh	F3h	F7h
F2h	F6h	FAh
F5h	F9h	FDh
F8h		FCh
FBh		FFh
FEh		

4.0 FUNCTION DESCRIPTION

4.1 DATA PROTECTION AND POWER TRANSITION SEQUENCE

4.1.1 Data Protection

The device is designed to offer protection from any involuntary program/erase during power transitions. An internal voltage detector disables all internal program/erase circuits when Vcc is below about 2V. WP_n pin provides hardware protection and is recommended to be kept at VIL during power transitions. Although two step command sequence for program/erase provides protection from any operations by unintentional command input, keeping CLE and ALE at VIL prevents any spurious commands asserted during power transitions.

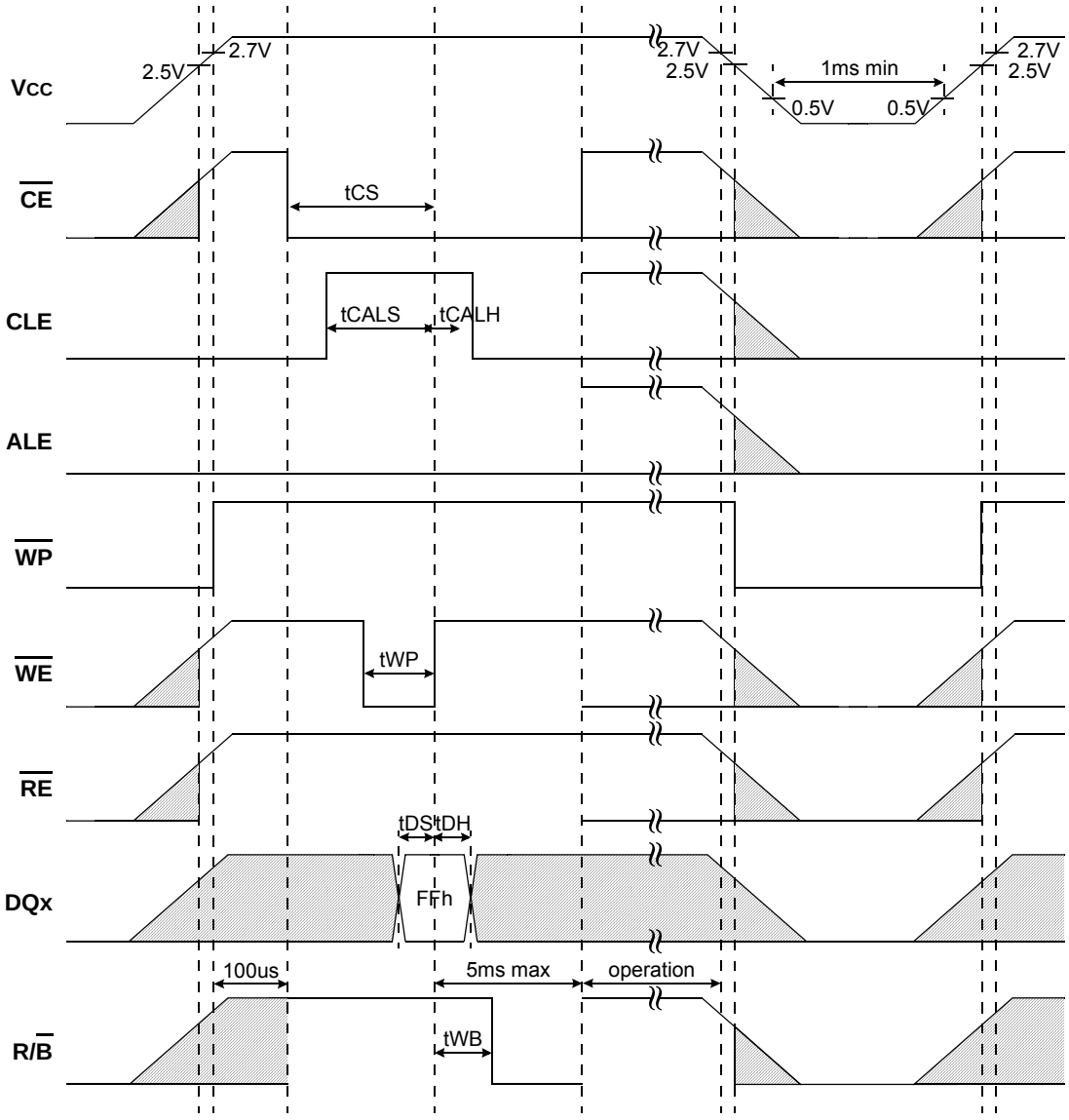
It is highly recommended to keep $\overline{CE}$ at VIH to prevent unnecessary current consumption during power transitions.

4.1.2 Power Up Sequence

For NAND devices that support VCCQ for I/O power supply, VCCQ must not exceed VCC during power up. The host must wait for R/B to be valid High before issuing Reset command (FFh) to initialize any targets that share same $\overline{CE}$. The R/B_n signal becomes valid after 100us since both VCC and VCCQ reach 2.7V (1.7V for 1.8V VCCQ). The RESET command (FFh) must be issued to all targets as the first command after the NAND device is powered up and R/B_n becomes valid. Each target (CE_n) will be busy for a maximum of 5ms after the RESET command (FFh) is issued. The RESET busy time can be monitored by polling R/B or issuing the READ STATUS(70h) command. Each NAND LUN(i.e. die) may draw less than 10mA over 1ms prior to the execution of the first RESET command (FFh) after the device is powered on. During the power up sequence including the RESET busy time, each LUN consumes a maximum current of 50mA.

4.1.3 Power Down Sequence

During power-down, VCCQ shall not exceed VCC.



[Figure 10] Initialization Timing

NOTE :
1) To minimize peak current during initialization, each LUN in a target can be selectively initialized by FAh(Reset LUN) command.
2) Vcc shall be same or 0.2V higher than VccQ. (VccQ-0.2V < Vcc)
3) Once Vcc drops under 2.5V, Vcc is recommended that it be driven down to 0.5V and stay low under 0.5V for at least 1ms before Vcc powered up.
4) Maximum DC voltage on input and I/O pins is VCCQ+0.3V which, during transition, may have overshoot that is defined in Table 6

4.2 Mode Selection

Table 22 describes the bus state for the Toggle DDR. Commands, addresses and data is all written through DQ's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Those are latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the DQ pins.
Host reads or writes data to the device using DQS signal. And data is latched on the falling and rising both edge of DQS on data input.

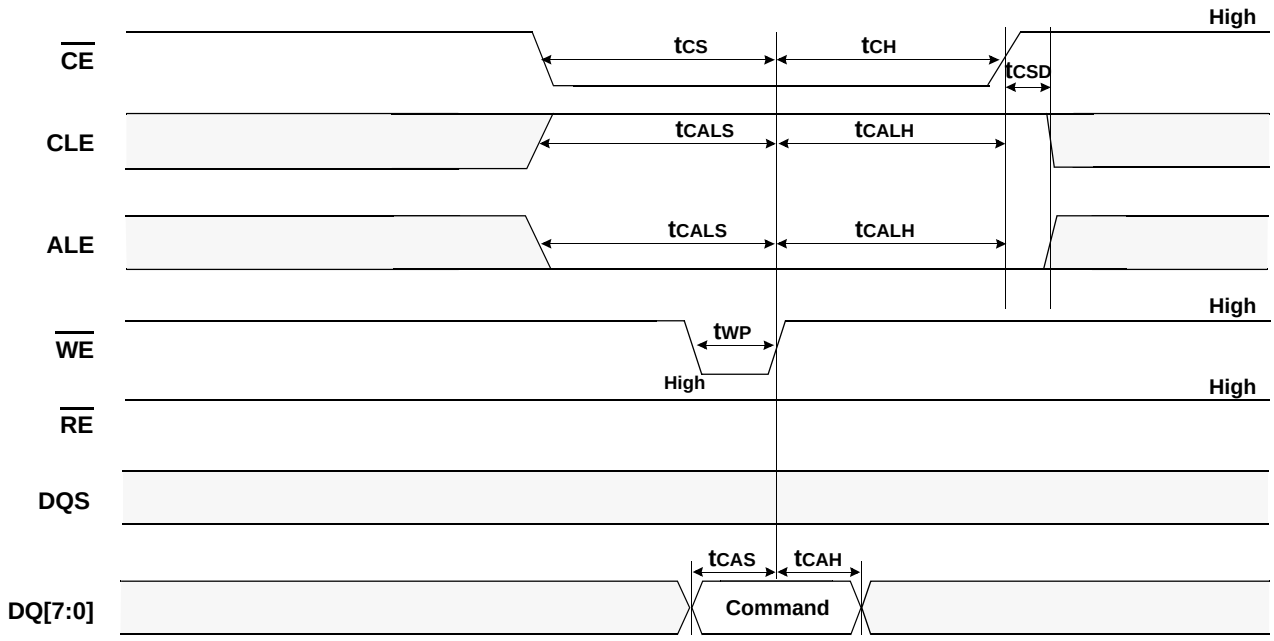
[Table 22] Mode Selection

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	DQS	$\overline{WP}$	Mode	
H	L	L		H	X(1)	X	Read Mode	Command Input
L	H	L		H	X	X		Address Input(5 cycles)
H	L	L		H	X	H	Write Mode	Command Input
L	H	L		H	X	H		Address Input(5 cycles)
L	L	L	H	H		H	Data Input	
L	L	L	H			X	Data Output	
X	X	X	X	H	X	X	During Read(Busy)	
X	X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	X	H	During Erase(Busy)	
X	X	X	X	X	X	L	Write Protect	
X	X	H	X	X	X	0V/Vcc(2)	Stand-by	

NOTE :
1) X can be VIL or VIH.
2) $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.
3) Data input by DQS transition in the middle of command input(e.g. 80h/81h/85h) and address input(e.g. 5 cycle of column address and row address) sequence is prohibited.

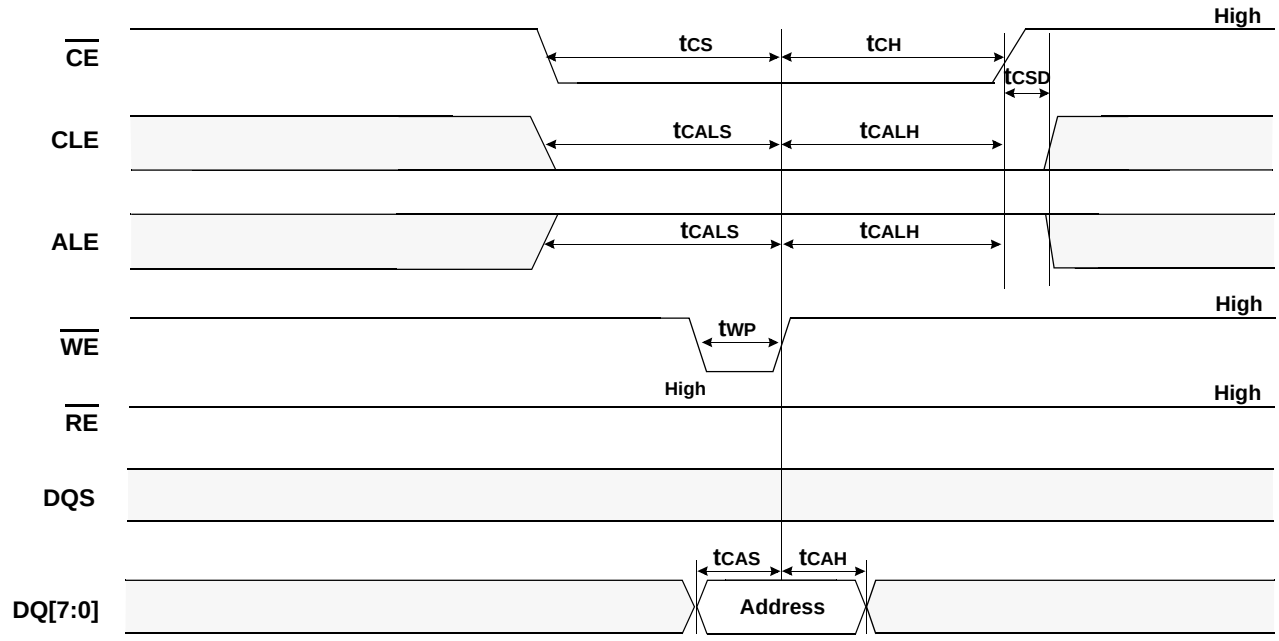
4.3 General Timing

4.3.1 Command Latch Cycle



NOTE :
1) Command information is latched by $\overline{WE}$ going 'High' when $\overline{CE}$ is 'Low', CLE is 'High', and ALE is 'Low'.

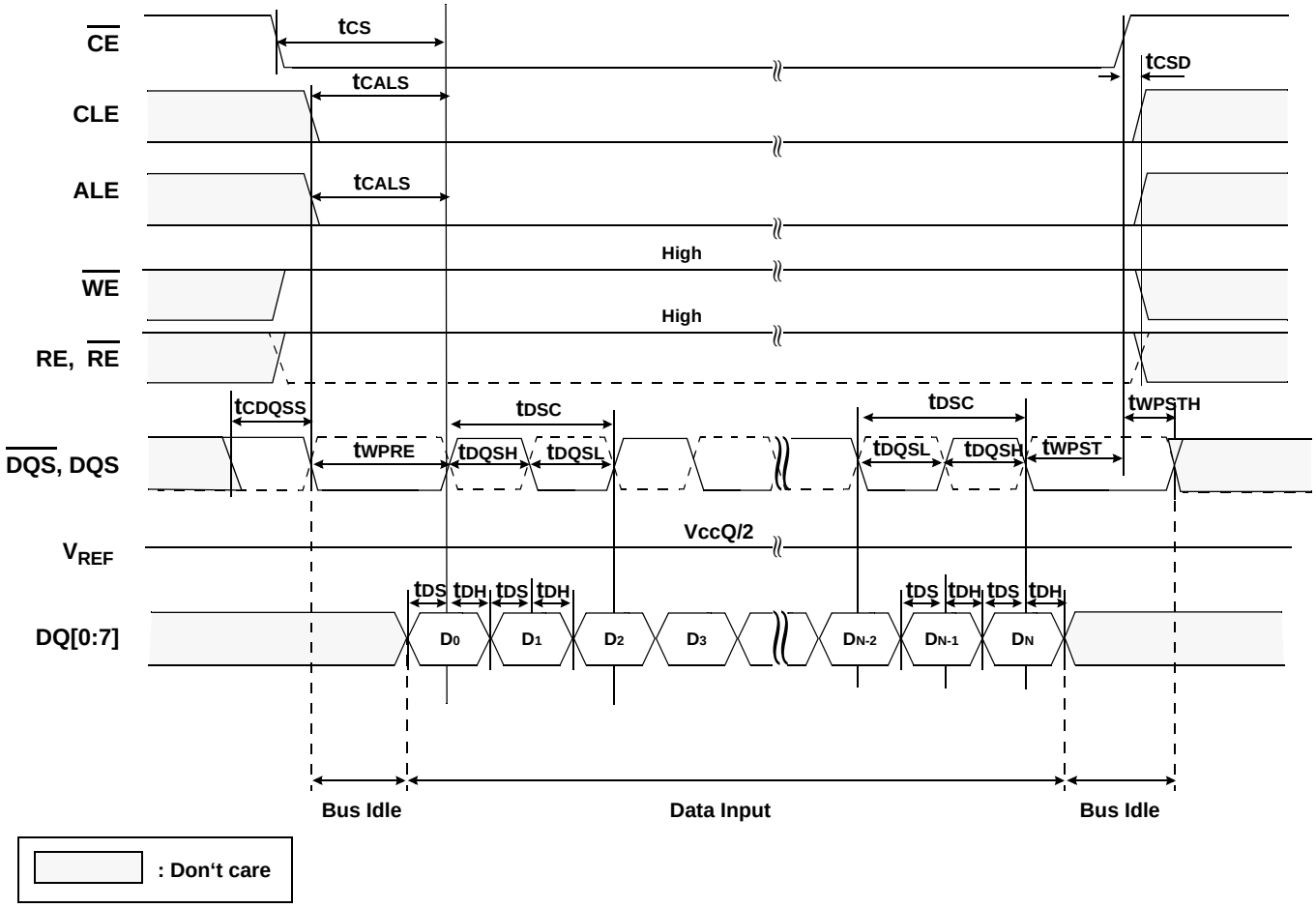
4.3.2 Address Latch Cycle



: Don't care

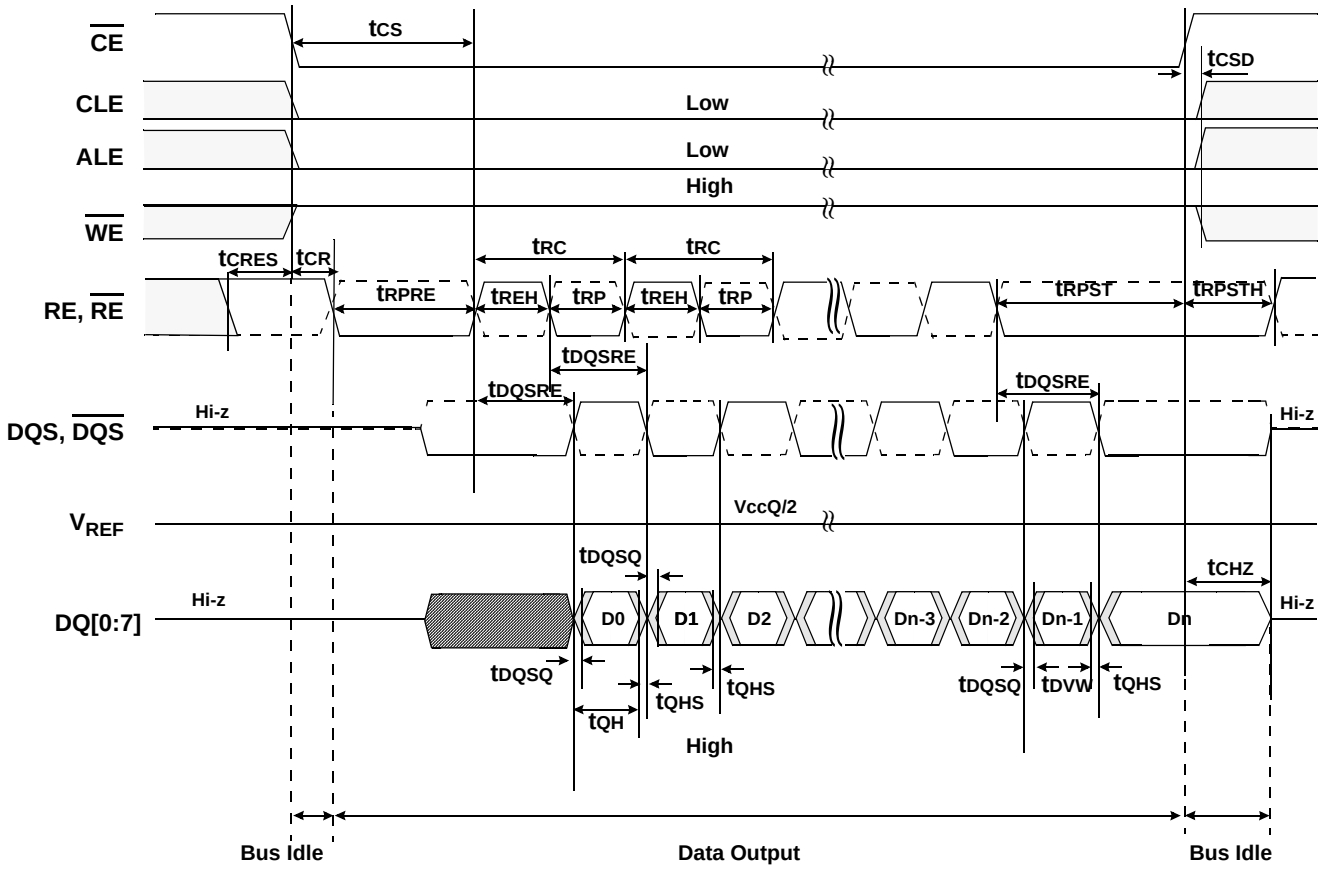
NOTE :
1) Address information is latched by $\overline{WE}$ going 'High' when $\overline{CE}$ is 'Low', CLE is 'Low', and ALE is 'High'.

4.3.3 Basic Data Input Timing



NOTE :
1) DQS, $\overline{DQS}$ and Data input buffers are turned-on when $\overline{CE}$ and DQS goes 'Low' and Data inputs begin with DQS, $\overline{DQS}$ toggling simultaneously.
2) ALE and CLE should not toggle during tWPRE period during tCALS.
3) DQS and Data input buffers are turned-off if either CLE or $\overline{CE}$ goes 'High'.
4) tCDQSS is defined from the last data input condition of the control signals such as $\overline{CE}$, CLE and ALE.
5) DQS can be high or low during tCDQSS.

4.3.4 Basic Data Output Timing

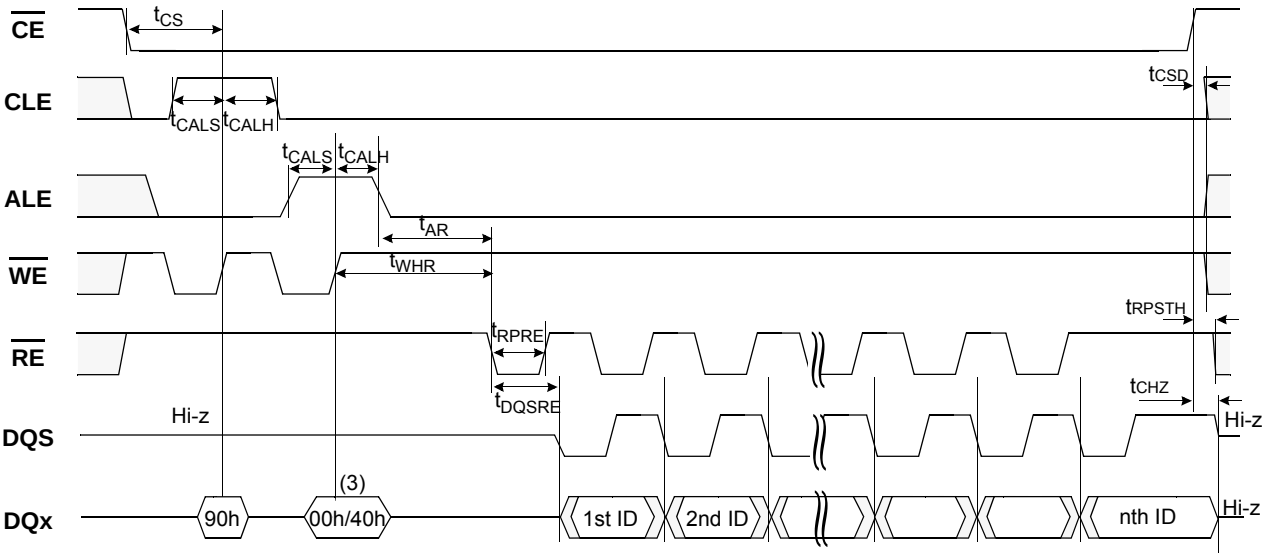


: Don't care

: Undefined(Driven by NAND)

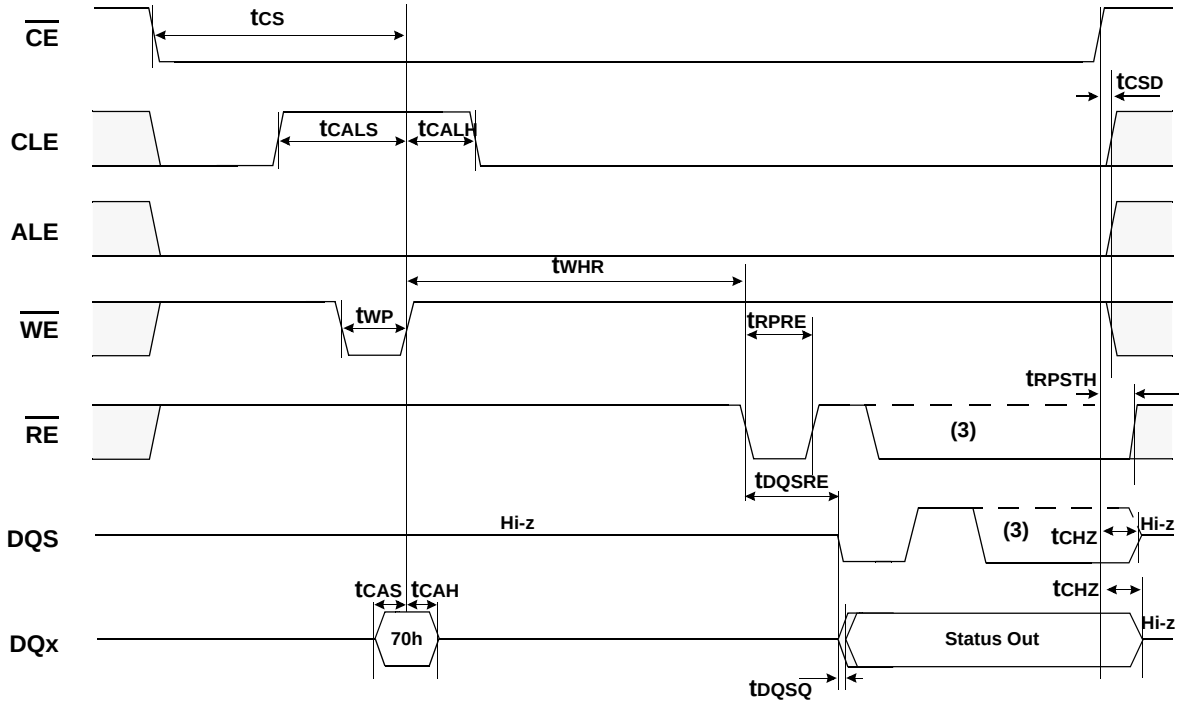
NOTE :
1) DQS, DQS and DQ drivers are turned-on when CE and RE goes Low for data out operation.
2) ALE and CLE should not toggle during tRPRE period regardless of tCALS.
3) DQS and DQ drivers turn from valid value to high-z if either CLE or CE goes high.
4) The least significant bit of the column address shall always be zero.
5) RE shall be high during tCRES

4.3.5 Read ID Operation



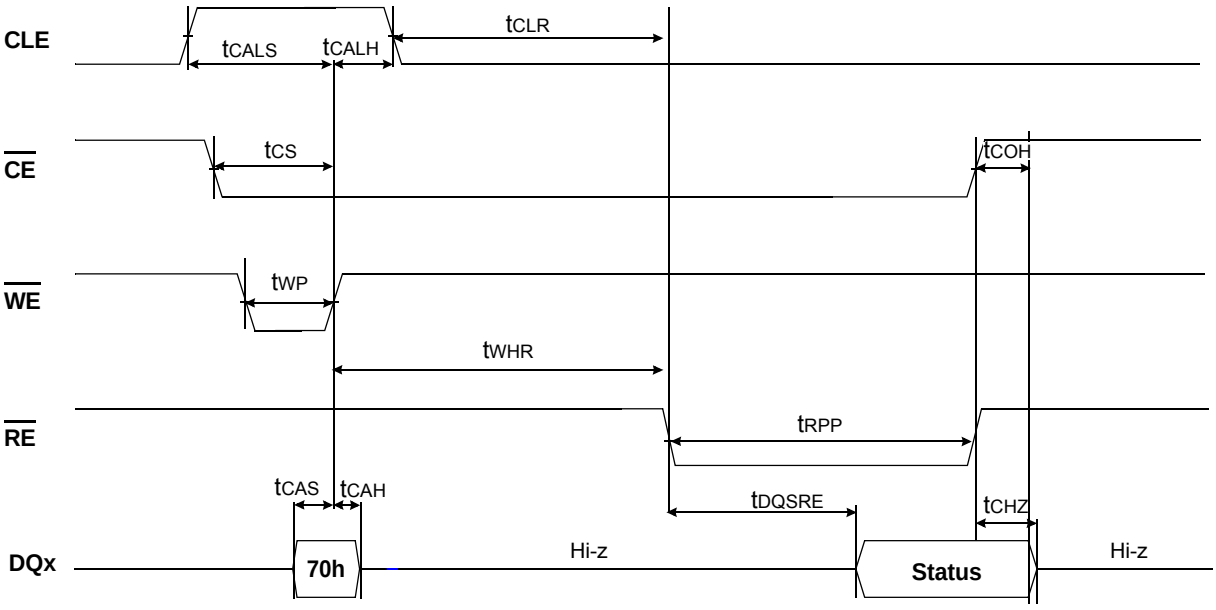
NOTE :
1) Even thougn toggle-mode NAND uses both low- and high-going edges of DQS for reads, ID read operation repeates each data byte twice, so that ID read timing becomes identical to that of conventional NAND
2) DQS and DQ drivers turn from valid value to high-z when $\overline{CE}$ or CLE goes High.
3) Address 00h is for Samsung conventional and 40h is for new JEDEC ID information.

4.3.6 Read Status Cycle

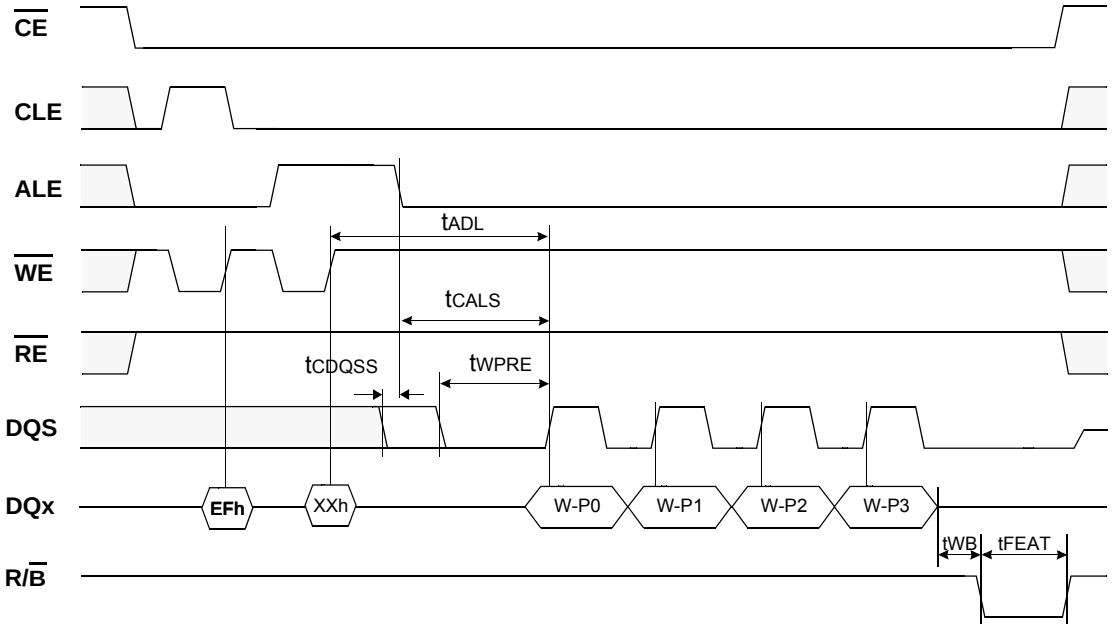


NOTE :
1) Even thougn toggle-mode NAND uses both low and high-going edges of DQS for reads, Read Status operation repeates same output until device status changes
2) DQS and Data out buffers turn from valid value to high-z when CE or CLE goes High
3) RE can toggle more than once.

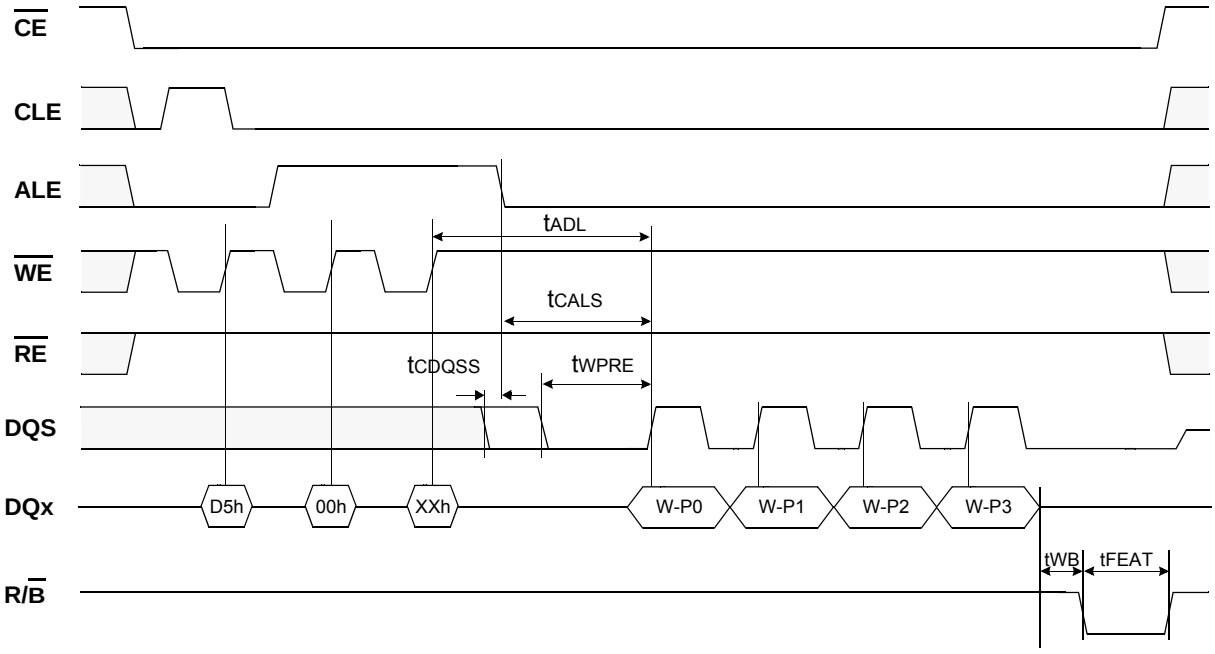
4.3.6.1 Read Status cycle before Toggle DDR setting at Initialization sequence by FFh command



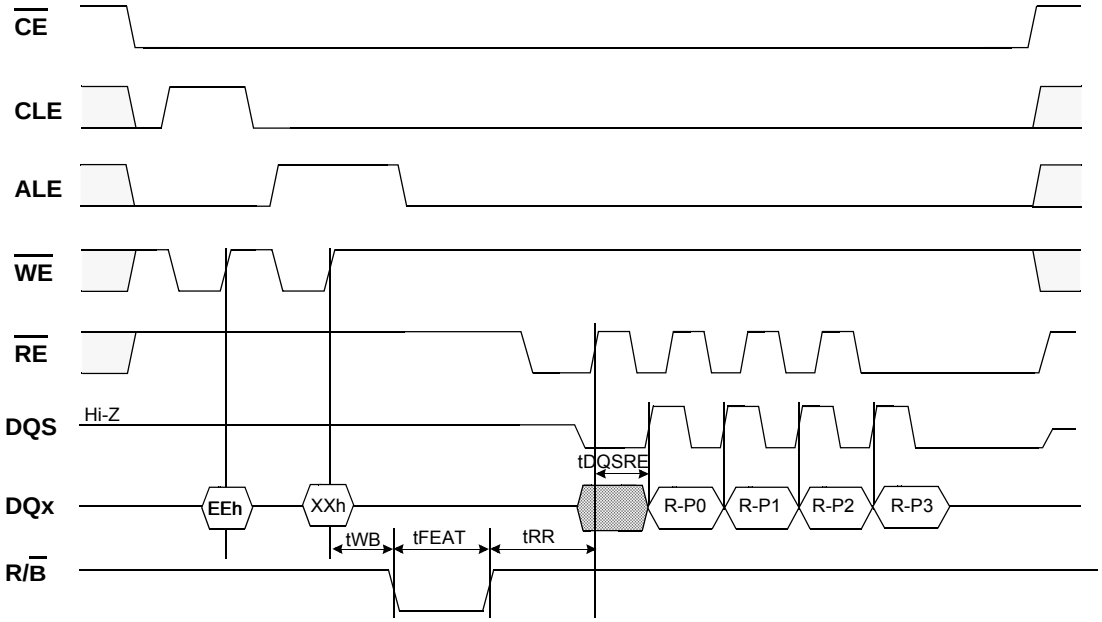
4.3.7 Set Feature-common



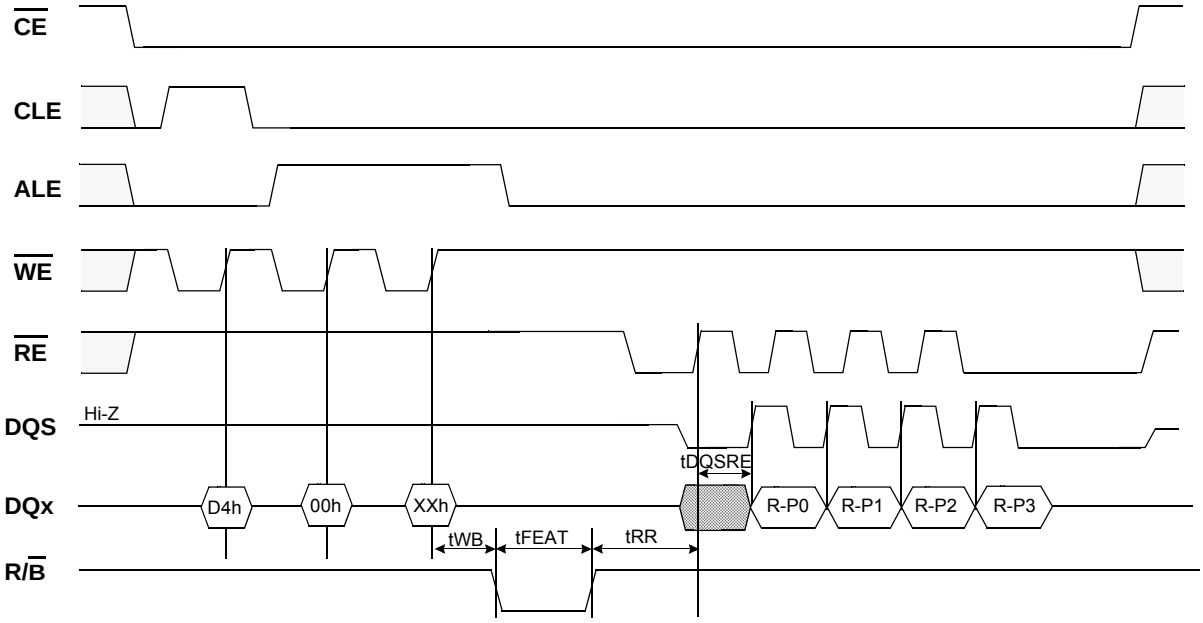
4.3.8 Set Feature-LUN Control within 1CE



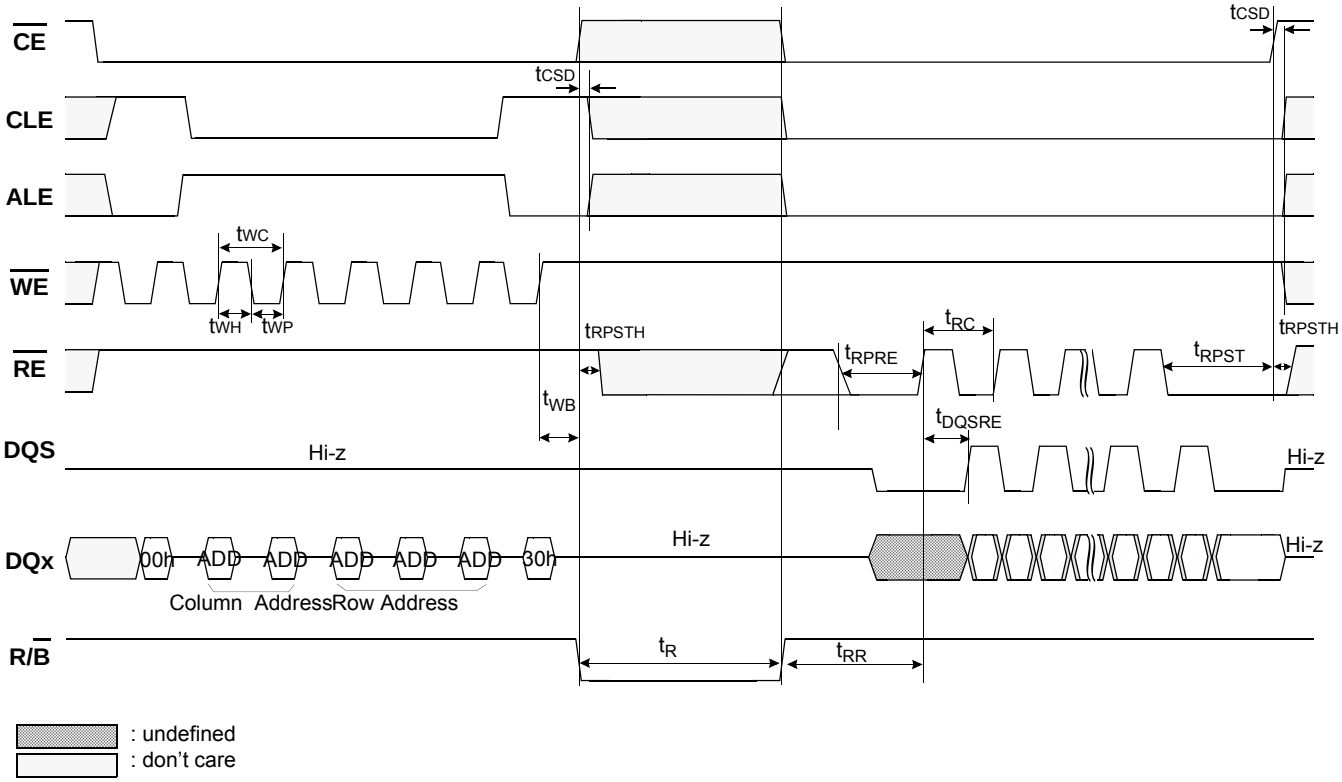
4.3.9 Get Feature-common



4.3.10 Get Feature-LUN Control within 1CE

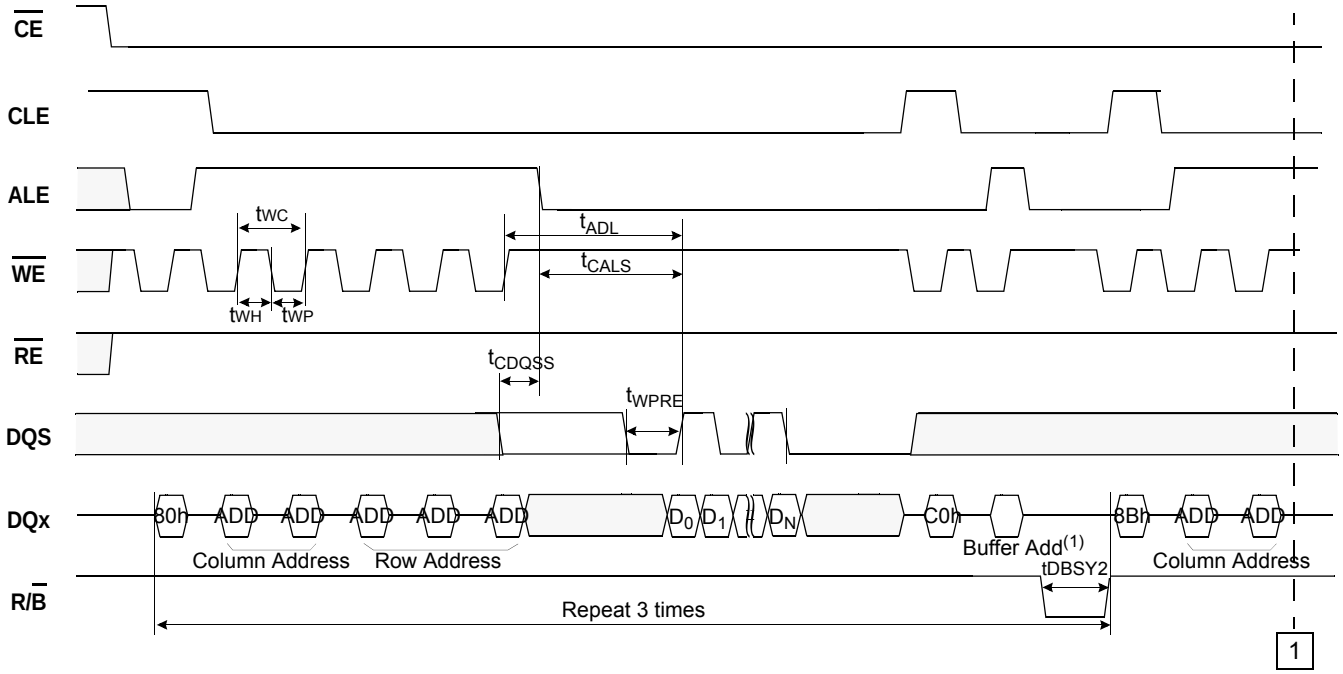


4.3.11 Page Read Operation

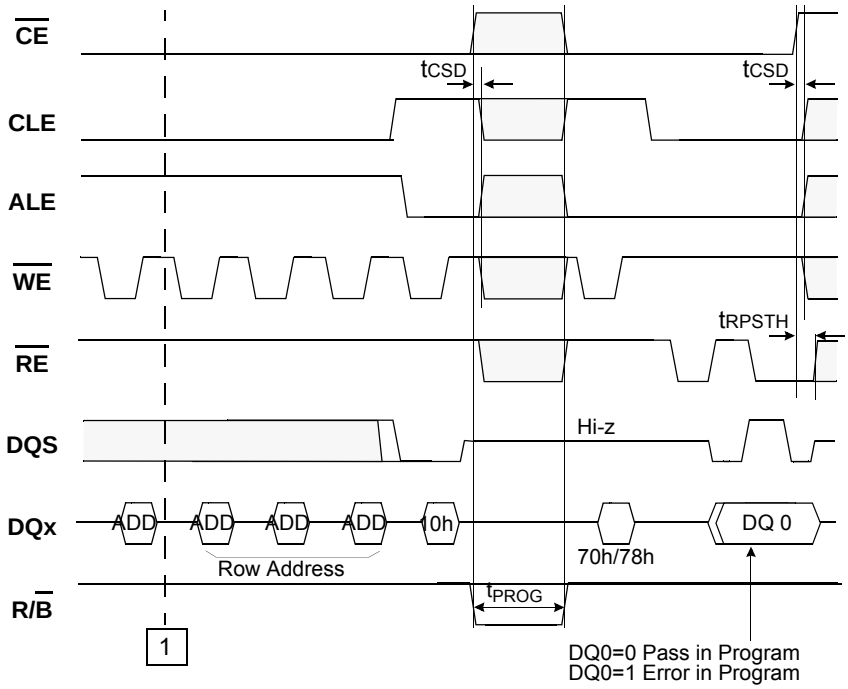


NOTE :
CE is once deasserted, it shall stay high over at least 125ns before it is asserted again.

4.3.12 Page Program Operation(1/2)



4.3.13 Page Program Operation(2/2)



NOTE :
1) $\overline{CE}$ is once deasserted, it shall stay high over at least 125ns before it is asserted again.
3pages Data which are LSB, CSB, and MSB has to be stored in each Program operation.
After C0h Command, buffer address is needed for definition of LSB,CSB or MSB page.
After 8Bh Command, 5 address cycles shall be inputted in sequence of the Program Order Address Information refered to Table 24 at p.27.
2) No data input is not allowed before the page program confirm command(10h) and page buffer latch dump command(C0h).

[Table 23] Buffer Address

	1st Program	2nd Program	3rd Program
Plane0	11h	12h	13h
Plane1	21h	22h	23h
Plane2	41h	42h	43h
Plane0 & 1	31h	32h	33h
Plane1 & 2	61h	62h	63h
Plane0 & 1 & 2	71h	72h	73h

4.4 AC Test Condition

[Table 24] AC Test condition

Parameter	K9XXGD8SXC
Input Pulse Levels	V_{IL} to V_{IH}
Input Rise and Fall Times	1.0V/ns
Input and Output Timing Levels	VccQ/2
Output Load	CL= 5pF

NOTE :
K9XXGD8SXC-XCB0:TA=0 to 70°C, XIB0 :TA=-40 to 85°C,VCC=2.7V~3.6V, unless otherwise noted

4.5 AC Timing Characteristics

4.5.1 Timing Parameters Description

[Table 25] Toggle DDR Timing Parameters Description

Parameter	Description
tR	Data Transfer from Flash array to Register
tPROG	Program Time
tBERS	Erase Time
tADL	Address to Data Loading Time
tAR	ALE Low to $\overline{RE}$ Low
tCALH	CLE/ALE Hold Time
tCALS	CLE/ALE Setup Time
tCAH	Command/Address Hold Time
tCAS	Command/Address Setup Time
tCH	$\overline{CE}$ Hold Time
tCDQSH	DQS Hold Time for data input finish
tCDQSS	DQS Setup Time for data input start
tCHZ	$\overline{CE}$ High to Output Hi-Z
tCLHZ	CLE High to Output Hi-Z
tCLR	CLE to $\overline{RE}$ Low
tCOH	Data Hold Time after $\overline{CE}$ disable
tCR	$\overline{CE}$ Low to $\overline{RE}$ Low
tCRES	$\overline{RE}$ Set up Time
tCS	$\overline{CE}$ Setup Time
tCSD	$\overline{CE}$ Disable to signal (CLE, ALE, $\overline{WE}$) don't care
tCWAW	Command Write Cycle to Address Write Cycle Time for Random Data Input and Register Read Out mode
tDH	Data Hold Time
tDQSH	DQS Input High Pulse Width
tDQSL	DQS Input Low Pulse Width
tDQSQ	Output skew among data output and corresponding DQS
tDQSRE	$\overline{RE}$ to DQS and DQ delay
tDSC	Data Strobe Cycle Time
tDS	Data Setup Time
tDVW	Output data valid window
tFEAT	Busy time for Set Feature and Get Feature
tQH	Output hold time from DQS
tQHS	DQS hold skew factor
tRC	Read Cycle Time
tREH	$\overline{RE}$ High pulse width
tRP	$\overline{RE}$ Low pulse width
tRPP	$\overline{RE}$ Low width for Read Status at power-up
tRPRE	Read Preamble
tRPST	Read Postamble
tRPSTH	Read Postamble Hold Time
tRR	Ready to $\overline{RE}$ High
tRST	Device Resetting Time(Read/Program/Erase)
tWB	$\overline{WE}$ High to Busy
tWC	Write Cycle Time
tWH	$\overline{WE}$ High pulse width
tWHR	$\overline{WE}$ High to $\overline{RE}$ Low
tWHR2	$\overline{WE}$ High to $\overline{RE}$ Low for Random data out
tWP	$\overline{WE}$ Low pulse Width
tWPRE	Write Preamble
tWPST	Write Postamble
tWPSTH	Write Postamble Hold Time
tWW	$\overline{WP}$ High/Low to $\overline{WE}$ low
tDBSY	Dummy Busy Time for Multi-plane Program
tDBSY2	Dummy Busy Time for Data setup
tCBSY	Dummy Busy Time for Cache Program
tDCBSYR	Cache Busy in Cache Read

4.5.2 Timing Parameters Table

AC Timing Characteristics

Parameter	Symbol	133Mhz		166Mhz		200Mhz		Unit
		Min	Max	Min	Max	Min	Max	
Address to Data Loading Time	tADL	300	-	300	-	300	-	ns
ALE Low to $\overline{RE}$ Low	tAR	10	-	10	-	10	-	ns
CLE/ALE Hold Time	tCALH	5	-	5	-	5	-	ns
CLE/ALE Setup Time	tCALS	15	-	15	-	15	-	ns
Command/Address Hold Time	tCAH	5	-	5	-	5	-	ns
Command/Address Setup Time	tCAS	5	-	5	-	5	-	ns
DQS Hold Time for data input finish	tCDQSH	100	-	100	-	100	-	ns
DQS Setup Time for data input start	tCDQSS	100	-	100	-	100	-	ns
$\overline{CE}$ Hold Time	tCH	5	-	5	-	5	-	ns
$\overline{CE}$ High to Output Hi-Z	tCHZ	-	30	-	30	-	30	ns
CLE High to Output Hi-Z	tCLHZ	-	30	-	30	-	30	ns
CLE to $\overline{RE}$ Low	tCLR	10	-	10	-	10	-	ns
Data Hold Time after $\overline{CE}$ disable	tCOH	5	-	5	-	5	-	ns
$\overline{CE}$ Low to $\overline{RE}$ Low	tCR	10	-	10	-	10	-	ns
$\overline{RE}$ Set up time	tCRES	10	-	10	-	10	-	ns
$\overline{CE}$ Setup Time	tCS	25	-	25	-	25	-	ns
$\overline{CE}$ Disable to signal don't care	tCSD	10	-	10	-	10	-	ns
Command Write cycle to Address Write cycle Time for Random data input and Register Read Out mode	tCWAW	300	-	300	-	300	-	ns
Data Hold Time	tDH	0.75	-	0.55	-	0.4	-	ns
DQS Input High Pulse Width	tDQSH	0.45*tRC	-	0.45*tRC	-	0.45*tRC	-	ns
DQS Input Low Pulse Width	tDQSL	0.45*tRC	-	0.45*tRC	-	0.45*tRC	-	ns
Output skew among data output and corresponding DQS	tDQSQ	-	0.6	-	0.5	-	0.4	ns
$\overline{RE}$ to DQS and DQ delay	tDQSRE	5	25	5	25	5	25	ns
Data Strobe Cycle Time	tDSC	7.5	-	6	-	5	-	ns
Data Setup Time	tDS	0.75	-	0.55	-	0.4	-	ns
Output data valid window	tDVW	tDVW = tQH - tDQSQ						ns
Busy time for Set Feature and Get Feature	tFEAT	-	1	-	1	-	1	µs
Output hold time from DQS	tQH	tQH = min[tREH, tRP] - tQHS						ns
DQS hold skew factor	tQHS	-	0.6	-	0.5	-	0.4	ns
Read Cycle Time	tRC	7.5	-	6	-	5	-	ns
$\overline{RE}$ High pulse width	tREH	0.45*tRC	-	0.45*tRC	-	0.45*tRC	-	ns
$\overline{RE}$ Low pulse width	tRP	0.45*tRC	-	0.45*tRC	-	0.45*tRC	-	ns
$\overline{RE}$ Low width for Read Status at power-up	tRPP	30	-	30	-	30	-	ns
Read Preamble	tRPRE	15	-	15	-	15	-	ns
Read Postamble	tRPST	tDQSRE+ 0.5xtRC	-	tDQSRE+ 0.5xtRC	-	tDQSRE+ 0.5xtRC	-	ns
Read Postamble Hold Time	tRPSTH	25	-	25	-	25	-	ns
Ready to $\overline{RE}$ High	tRR	20	-	20	-	20	-	ns
Device Resetting Time (Read/Program/Erase)	tRST(1)	10 /30 /200						µs
$\overline{WE}$ High to Busy	tWB	-	100	-	100	-	100	ns
Write Cycle Time	tWC	25	-	25	-	25	-	ns
$\overline{WE}$ High pulse width	tWH	11	-	11	-	11	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	tWHR	120	-	120	-	120	-	ns

Parameter	Symbol	133Mhz		166Mhz		200Mhz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{WE}$ High to $\overline{RE}$ Low for Random data out	tWHR2	300	-	300	-	300	-	ns
$\overline{WE}$ Low pulse Width	tWP	11	-	11	-	11	-	ns
Write Preamble	tWPRE	15	-	15	-	15	-	ns
Write Postamble	tWPST	6.5	-	6.5	-	6.5	-	ns
Write Postamble Hold Time	tWPSTH	25	-	25	-	25	-	ns
$\overline{WP}$ High/Low to $\overline{WE}$ low	tWW	100ns	-	100ns	-	100ns	-	ns

NOTE :
1) If reset command(FFh) is written at Ready state, the device goes into Busy for maxium 10us.

4.5.3 Read/Program / Erase Characteristics

[Table 26] NAND Read/Program/Erase Characteristics

Parameter	Symbol		Min	Typ	Max	Unit
Data Transfer from Flash array to Register	tR(8KB)	TLC	-	85	90	µs
		SLC	-	40	50	
	tR(4KB)		-	50	70	µs
Program Time	tPROG	TLC	-	1.65	5	ms
		SLC	-	0.35	5	
Dummy Busy Time for Multi-plane setting	tDBSY		-	0.5	1	µs
Dummy Busy Time for Data setup	tDBSY2		-	-	10	µs
Dummy Busy Time for Cache Program	tCBSY		-	-	tPROG	ms
Cache Busy in Cache Read	t_{DCBSYR}		-	-	tR	µs
Number of Partial Program Cycles in the Same Page	Nop		-	-	1	cycle
Block Erase Time	tBERS	TLC	-	5	10	ms
		SLC	-	10	20	

NOTE :
1) Typical program time is measured at Vcc=3.3V, TA=25°C. Not 100% tested.
2) Typical Program time is defined as the time within which more than 50% of the whole pages are programed at 3.3V Vcc and 25°C temperature.
3) tCBSY depends on the timing between internal programming time and data in time.
4) tR is average of the 1st/2nd/3rd page's Read time.

5.0 COMMAND DESCRIPTION AND DEVICE OPERATION

5.1 Basic Command Sets

Toggle DDR NAND Flash Memory has addresses multiplexed into 8 I/Os. Command, address and data is all written through DQ[7:0] by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Those are latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the DQ[7:0] pins. Commands which apply to a specific page or block typically have a second command and ones that apply to a target or a LUN have a first command only.

Table 27 below defines the basic command sets.

[Table 27] Basic Command Sets

Mode	Function	1st Set	Address Cycles	2nd Set	Acceptable while Accessed LUN is Busy	Acceptable while Other LUNs are Busy
Common	Page Read	00h	5	30h		Y
	Sequential Cache Read	31h	-	-		Y
	Read Start for Last Page Cache Read	3Fh	-	-		Y
	Random Cache Read	00h	5	31h		Y
	Block Erase	60h	3	D0h		Y
	Read for Copy-Back	00h	5	35h		Y
	Random Data Input(1)	85h	2	-		Y
	Random Data Output(1)	05h	2	E0h		Y
	Read Status	70h	-	-	Y	
	Reset	FFh	-	-	Y	
	Reset LUN	FAh	3	-	Y	Y
TLC	Serial Data input for Program / Cache Program	80h	5	-		Y
	Serial Data input for Copy-Back Program	85h	5	-		Y
	Set Feature-Common	EFh	1	-		
	Get Feature-Common	EEh	1	-		
	Set Feature-LUN control within 1 $\overline{CE}$	D5h	2	-		
	Get Feature-LUN control within 1 $\overline{CE}$	D4h	2	-		
	Read ID	90h	1	-		
	Page Buffer Latch Dump	C0h	1	-		Y
	Program / Copy-Back Program Confirm	8Bh	5	10h		Y
	Cache Program Confirm	8Bh	5	15h		Y
	Fast 4KB Read (Half page)	00h	5	20h		Y
SLC	Page Program(2)	80h	5	10h		Y
	Cache Program(2)	80h	5	15h		Y
	Copy-Back Program(2)	85h	5	10h		Y
	SLC Mode Access	DAh	-	-		
	SLC Mode Abort	DFh	-	-		

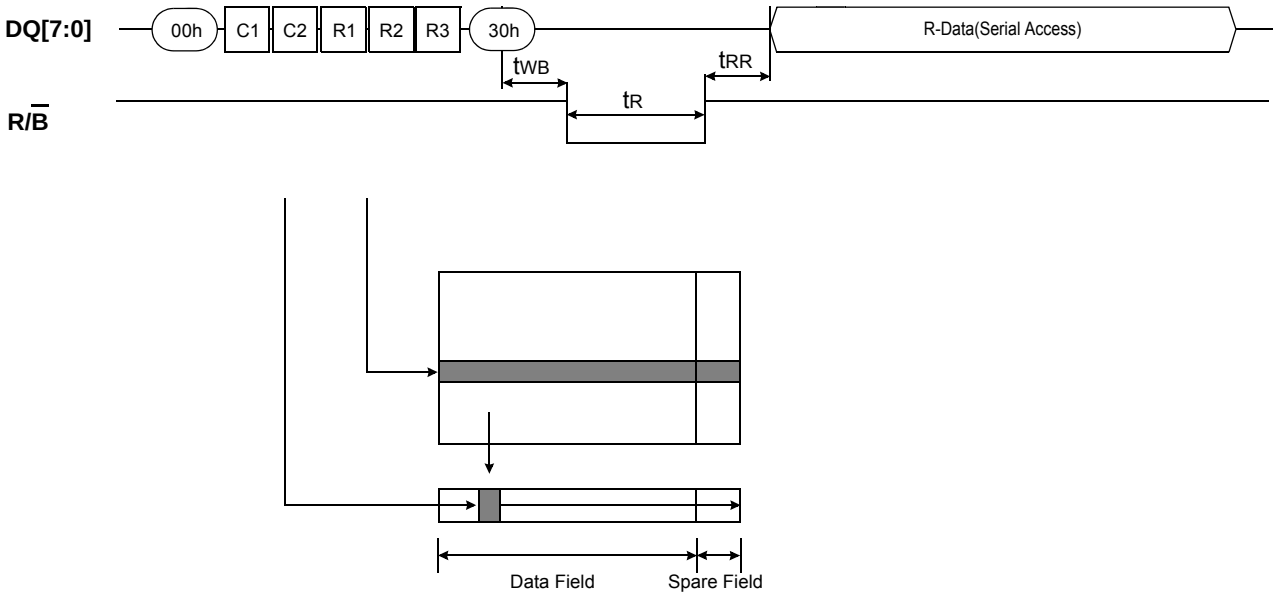
NOTE :
1) Random Data Input/Output can be executed in a page.
2) Page Program/Cache Program/Copy-back Program must be excuted at SLC mode.
3) TLC mode program command input (8Bh) is not allowed after SLC mode access.

Caution :
Any undefined command inputs are prohibited except for above command set.

5.2 Basic Operation

5.2.1 Page Read Operation

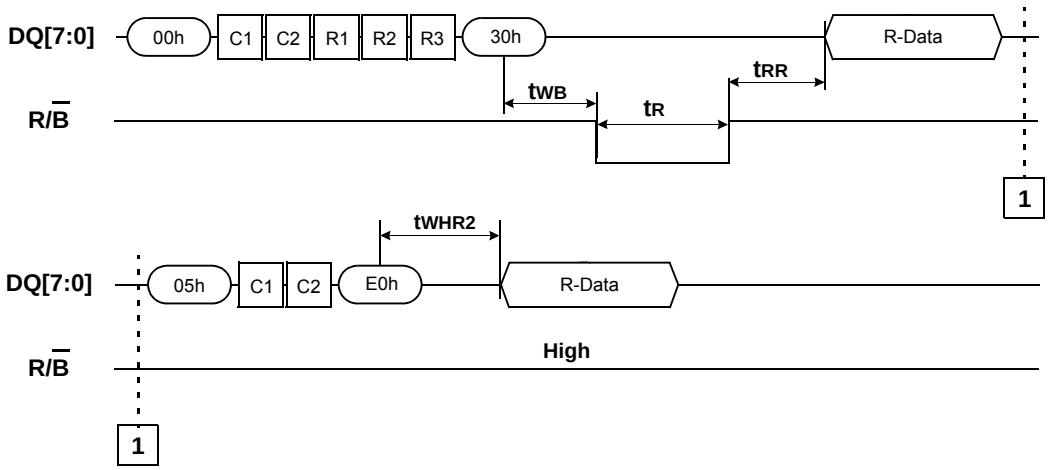
The Page Read function reads a page of data identified by row address for the selected LUN. The page of data is made available to be read from the page register starting at the specified column address. Figure 11 defines the Page Read behavior and timings. Reading beyond the end of a page results in indeterminate values being returned to the host. Page Read out is only possible when the 3rd program is completed.



[Figure 11] Page Read Sequence

5.2.1.1 Page Read Operation with Random Data Output

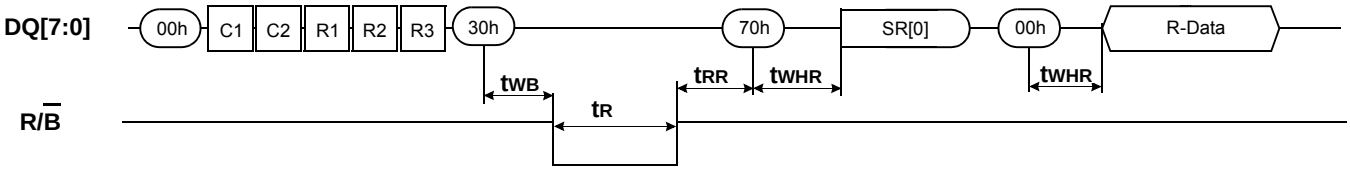
The Random Data Output function changes the column address from which data is being read in the page register for the selected LUN. The Random Data Output command shall only be issued when the LUN is in a read idle condition. Figure 12 defines the Random Data Output behavior and timings. The host shall not read data from the LUN until tWHR(ns) after the second command (i.e. E0h) is written to the LUN. Page Read out is only possible when the 3rd program is completed.



[Figure 12] Page Read with Random Data Output Sequence

5.2.1.2 Data Out After Read Status

While monitoring the read status to determine when the tR (transfer from Flash array to apage register) is complete, the host shall re-issue the 00h command to start reading data. Issuing the 00h command will cause data to be returned starting at the selected column address.

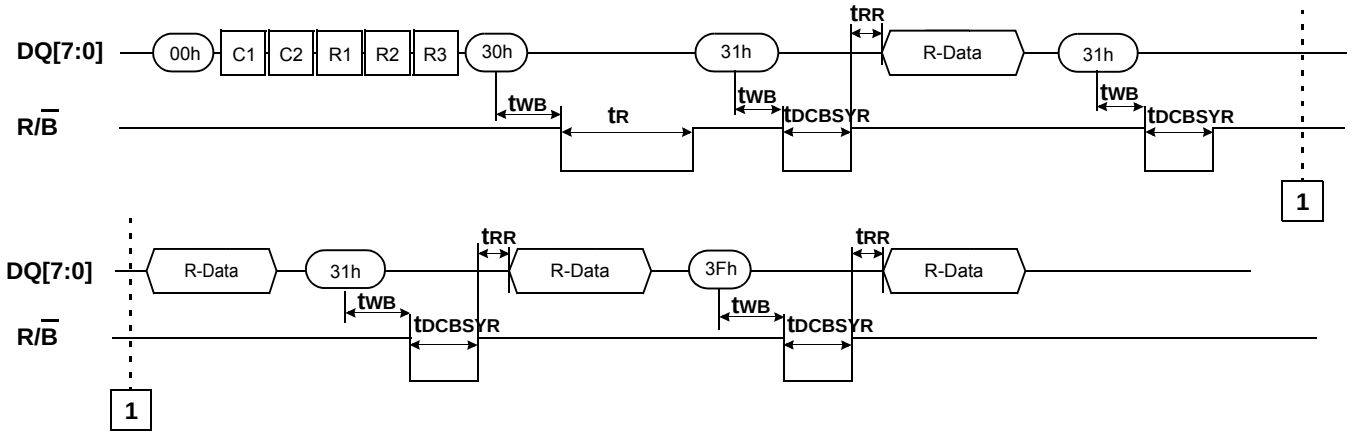


[Figure 13] Data Out After Read Status Sequence

5.2.2 Sequential Cache Read Operation

The Sequential Cache Read offers loading page ahead operation, that is a page to be loaded from the Flash array while already loaded page is read by a host. A Read Page command shall be issued prior to the initial Sequential Cache Read command in a cache read sequence. A Sequential Cache Read command (i.e. 31h) shall be issued until the Sequential Cache Read Operation is completed by the Read Start for Last Page Cache Read command(i.e. 3Fh)

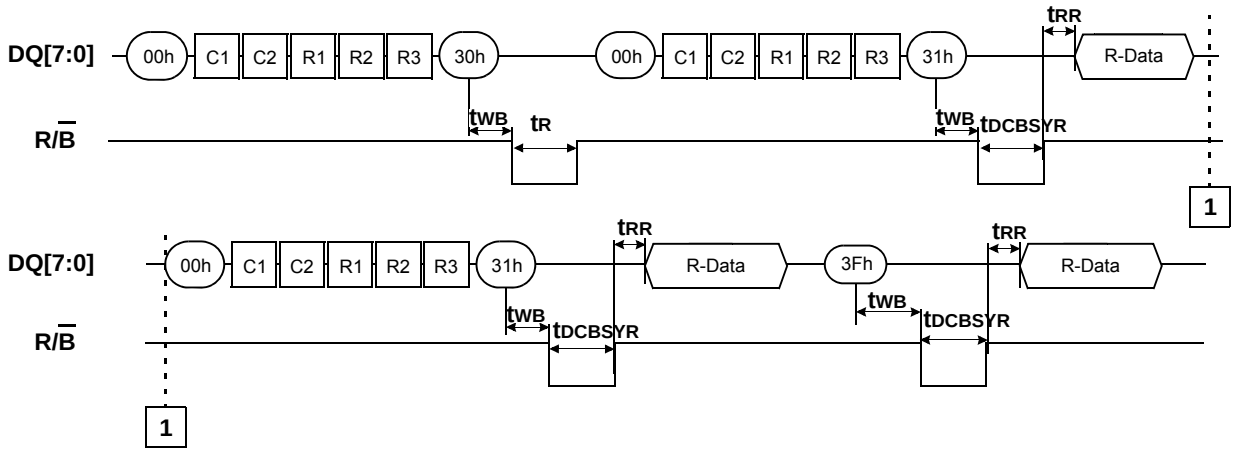
The Sequential Cache Read command may be issued after the Read function is complete (i.e. SR[6] is set to one). Data output always begins at column address 00h. When the Sequential Cache Read command(i.e. 31h) is issued, SR[6] is cleared to zero (i.e. busy). After the operation finishes, SR[6] turns to one (i.e. ready) and the host may begin to read the data loaded by the previous Sequential Cache Read operation. The data loaded by a Sequential Cache Read command from Flash array to a page register is copied to a cache register by a following Sequential Cache Read command. To check internal cache operation progress, ready/busy for Flash array (i.e. SR[5]) from READ STATUS or READ STATUS ENHANCED table shall be referenced. During 'busy for Flash array' period, illegal commands which is not related to Sequential Cache Read operation except RESET and READ STATUS commands are prohibited. And the data of a final page loaded onto a page register is transferred to a cache register by 3Fh command. The host shall not issue a Sequential Cache Read command(31h) after the last page of a block is read. Page Read out is only possible when the 3rd program is completed.



[Figure 14] Sequential Cache Read Sequence

5.2.3 Random Cache Read Operation

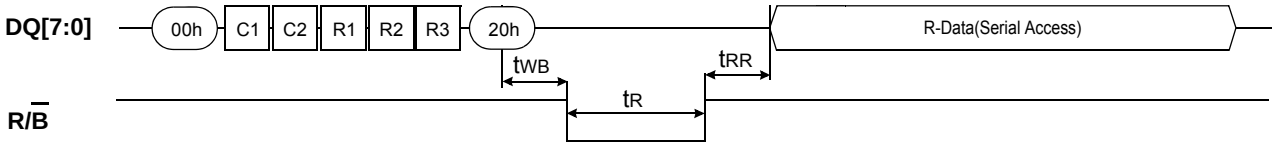
A Read Page command shall be issued prior to the initial Random Cache Read command in a cache read sequence like the Sequential Cache Read operation. Colunm address shall be fixed to 00h during Random Cache Read operation. 3Fh command is required to finish the sequence and read the final cached page. To check internal cache operation progress, ready/busy for Flash array (i.e. SR[5]) from READ STATUS or READ STATUS ENHANCED table shall be referenced. During 'busy for Flash array' period, illegal commands which is not related to Random Cache Read operation except RESET and READ STATUS commands are prohibited. The page and block address can be accessed in a random manner while the plane address shall stay the same. Figure 15 defines the Random Cache Read behavior and timings. Page Read out is only possible when the 3rd program is completed.



[Figure 15] Random Cache Read Sequence

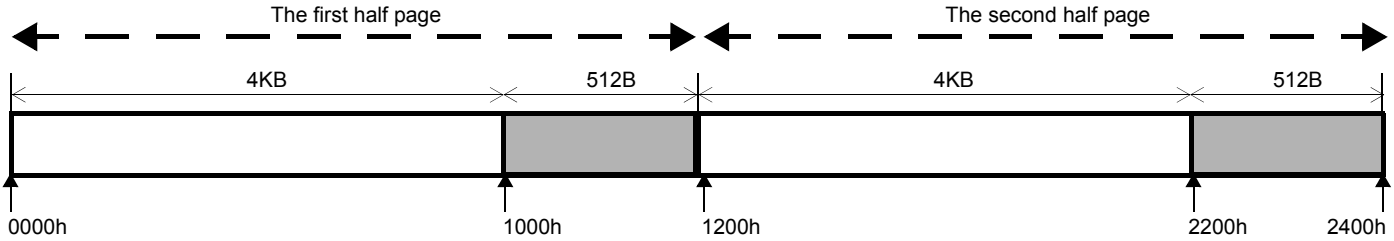
5.2.4 Fast 4KB Read (Half page Read)

(WARNING : SAMSUNG RECOMMENDS THE USER TO CONTACT AND CONSULT SAMSUNG BEFORE ENABLING THIS FUNCTION. ENABLING THIS FUNCTION MAY CAUSE MALFUNCTION, INCLUDING BUT NOT LIMITED TO PERMENANT DAMAGE TO THE CHIP).
The Fast 4KB Read function transfers only half page (i.e. 4KB+512B) data in NAND array to page register. This function helps applications maximize random read or write throughput. Since Fast 4KB Read functoin transfers only half page, to transfer other side half page data, another Fast 4KB Read operation is required.



[Figure 16] Fast 4KB READ sequence

Target 4KB data shall be determined by latched address between 00h and 20h command. When the address between 0000h and 11FFh is set, the first half page data shall be transferred and when the address between 1200h and 2400h is set, the second half page data shall be transferred. Figure 17 represents the page layout when Fast 4KB Read is used. Page Read out is only possible when the 3rd program is completed.



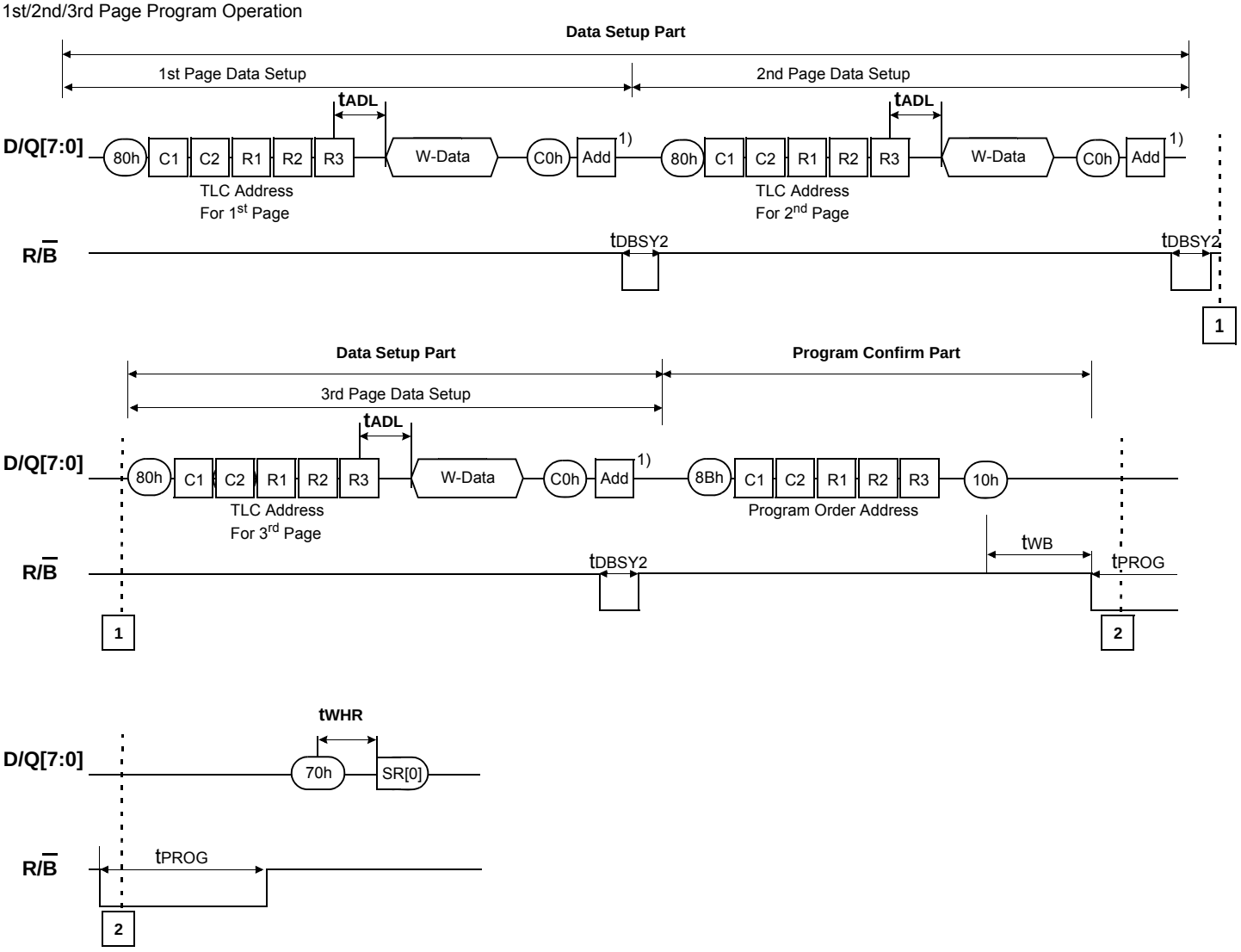
[Figure 17] Page layout for Fast 4KB READ

5.2.5 Page Program Operation

The device is programmed basically on a page basis, and each page shall be programmed only once before being erased. The addressing order shall be sequential within a block. The contents of the page register are programmed into the Flash array specified by row address. SR[0] is valid for this command after SR[6] transitions from zero to one until the next transition of SR[6] to zero.3bit/cell NAND has the following programming characteristics. The fine programming to one WL consists of 3 steps of program operation. 3 pages' data, LSB, CSB and MSB, has to be stored for each program operation to make 8 program states at the same time.

Each programming step has its own program order address which is not same as physical page address. The following is the program order address to minimize the coupling. The Program operation shall be followed in below sequence. 1st Program operation at WL0 -> 1st Program operation at WL1 -> 1st Program operation at WL2 ->3rd Program operation at WL1 -> 1st Program operation at WL4 -> 1st Program operation at WL5 etc. The programmed data of each page can be read out only if 3rd program is completed. Figure 19 defines the Page Program behavior and timings. Writing beyond the end of the page register is undefined.

1st/2nd/3rd Page Program Operation



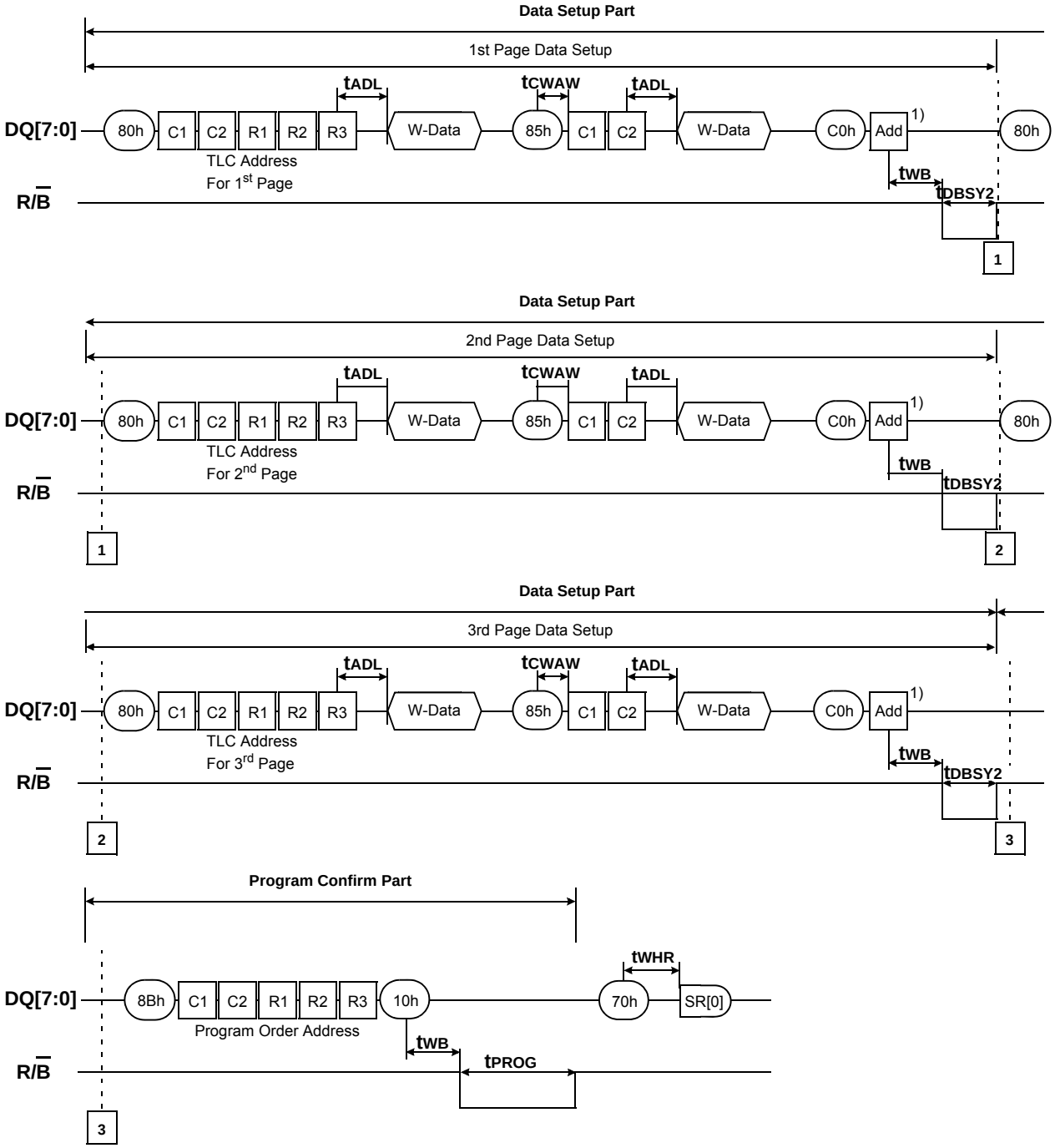
[Figure 18] 1st/2nd/3rd Page Program Operation

NOTE :
1) For address followed by C0h command, refer to the buffer address Table 23

5.2.5.1 Program Operation with Random Data Input

The device supports random data input in a page. The column address for the next data, which will be written, may be changed to the address using Random data input command(i.e. 85h). Random data input may be operated multiple times without limitation.

1st/2nd/3rd Page Program Operation with Random Data Input



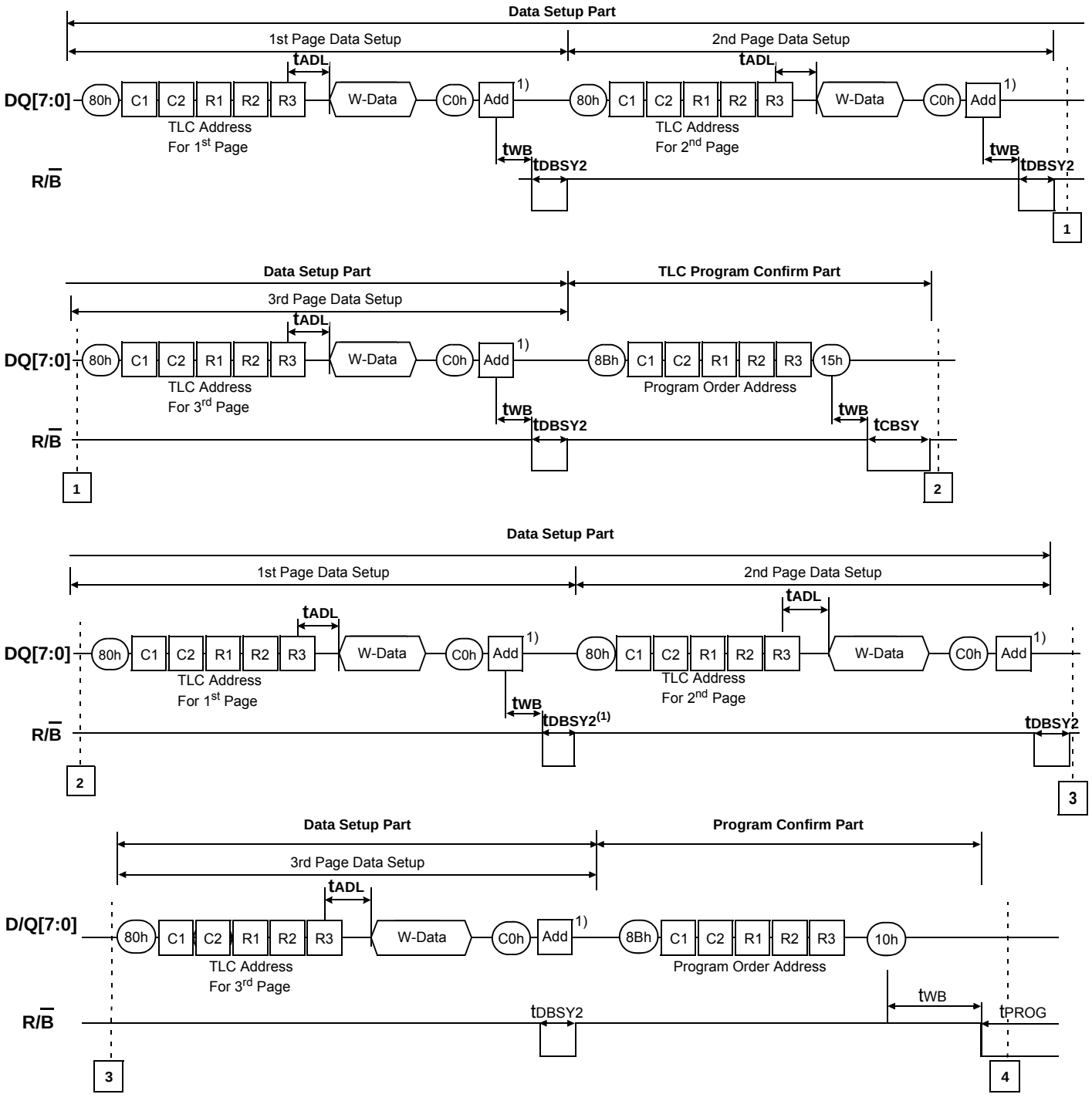
[Figure 19] 1st/2nd/3rd Page Program operation with Random Data Input Sequence

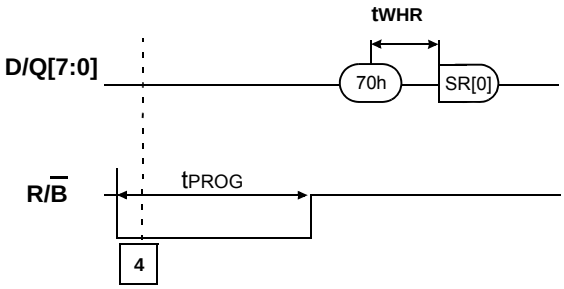
NOTE :
1) For address followed by C0h command, refer to the buffer address Table 23

5.2.6 Cache Program Operation

The Cache Program function allows the host to write the next data for another page to the page register while a page of data to be programmed to the Flash array for the selected LUN. When command 15h is issued, R/$\overline{B}$ returns high (i.e. ready) when a cache register is ready to be written after data in the cache register is transferred to a page register. To check internal cache operation progress, ready/busy for Flash array (i.e. SR[5]) from READ STATUS or READ STATUS ENHANCED table shall be referenced. During 'busy for Flash array' period, illegal commands which is not related to Cache Program operation except RESET and READ STATUS commands are prohibited.
When command 10h is issued for the final page, R/$\overline{B}$ turns to high after outstanding program operation performed by previous Cache Program command and the program operation for the final page is completed. SR[0] is valid for this command after SR[5] transitions from zero to one until the next transition. SR[1] is valid for this command after SR[6] transitions from zero to one, and it is invalid after the first Cache Program Command completion since there is no previous Cache Program operation. Cache Program operation shall work only within a block. Figure 22 defines the Cache Program behavior and timings.
Note that tPROG at the end of the caching operation may be longer than typical as this time also includes completing the programming operation for the previous page. Writing beyond the end of the page register is undefined.

1st/2nd/3rd Page Cache Program Operation



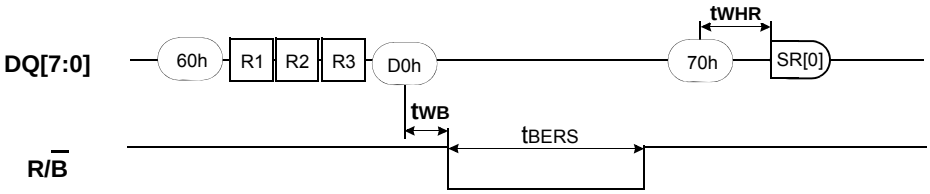


[Figure 20] 1st/2nd/3rd Page Cache Program Operation

NOTE :
1) For address followed by C0h command, refer to the buffer address Table 23
2) tDBSY2' = tCBSY(Dummy busy time for Cache Program) + tDBSY2

5.2.7 Block Erase Operation

The Block Erase operation is done on a block basis. Only three cycles of row addresses are required for Block Erase operation and a page address within the cycles is ignored while plane and block address are valid.
After Block Erase operation passes, all bits in the block shall be set to one. SR[0] is valid for this command after SR[6] transitions from zero to one(i.e. the selected LUN is ready) until the LUN goes in busy state by a next command. Figure 21 defines the Block Erase behavior and timings.

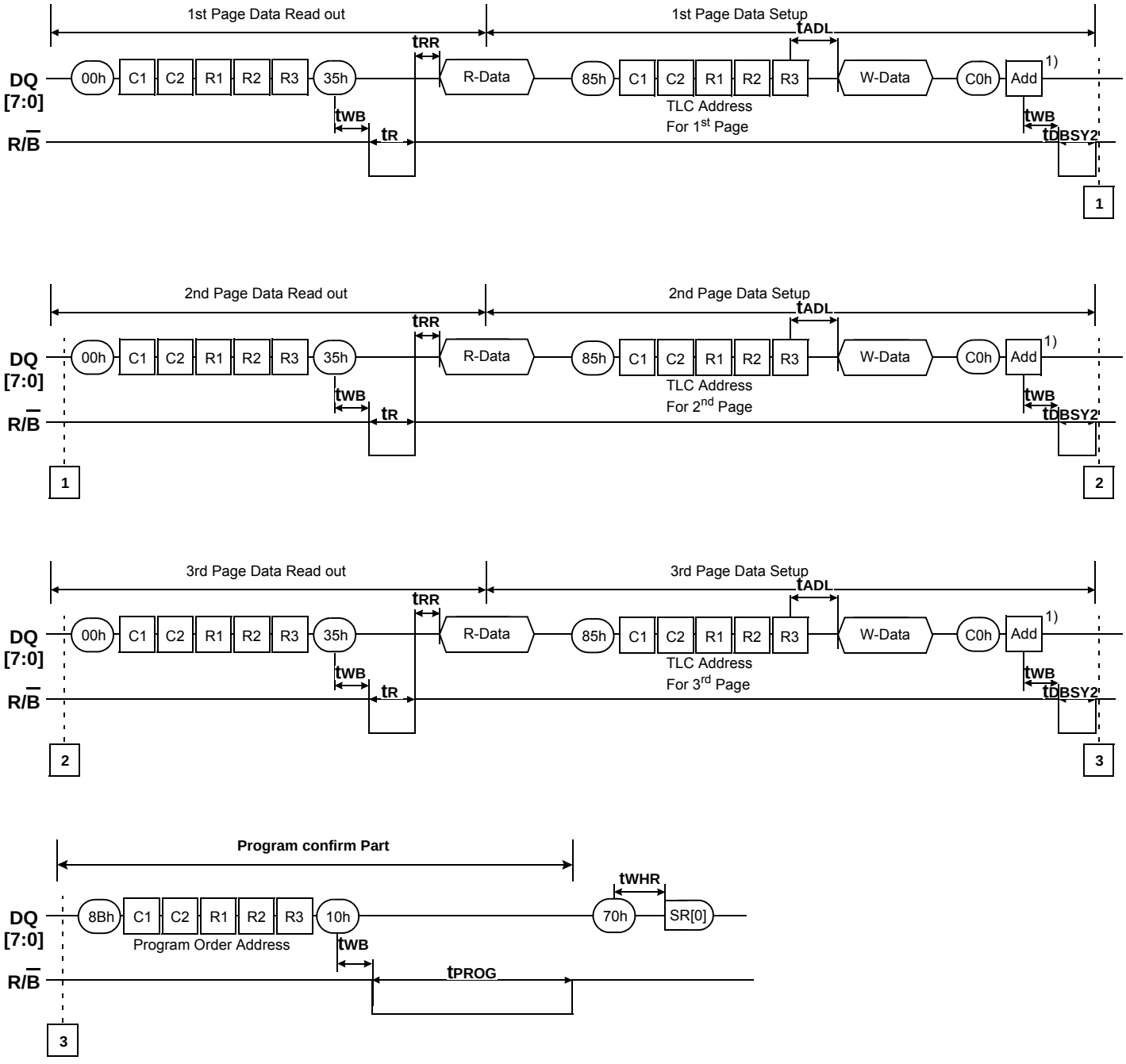


[Figure 21] Block Erase Sequence

5.2.8 Copy-Back Program Operation

The Copy-Back Program with Read for Copy-Back is configured to efficiently rewrite data stored in a page without data re-loading when no error within the page is found. Since the time-consuming re-loading cycles are removed, copy-back operation helps the system performance improve. The benefit is especially obvious when a part of a block is updated and the rest of the block also needs to be copied to the newly assigned free block.
The Copy-Back operation consists of 'Read for Copy-Back' and 'Copy-Back Program'. A host reads a page of data from a source page using 'Read for Copy-Back' and copies read data back to a destination page on the same LUN by 'Copy-Back Program' command. Copy-Back Program Operation shall work only within the same plane. Figure 22 defines the Copy-Back Program behavior and timings.

1st/2nd/3rd Page Copy-Back Program Operation



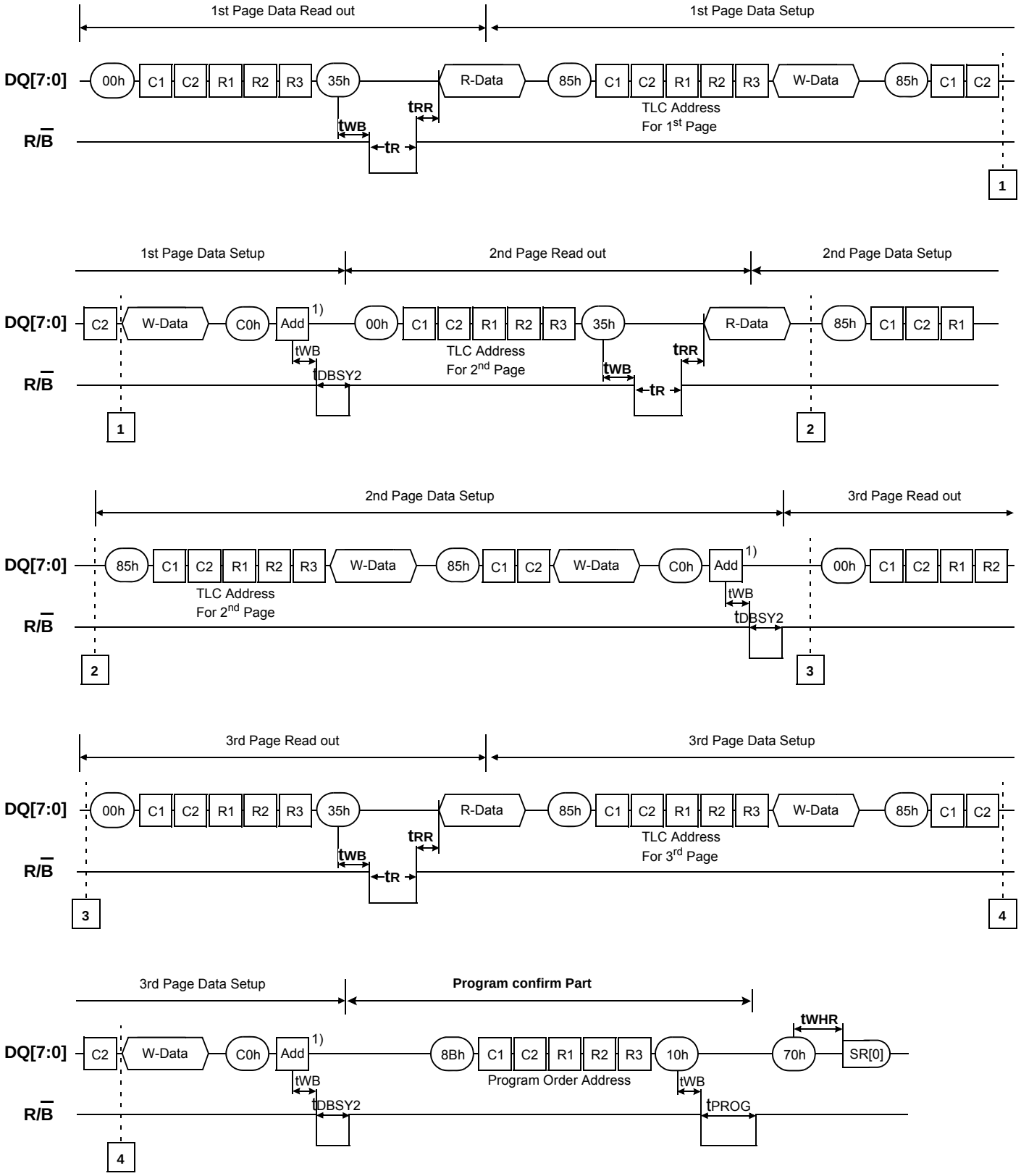
[Figure 22] 1st/2nd/3rd Page Copy-Back Program Operation

NOTE :
1) For address followed by C0h command, refer to the buffer address Table 23

5.2.8.1 Copy-Back Program Operation with Random Data Input

After a host completes to read data from a page register, the host may modify data using Random Data Input command if required. Figure 23 defines the Copy-Back Program with Random Data Input behavior and timings.

1st/2nd/3rd Page Copy-Back Program Operation with Random Data Input

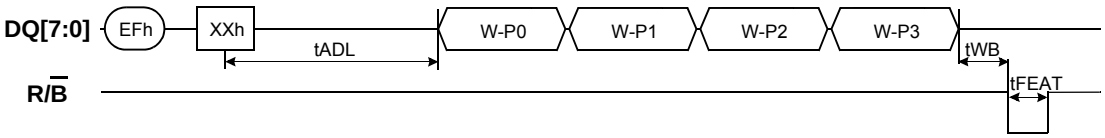


[Figure 23] 1st/2nd/3rd Page Copy-Back Program Operation with Random Data Input

NOTE :
1) For address followed by C0h command, refer to the buffer address Table 23

5.2.9 Set Feature Operation - Common

Users may set particular features using 'Set Feature' operation. Once a feature is set by users, it shall not be changed until the device is powered off or setting is changed by users. Figure 24 defines the Set Features behavior and timings and Table 29 defines features that users can change.



[Figure 24] Set Feature Sequence - Common

[Table 28] Set feature addresses

Address	Description
02h	Toggle 2.0 specific setting
10h	Driver strength setting
30h	External V_{PP} setting

5.2.9.1 Toggle 2.0 specific setting (02h)

This setting is required in order to use reference voltage and complementary signal. DQS latency cycle can also be configured by this SET FEATURE operation to read the first valid data correctly.
When Vref signal or complementary signals are set, those signals shall be applied before SET FEATURE sequence. The setting is done at the rising edge of R/B, thus the signals are used to check ready by READ STATUS operation.

[Table 29] Toggle 2.0 specific setting assignment

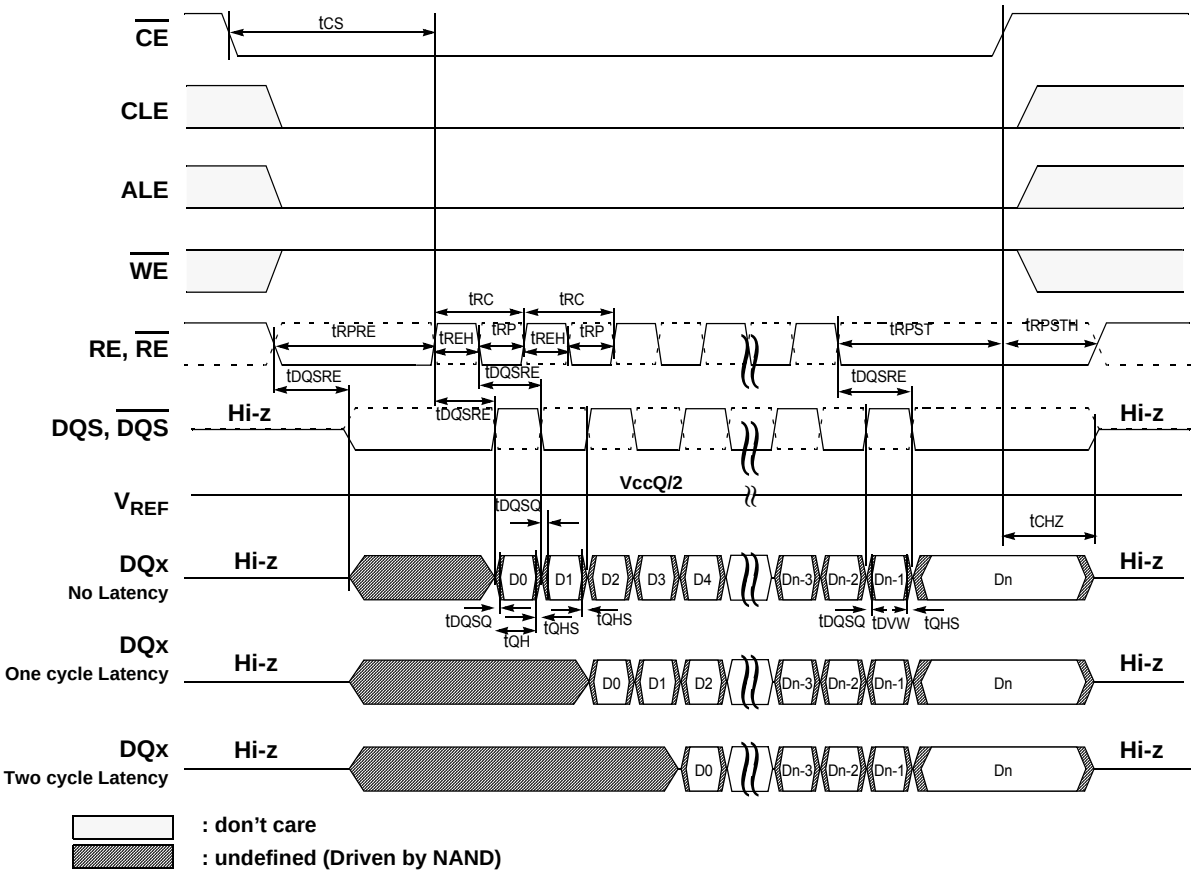
P0	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
	N/A				Reserved	RE	DQS	Vref

P1	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
	# of Latency DQS cycle for Write				# of Latency DQS cycle for READ			

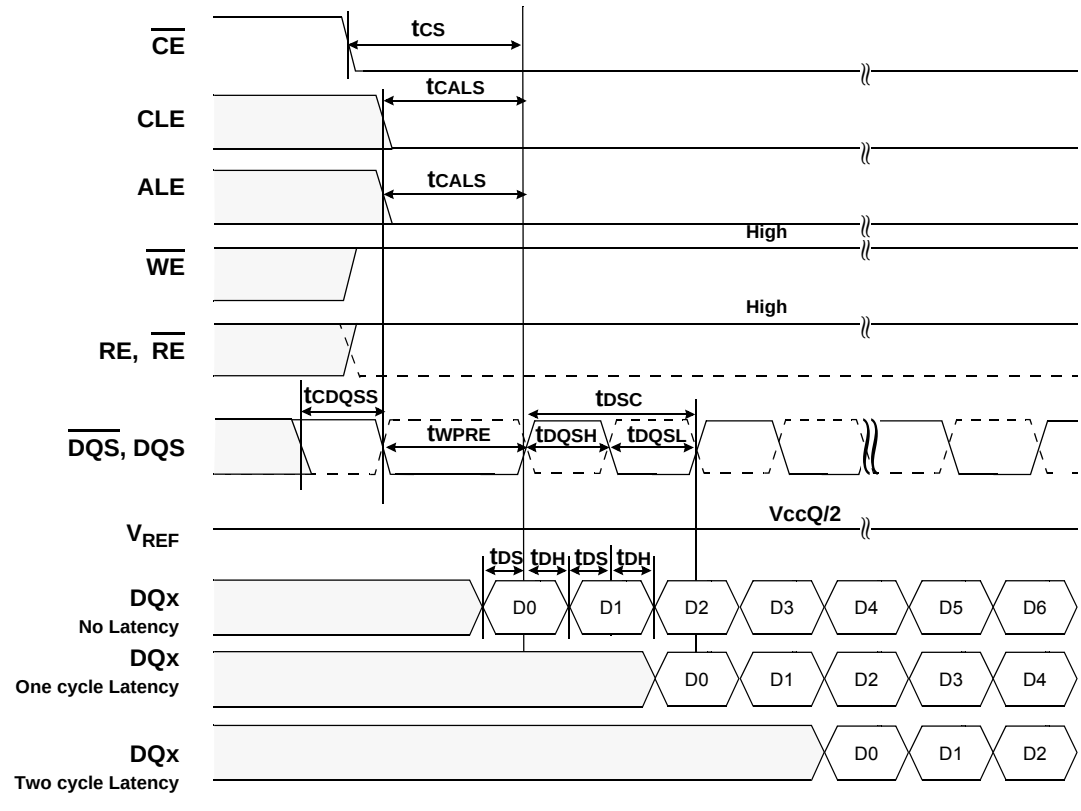
NOTE :
1) P2 and P3 are reserved.
2) P2, P3, N/A, and reserved shall be written with 00h.
3) When differential signaling (i.e. RE and DQS) is used, Vref shall be set to be enabled for DQ.

[Table 30] Definition of Toggle 2.0 specific setting

	Description
Vref	0 : Disabled (dafault) 1 : Endbled
DQS	0 : Disabled (default) 1 : Enabled
RE	0 : Disabled (default) 1 : Enabled
# of Latency DQS Cycle (READ)	0000 : No latency DQS cycle (default) 0001 : One latency DQS cycle 0010 : Two latency DQS cycle
# of Latency DQS Cycle (WRITE)	0000 : No latency DQS cycle (default) 0001 : One latency DQS cycle 0010 : Two latency DQS cycle



[Figure 25] Example of DQS latency(Read)



[Figure 26] Example of DQS latency(Write)

5.2.9.2 Driver strength setting (10h)

Driver strength is configured according to the P0 value.

[Table 31] Definition of Driver strength setting

P0 Value	Description
00h	Driver Multiplier : Underdriver(x0.3)
01h	Driver Multiplier : Underdriver(x0.4)
02h	Driver Multiplier : Underdriver(x0.7)
03h	Reserved
04h	Driver Multiplier : 1 (default)
05h	Reserved
06h	N/A
07h	Reserved
08h	N/A
09h ~ FFh	Reserved

NOTE :
P1, P2 and P3 are reserved and shall be written with 00h.

5.2.9.3 External V_{PP} (30h)

(WARNING : SAMSUNG RECOMMENDS THE USER TO CONTACT AND CONSULT SAMSUNG BEFORE ENABLING THIS FUNCTION. ENABLING THIS FUNCTION MAY CAUSE MALFUNCTION, INCLUDING BUT NOT LIMITED TO PERMENANT DAMAGE TO THE CHIP).
External high voltage(i.e. typical 12V) feature offers power saving on program and read operations. The external high voltage shall be supplied prior to the feature setting and it shall persist within 11V to 13V until it is set to defalut(i.e. off). The maximum external Vpp supply current per LUN is 5mA.

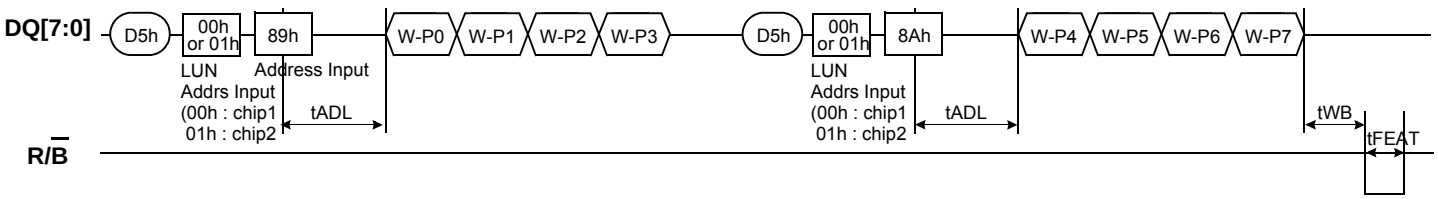
[Table 32] Definition of External Vpp

P0 Value	Description
00h	OFF(default)
01h	ON
02h ~ FFh	Reserved

NOTE :
P1, P2 and P3 are reserved and shall be written with 00h.

5.2.10 Set Feature Operation - LUN control within 1CE

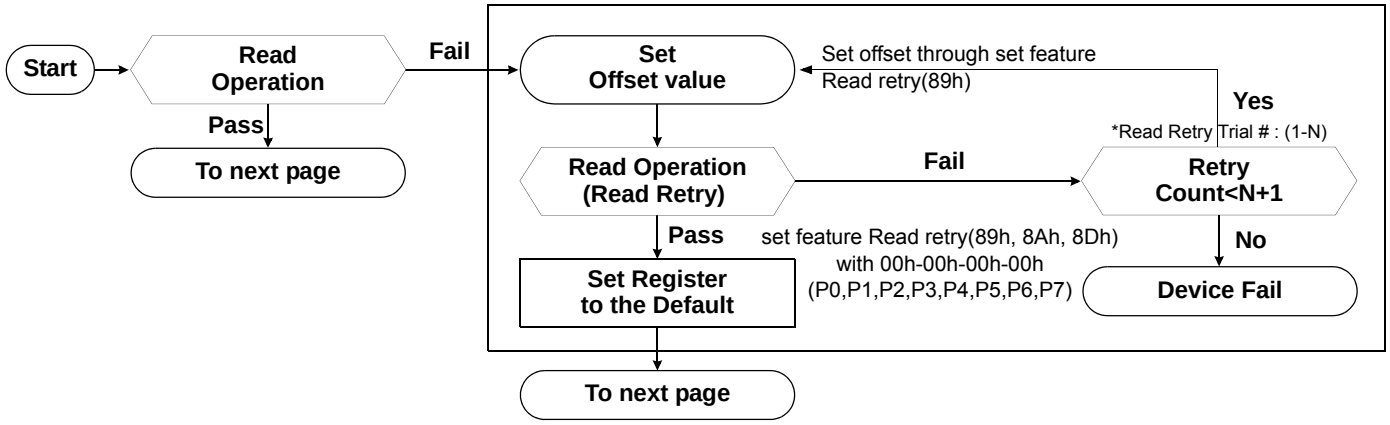
Users may set particular features using 'Set Feature' operation by inputting chip address . Once a feature is set by users, it shall not be changed until the device is powered off or setting is changed by users. Figure 28 defines the Set Features behavior and timings.



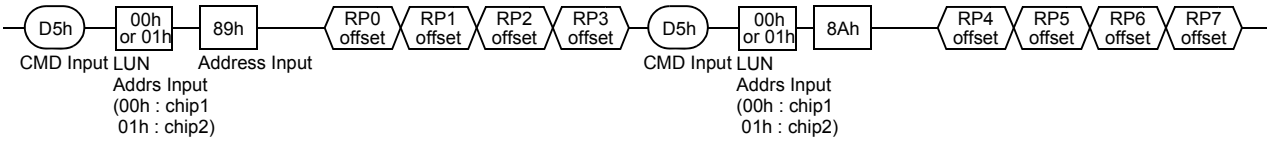
[Figure 27] Set Feature Sequence - UN control within 1CE

5.2.10.1 Read Retry setting (89h, 8Ah, 8Dh)

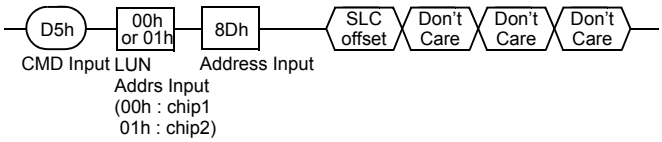
Read Retry feature can relieve fail bit by reading again when read error occurs. If read operation is fail, read level should be set through set feature-read retry (89h). Read operation at read level newly set can relieve fail bit.



[Figure 28] Read Retry sequence



[Figure 29] Set offset value for Read Retry(3bit MLC)



[Figure 30] Set offset value for Read Retry(SLC)

• Description of setting data for Read retry
- P0 value : setting offset data for R1
- P1 value : setting offset data for R2
- P2 value : setting offset data for R3
- P3 value : setting offset data for R4
- P4 value : setting offset data for R5
- P5 value : setting offset data for R6
- P6 value : setting offset data for R7
- P7 value : Don't Care

P0	P1	p2	p3	p4	p5	p6	p7	Description
00h	00h	00h	00h	00h	00h	00h	00h	Read Retry off(default)
P0,P1,P2,P3 ≠ 00h								Read retry Offset setting

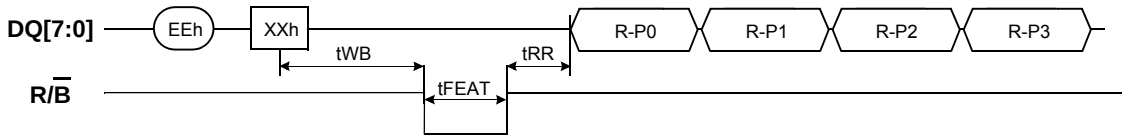
[Table 33] Specific data of Read retry

P0/P1/P2/P3 value	Definition	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
0h	default	0	0	0	0	0	0	0	0
1h	+ΔmV	0	0	0	0	0	0	0	1
2h	+2ΔmV	0	0	0	0	0	0	1	0
3h	+3ΔmV	0	0	0	0	0	0	1	1
4h	+4ΔmV	0	0	0	0	0	1	0	0
:									
:									
FCh	-4ΔmV	1	1	1	1	1	1	0	0
FDh	-3ΔmV	1	1	1	1	1	1	0	1
FEh	-2ΔmV	1	1	1	1	1	1	1	0
FFh	-ΔmV	1	1	1	1	1	1	1	1

5.2.11 Get Feature Operation - Common

Users find how the target is set through 'Get Feature' command. The function shall return the current setting information. If a host starts to read the first byte of data (i.e. P0 value), the host shall complete reading all four bytes of data before issuing another command (including Read Status or Read Status Enhanced). Figure 31 defines the Get Features behavior and timings.

If Read Status (or Read Satus Enhanced) is used to monitor whether the tFEAT time is complete, the host shall issue Read command (i.e. 00h) to read P0-P1-P2-P3.

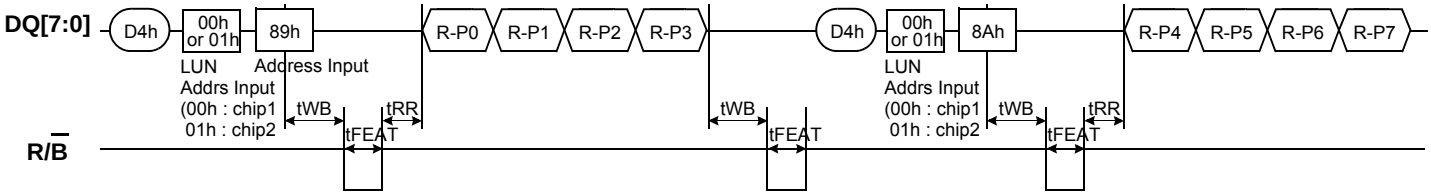


[Figure 31] Get Feature Sequence - Common

5.2.12 Get Feature Operation - LUN control within 1CE

Users find how the target is set through 'Get Feature' command by inputting chip address. The function shall return the current setting information. If a host starts to read the first byte of data (i.e. P0 value), the host shall complete reading all four bytes of data before issuing another command (including Read Status or Read Status Enhanced). Figure 32 defines the Get Features behavior and timings.

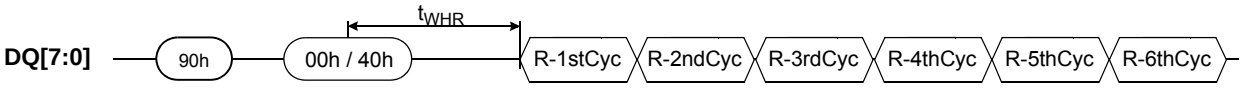
If Read Status (or Read Satus Enhanced) is used to monitor whether the tFEAT time is complete, the host shall issue Read command (i.e. 00h) to read P0-P1-P2-P3.



[Figure 32] Get Feature Sequence - LUN control within 1CE

5.2.13 Read ID Operation

The ID of a target is read by command 90h followed by 00h or 40h address. Read ID operation shall work on lower than 133Mbps. Figure 33 defines Read ID operation behavior and timings.



[Figure 33] Read ID Sequence

5.2.13.1 00h Address ID Definition

Users can read six bytes of ID containing manufacturer code, device code and architecure information of the target by command 90h followed by 00h address. The command register remains in Read ID mode until another command is issued.

5.2.13.1.1 00h Address ID Cycle

Device	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
K9ACGD8S0C	ECh	DEh	B8h	DEh	86h	C5h

[Table 34] 00h Address ID Definition Table

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	Internal Chip Number, Cell Type, Number of Simultaneously Programmed Pages, Etc.
4th Byte	Page Size, Block Size,Redundant Area Size.
5th Byte	Plane Number, ECC Level, Organization.
6th Byte	Device Technology, EDO, Interface.

[Table 35] 3rd ID Data

	Description	DQ7	DQ6	DQ5 DQ4	DQ3 DQ2	DQ1 DQ0
Internal Chip Number	1 2 4 8					0 0 0 1 1 0 1 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell				0 0 0 1 1 0 1 1	
Number of Simultaneously Programmed Pages	1 2 4 3			0 0 0 1 1 0 1 1		
Interleaving operation between multiple chips	Not Support Support		0 1			
Cache Program	Not Support Support	0 1				

[Table 36] 4th ID Data

	Description	DQ7	DQ6	DQ5 DQ4	DQ3	DQ2	DQ1 DQ0
Page Size (w/o redundant area)	Reserved Reserved 8KB 16KB						0 0 0 1 1 0 1 1
Block Size (w/o redundant area)	4.5MB 6MB 512KB 1MB 1.5MB 2MB 3MB 4MB	0 0 0 0 1 1 1 1		0 0 0 1 1 0 1 1 0 0 0 1 1 0 1 1			
Spare area size	768KB 896KB 1792B 2KB Reserved 512B 640B 1KB		0 0 0 0 1 1 1 1		0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	

[Table 37] 5th ID Data

	Description	DQ7	DQ6 DQ5 DQ4	DQ3 DQ2 DQ1	DQ0
Plane number	1 2 3 4 6 8 16			0 0 0 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	
ECC Level	1bit 2bit 4bit 8bit 16bit 24bit 40bit 60bit LDPC	0 0 0 0 0 0 0 0 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1 **0 0 0**		
Reserved					0

[Table 38] 6th ID Data

	Description	DQ7	DQ6	DQ5 DQ4 DQ3	DQ2 DQ1 DQ0
Device Version	50nm 40nm 30nm 2xnm 2ynm 1xnm Reserved Reserved				0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 0
EDO	Not Support Support		0 1		
Interface	Conventional Mode Toggle Mode	0 1			
Reserved				0 0 0	

5.2.13.2 40h Address ID Definition

Toggle DDR NAND also provide a six bytes of JEDEC standard signature ID. Users can read the ID by command 90h followed by 40h address. Any data returned after the six bytes of JEDEC standard signature is considered reserved for future use.

[Table 39] 40h Address ID Cycle

1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
4Ah	45h	44h	45h	43h	02h

[Table 40] 40h Address ID Definition

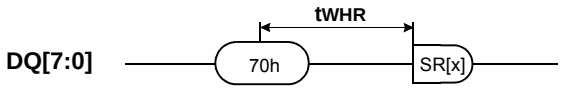
Cycle	Description	IDQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
1st	J	0	1	0	0	1	0	1	0
2nd	E	0	1	0	0	0	1	0	1
3rd	D	0	1	0	0	0	1	0	0
4th	E	0	1	0	0	0	1	0	1
5th	C	0	1	0	0	0	0	1	1
6th	Conventional Asynchronous SDR Toggle DDR	0	0	0	0	0 0	0 0	0 1	1 0

5.2.14 Read Status Operation

In the case of non-Multi-plane operations, the Read Status function retrieves a status value for the last operation issued. If multiple Multi-plane operations are in progress on a single LUN, then Read Status returns the composite status value. Specifically, Read Status shall return the combined status value of the independent status register bits according to Table 41. Figure 34 defines the Read Status behavior and timings.

[Table 41] Read Status Definition

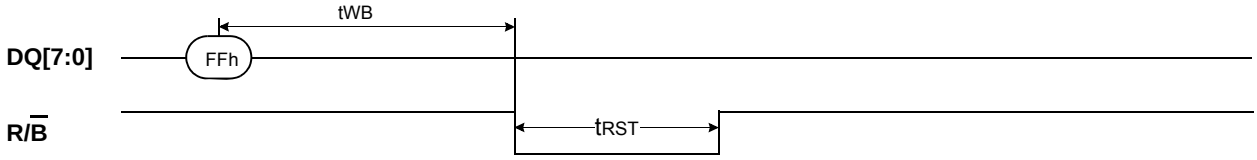
	DQ 0	DQ 1	DQ 2	DQ 3	DQ 4	DQ 5	DQ 6	DQ 7
Definition of value	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Reserved	Reserved	Reserved	Busy : "0" Ready : "1"	Busy : "0" Ready : "1"	Protected : "0" Not Protected : "1"
Block Erase	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Page Program	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Cache Program	Pass/Fail for the current page	Pass/Fail for the previous page	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Busy/Ready for Host	Write Protect
Read	Not Use	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Cache Read	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Busy/Ready for Host	Write Protect



[Figure 34] Read Status Sequence

5.2.15 Reset Operation

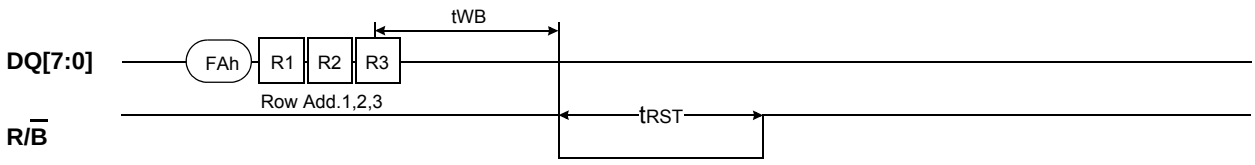
Toggle DDR NAND offers a reset function by command FFh. When the device is in 'Busy' state during any operation, the Reset operation will abort these operations except during power-on when Reset shall not be issued until R/B# is set to one (i.e. ready). The contents of memory cells being programmed are no longer valid, as the data will be partially programmed or erased. Although the device is already in process of reset operation, a new reset command will be accepted. Figure 35 defines the Reset behavior and timings.



[Figure 35] Reset Sequence

5.2.16 Reset LUN operation

A certain LUN within a target can be reset by command FAh followed by row addresses. Row addresses are required to set a LUN to be reset. Figure 36 defines the Reset LUN behavior and timings.



[Figure 36] Single chip Reset Sequence

5.3 Extended Operation

5.3.1 Extended Command Sets

Table 42 defines the Extended Command Sets.

[Table 42] Extended Command Sets

Mode	Function	1st Set	Address Cycles for 1st Set	2nd Set	Address Cycles for 2nd Set	Interleaving Operation Supportablity
Common	Multi-plane Page Read / Multi-plane Page Cache Read	00h--32h	5	00h--30h	5	Y
	Multi-plane Random Cache Read	00h--32h	5	00h--31h	5	
	Multi-plane Random Data Output 1)	00h---05h	5	---E0h	2	
	Multi-plane Block Erase	60h--	3	--D0h	-	Y
	Multi-plane Read for Copy-Back	00h--32h	5	00h--35h	5	Y
	Multi-plane Copy-Back Program2)	85h--11h	5	81h--11h3), 81h--10h4)	5	Y
	Read status enhanced	78h--	3	-	-	Y
TLC	Device Identification Table Read	ECh--	1	-	-	
	Multi-planeTLC Program Confirm	8Bh--11h	5	8Bh--10h	5	Y
	Multi-plane TLC Cache Program Confirm	8Bh--11h	5	8Bh--15h	5	Y
	Page Buffer Latch Dump	C0h	1	-	-	
SLC	Multi-plane Page Program 2)	80h--11h2)	5	81h--11h3), 81h--10h4)	5	Y
	Multi-plane Cache Program2)	80h--11h2)	5	81h--11h3), 81h--15h4)	5	
	SLC Mode Access	DAh	-	-	-	
	SLC Mode Abort	DFh	-	-	-	

NOTE :

1) Multi-plane Random Data out must be used after Multi-plane Page Read or Multi-plane Cache Read operation.

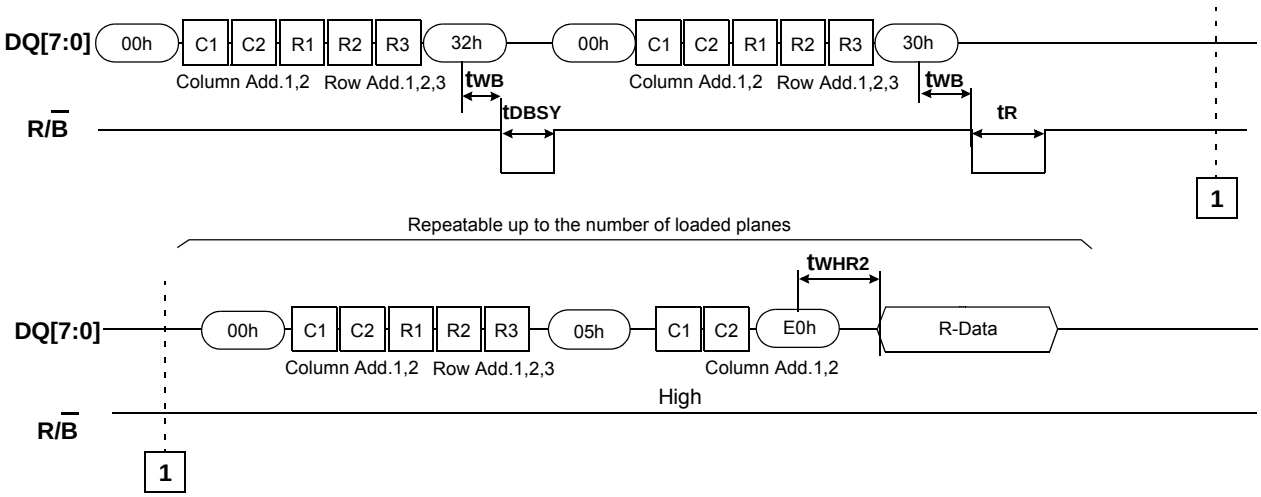
2) Any command between 11h/80h/81h/85h and 32h-00h is prohibited except 70h/78h/FAh and FFh.

3) 81h-11h command is for the 2nd plane program operation for 3-Plane operation.

4) 81h-11h/15h command is for the last plane program operation : the 2nd plane for 2-Plane operation and the 3rd plane for 3- Plane operation.

5.3.2 Multi-plane Page Read Operation

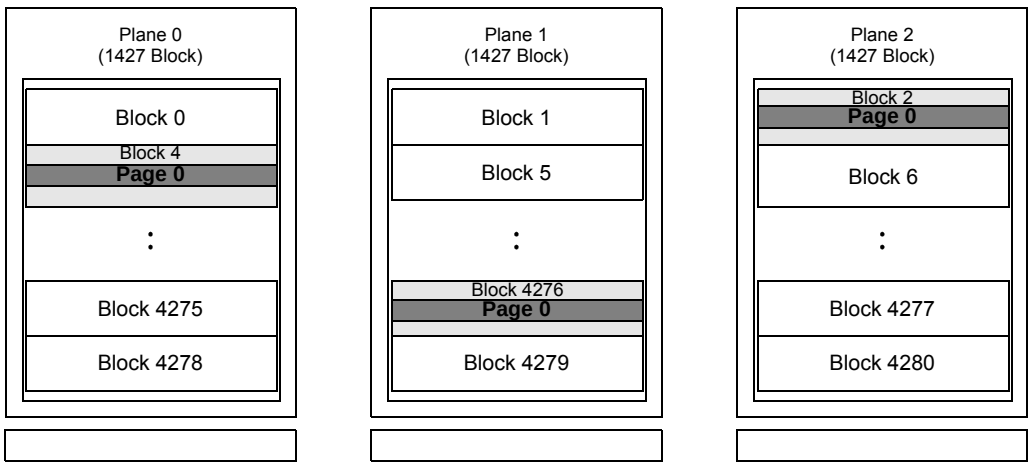
The Multi-plane Page Read operation is an extension of the Page Read operation. The device supporting Multi-plane page read operation also allows multiple Random data-output from each plane(i.e. Multi-plane Random Data Output) once multi-pages from each plane are loaded to page registers. With the primary command, R/$\overline{B}$ returns to ready in a short time(i.e. tDBSY) after the first command 32h since it does not load data from a selected page, and the selected page data of each plane are transferred to the cache registers via page registers in less than tR after command 30h. When setting page addresses of each plane, the page addresses shall be identical although block addresses differ.
The Multi-plane addresses shall be set in a consecutive manner from a lower address plane to a higher address plane and the same plane address shall not be set twice within a set of address setting sequence for the Multi-plane Page Read Operation. Starting plane address shall be plane0 and plane1. Once the data is loaded into the cache registers, the data on the second and third planes can be read out by issuing the Multi-plane Random Data Output command. The data on the other plane can be also read out using the identical command sequences. Figure 37 and Figure 33 define Multi-plane Page Read and Multi-plane Random Data Output behavior and timings. Page Read out is only possible when the 3rd page program of Multi-plane operation.



[Figure 37] Example Sequence with Multi-plane Page Read

5.3.3 Unaligned Multi-plane operation

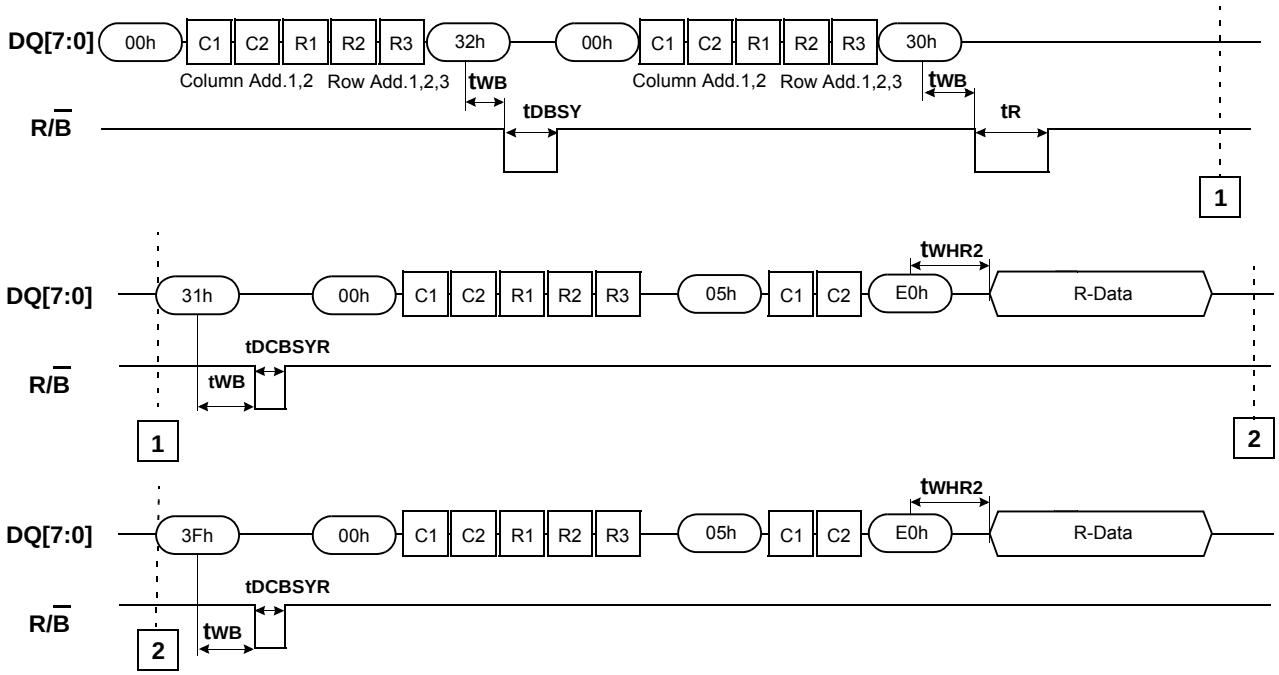
Multi-page Read / Program operation is supported in unaligned block addresses, as long as page addresses are same in all planes.



[Figure 38] Example of Unaligned Multi-plane Operation

5.3.4 Multi-Plane Sequential Cache Read Operation

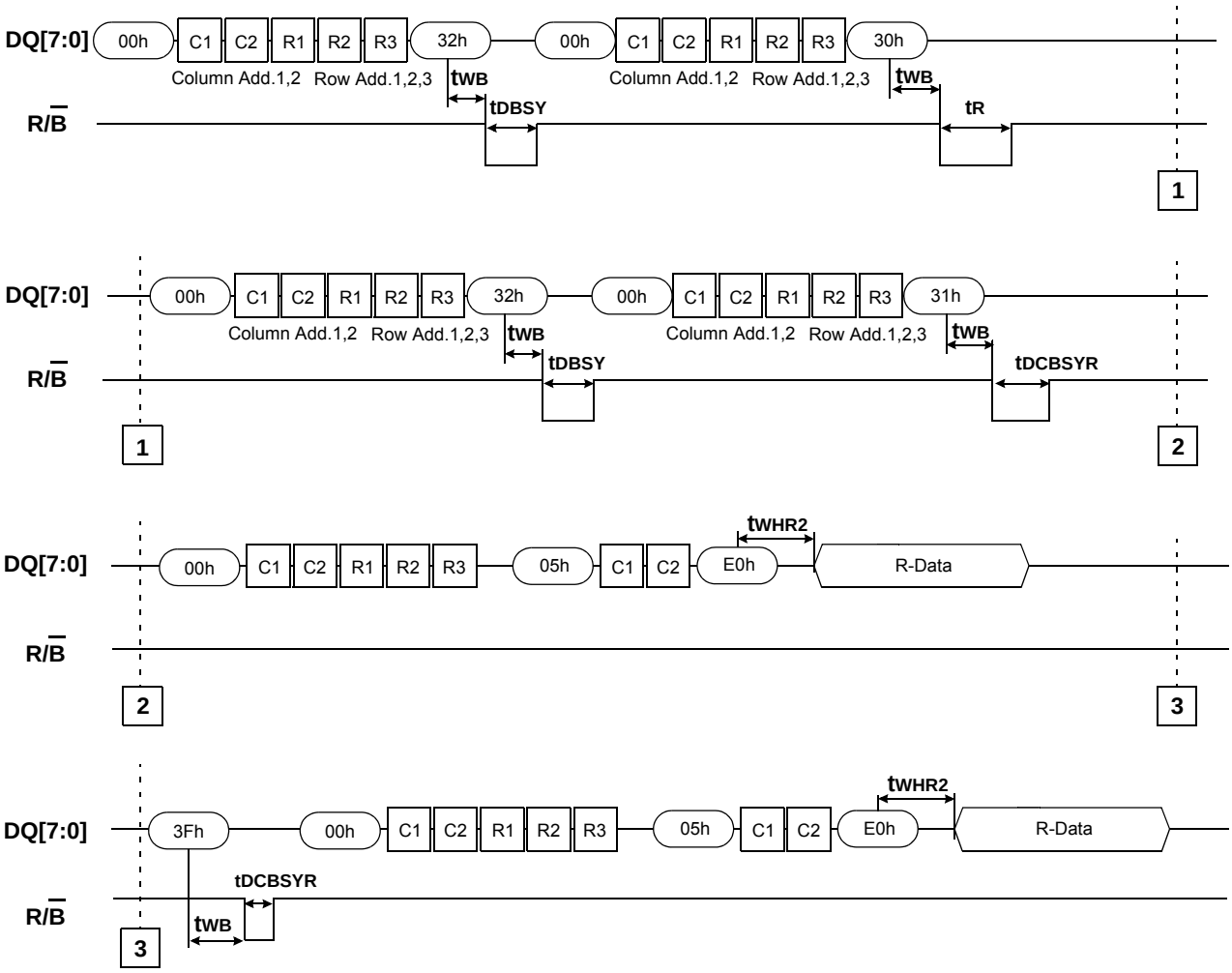
Multi-Plane Sequential Cache Read operation provides fast sequential read function after the initial Multi-Plane Read operation is set. Once Multi-Plane Read operation performs, next page data of each plane can be loaded to page register by command 31h without additional address setting while a host reads data, which is loaded by Multi-Plane Read operation, from cache registers. Since the next page data is loaded to page registers during host read-out period, R/$\overline{B}$ turns to high (i.e. ready) in a short time after command 31h although data loading by command 31h is being performed internally. If the previous data is still being loaded after command 31h, R/$\overline{B}$ busy state may take as long as tR, hence the maximum time of tDCBSYR is identical to tR. To check internal cache operation progress, ready/busy for Flash array (i.e. SR[5]) from READ STATUS or READ STATUS ENHANCED table shall be referenced. During 'busy for Flash array' period, illegal commands which is not related to Multi-Plane Sequential Cache Read operation except RESET and READ STATUS commands are prohibited. At the last page, command 3Fh shall be issued to transfer data from page registers to cache registers.
The multi-plane addresses shall be set in a consecutive manner from a lower address plane to a higher address plane and the same plane address shall not be set twice within a set of address setting sequence for the Multi-Plane Sequential Cache Read Operation. Starting plane address shall be plane0 and Plane1. Figure 39 and Figure 36 defines Multi-Plane Sequential Cache Read behavior and timings.



[Figure 39] Example Sequence with Multi-plane Cache Read

5.3.5 Multi-Plane Random Cache Read

Multi-Plane Random Cache Read function requires multiple address setting ahead of command 31h to load data of particular pages. Since the selected pages are loaded to page register while a host read data from cache register where previous data is loaded, R/B returns high (i.e. ready) in a short time unless the previous data is still being loaded. To check internal cache operation progress, ready/busy for Flash array (i.e. SR[5]) from READ STATUS or READ STATUS ENHANCED table shall be referenced. During 'busy for Flash array' period, illegal commands which is not related to Multi-Plane Random Cache Read operation except RESET and READ STATUS commands are prohibited.
The multi-plane addresses shall be set in a consecutive manner from a lower address plane to a higher address plane and the same plane address shall not be set twice within a set of address setting sequence for the Multi-plane Sequential Cache Read Operation. Starting plane address shall be plane0 and Plane1. The activated planes for the first Multi-Plane Random Cache Read shall be kept using in the next address sequence until the Multi-Plane Random Cache operation is completed by command 3Fh. Figure 40 defines Multi-Plane Random Cache Read behavior and timings

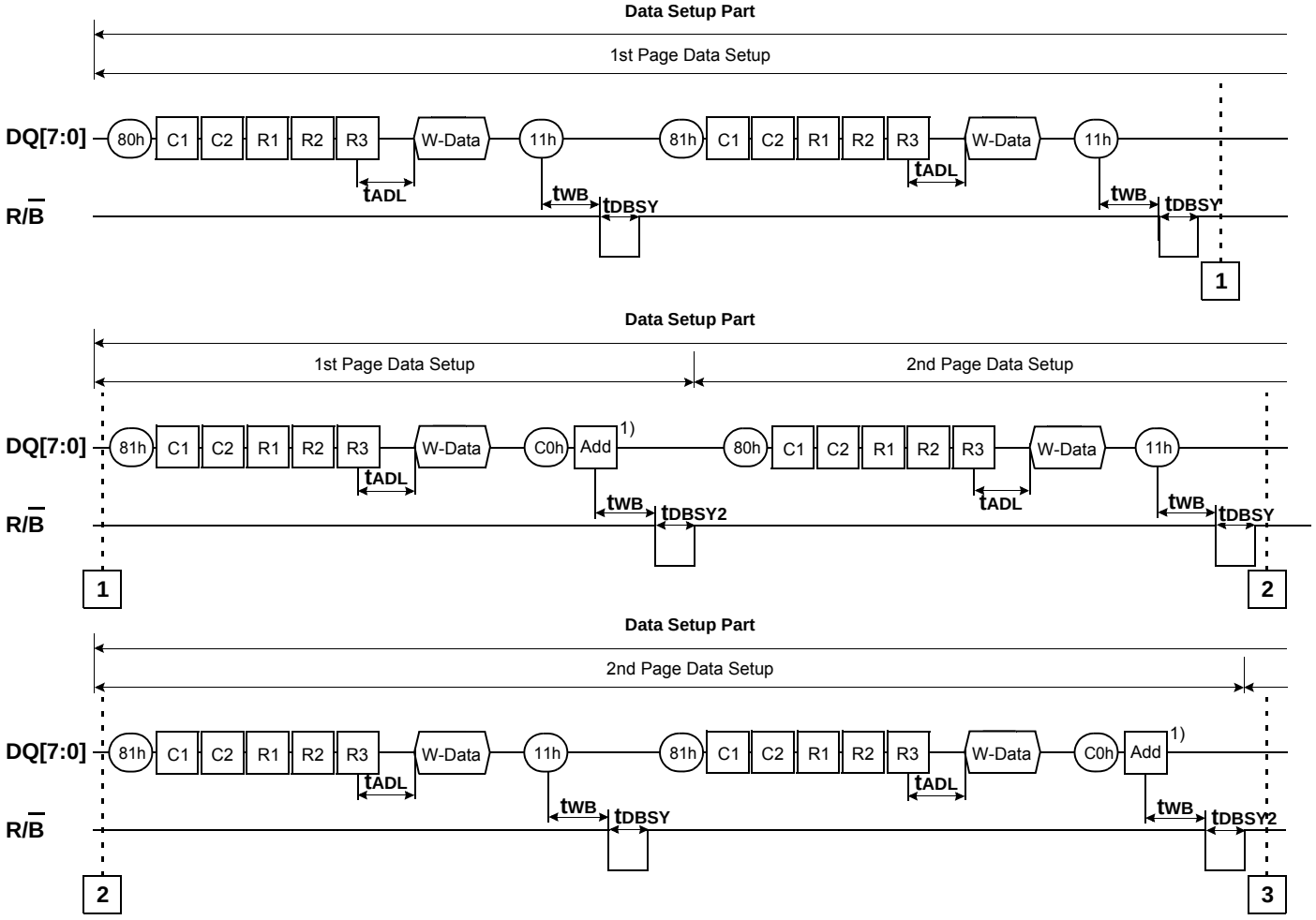


[Figure 40] Example Sequence with Multi-plane Cache Read

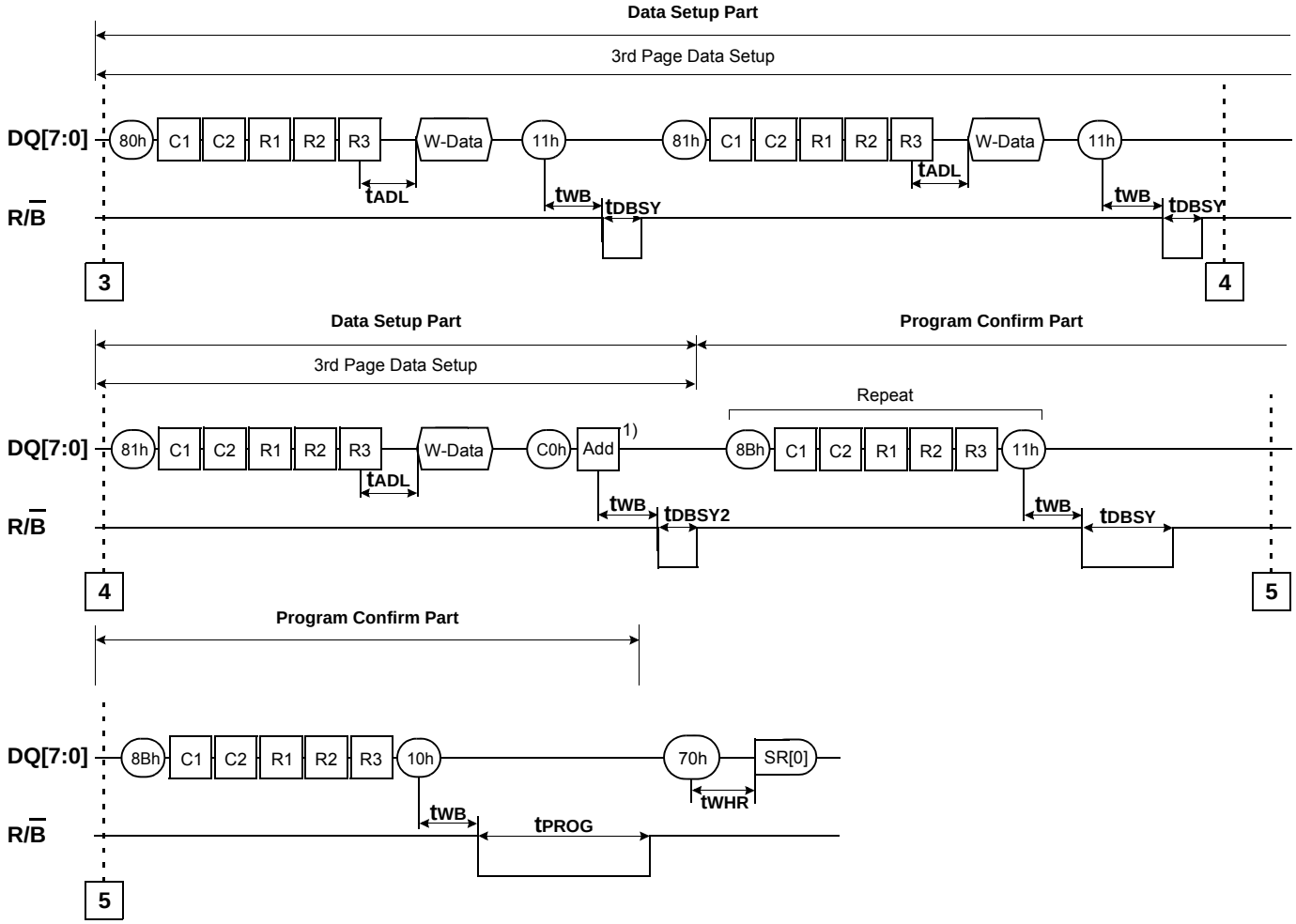
5.3.6 Multi-Plane Page Program Operation(1/2)

Multi-plane Page Program function extends an effective programmable page size using multiple planes.
When a host moves on a plane for loading another data, 81h--11h command set shall be used for the 2nd planes in 3-plane page program operation. At the last page loading, 8Bh--10h command set shall be used. After command 10h, all loaded data in each plane starts to be programmed to Flash array simultaneously.
The Multi-Plane addresses shall be set in a consecutive manner from a lower address plane to a higher address plane and the same plane address shall not be set twice within a set of address setting sequence for the Multi-Plane Page Program Operation. Starting plane address shall be plane0 and Plane1.
3bit/cell NAND has the following programming characteristics. The fine programming to one WL consists of 3 steps of program operation. 3 pages' data, LSB, CSB and MSB, has to be stored for each program operation to make 8 program states at the same time.

Each programming step has its own program order address which is not same as physical page address. The following is the program order address to minimize the coupling. The Program operation shall be followed in below sequence. 1st Program operation at WL0 -> 1st Program operation at WL1 -> 1st Program operation at WL2 ->3rd Program operation at WL1 -> 1st Program operation at WL4 -> 1st Program operation at WL5 etc.The programmed data of each page can be read out only if 3rd program is completed. Figure 41 defines Multi-Plane Page Program behavior and timings.



5.3.7 Multi-Plane Page Program Operation(2/2)

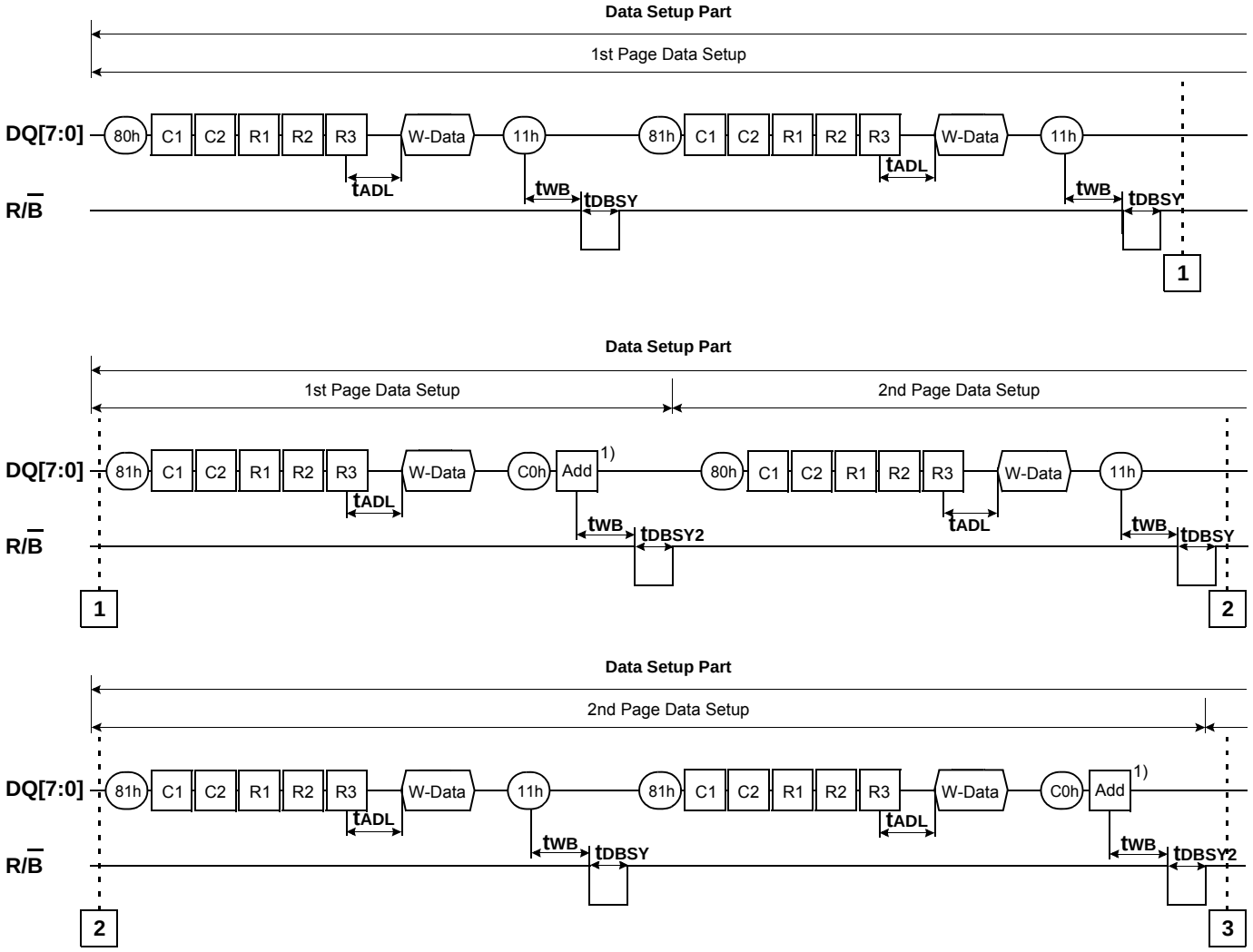


[Figure 41] Example Sequence with Multi-plane Page Program

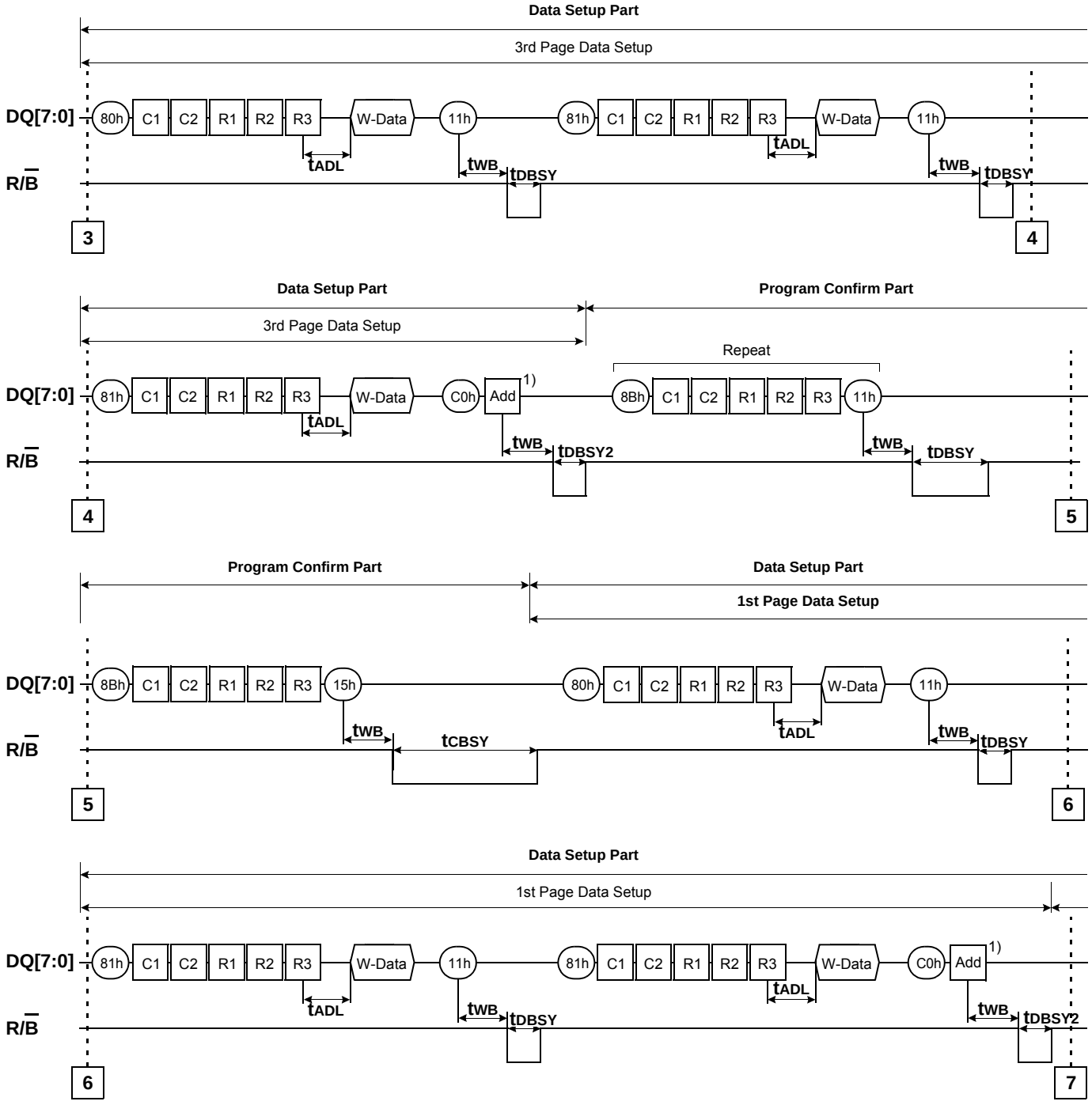
NOTE :
1) For address followed by C0h command, refer to the buffer address Table 23

5.3.8 Multi-Plane Cache Program Operation(1/3)

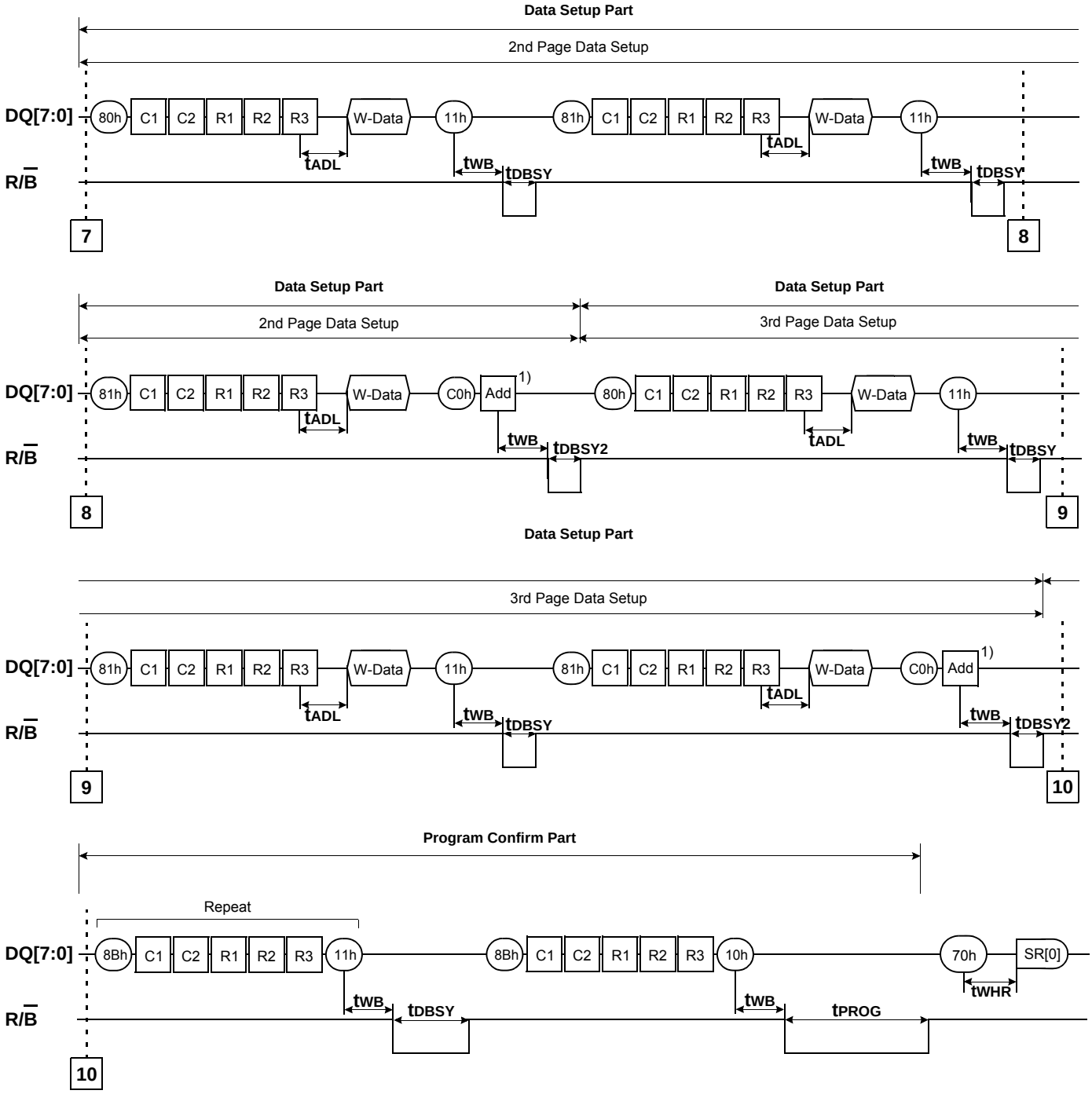
The Multi-Plane Cache Program is an extension of the Cache Program. 81h-11h command set is required for the 2nd planes in 3-Plane Cache Program Operation. 8Bh-15h command set is needed for the last plane in Multi-Plane Cache Program operaton. After command 15h, R/$\overline{B}$ returns high once transferring data from cache register to page register is completed. Internal program operation is in progress after R/$\overline{B}$ returns while other pages is loaded by a host. To check internal cache operation progress, ready/busy for Flash array (i.e. SR[5]) from READ STATUS or READ STATUS ENHANCED table shall be referenced. During 'busy for Flash array' period, illegal commands which is not related to Multi-Plane Cache Program operation except RESET and READ STATUS commands are prohibited. At the last page loading for the entire Multi-Plane Cache Program, command 10h is required to finalize the operation and R/$\overline{B}$ stays busy as long as tPROG.
The multi-plane addresses shall be set in a consecutive manner from a lower address plane to a higher address plane and the same plane address shall not be set twice within a set of address setting sequence for the Multi-Plane Cache Program Operation. Starting plane address shall be plane0 and plane1. The activated planes for the first Multi-Plane Cache Program shall be kept using in the next address sequence until the Multi-Plane Cache Program operation is completed by command 10h. Figure 42 defines Multi-Plane Cache Page Program behavior and timings.



5.3.9 Multi-Plane Cache Program Operation(2/3)



5.3.10 Multi-Plane Cache Program Operation(3/3)

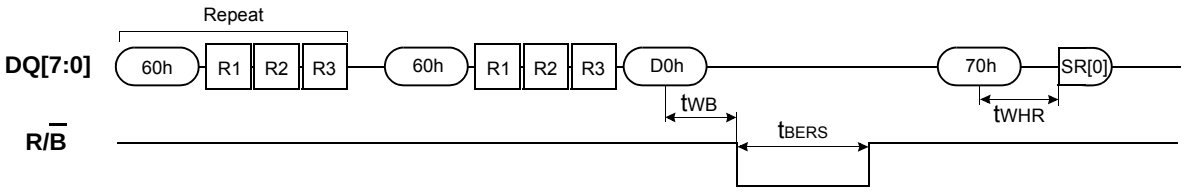


[Figure 42] Example Sequence with Multi-plane Cache Program

NOTE :
1) For address followed by C0h command, refer to the buffer address Table 23
2) tDBSY2' = tCBSY(Dummy Busy time for Cache Program) + tDBSY2

5.3.11 Multi-Plane Block Erase Operation

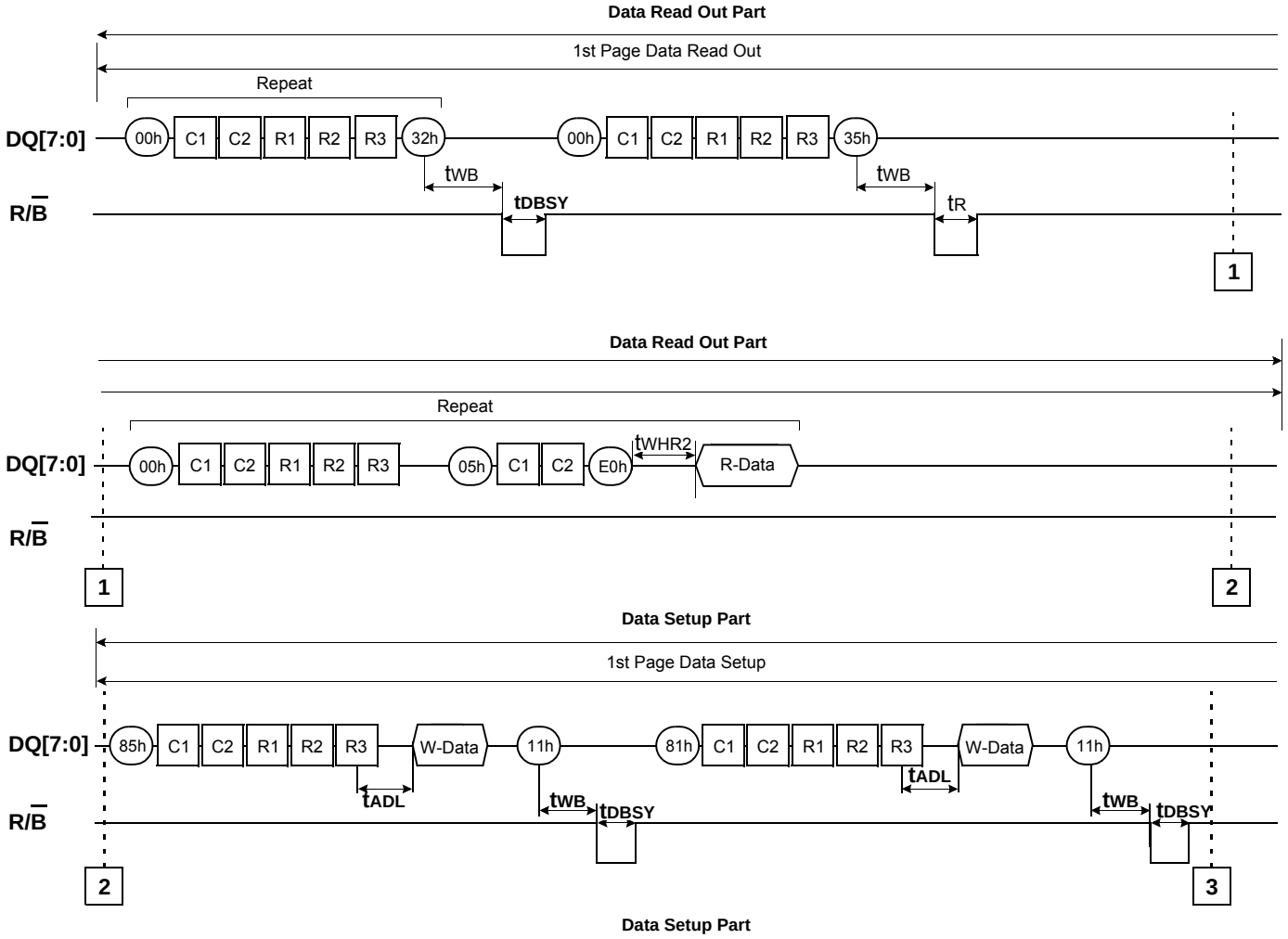
Multi-Plane Block Erase allows users to erase multiple blocks comprising a block of each plane simultaneously.
The Multi-Plane addresses shall be set in a consecutive manner from a lower address plane to a higher address plane and the same plane address shall not be set twice within a set of address setting sequence for the Multi-Plane Block Erase Operation. Starting plane address shall be plane0 and plane1.
Figure 43 defines Multi-Plane Block Erase behavior and timings.



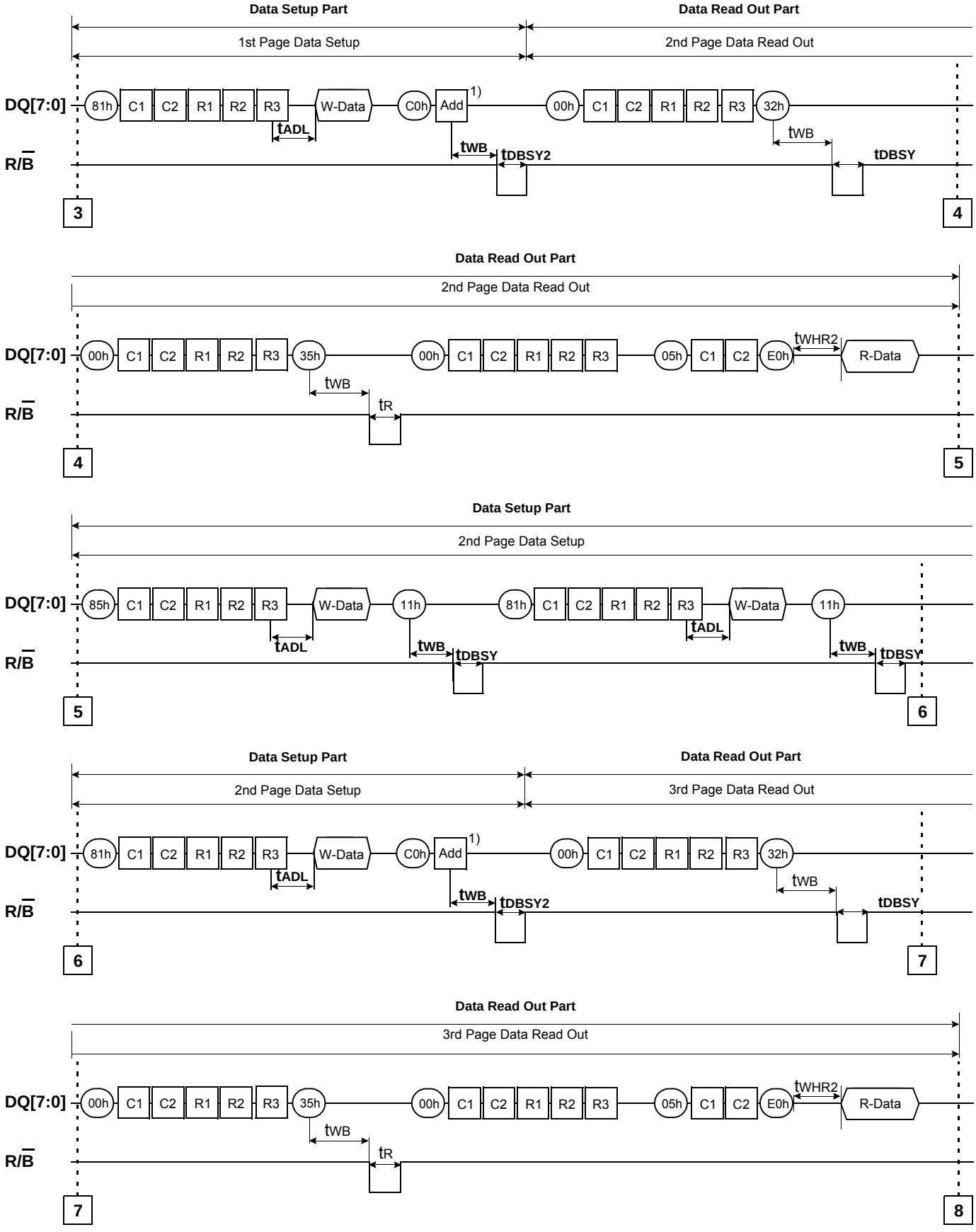
[Figure 43] Example Sequence with Multi-plane Block Erase

5.3.12 Multi-Plane Copy-Back Program Operation(1/3)

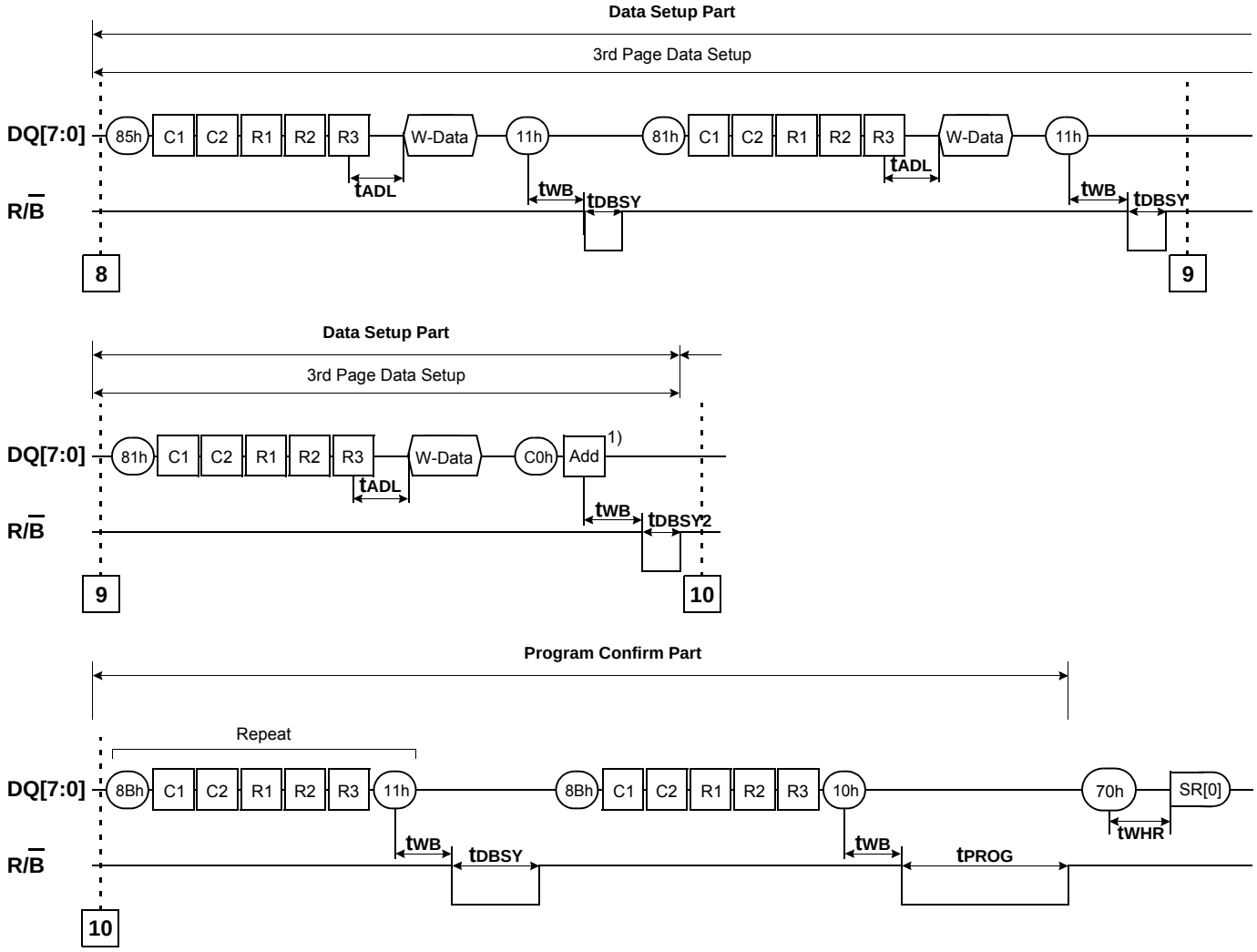
The Multi-Plane Copy-Back Program is an extension of the Copy-back Program. Multi-Plane Copy-Back Program operation is executed multi sets of commands, Multi-Plane Read for Copy-Back and Multi-Plane Copy-Back Program.
The Multi-plane addresses shall be set in a consecutive manner from a lower address plane to a higher address plane and the same plane address shall not be set twice within a set of address setting sequence for the Multi-Plane Copy-Back Program Operation. Starting plane address shall be plane0 and plane1.The read Data shall be copied back to a page in the same plane. Figure 44 and Figure 40 defines Multi-Plane Copy-Back Program behavior and timings.



5.3.13 Multi-Plane Copy-Back Program Operation(2/3)



5.3.14 Multi-Plane Copy-Back Program Operation(3/3)



[Figure 44] Example Sequence with Multi-plane Copy-Back Program

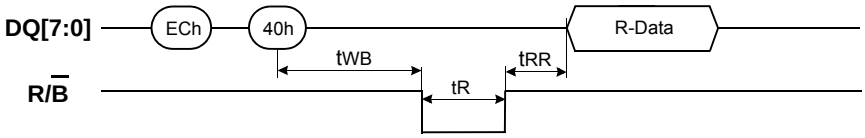
NOTE :
1) For address followed by C0h command, refer to the buffer address Table 23

5.3.15 Device Identification Table Read Operation

The device shall return a JEDEC standard formatted parameter page during the data out phase of the READ PARAMETER PAGE command when address 40h is inputted. The READ PARAMETER PAGE command is a ECh value for the command cycle and a 40h value for the address cycle, and the bytes of the parameter page are returned in the data output (DOUT) cycles.

After the command ECh address 40h is received by the NAND device, it will go busy for a period of time (tR in the figure) after which, the parameter page can be read from the device. The length and contents of the parameter page is to be determined. The timing associated with the bus cycles for the READ PARAMETER PAGE command is defined elsewhere in the JEDEC standard.

The READ ID command is used by the controller to identify the device that is attached. This command is used by the controller to gather information about the target flash device. Figure 45 defines the behavior and timings.



[Figure 45] Device Identification Table Read Sequence

5.3.15.1 Device Identification Table Definition

Table 43 defines the parameter page data structure. For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte.
Values are reported in the parameter page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the target will return how many data bytes are in a page.
All optional parameters that are not implemented shall be cleared to 00h by the target.

[Table 43] Parameter Page Definitions

Byte	O/M	Description
Revision information and features block		
0-3	M	Parameter page signature Byte 0: “J” (= 4Ah) Byte 1: “E” (= 45h) Byte 2: “S” (= 53h) Byte 3: “D” (= 44h)
4-5	M	Revision number 2-15: Reserved (0) 1: 1 = supports revision 1.0 0: Reserved (0)
6-7	M	Features supported 0-15 Reserved (0) <To be defined based on feature discussions.>
8-10	M	Optional commands supported 0-23: Reserved (0) <To be defined based on command set discussions.>
11-31		Reserved (0)
Manufacturer information block		
32-43	M	Device manufacturer (12 ASCII characters)
44-63	M	Device model (20 ASCII characters)
64-69	M	JEDEC manufacturer ID (6 bytes)
70-71	TBD	TBD
72-79		Reserved (0)
Memory organization block		
80-83	M	Number of data bytes per page
84-85	M	Number of spare bytes per page
86-89	M	Number of data bytes per partial page
90-91	M	Number of spare bytes per partial page
92-95	M	Number of pages per block
96-99	M	Number of blocks per logical unit (LUN)
100	M	Number of logical units (LUNs)
TBD-TBD	TBD	TBD
Memory organization block		
101	M	Number of address cycles 4-7: Column address cycles 0-3: Row address cycles
102	M	Number of bits per cell
103	M	Number of programs per page
104	M	Multi-Plane addressing 4-7: Reserved (0) 0-3: Number of plane address bits
105	M	Multi-Plane operation attributes 3-7: Reserved (0) 2: Address restrictions for cache operations 1: 1= read cache supported 0: 1 = program cache supported
106-143		Reserved (0)
Electrical parameters block		

144-145	O	0-15: Reserved (0)
146-147	O	Toggle DDR speed grade 8-15: Reserved (0) 7: 1 = supports 5 ns speed grade (~200 MHz) 6: 1 = supports 6 ns speed grade (~166 MHz) 5: 1 = supports 7.5 ns speed grade (~133 MHz) 4: 1 = supports 10 ns speed grade (~100 MHz) 3: 1 = supports 12 ns speed grade (~83 MHz) 2: 1 = supports 15 ns speed grade (~66 MHz) 1: 1 = supports 25 ns speed grade (40 MHz) 0: 1 = supports 30 ns speed grade (~33 MHz)
148-149	O	0-15: Reserved (0)
150	O	0-7: Reserved (0)
151	O	Toggle DDR features 0-7: Reserved (0)
152	O	0-7: Reserved (0)
153-154	M	tPROG Maximum page program time (µs)
155-156	M	tBERS Maximum block erase time (µs)
157-158	M	tR Maximum page read time (µs)
159-160	O	tR Maximum Multi-Plane page read time (µs)
161-162	O	tCCS Minimum change column setup time (ns)
163-164	M	I/O pin capacitance, typical
165-166	M	Input pin capacitance, typical
167-168	O	Reserved
169	M	Driver strength support 3-7: Reserved (0) 2: 1 = supports Overdrive 2 driver strength 1: 1 = supports Overdrive 1 driver strength 0: 1 = supports driver strength settings
170-207		Reserved (0)
ECC and endurance block		
208	M	Guaranteed valid blocks at beginning of target
209-210	M	Block endurance for guaranteed valid blocks
211-218	M	ECC and endurance information block 0 Byte 211: Number of bits ECC correctability Byte 212: Codeword size Byte 213-214: Bad blocks maximum per LUN Byte 215-216: Block endurance Byte 217-218: Reserved (0)
219-226	O	ECC and endurance information block 1 Byte 219: Number of bits ECC correctability Byte 220: Codeword size Byte 221-222: Bad blocks maximum per LUN Byte 223-224: Block endurance Byte 225-226: Reserved (0)
227-234	O	ECC and endurance information block 2 Byte 227: Number of bits ECC correctability Byte 228: Codeword size Byte 229-230: Bad blocks maximum per LUN Byte 231-232: Block endurance Byte 233-234: Reserved (0)
235-242	O	ECC and endurance information block 3 Byte 235: Number of bits ECC correctability Byte 236: Codeword size Byte 237-238: Bad blocks maximum per LUN Byte 239-240: Block endurance Byte 241-242: Reserved (0)
243-271	Reserved (0)	
Reserved		
272-419		Reserved (0)

Vendor specific block		
420-421	M	Vendor specific Revision number
422-509		Vendor specific
CRC for Parameter Page		
510-511	M	Integrity CRC
Redundant Parameter Pages		
512-1023		Value of bytes 0-511
1024-1535		Value of bytes 0-511
1536+		Additional redundant parameter pages

Byte 0-3: Parameter page signature
This field contains the parameter page signature.
When two or more bytes of the signature are valid, then it denotes that a valid copy of the parameter page is present.

Byte 0 shall be set to 4Ah.
Byte 1 shall be set to 45h.
Byte 2 shall be set to 53h.
Byte 3 shall be set to 44h.

Byte 4-5: Revision number
This field indicates the revisions of the standard that the target complies to.
The target may support multiple revisions of the standard.
This is a bit field where each defined bit corresponds to a particular specification revision that the target may support.

Bit 0 shall be cleared to zero.
Bit 1 when set to one indicates that the target supports revision 1.0.
Bits 2-15 are reserved and shall be cleared to zero.

Byte 6-7: Features supported
This field indicates the optional features that the target supports.

<TBD based on feature discussions.>

Byte 8-10: Optional commands supported
This field indicates the optional commands that the target supports.

<TBD based on command discussions.>

Byte 32-43: Device manufacturer
This field contains the manufacturer of the device.
The content of this field is an ASCII character string of twelve bytes.
The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

There is no standard for how the manufacturer represents their name in the ASCII string.
If the host requires use of a standard manufacturer ID, it should use the JEDEC manufacturer ID.

Byte 44-63: Device model
This field contains the model number of the device.
The content of this field is an ASCII character string of twenty bytes.
The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

Byte 64-69: JEDEC manufacturer ID
This field contains the JEDEC manufacturer ID for the manufacturer of the device.

Byte 70-71: TBD

Byte 80-83: Number of data bytes per page
This field contains the number of data bytes per page.
The value reported in this field shall be a power of two.
The minimum value that shall be reported is 512 bytes.

Byte 84-85: Number of spare bytes per page
This field contains the number of spare bytes per page. There are no restrictions on the value.

<TBD: Recommendations should be developed based on ECC strength needed.>

Byte 86-89: Number of data bytes per partial page
This field contains the number of data bytes per partial page.
The value reported in this field shall be a power of two.
The minimum value that shall be reported is 512 bytes.

Byte 90-91: Number of spare bytes per partial page
This field contains the number of spare bytes per partial page.
There are no restrictions on the value.

Byte 92-95: Number of pages per block
This field contains the number of pages per block.

<TBD: Should reference address format.>

Byte 96-99: Number of blocks per logical unit
This field contains the number of blocks per logical unit.
There are no restrictions on this value.

<TBD: Should reference address format.>

Byte 100: Number of logical units (LUNs)
This field indicates the number of logical units the target supports.
Logical unit numbers are sequential, beginning with a LUN address of 0.
This field shall be greater than zero.

<TBD: Should reference address format.>

Byte 101: Number of Address Cycles
This field indicates the number of address cycles used for row and column addresses.
The reported number of address cycles shall be used by the host in operations that require row and/or column addresses (e.g. Page Program).

Bits 0-3 indicate the number of address cycles used for the row address. This field shall be greater than zero.
Bits 4-7 indicate the number of address cycles used for the column address. This field shall be greater than zero.

NOTE :
Throughout this standard examples are shown with 2-byte column addresses and 3-byte row addresses. However, the host is responsible for providing the number of column and row address cycles in each of these sequences based on the values in this field.

Byte 102: Number of bits per cell
This field indicates the number of bits per cell in the Flash array.
This field shall be greater than zero.

Byte 103: Number of programs per page
This field indicates the maximum number of times a portion of a page may be programmed without an erase operation.
After the number of programming operations specified have been performed, the host shall issue an erase operation to that block before further program operations to the affected page.
This field shall be greater than zero.

Byte 104: Multi-Plane addressing
This field describes parameters for Multi-Plane addressing.
Bits 0-3 indicate the number of bits that are used for plane addresses.
This value shall be greater than 0h when Multi-Plane operations are supported.
Bits 4-7 are reserved.

Byte 105: Multi-Plane operation attributes
This field describes attributes for Multi-plane operations.
This byte is mandatory when Multi-plane operations are supported as indicated in the Features supported field.

Bit 0 indicates whether program cache is supported with Multi-plane programs.
If set to one then program cache is supported for Multi-plane program operations.
If cleared to zero then program cache is not supported for Multi-plane program operations.
Note that program cache shall not be used with Multi-plane copyback program operations.
See bit 2 for restrictions on the plane addresses that may be used.

Bit 1 indicates whether read cache is supported with Multi-plane reads.
If set to one then read cache is supported for Multi-plane read operations.
If cleared to zero then read cache is not supported for Multi-plane read operations.
Note that read cache shall not be used with Multi-plane copyback read operations.

Bit 2 indicates whether plane addresses may change during afafa:
a) a program cache sequence between 15h commands, or b) a read cache sequence between 31h commands.
If set to one and bit 0 is set to one, then the host may change the number and value of plane addresses in the program cache sequence.
If set to one and bit 1 is set to one, then the host may change the number and value of plane addresses in the read cache sequence.
If cleared to zero and bit 0 is set to one, then for each program cache operation the plane addresses and number of plane addresses issued to the LUN shall be the same.
If cleared to zero and bit 1 is set to one, then for each read cache operation the plane addresses and number of plane addresses issued to the LUN shall be the same.
Bits 3-7 are reserved.

Byte 144-145: Reserved.

Byte 146-147: Toggle DDR speed grade
This field indicates the Toggle DDR speed grades supported. The target shall support an inclusive range of speed grades.

Bit 0 when set to one indicates that the target supports the 30 ns speed grade (~33 MHz).
Bit 1 when set to one indicates that the target supports the 25 ns speed grade (40 MHz).
Bit 2 when set to one indicates that the target supports the 15 ns speed grade (~66 MHz).
Bit 3 when set to one indicates that the target supports the 12 ns speed grade (~83 MHz).
Bit 4 when set to one indicates that the target supports the 10 ns speed grade (~100 MHz).
Bit 5 when set to one indicates that the target supports the 7.5 ns speed grade (~133 MHz).
Bit 6 when set to one indicates that the target supports the 6 ns speed grade (~166 MHz).
Bit 7 when set to one indicates that the target supports the 5 ns speed grade (~200 MHz).
Bits 8-15 are reserved and shall be cleared to zero.

Byte 148-149: Reserved

Byte 150: Reserved

Byte 151: Toggle DDR features
This field describes features and attributes for Toggle DDR operation.
This byte is mandatory when the Toggle DDR data interface is supported.
Bits 0-7 are reserved.

Byte 152: Reserved

Byte 153-154: Maximum page program time
This field indicates the maximum page program time (tPROG) in microseconds.

Byte 155-156: Maximum block erase time
This field indicates the maximum block erase time (tBERS) in microseconds.

Byte 157-158: Maximum page read time
This field indicates the maximum page read time (tR) in microseconds.

Byte 159-160: Maximum multi-plane page read time
This field indicates the maximum page read time (tR) for multi-plane page reads in microseconds.
Multi-plane page read times may be longer than single page read times.
This field shall be supported if the target supports multi-plane reads as indicated in the Features supported field.

Byte 161-162: Minimum change column setup time.
This field indicates the minimum change column setup time (tCCS) in nanoseconds.
This parameter is used for the asynchronous SDR and synchronous DDR data interfaces.

After issuing a Change Read Column command, the host shall not read data until a minimum of tCCS time has elapsed.
After issuing a Change Write Column command including all column address cycles, the host shall not write data until a minimum of tCCS time has elapsed.
The value of tCCS shall always be longer than or equal to tWHR and tADL when the Toggle DDR or synchronous DDR data interface is supported.

Byte 163-164: I/O pin capacitance, typical
This field indicates the typical I/O pin capacitance for the target. This field is specified in 0.1 pF units.
For example, a value of 31 corresponds to 3.1 pF.
The variance from this value is less than +/- 0.5 pF per LUN. As an example, if two LUNs are present than the total variance is less than +/- 1 pF.

Byte 165-166: Input pin capacitance, typical
This field indicates the typical input pin capacitance for the target.
This value applies to all inputs except the following: $\overline{CE}$ and $\overline{WP}$ signals.
This field is specified in 0.1 pF units. For example, a value of 31 corresponds to 3.1 pF.
The variance from this value is less than +/- 0.5 pF per LUN.
As an example, if two LUNs are present than the total variance is less than +/- 1 pF.

Byte 167-168: Reserved

Byte 169: Driver strength support
This field describes if the target supports configurable driver strengths and its associated features.

Bit 0 when set to one indicates that the target supports configurable driver strength settings as defined in Table TBD.
If this bit is set to one, then the device shall support both the Nominal and Underdrive settings.
If this bit is set to one, then the device shall power-on with a driver strength at the Nominal value defined in Table TBD.

If this bit is cleared to zero, then the driver strength at power-on is undefined.
This bit shall be set to one for devices that support the synchronous DDR or Toggle DDR data interface.

Bit 1 when set to one indicates that the target supports the Overdrive 1 setting in Table TBD for use in the I/O Driver Strength setting.
This bit shall be set to one for devices that support the synchronous DDR or Toggle DDR data interface.

Bit 2 when set to one indicates that the target supports the Overdrive 2 setting in Table TBD for use in the I/O Driver Strength setting.
This bit shall be set to one for devices that support the synchronous DDR or Toggle DDR data interface.
Bits 3-7 are reserved.

Byte 208: Guaranteed valid blocks at beginning of target
This field indicates the number of guaranteed valid blocks starting at block address 0 of the target.
The minimum value for this field is 1h.
The blocks are guaranteed to be valid for the endurance specified for this area when the host follows the specified number of bits to correct in ECC information block 0.

Byte 209-210: Block endurance for guaranteed valid blocks
This field indicates the minimum number of program/erase cycles per addressable page/block in the guaranteed valid block area.
This value requires that the host is using at least the minimum ECC correctability reported in ECC information block 0. This value is not encoded.
If the value is 0000h, then no minimum number of cycles is specified, though the block(s) are guaranteed valid from the factory.

Byte 211-218: ECC information block 0
This block of parameters describes a set of ECC and endurance information.
The parameters are related, and thus the parameters are specified as a set.

Byte 211: Number of bits ECC correctability.
This field indicates the number of bits that the host should be able to correct per codeword.
The codeword size is reported in byte 212. With this specified amount of error correction by the host, the target shall achieve the block endurance specified in bytes 215-216.
When the specified amount of error correction is applied by the host and the block endurance is followed, then the maximum number of bad blocks specified in bytes 213-214 shall not be exceeded by the device.
All used bytes in the page shall be protected by ECC including the spare bytes if the ECC requirement reported in byte 211 has a value greater than zero.
When this value is cleared to zero, the target shall return valid data.

Byte 212: Codeword size. The number of bits of ECC correctability specified in byte 211 is based on a particular ECC codeword size.
The ECC codeword size is specified in this field as a power of two.
The minimum value that shall be reported is 512 bytes (a value of 9).

Byte 213-214: Bad blocks maximum per LUN.
This field contains the maximum number of blocks that may be defective at manufacture and over the life of the device per LUN.
The maximum rating assumes that the host is following the block endurance requirements and the ECC requirements reported in this ECC and endurance information block.

Byte 215-216: Block endurance.
This field indicates the maximum number of program/erase cycles per addressable page/block.
This value assumes that the host is using the ECC correctability reported in byte 211.
The block endurance is reported in terms of a value and a multiplier according to the following equation: value x $10^{multiplier}$. Byte 215 comprises the value. Byte 216 comprises the multiplier.
For example, a block endurance of 75,000 cycles would be reported as a value of 75 and a multiplier of 3 (75 x 10^3).
The value field shall be the smallest possible; for example 100,000 shall be reported as a value of 1 and a multiplier of 5 (1 x 10^5).

Byte 219-226: ECC information block 1
This block of parameters describes an additional set of ECC and endurance information.
The parameters are related, and thus the parameters are specified as a set.
The layout is and definition for this block is equivalent to ECC information block 0.
If this set of parameter is not specified, the block shall be cleared to 0h.

Byte 227-234: ECC information block 2
This block of parameters describes an additional set of ECC and endurance information.
The parameters are related, and thus the parameters are specified as a set.
The layout is and definition for this block is equivalent to ECC information block 0.
If this set of parameter is not specified, the block shall be cleared to 0h.

Byte 235-242: ECC information block 3
This block of parameters describes an additional set of ECC and endurance information.
The parameters are related, and thus the parameters are specified as a set.
The layout is and definition for this block is equivalent to ECC information block 0.
If this set of parameter is not specified, the block shall be cleared to 0h.

Byte 420-421: Vendor specific Revision number
This field indicates a vendor specific revision number.
This field should be used by vendors to indicate the supported layout for the vendor specific parameter page area and the vendor specific feature addresses. The format of this field is vendor specific.

Byte 422-509: Vendor specific
This field is reserved for vendor specific use.

Byte 510-511: Integrity CRC
The Integrity CRC (Cyclic Redundancy Check) field is u
sed to verify that the contents of the parameter page were transferred correctly to the host.
The CRC of the parameter page is a word (16-bit) field. The CRC calculation covers all of data between byte 0 and byte 509 of the parameter page inclusive.
The CRC shall be calculated on byte (8-bit) quantities starting with byte 0 in the parameter page.
The bits in the 8-bit quantity are processed from the most significant bit (bit 7) to the least significant bit (bit 0).

The CRC shall be calculated using the following 16-bit generator polynomial:
G(X) = X16 + X15 + X2 + 1
This polynomial in hex may be represented as 8005h.

The CRC value shall be initialized with a value of 4F4Eh before the calculation begins. There is no XOR applied to the final CRC value after it is calculated. There is no reversal of the data bytes or the CRC calculated value.

Byte 512-1023: Redundant Parameter Page 1
This field shall contain the values of bytes 0-511 of the parameter page. Byte 512 is the value of byte 0.

The redundant parameter page is used when the integrity CRC indicates that there was an error in bytes 0-511. The redundant parameter page shall be stored in non-volatile media; the target shall not create these bytes by retransmitting the first 512 bytes.

Byte 1024-1535: Redundant Parameter Page 2
This field shall contain the values of bytes 0-511 of the parameter page. Byte 1024 is the value of byte 0.

The redundant parameter page is used when the integrity CRC indicates that there was an error in bytes 0-511 and in the first redundant parameter page.
The redundant parameter page shall be stored in non-volatile media; the target shall not create these bytes by retransmitting the first 512 bytes.

Byte 1536+: Additional Redundant Parameter Pages
Bytes at offset 1536 and above may contain additional redundant copies of the parameter page.
There is no limit to the number of redundant parameter pages that the target may provide.
The target may provide additional copies to guard against the case where all three mandatory copies have invalid CRC checks.

The host should determine whether an additional parameter page is present by checking the first Dword.
If at least two out of four bytes match the parameter page signature, then an additional parameter page is present.

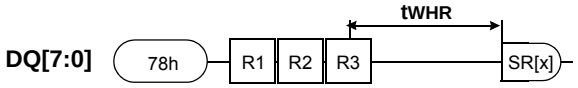
5.3.16 Read Status Enhanced

Read Status Enhanced function is used to check status of selected plane of a LUN and LUN(chip). Thus, the function requires row address setting steps before reading status value. Table 44 defines status values of each operation and Figure 46 defines Read Status Enhanced behavior and timings.

[Table 44] Read Status Enhanced Definition

	DQ 0	DQ 1	DQ 2	DQ 3	DQ 4	DQ 5	DQ 6	DQ 7
Definition of value	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Reserved	Busy : "0" Ready : "1"	Busy : "0" Ready : "1"	Protected : "0" Not Protected : "1"
Block Erase	Pass/Fail	Not Use	Pass/Fail	Not Use	Not Use	Not Use	Ready/Busy	Write Protect
Page Program	Pass/Fail	Not Use	Pass/Fail	Not Use	Not Use	Not Use	Ready/Busy	Write Protect
Cache Program	Pass/Fail for the current page	Pass/Fail for the previous page	Pass/Fail for the current page	Pass/Fail for the previous page	Not Use	Busy/Ready for Flash array	Ready/Busy for Host	Write Protect
Read	Not Use	Not Use	Not Use	Not Use	Not Use	Not Use	Ready/Busy	Write Protect
Cache Read	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Ready/Busy for Host	Write Protect

NOTE :
DQ0 and DQ1 provides status of plane selected. DQ2 and DQ3 provides LUN(chip) status for Block Erase, Page Program and Cache Program.

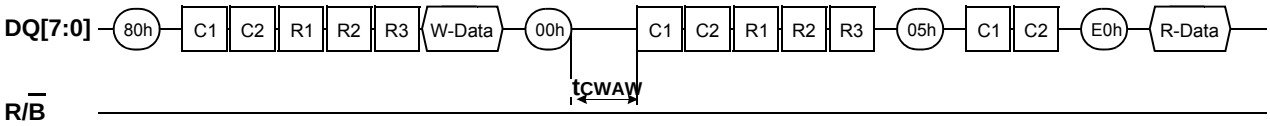


[Figure 46] Read Status Sequence

5.3.17 Register Read Out Mode 1

At program operation, loaded data to the register can be read out before program confirm command(10h). The sequence is as follows. To continue program operation after reading data, Copy-back Program operatiion (i.e. 85h- Address(5cycle) - Data - 10h) is required.

Register Read Out with SLC operation

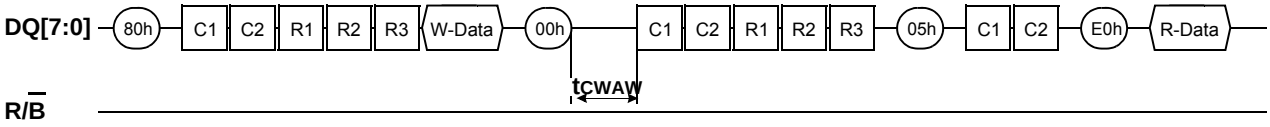


NOTE :
Register read out operation is prohibited during cache program operation.

5.3.18 Register Read Out Mode 2

At program operation, loaded data to the register can be read out before page buffer latch dump command(C0h) during data setup part. The sequence is as follows. To continue program operation after reading data, 85h- Address(5cycle) - Data - C0h - Address(1cycle) and insert next program command sequence is required.

Register Read Out with TLC operation

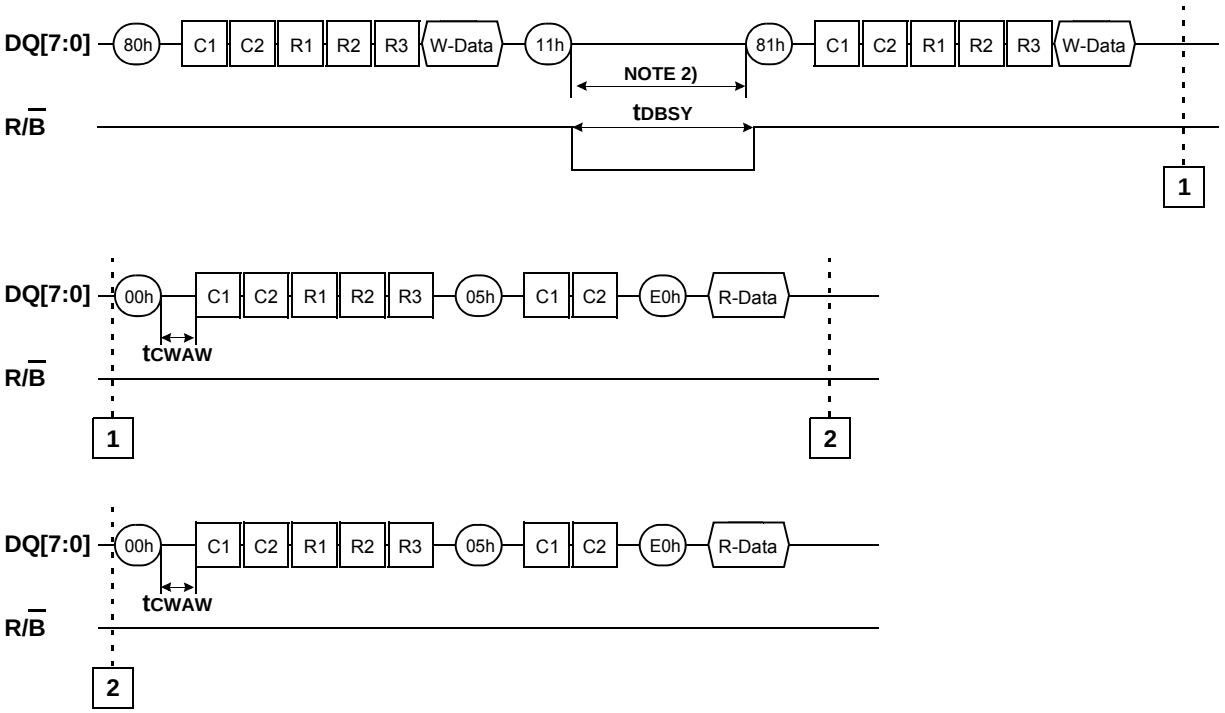


NOTE :
Register read out operation is prohibited during cache program operation.

5.3.19 Two-Plane Register Read Out Mode 1

At Two-Plane program operation, loaded data to the register can be read out before program confirm command(10h). The sequence is as follows.To continue Two-Plane program operation after reading data, Two-Plane Random Data Copy-back Program sequence is required.

Two-Plane Register Read Out Mode with SLC operation

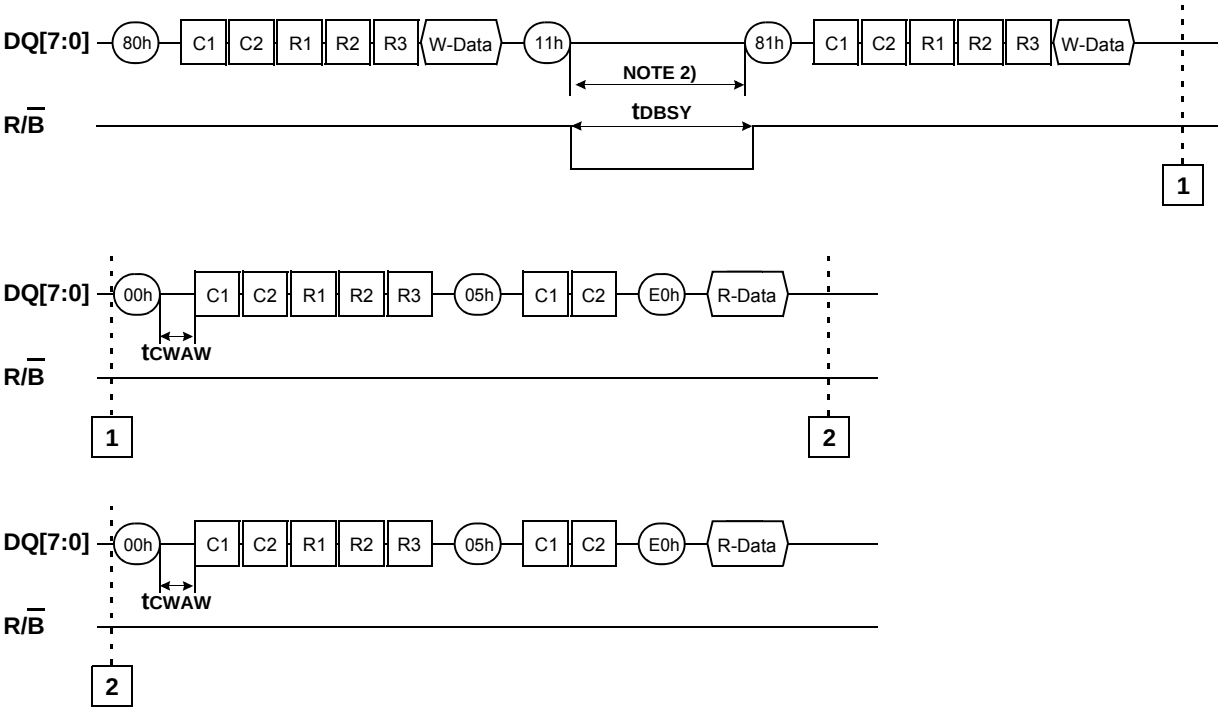


NOTE :
1) Any command between 11h and 81h is prohibited except 70h/78h/FAh and FFh.
2) Register read out operation is prohibited during cache program operation.

5.3.20 Two-Plane Register Read Out Mode 2

At Two-Plane program operation, loaded data to the register can be read out before page buffer latch dump command(C0h) during data setup part. The sequence is as follows.To continue Two-Plane program operation after reading data, 85h- Address(5cycle) - Data - 11h- 81h - Address(5cycle) - Data - C0h - Address(1cycle) and insert next program command sequence is required.

Two-Plane Register Read Out Mode with TLC operation



NOTE :
1) Any command between 11h and 81h is prohibited except 70h/78h/FAh and FFh.
2) Register read out operation is prohibited during cache program operation.

5.4 Interleaving Operation

When multiple LUNs share a common $\overline{CE}$, it provides interleaving operation between LUNs.

At first, the host issues a operation command to one of the LSB chips, say (LUN #0). Due to DDP device goes into busy state. During this time, MSB chip (LUN #1) is in ready state. So it can execute the operation command issued by the host.

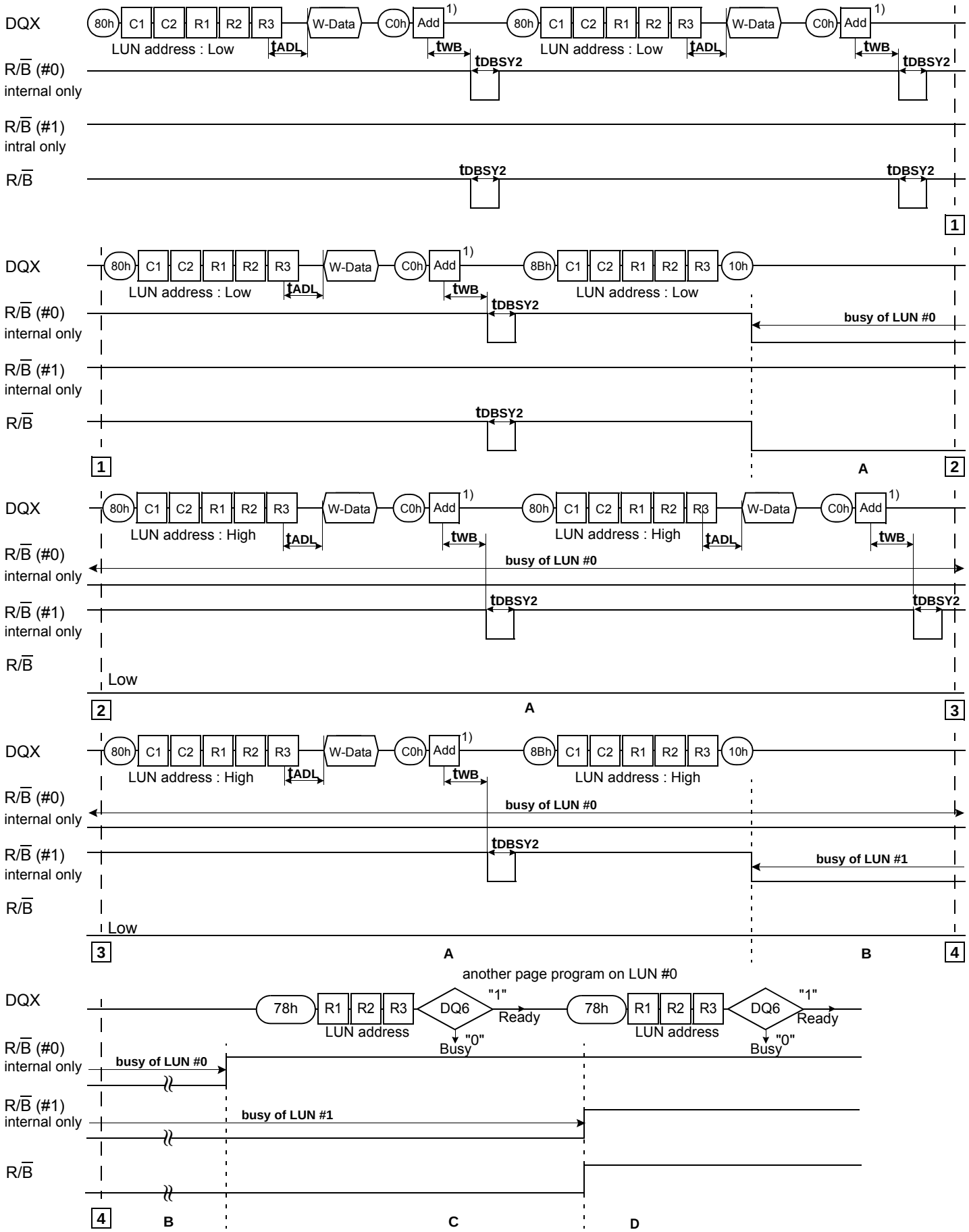
After the execution of operation by LSB chip (LUN #0), it can execute another operation regardless of MSB chip (LUN #1). Before that the host needs to check the status of LSB chip (LUN #0) by issuing 78h command. Only when the status of LSB chip (LUN #0) becomes ready status, host can issue another operation command. If LSB chip (LUN #0) is in busy state, the host has to wait for LSB chip (LUN #0) to get into ready state.

Similarly, MSB chip (LUN #1) can execute another operation after the completion of the previous operation. The host can monitor the status of MSB chip (LUN #1) by issuing 78h command. When MSB chip (LUN #1) goes ready state, host can issue another operation command to MSB chip (LUN #1).

This interleaving operation helps the system improve the system throughput.

NOTE :
During interleave operations, 70h command is prohibited and 78h command is used to check the status.
Interleaving operation must be excuted between the blocks in the same status. It means that TLC to SLC and SLC to TLC interleaving operations are prohibited.

5.4.1 Interleaving Page Program

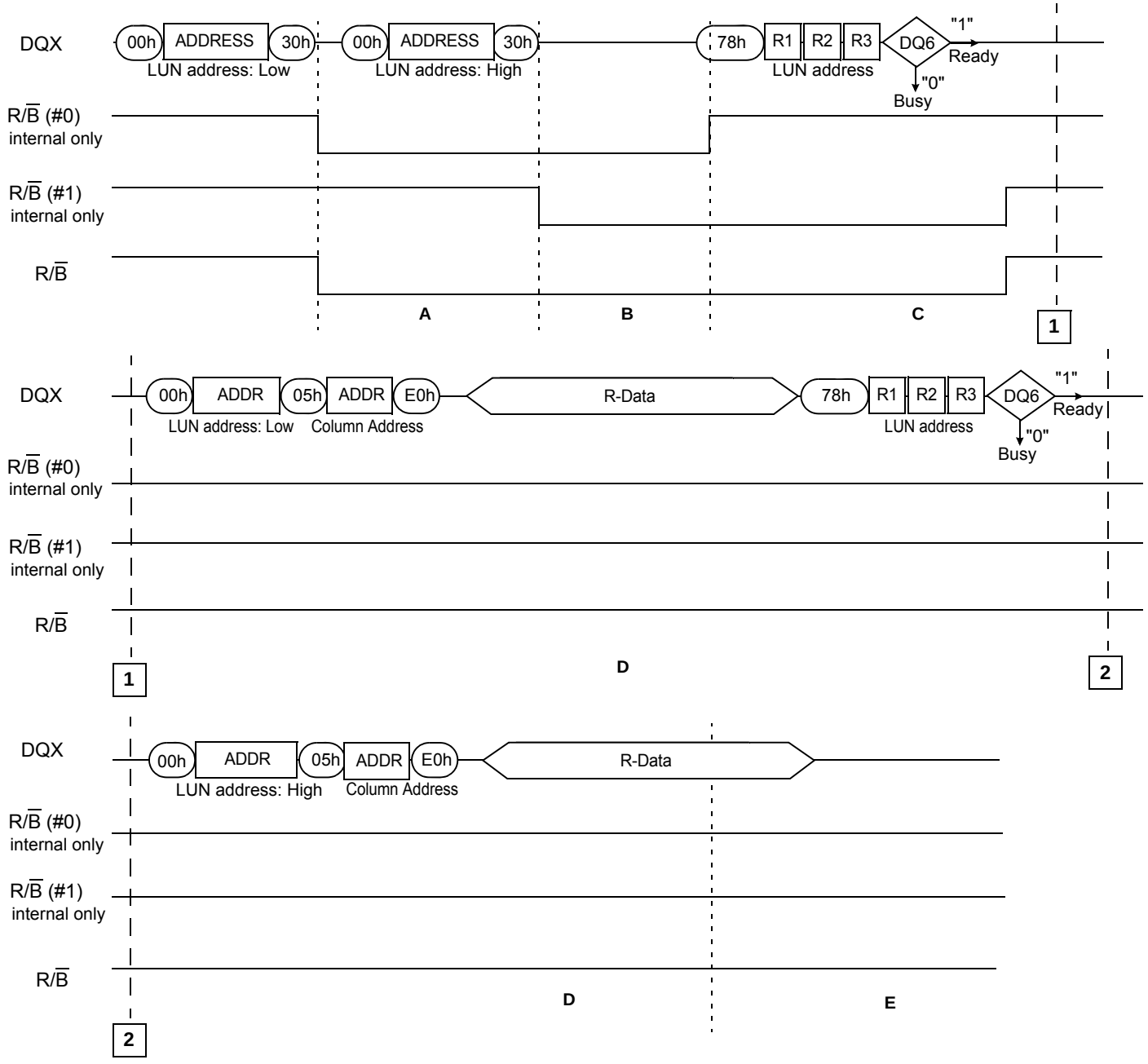


State A : LUN #0 is executing page program operation and LUN #1 is in ready state. So the host can issue page program command to LUN #1.
State B : Both LUN #0 and LUN #1 are executing page program operation.
State C : Page program on LUN #0 is completed, but page program on LUN #1 is still ongoing. And the system should issue 78h command to detect the status of LUN #0. If LUN #0 is ready, status I/O6 is "1" and the system can issue another page program command to LUN #0.
State D : Both of LUN #0 and LUN #1 are ready.

Depending on the above process, the system can operate page program on LUN #0 and LUN #1 alternately.

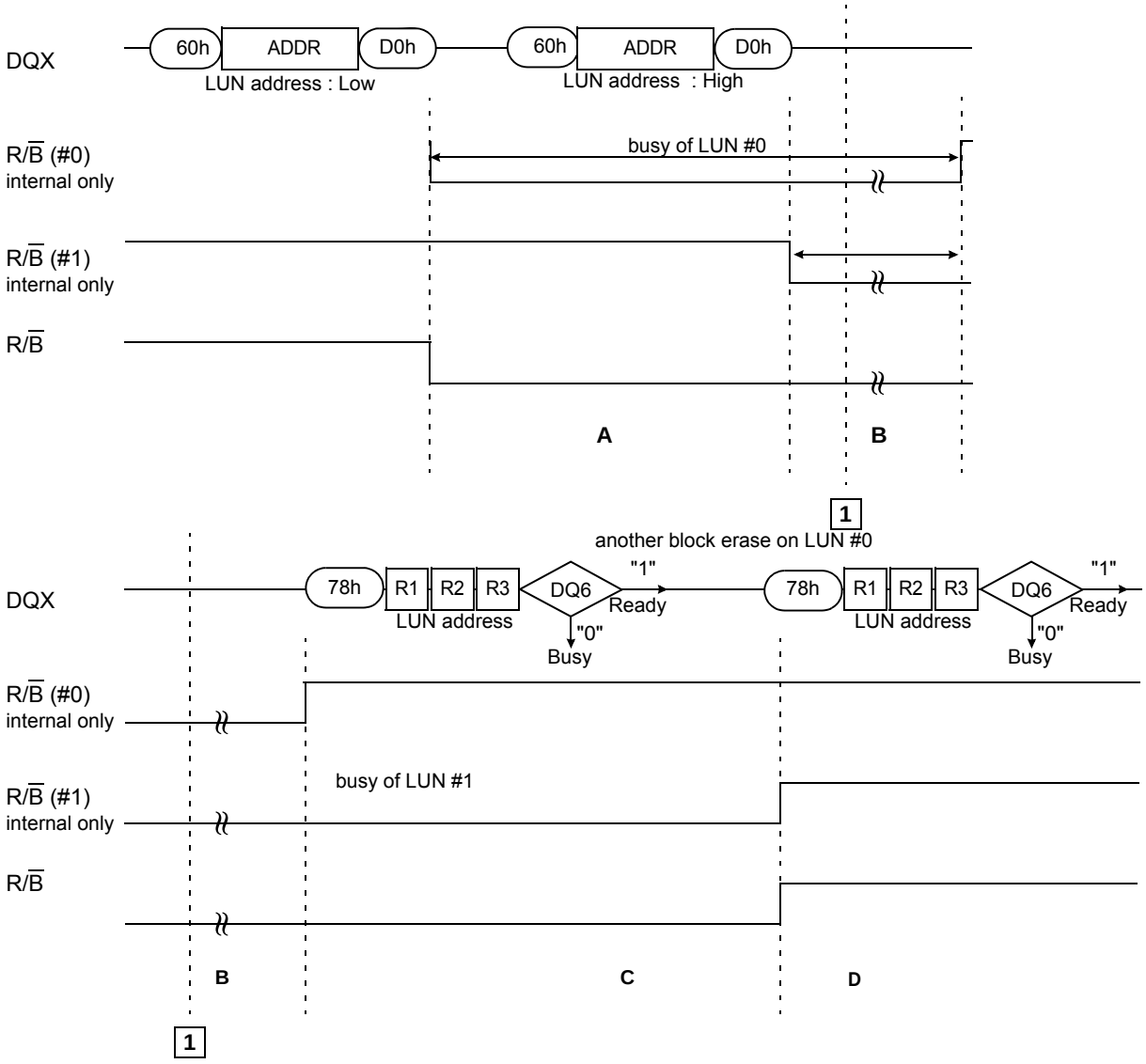
NOTE :
1) For address followed by C0h command, refer to the buffer address Table 23

5.4.2 Interleaving Page Read



State A : LUN #0 is executing page read operation, and LUN #1 is in ready state. So the host can issue page read command to LUN #1.
State B : Both LUN #0 and LUN #1 are executing page read operation.
State C : Page read on LUN #0 is completed and LUN #1 is still executing page read operation.
State D : Before the host read the data, the host should check the Ready/Busy status for both LUNs by 78h commands.
State E : LUN #0 and LUN #1 are ready.

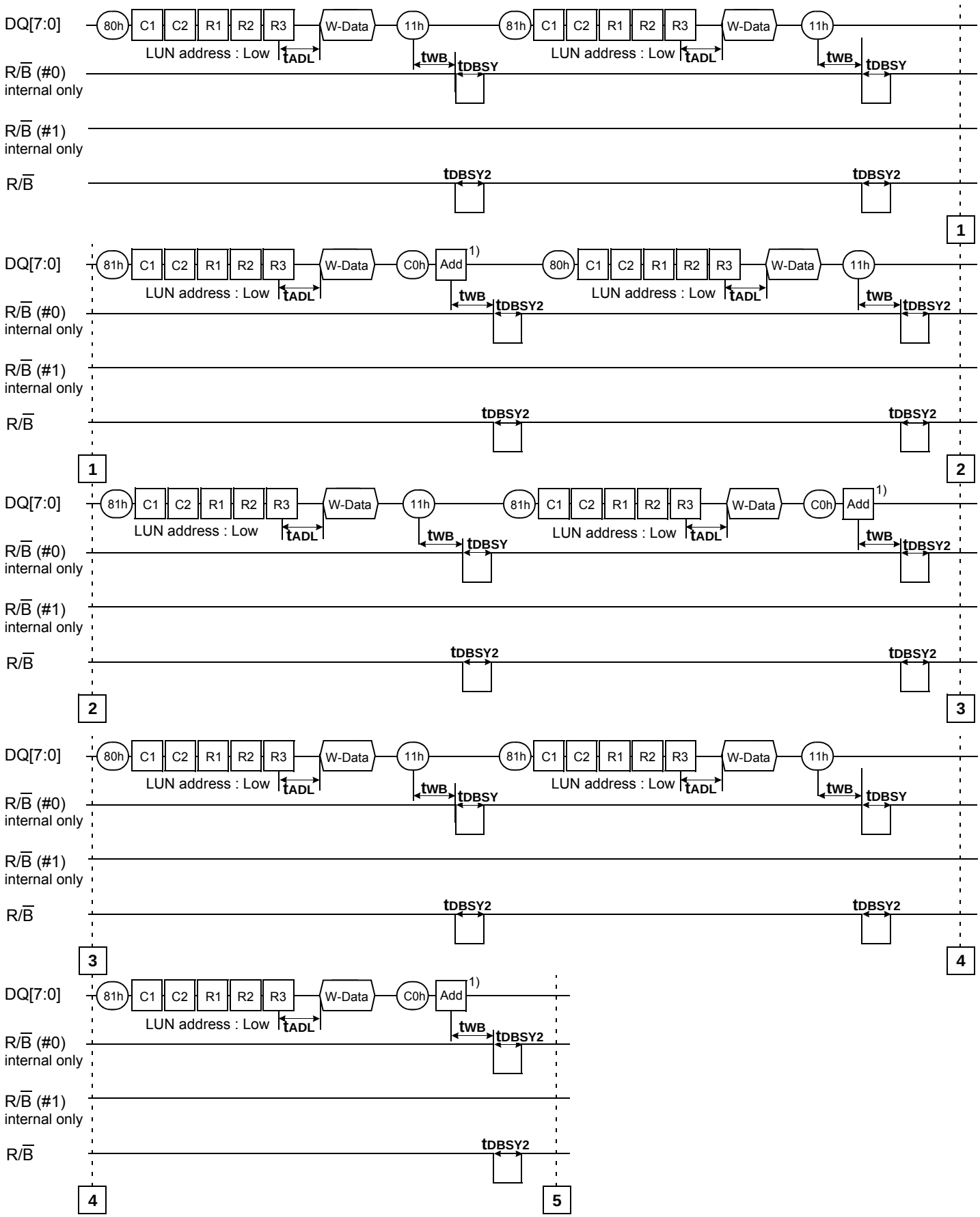
5.4.3 Interleaving Block Erase



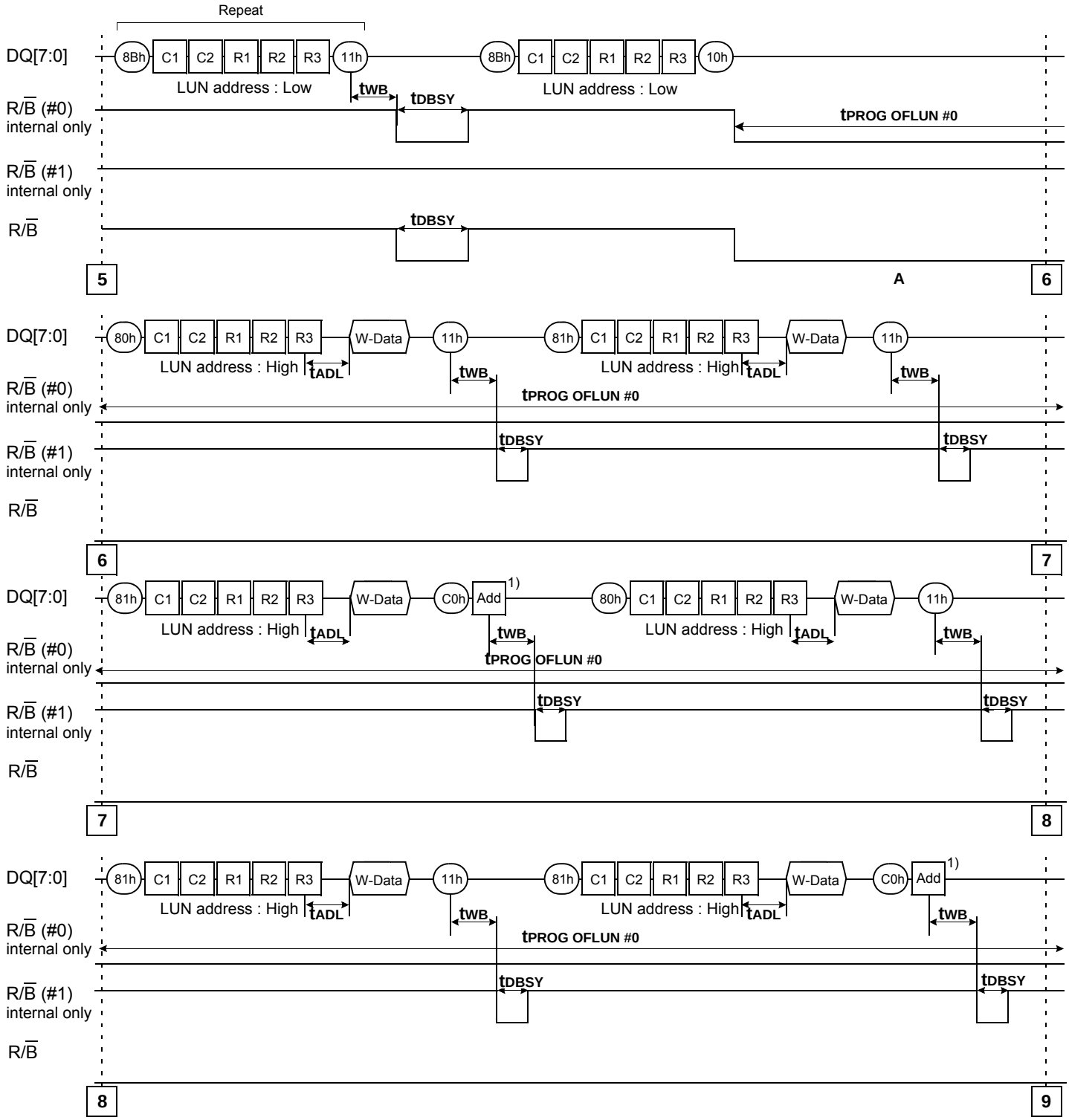
State A : LUN #0 is executing block erase operation, and LUN #1 is in ready state. So the host can issue block erase command to LUN #1.
State B : Both LUN #0 and LUN #1 are executing block erase operation.
State C : Block erase on LUN #0 is terminated, but block erase on LUN #1 is still operating. And the system should issue 78h command to detect the status of LUN #0. If LUN #0 is ready, status I/O6 is "1" and the system can issue another block erase command to LUN #0.
State D : LUN #0 and LUN #1 are ready.

Depending on the above process, the system can operate block erase on LUN #0 and LUN #1 alternately.

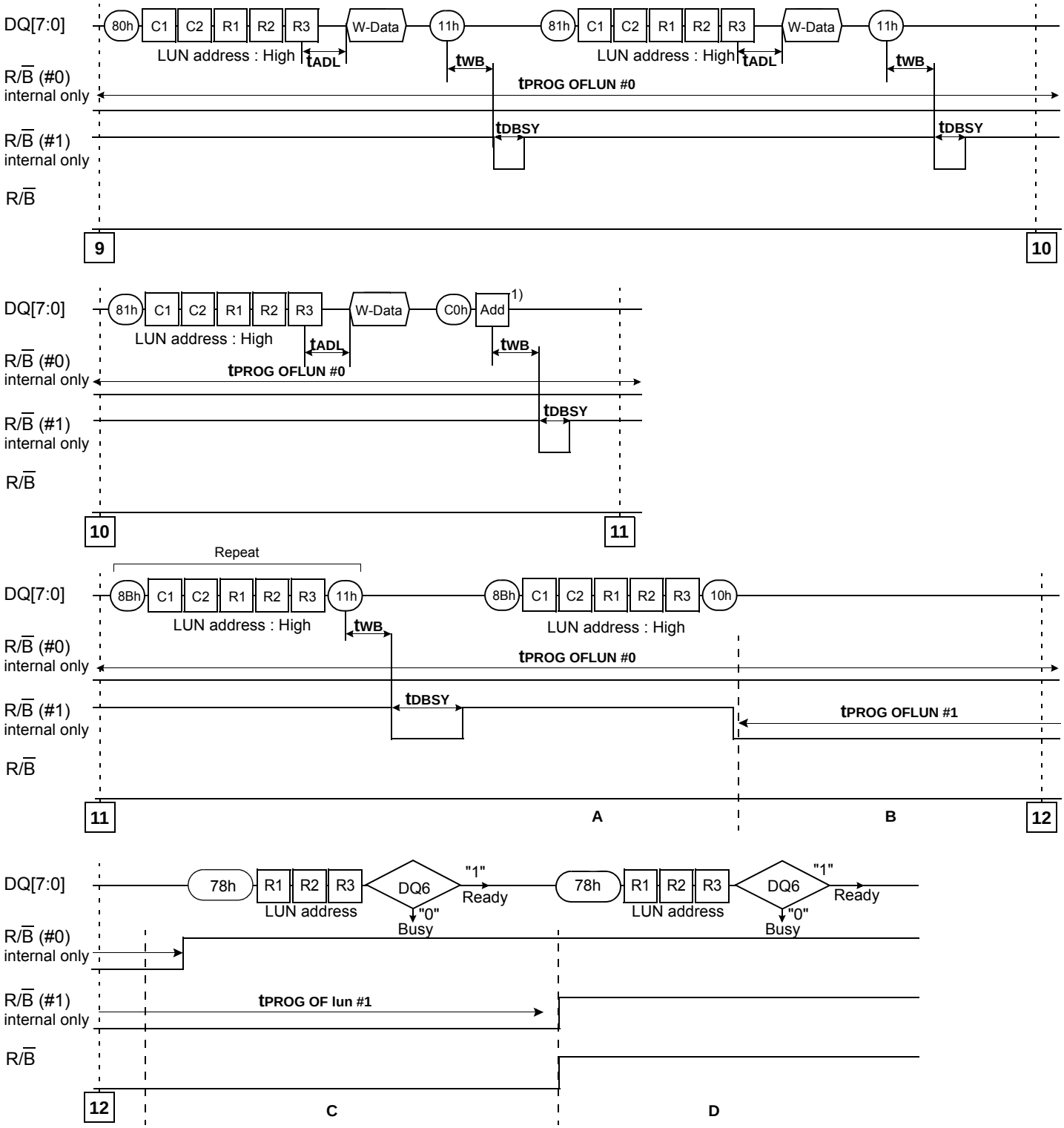
5.4.4 Interleaving Multi-Plane Page Program(1/3)



5.4.5 Interleaving Multi-Plane Page Program(2/3)



5.4.6 Interleaving Multi-Plane Page Program(3/3)

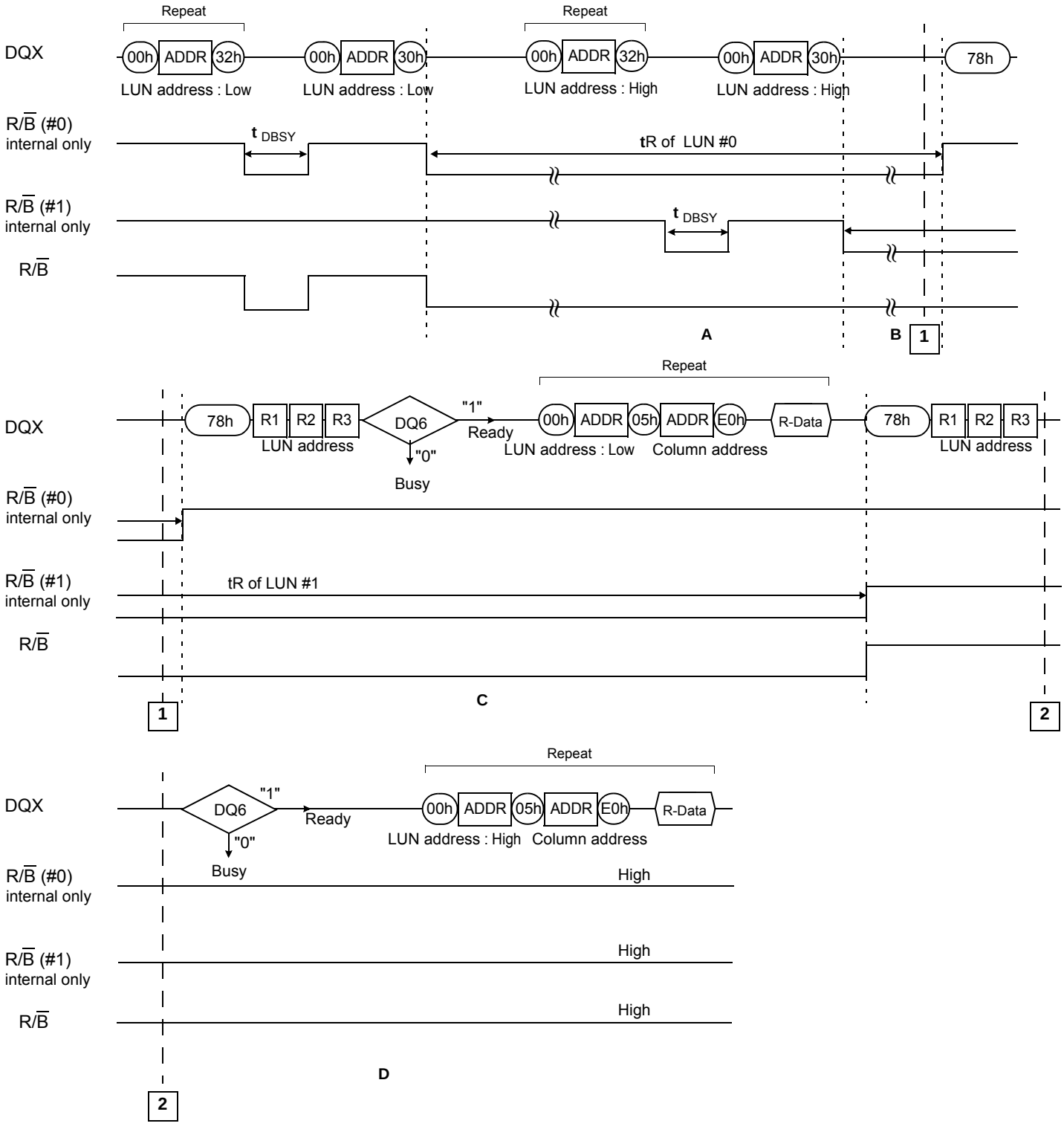


State A : LUN #0 is executing Multi-plane page program operation, and LUN #1 is in ready state. So the host can issue Multi-plane page program command to LUN #1.
State B : Both LUN #0 and LUN #1 are executing Multi-plane page program operation.
State C : Multi-plane page program on LUN #0 is completed and LUN #0 is ready for the next operation. LUN #1 is still executing Multi-plane page program operation.
State D : Both LUN #0 and LUN #1 are ready.

NOTE :
1) For address followed by C0h command, refer to the buffer address Table 23

Depending on the above process, the system can operate Multi-plane page program on LUN #0 and LUN #1 alternately.

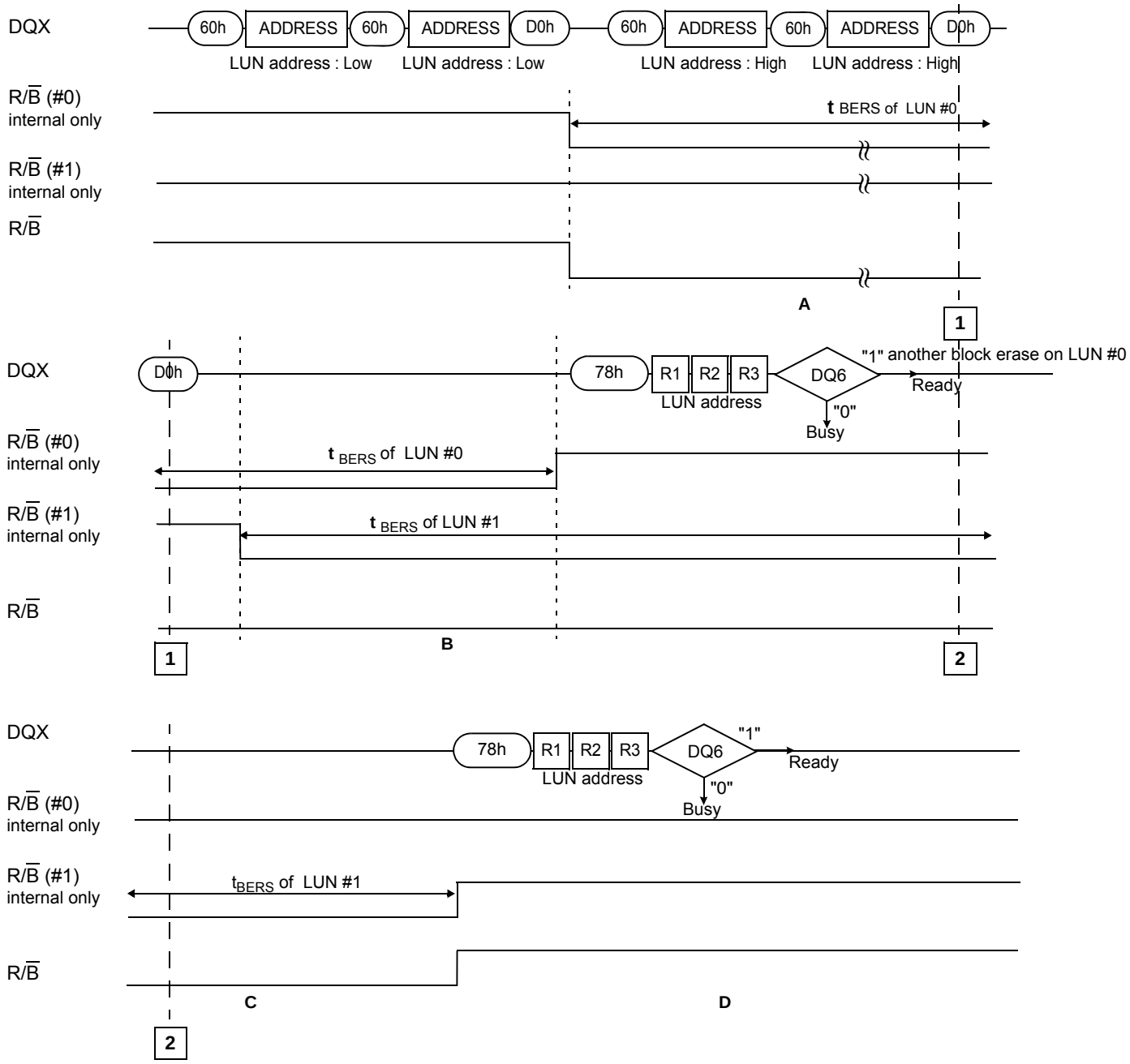
5.4.7 Interleaving Multi-plane page Read



State A : LUN #0 is executing Multi-plane page read operation, and LUN #1 is in ready state. So the host can issue Multi-plane page read command to LUN #1.
State B : Both LUN #0 and LUN #1 are executing Multi-plane page read operation.
State C : Multi-plane page read on LUN #0 is completed and LUN #0 is ready for the next operation. LUN #1 is still executing Multi-plane page read operation.
State D : Both LUN #0 and LUN #1 are ready.

NOTE :
F8h command shall be required to check the Read status of LUN #0 and LUN #1.
Depending on the above process, the system can operate Multi-plane page read on LUN #0 and LUN #1 alternately.

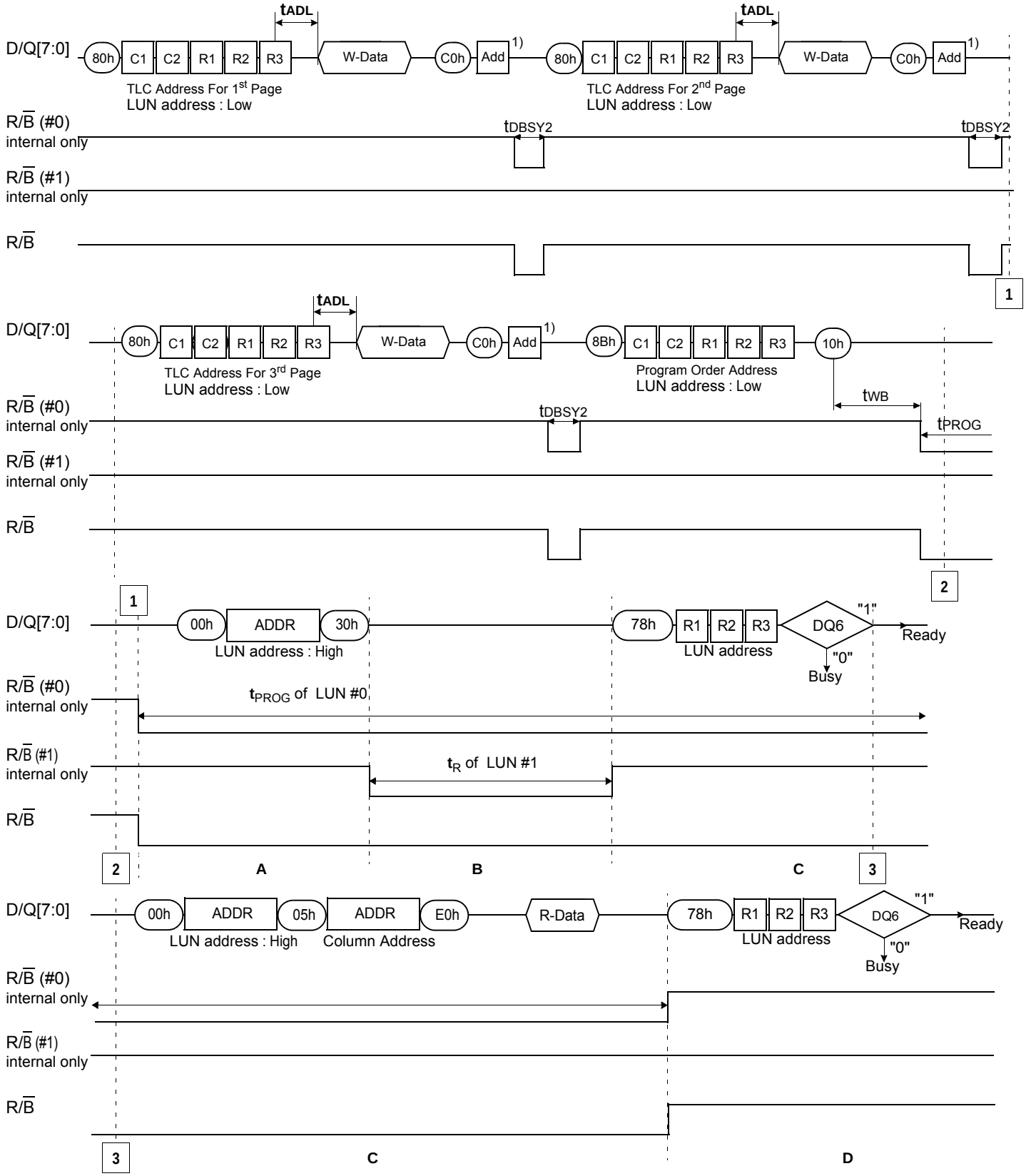
5.4.8 Interleaving Multi-plane Block Erase



State A : LUN #0 is executing Multi-plane block erase operation, and LUN #1 is in ready state. So the host can issue Multi-plane block erase command to LUN #1.
State B : Both LUN #0 and LUN #1 are executing Multi-plane block erase operation.
State C : Multi-plane block erase on LUN #0 is completed and LUN #0 is ready for the next operation. LUN #1 is still executing Multi-plane block erase operation.
State D : Both LUN #0 and LUN #1 are ready.

According to the above process, the system can operate Multi-plane block erase on LUN #0 and LUN #1 alternately.

5.4.9 Interleaving Read to Page Program

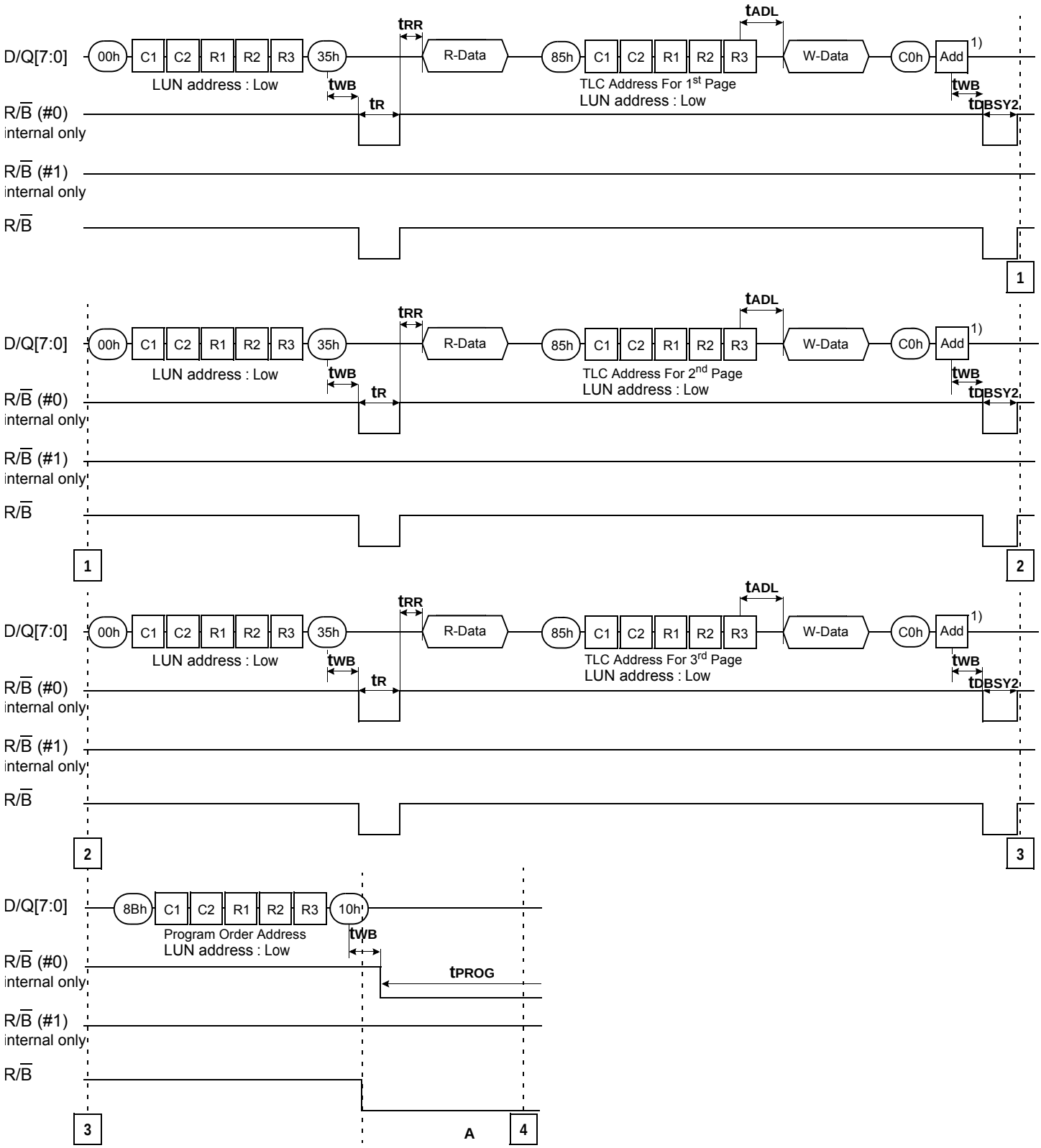


State A : LUN #0 is executing page program operation, and LUN #1 is in ready state. So the host can issue read command to LUN #1.
State B : Both LUN #0 is executing page program operation and LUN #1 is executing read operation.
State C : Read operation on LUN #1 is completed and LUN #1 is ready for the next operation. LUN #0 is still executing page program operation.
State D : Both LUN #0 and LUN #1 are ready.

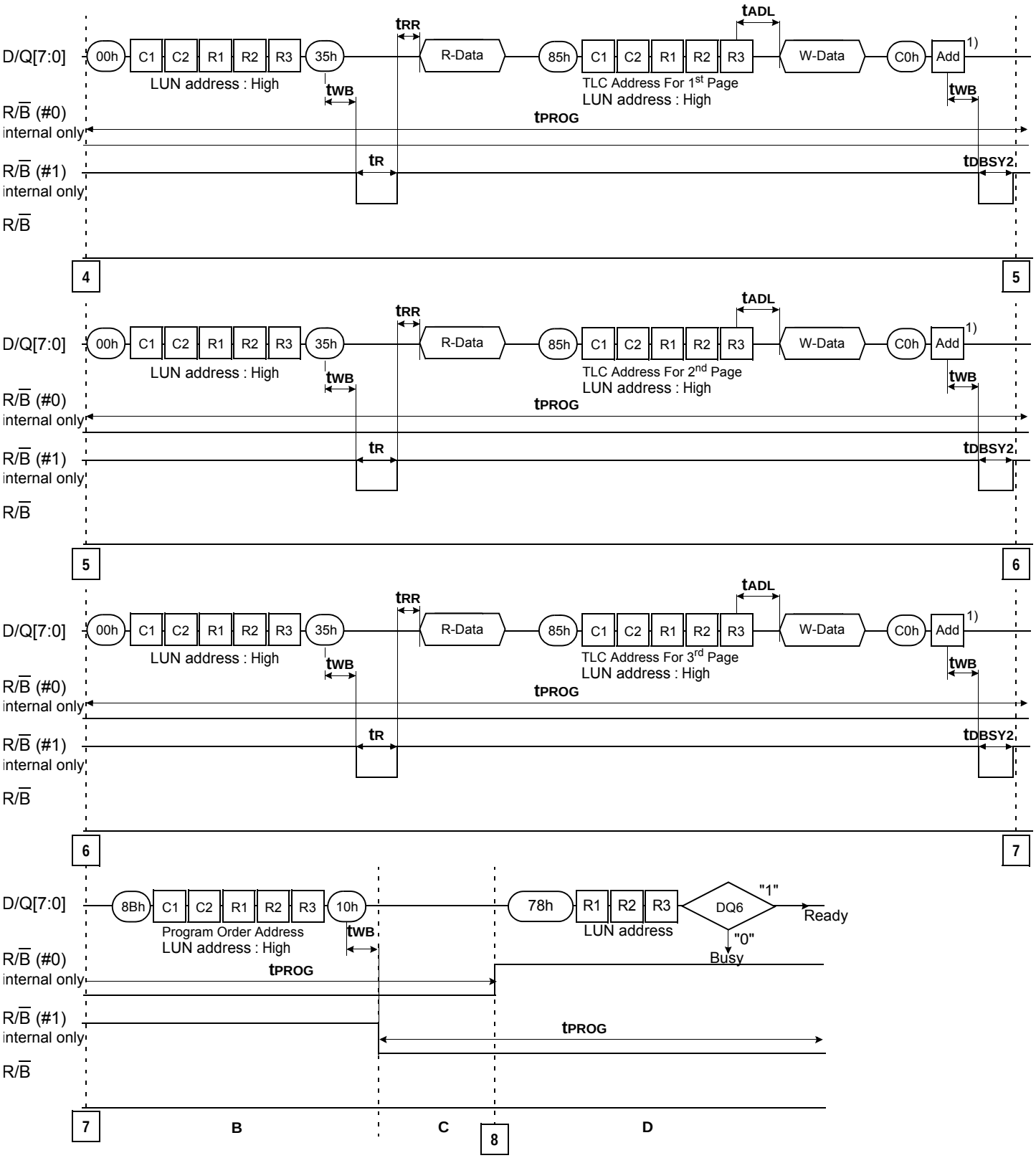
As the above process, the system can operate Interleave read to page porgram on LUN #0 and LUN #1 alternatively.

NOTE :
1) For address followed by C0h command, refer to the buffer address Table 23

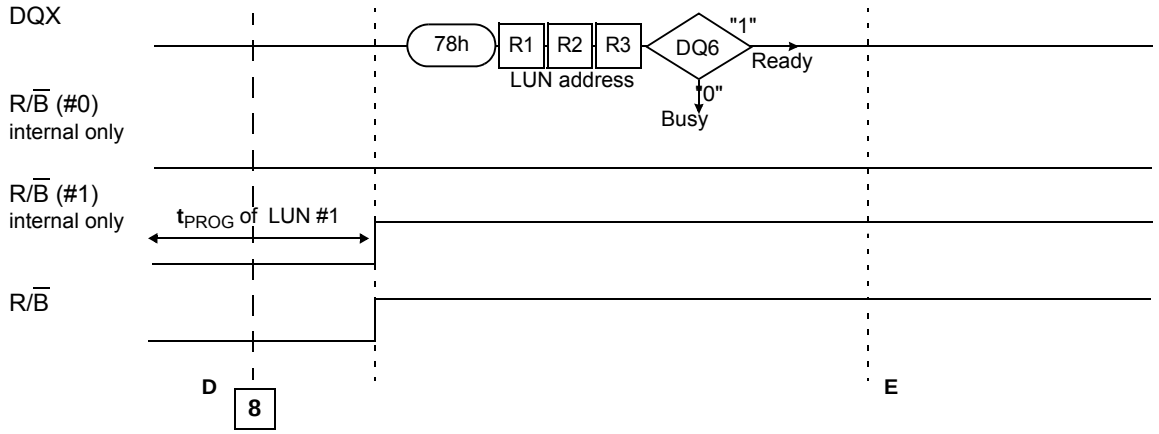
5.4.10 Interleaving Copy-Back Program (1/3)



5.4.11 Interleaving Copy-Back Program (2/3)



5.4.12 Interleaving Copy-Back Program (3/3)

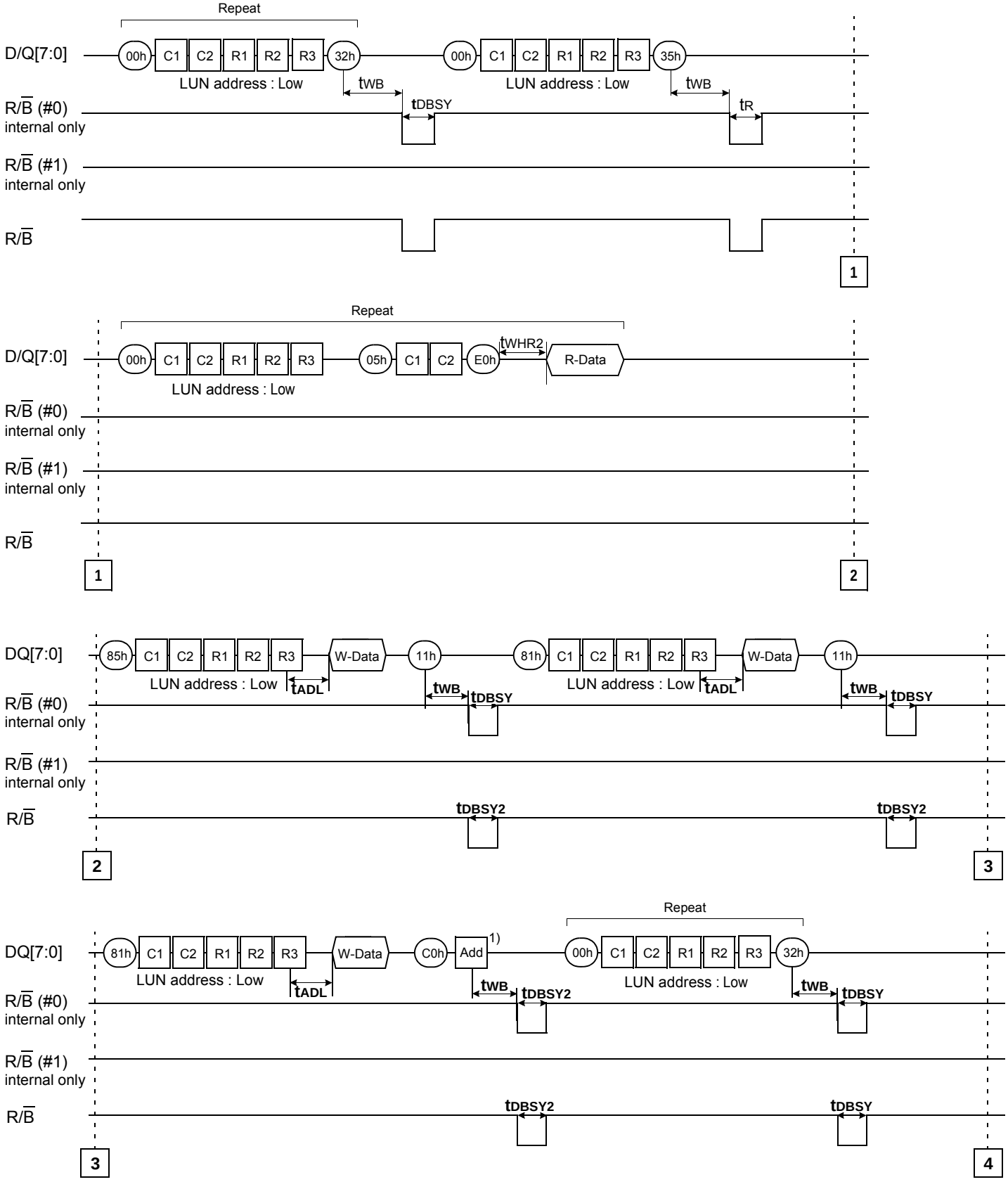


State A : LUN #0 is executing copy-back program operation, and LUN #1 is in ready state. So the host can issue read for copy-back command to LUN #1.
State B : Read for copy-back operation on LUN #1 is completed and LUN #1 is ready for the next operation. LUN #0 is still executing copy-back program operation.
State C : Both LUN #0 and LUN #1 are executing copy-back program operation.
State D : LUN #1 is still executing a copy-back program operation, and LUN #0 is in ready for the next operation.
State E : Both LUN #0 and LUN #1 are ready.

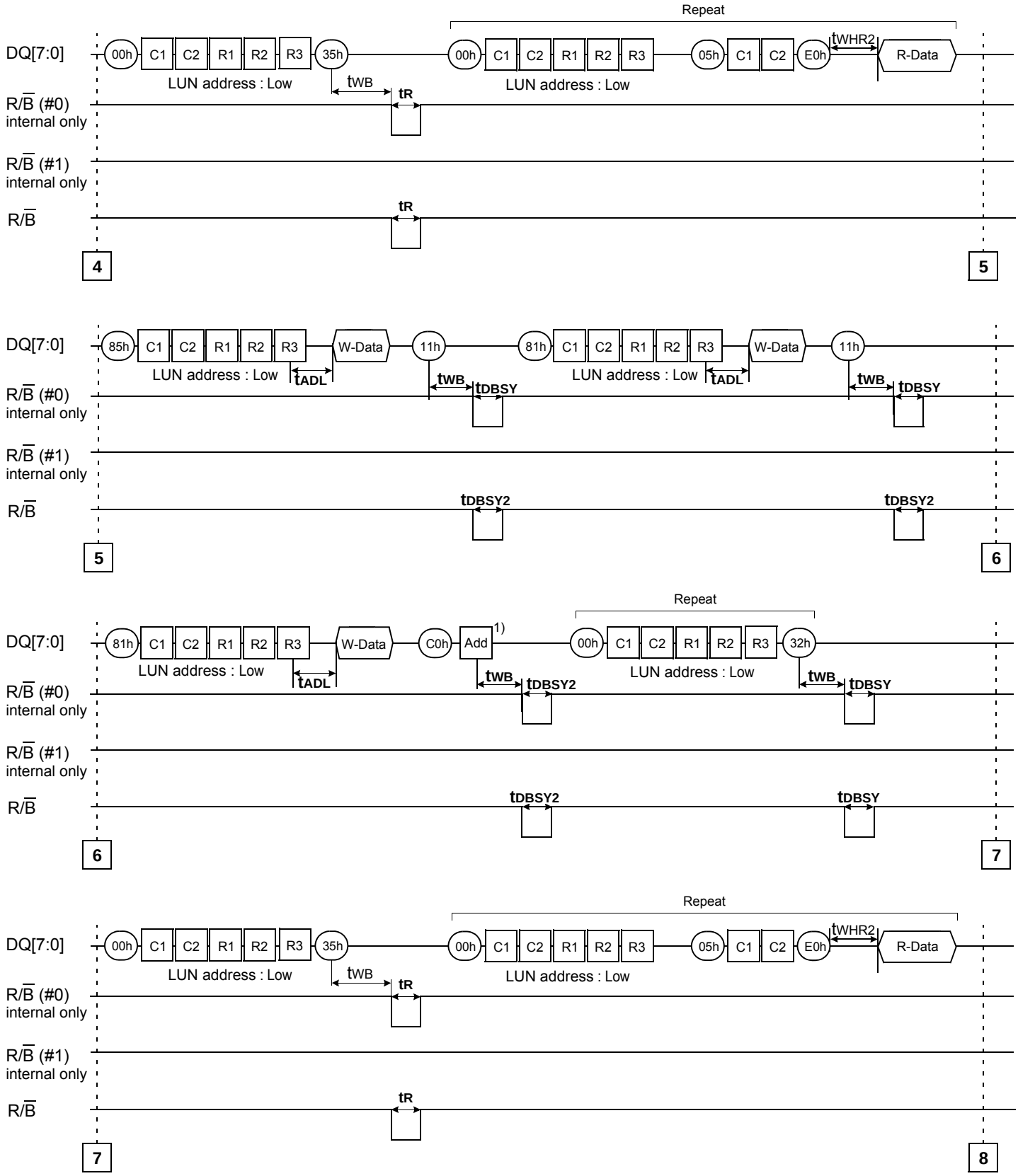
Depending on the above process, the system can operate Interleave copy-back program on LUN #0 and LUN #1 alternatively

NOTE :
1) For address followed by C0h command, refer to the buffer address Table 23

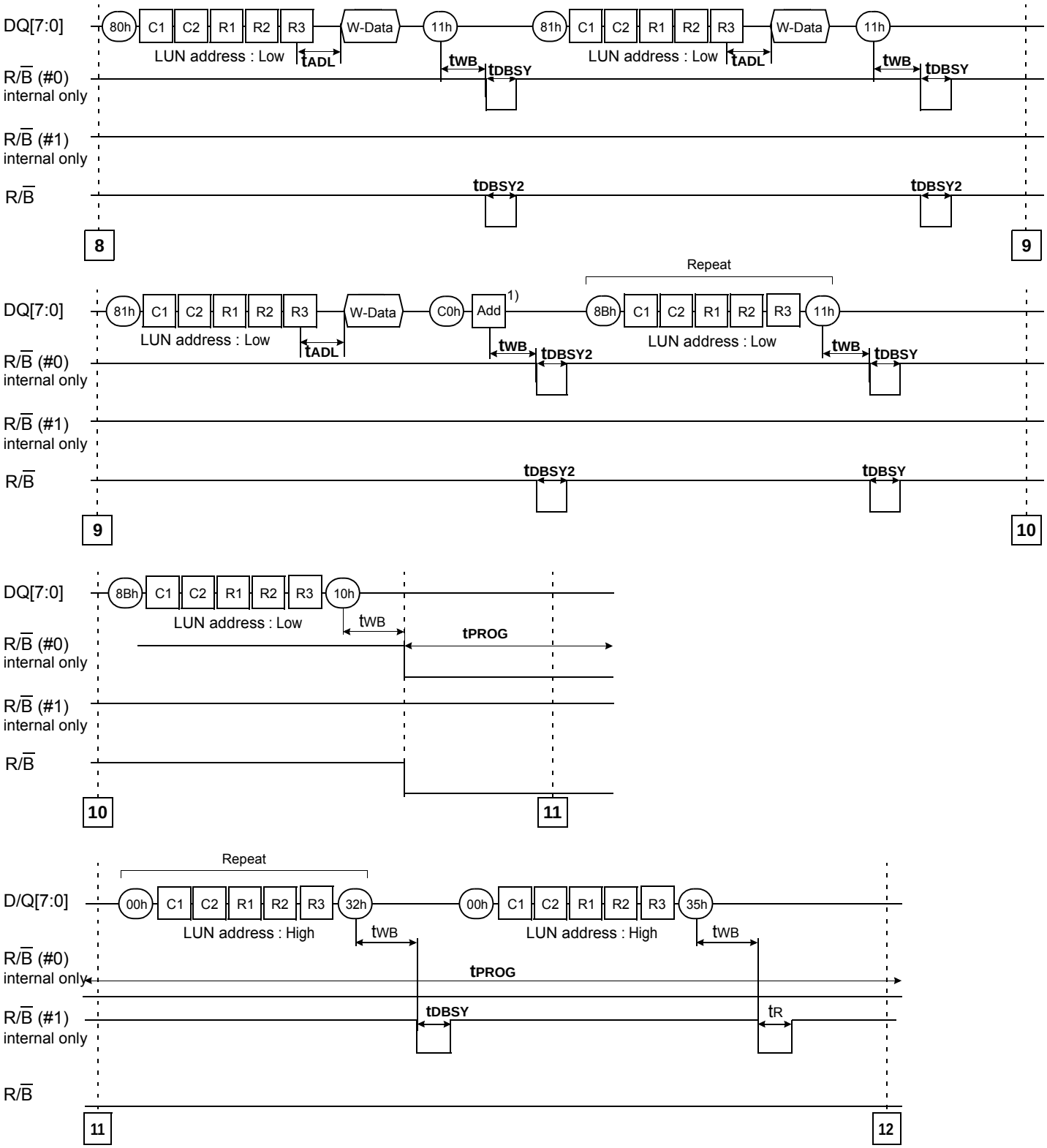
5.4.13 Interleaving Multi-plane Copy Back Program(1/7)



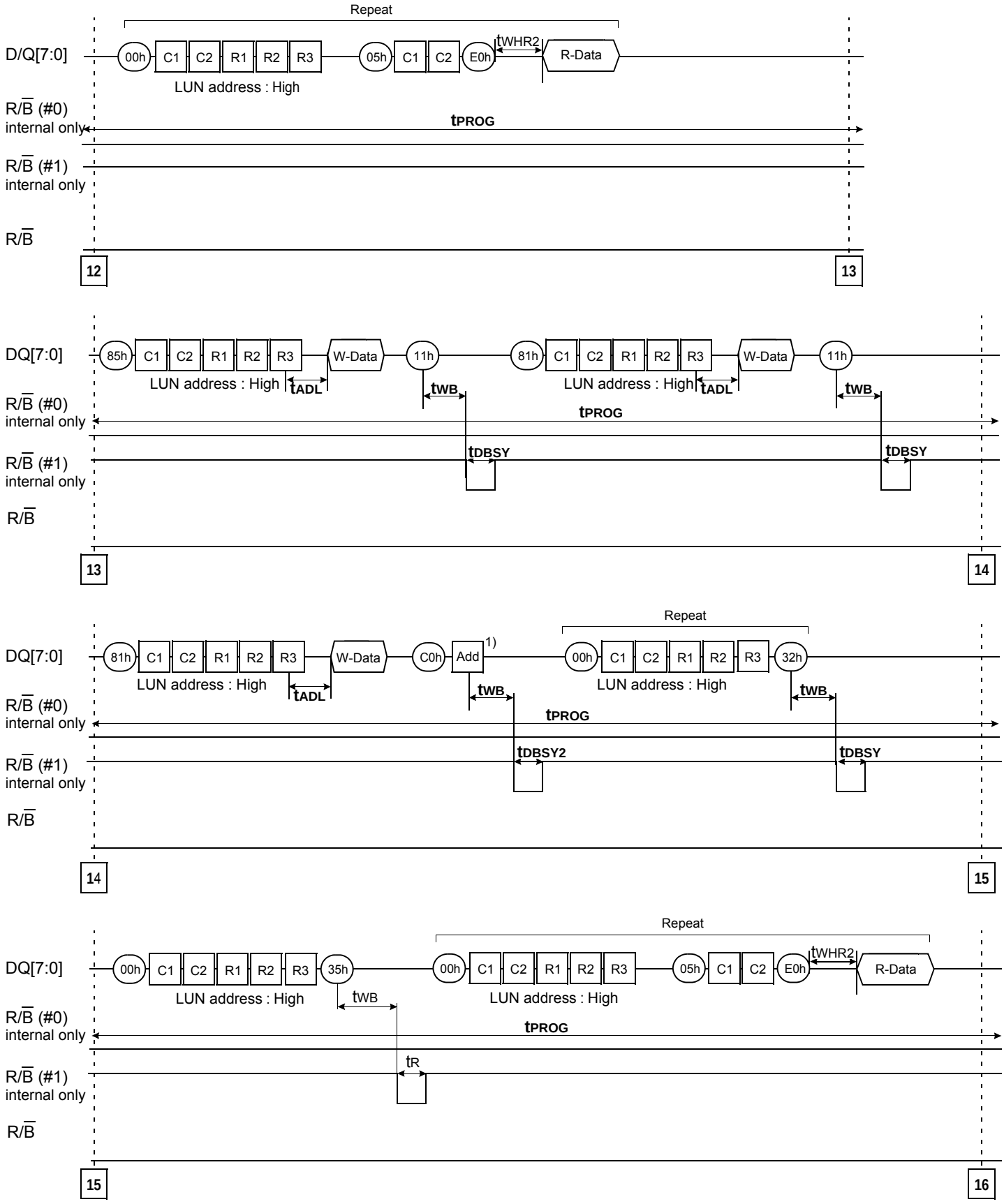
5.4.14 Interleaving Multi-plane Copy Back Program(2/7)



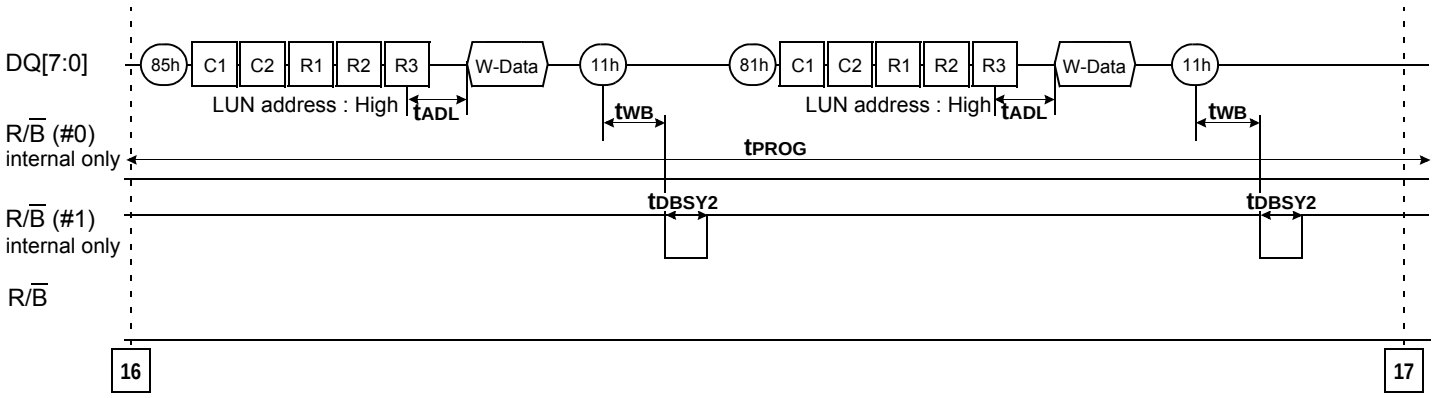
5.4.15 Interleaving Multi-plane Copy Back Program(3/7)

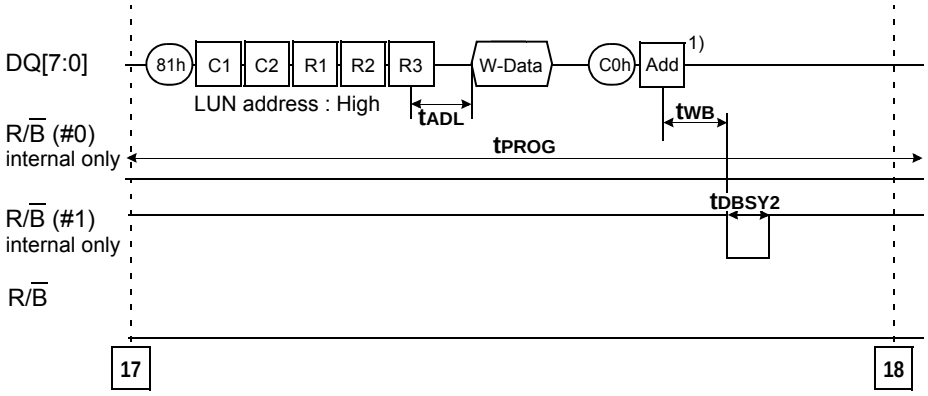


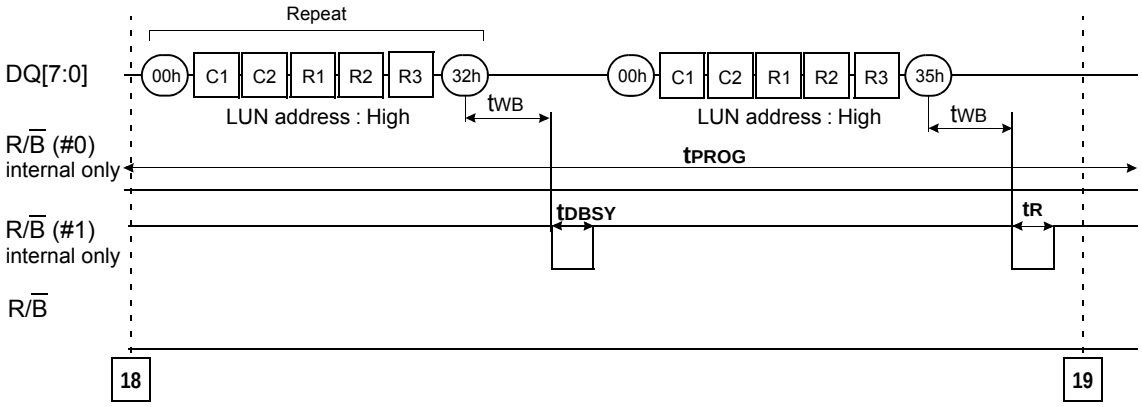
5.4.16 Interleaving Multi-plane Copy Back Program(4/7)

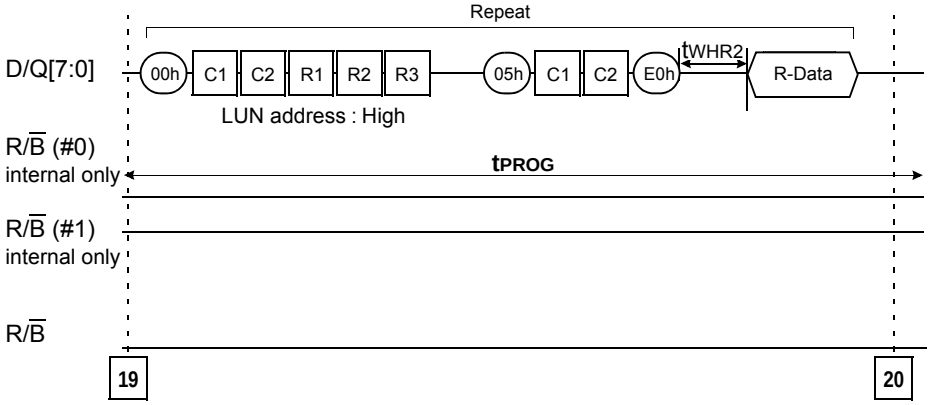


5.4.17 Interleaving Multi-plane Copy Back Program(5/7)

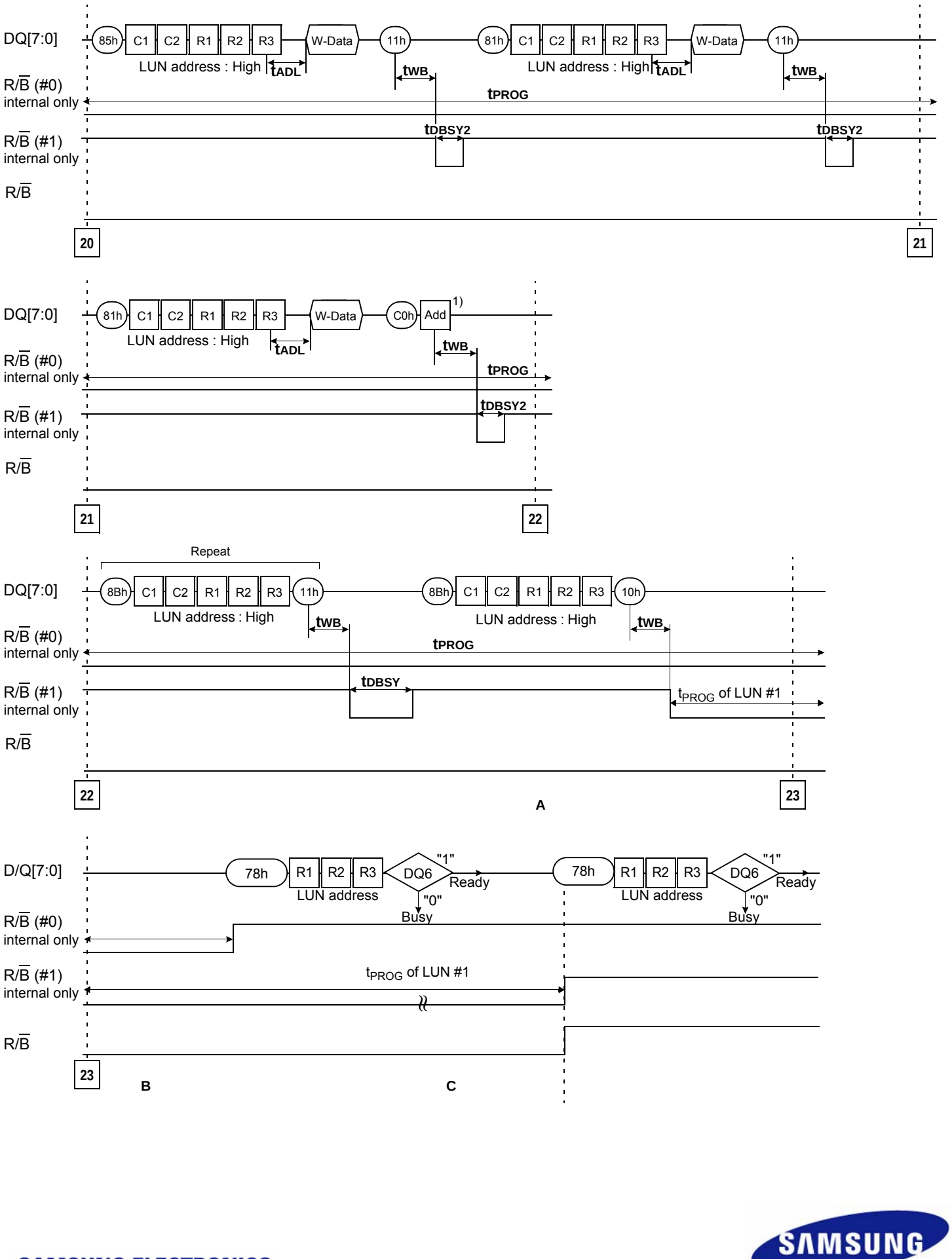








5.4.18 Interleaving Multi-plane Copy Back Program(6/7)



5.4.19 Interleaving Multi-plane Copy Back Program(7/7)

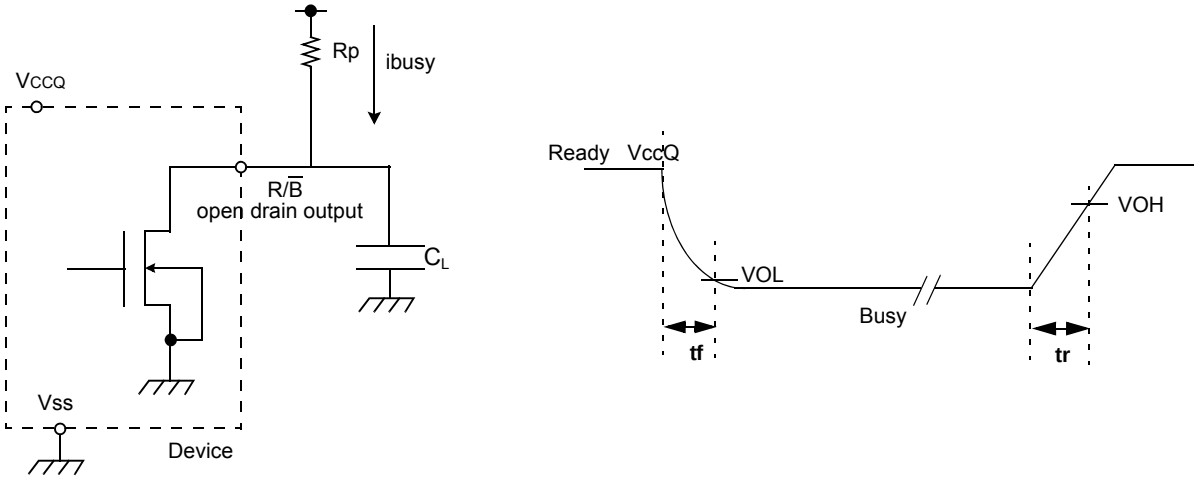
State A : LUN #0 is executing Multi-plane copy-back program operation, and LUN #1 is in ready state. So the host can issue Multi-plane read for copy-back command to LUN #1.
State B : LUN #0 is executing Multi-plane copy-back program operation and LUN #1 is executing Multi-plane read for copy-back operation.
State C : Multi-plane read for copy-back operation on LUN #1 is completed and LUN #1 is ready for the next operation. LUN #0 is still executing Multi-plane copy-back program operation.
State D : Both LUN #0 and LUN #1 are executing Multi-plane copy-back program operation.
State E : LUN #1 is still executing a Multi-plane copy-back program operation, and LUN #0 is in ready for the next operation.
State F : Both LUN #0 and LUN #1 are ready.

NOTE :
1) For address followed by C0h command, refer to the buffer address Table 23

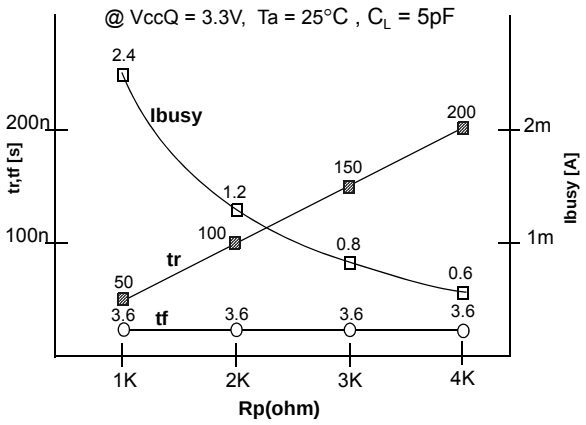
Depending on the above process, the system can operate Interleave Multi-plane copy-back program on LUN #0 and LUN #1 alternatively.

5.5 Ready/$\overline{\text{Busy}}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart. Its value can be determined by the following guidance.



Rp vs tr ,tf & Rp vs ibusy



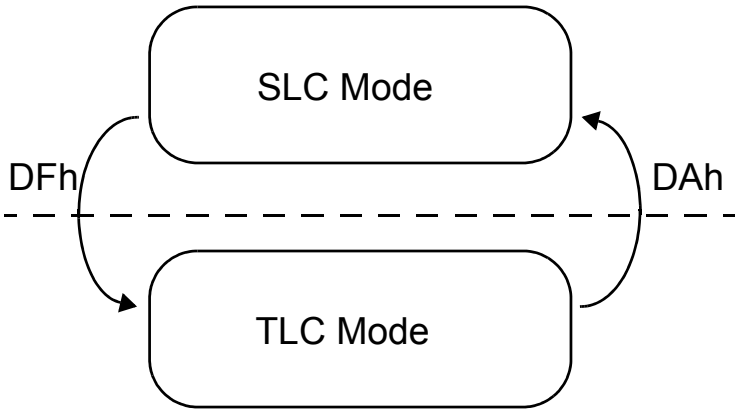
Rp value guidance

$$Rp(min, 3.3V\ part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

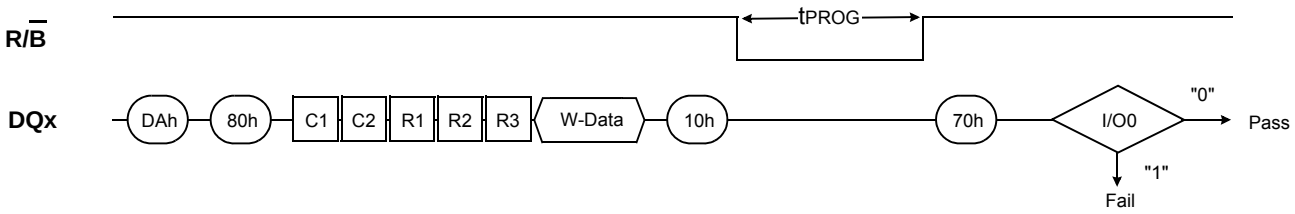
where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.
Rp(max) is determined by maximum permissible limit of tr

5.6 Mode Change

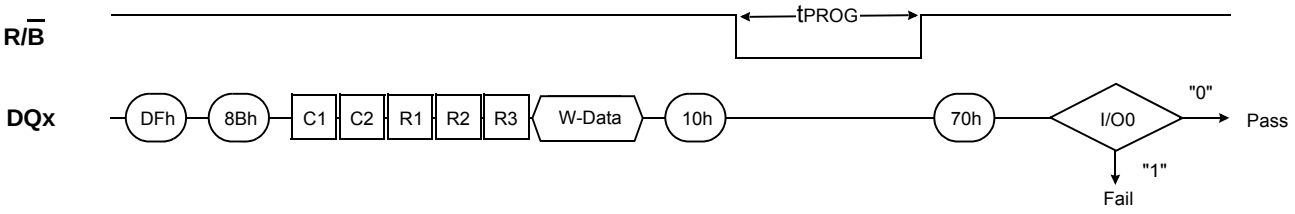
The device can support two type of operation: SLC mode operation and TLC mode operation.
SLC mode expects to be operated with data which requires frequent update, high-speed and high-reliability. On the other side TLC mode expects to be operated with data which is large-sized or sequential.
After initial power-up, device is ready to operate with TLC mode. In order to operate with SLC mode, DAh command must be added in front of normal command. For example, in case of Page Program operation, 80h command must be followed by 10h confirm command. If the page should be programmed reliably, DAh command must be added in front of 80h. Once device enters into SLC mode, it can be used reliably without additional DAh command until it meets SLC mode termination command DFh. As well as Program Operation, DAh command should be added in front of SLC mode Read or Erase Operation in order to Read or Erase SLC mode-programmed page.
The important thing is that SLC operation should access only the pages which are defined from 00h to 3Fh.
In a block, once the device enter a certain mode, it cannot be changed to the other mode.



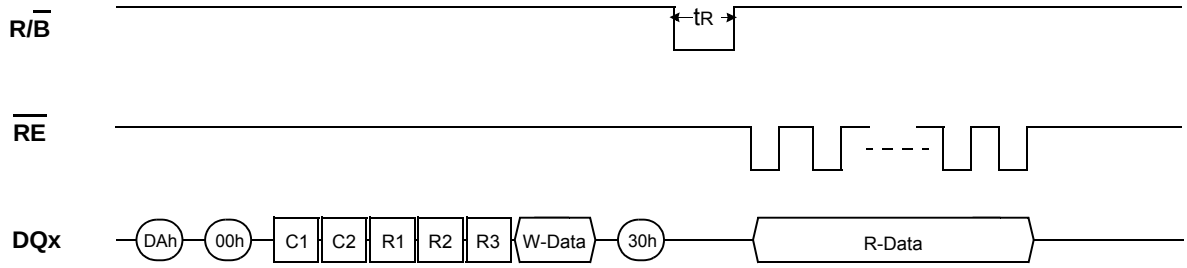
SLC Program Operation



Restoring to TLC mode Program Operation



SLC Read Operation



NOTE :
SLC mode read must be used in the block which has beed programmed with SLC mode program.

SLC Block Erase Operation