Jackson Ludwig

CSE 222 Final

Truth Table:

Binary				7-Segment Code						
w	x	у	Z	а	b	С	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	0	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	0	0	1	1
1	0	1	0	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	1	1	1
1	1	0	0	1	0	0	1	1	1	0
1	1	0	1	1	1	1	1	1	1	0
1	1	1	0	1	0	0	1	1	1	1
1	1	1	1	1	0	0	0	1	1	1

Un-simplified Boolean Equations:

A:

• $\overline{W} \overline{X} \overline{Y} \overline{Z} + \overline{W} \overline{X} Y \overline{Z} + \overline{W} \overline{X} Y Z + \overline{W} X \overline{Y} Z + \overline{W} X \overline{Y} Z + W \overline{X} \overline{Y} \overline{Z} + W \overline{X} \overline{Y} Z + W \overline{X} \overline{X} Z$

B:

• $\overline{W} \, \overline{X} \, \overline{Y} \, \overline{Z} + \overline{W} \, \overline{X} \, \overline{Y} \, \overline{Z} + \overline{W} \, \overline{X} \, Y \, \overline{Z} + \overline{W} \, \overline{X} \, Y \, Z + \overline{W} \, X \, \overline{Y} \, \overline{Z} + \overline{W} \, X \, Y \, Z + W \, \overline{X} \, \overline{Y} \, \overline{Z} + W \, \overline{X} \, \overline{Y} \, \overline{Z} + W \, \overline{X} \, \overline{Y} \, \overline{Z} + W \, \overline{X} \, \overline{Y} \, Z + W \, \overline{X} \, \overline{Y} \, \overline{Z} + W \, \overline{X} \, \overline{Z} + W \, \overline{X} \, \overline{Z} + W \, \overline{X} \, \overline{Z} + W \, \overline{Z} \, \overline{Z$

C:

D:

• $\overline{W} \overline{X} \overline{Y} \overline{Z} + \overline{W} \overline{X} Y \overline{Z} + \overline{W} \overline{X} Y Z + \overline{W} X \overline{Y} Z + \overline{W} X \overline{Y} \overline{Z} + W \overline{X} \overline{Y} \overline{Z} + W \overline{X} \overline{Y} \overline{Z} + W X \overline{Z} +$

E:

• $\overline{W} \, \overline{X} \, \overline{Y} \, \overline{Z} + \overline{W} \, \overline{X} \, Y \, \overline{Z} + \overline{W} \, \overline{X} \, Y \, Z + \overline{W} \, X \, Y \, \overline{Z} + W \, \overline{X} \, \overline{Y} \, \overline{Z} + W \, \overline{X} \, \overline{Y} \, \overline{Z} + W \, X \, \overline{Z$

F:

G:

Simplified circuits:





