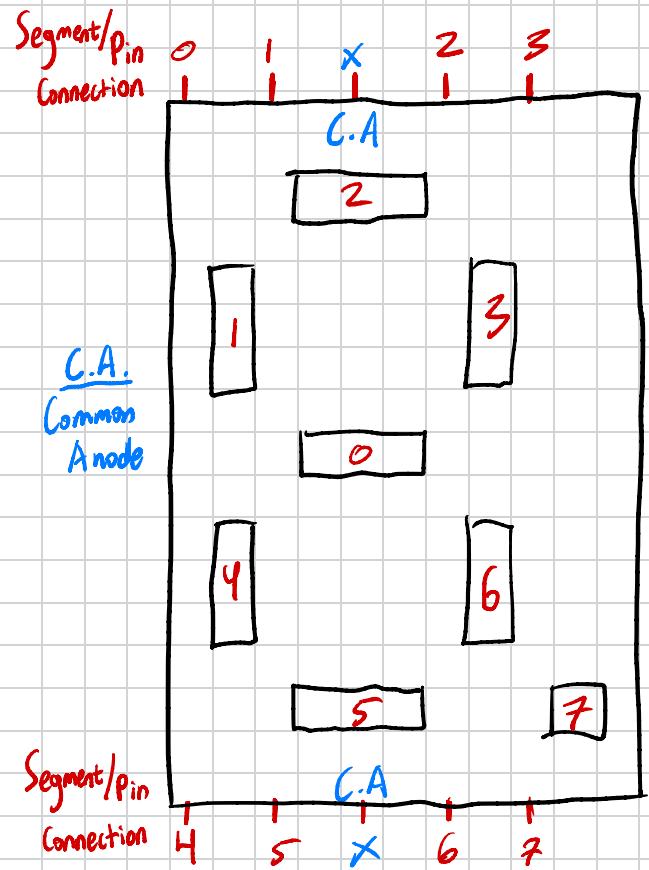
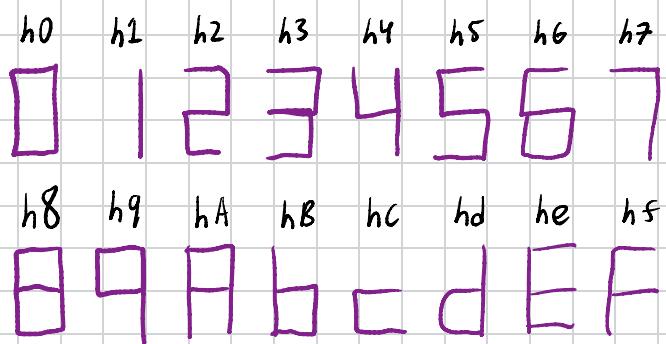


# UA 5651 - 11EWRS Mapping



# Display Design

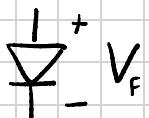


# Display Truth Table

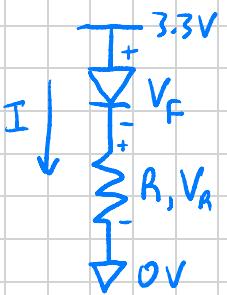
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
seg 0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
seg 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
seg 2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
seg 3	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
seg 4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
seg 5	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
seg 6	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

# Display Resistor Calculations

Each segment in our circuit may be drawn:



For forward voltage  $V_F = 2.1V$  typical.  
Maximum forward current is  $I_{max} = 30mA$ .



Using our 3.3V rail, we add a resistor to yield:

$$\text{Desiring an } I \text{ between } 5-20mA, \text{ we see the relation: } \frac{V_R}{I} = R$$

With  $V_R = 1.2V$ , if  $I = 5mA \Rightarrow R = 240\Omega$ ; if  $I = 20mA \Rightarrow R = 60\Omega$ .

Given that I want to reduce power consumption, and that a test of  $240\Omega$  revealed that the segment was plenty bright, I chose to use  $240\Omega$  resistors across each segment to ensure each was equally bright with equal current.

# Lab 1

<u>Signal</u>	<u>bits</u>	<u>logic</u>	<u>Description</u>
clk	/	input	48 MHz clk on FPGA
dip	[3:0]	input	DIP switches
led	[2:0]	output	Onboard LED's
seg	[6:0]	output	7-seg display through GPIO

## LED Logic:

dip3	dip2	led1
0	0	0
0	1	0
1	0	0
1	1	1

Logic Statement

$$\text{led1} = \text{dip3} \& \text{ dip2}$$

↑  
AND

dip1	dip0	led0
0	0	0
0	1	1
1	0	1
1	1	0

Logic Statement

$$\text{led0} = \text{dip1} \mid \text{dip0}$$

↑  
OR

led2 must blink at 2.4 Hz

FPGA has 2 onboard oscillators:

↳ Low Frequency LFOSC, at 10 kHz;

↳ High Frequency HFOSC, at 48 MHz.

Implementing a counter that divides the frequency by some  $x$ , where:  $\frac{48 \text{ MHz}}{x} = 2.4 \text{ Hz} \rightarrow x = 20 \text{ million}$

yields a blinking led at 2.4 Hz.

$2^{25} = 33.5 \text{ million}$ , so a 25 bit counter may be used.

