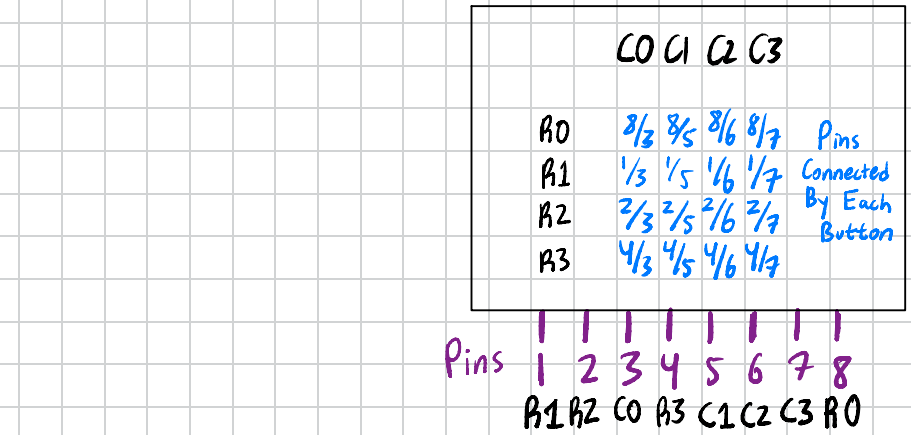
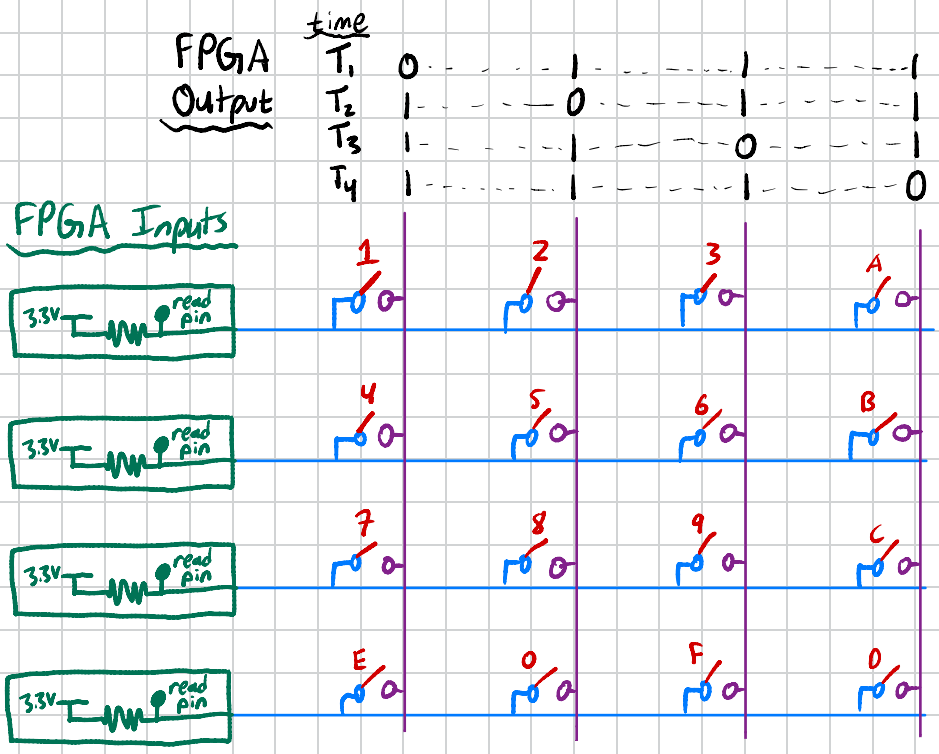
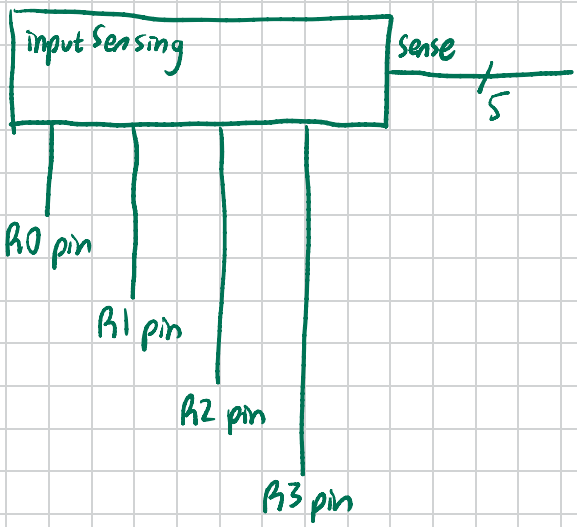
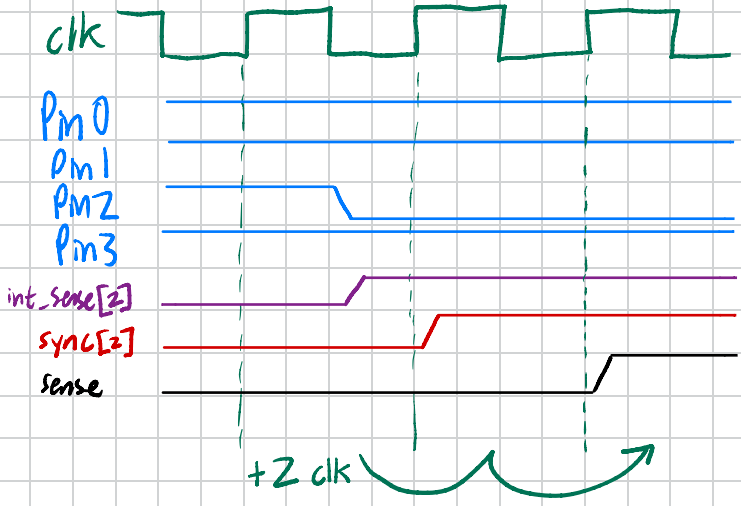
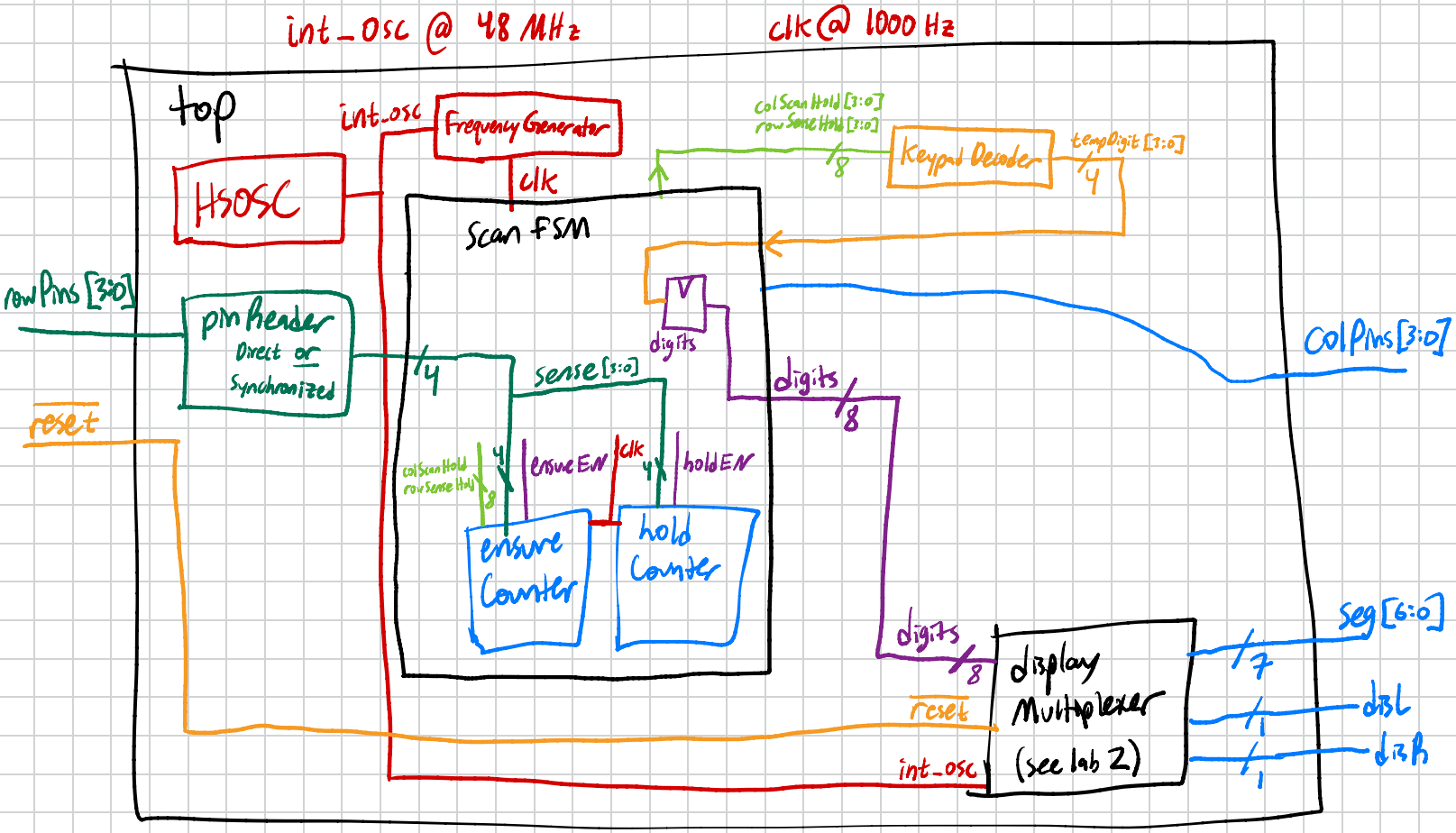

C0 C1 C2 C3
R0 8/3 8/5 8/6 8/7
R1 1/3 1/5 1/6 1/7
R2 2/3 2/5 2/6 2/7
R3 4/3 4/5 4/6 4/7
Pins Connected By Each Button
Pins 1 2 3 4 5 6 7 8
R1 R2 C0 R3 C1 C2 C3 R0


FPGA Output
time
T1
T2
T3
T4
FPGA Inputs
3.3V
read pin
1
2
3
A
4
5
6
B
7
8
9
C
E
0
F
D



Sense = 4'b0 if 0 or 2+ inputs
Sense = 4'b #, with input on RO = sense[0]
R1 = sense[1]
R2 = sense[2]
R3 = sense[3]




int_osc @ 48 MHz
clk @ 1000 Hz
top
int_osc
Frequency Generator
clk
HSOSC
colScanHold [3:0]
rowSenseHold [3:0]
8
Keypad Decoder
tempDigit [3:0]
4
Scan FSM
rowPins [3:0]
pin Header
Direct or Synchronized
4
digits
V
colPins [3:0]
sense [3:0]
digits
8
reset
colScanHold
rowSenseHold
8
4
ensureEN
clk
4
holdEN
ensure Counter
hold Counter
digits
8
display Multiplexer (see lab 2)
reset
int_osc
seg [6:0]
7
dig1
1
dig0
1