to IWDG LSI RC 32 kHz LSCO to RTC and LCD OSC32_OUT LSE OSC 32.768 kHz /32 OSC32_IN LSE LSI HSE to PWR SYSCLK МСО / 1→16 HSI16 Clock RC48 source AHB HCLK FCLK Cortex free running clock control PRESC / 1,2,..512 HSE OSC 4-48 MHz to Cortex system timer HSE / 8 OSC_IN Clock MSI SYSCLK APB1 PRESC PCLK1 HSI16 to APB1 peripherals / 1,2,4,8,16 x1 or x2 to TIMx 16 MHz x=2,3,6,7 LSE HSI16 SYSCLK to USARTx x=2,3,4 to LPUART1 MSI RC 100 kHz – 48 MHz to I2Cx x=1,2,3,4 LSI LSE HSI16 to LPTIMx x=1,2 HSI16to SWPMI HSI16 HSE MSI PCLK2 APB2 PRESC / M to APB2 peripherals PLLSAI2CLK VCO / P / 1,2,4,8,16 PLL48M1CLK -[xN] /Q x1 or x2 to TIMx PLLCLK / R x=1,15,16 to
USART1 PLLSAI1CLK VCO PLL48M2CLK χN / Q MSI PLLADC1CLK RNG, SDMMC / R PLLSAI1(2) to ADCx SYSCLK (x = 1,2)HSI16 HSI RC to SAI1 HSI16 CRS to DFSDM1 SYSCLK SAI1_EXTCLK

Figure 13. Clock tree



MS49687V4

Only SYSCLK coud be selected on STM32L41xxx and STM32L42xxx devices.
 PLLSAI1 not available on STM32L41xxx and STM32L42xxx devices