**ALGORITHM FOR SOLUTION OF TRAVELLING SALESMAN PROBLEM**

General Note :- This note is for finding a polynomial time solution for the "Travelling Salesman Problem" for a "Complete graph" for any number of vertices. The example that is solved in this document is taken from the internet, because this example gives a more detailed view of how the solution works.

**NOTATION SECTION**

A brief description about the Notations.

Beginning of Notations.

A notation is followed by '::-' characters. After '::-' characters, an explanation is given about the notation starting in the next line. In order to make it simple , I have given the examples in the notation itself , in order to explain the notation.

The vertices of a graph can be alphabets, numbers or a combination of both ie:- alphanumeric characters.

[] ::-

The square brackets denote a partial circuit . A partial circuit is a graph in which any vertex of the graph is joined to another vertex by only a single edge. The partial circuit may be empty or it may consists of vertices or both vertices and edges.

[a] ::-

Denotes a partial circuit containing a single vertex or it denotes a single vertex. Here it denotes a partial circuit containing a vertex named 'a'.

[a,b] ::-

Denotes that vertex 'a' is joined to vertex 'b' or that there is an edge which joins vertex 'a' with vertex 'b'. Here each vertex is separated by a comma.

[a,b,c] ::-

Denotes that vertex 'a' is joined to vertex 'b' and vertex 'b' is joined to vertex 'c'.

So in the '[]' notation, any number of vertices( each vertex separtated by comma ) can be written.

[a,b,c,a] ::-

Denotes a partial circuit in which it is also a hamilton circuit, because here vertex 'a' is joined to vertex 'b' and vertex 'b' is joined to vertex 'c' and vertex 'c' is joined to vertex 'a'. This partial circuit can also be written as [b,c,a,b]. So [a,b,c,a] is the same partial circuit as that of [b,c,a,b].

w[a,b,c] ::-

Denotes the weight of the partial circuit. This weight is the sum total of all the individual weights of the edges of the partial circuit. For eg:- if w[a,b] = 20 and w[b,c] = 30, then w[a,b,c] = w[a,b] + w[b,c] = 20 + 30 = 50.

[a,b,c] + [b,c,d] = [a,b,c,d] ::-

Here the two partial circuits [a,b,c] and [b,c,d] are combined to get [a,b,c,d] because the edge of [b,c] is common in both partial circuits. Here the total weight of [a,b,c,d] should be got by taking into consideration the common edge of [b,c]. So w[b,c] only needs to be added once.

For eg:-

if

w[a,b,c] = w[a,b] + w[b,c] = 20 + 30 = 50

and

w[b,c,d] = w[b,c] + w[c,d] = 30 + 40 = 70

and

if [a,b,c,d] = [a,b,c] + [b,c,d]

Then,

w[a,b,c,d] = w[a,b] + w[b,c] + w[c,d] = 20 + 30 + 40 = 90

So w[a,b,c,d] is not got by directly adding the weights of w[a,b,c] and w[b,c,d] , since there is a common edge of [b,c] present in both [a,b,c] and [b,c,d]. So w[a,b,c,d] is not equal to w[a,b,c] + w[b,c,d] ie:- not equal to 120 (50 + 70 = 120).

ec[a] ::-

Denotes an 'edge count' of the vertex 'a'. An 'edge count' is the number of edges attached to a vertex. For eg:- in [a,b,c] , ec[a] = 1, ec[b] = 2 and ec[c] = 1. Here the edge count of [b] is 2 since there are 2 edges attached to vertex 'b'. ec[a] = 1 , because there is only one edge attached to vertex 'a'. In a partial circuit, the edge count of each vertex should be less than or equal to 2, to satisfy the criterion of a hamilton circuit, when the partial circuit is used to form the hamilton circuit in the end of the process.

Section #1.m (BEGIN) ::-

This denotes the section of "Example 1". 'm' denotes any number greater than or equal to one. Also 'BEGIN' denotes the beginning of the section.

Section #1.m (END) ::-

This denotes the section of "Example 1". 'm' denotes any number greater than or equal to one. Also 'END' denotes the end of the section.

Step-m ::-

Here 'Step-m' means the step number of an algorithm where 'm' denotes any number greater than or equal to one.

->{Dm} ::-

Here 'D' means description. 'm' stands for any number greater than or equal to one. This marker ie:- '->{Dm}' gives the statement number of the statement which it marks ( The statement which is marked precedes the '->{Dm}' marker ). This marker is then written as '->Dm' elsewhere which gives a description of the statement which '->{Dm}' has marked. This marker is used mainly inside sections when space is required for writing descriptions. (The description of the notation '->Dm' is given below.)

->Dm. ::-

Here 'D' means description and 'm' stands for any number greater than or equal to one. This marker ie:- '->Dm' gives a description of the statement which it has marked.

->Lm ::-

Here 'L' means Level and 'm' stands for any number greater than or equal to one. This marker ie:- '->Lm' gives the Level number to which the partial circuit will be assigned.

NPC ::-

Here 'NPC' means necessary partial circuit. A necessary partial circuit is a partial circuit which will the first partial circuit used in the process of finding a hamilton circuit.

->{NPC-m} ::-

Here 'NPC' means 'necessary partial circuit'. 'm' stand for any number greater than or equal to one. This marker ie:- '->{NPC-m}' serves as a marker of the partial circuit which is to be taken as a necessary partial circuit.

->NPC-m ::-

Here 'NPC' means 'necessary partial circuit' and 'm' stands for any number greater than or equal to one. This marker shows the statement number which gives the details of the process that occurs with the necessary partial circuit when used in finding the minimum weight hamilton circuit.

[NPC-m-BEGIN] ::-

Here 'NPC' means 'necessary partial circuit' and 'm' stands for any number greater than or equal to one. This marker ie:- '[NPC-m-BEGIN]' marks the beginning of the process of finding the hamilton circuit using 'NPC-m'.

[NPC-m-END] ::-

Here 'NPC' means 'necessary partial circuit' and 'm' stands for any number greater than or equal to one. This marker ie:- '[NPC-m-END]' marks the end of the process of finding the hamilton circuit using 'NPC-m'.

PR-m ::-

Here 'PR-m' means property number 'm' where 'm' is any number greater than or equal to one. 'PR-m' is a marker of the description of a particular property of the joining of partial circuits.

C(n,r) ::-

This means a 'combination' of 'n' number of edges taken 'r' at a time. Here 'n' and 'r' are numbers. This 'combination' is the same combination that is there in mathematics. Here C(n,r) = n!/(r!\*(n-r)!)

End of Notations.

Below are given some examples for describing properties of joining of partial circuits.

1) PR-1

Two partial circuits are [a,b,c,d,e] and [e,f,g]. These two partial circuits can be joined at the common vertex 'e'. So the partial circuit after joining is [a,b,c,d,e,f,g].

2) PR-2

Two partial circuits are [a,b,c,d,e] and [d,e,f]. These two partial circuits can be joined at the common edge [d,e]. So the partial circuit after joining is [a,b,c,d,e,f].

3) PR-3

Two partial circuits are [a,b,c,d,e] and [c,f,d]. If these two partial circuits are joined, then ec[c] = 3 and ec[d] = 3 and the property of a hamilton circuit will be violated. But only this type of joining is allowed as an exception in which the edge [c,d] of [a,b,c,d,e] can be replaced by the partial circuit [c,f,d]. So the new partial circuit after joining is [a,b,c,f,d,e] while preserving the property of the hamilton circuit. In this joining of partial circuits , the edge of the partial circuit is replaced by two new edges and a new vertex is also added to the partial circuit.

4) PR-4

Two partial circuits are [a,b,c] and [a,d,c]. If the hamilton circuit required to be found consists of only 4 vertices, then these partial circuits can be joined. So if the hamilton circuit consists of only 4 vertices, then the two partial circuits can be joined to get the partial circuit [a,b,c,d,a]. This partial circuit ie:- [a,b,c,d,a] is a hamilton circuit consisting of 4 vertices.

5) PR-5

Two partial circuits are [a,b,c,d,e] and [c,f,e]. They cannot be joined, because ec[c] will become 3 and so it would violate the hamilton circuit property. Also here [c,d,e] cannot be replaced by [c,f,e] because if a new vertex 'f' is obtained, in its place another vertex 'd' becomes lost. So such a joining is not allowed.

6) PR-6

Two partial circuits are [a,b,c,d,e] and [d,f,g]. These two partial circuits cannot be joined at the common vertex 'd', since if the two partial circuits are joined, it would violate the edge count of vertex 'd' ie:- ec[d] would become 3.

7) PR-7

Two partial circuits are [a,b,c,d,e] and [e,d,f]. These two partial circuits cannot be joined at the common edge [d,e], because if the two partial circuits are joined, it would violate the edge count of vertex 'd' ie:- the ec[d] would become 3.

8) PR-8

Two partial circuits are [a,b,c,d,e] and [c,e,f]. These two partial circuits cannot be joined because if [c,e,f] is joined to [a,b,c,d,e], then ec[c] = 3 and ec[e] = 3. So such a joining is not allowed.

9) PR-9

Two partial circuits are [a,b,c,d,e] and [c,e,d]. These two partial circuits cannot be joined because if [c,e,d] is joined to [a,b,c,d,e], then the ec[c] will become 3. So such a joining is not allowed.

So the only type of joining of partial circuits which are allowed are given in PR-1 , PR-2 and PR-3. PR-4 joining is only allowed for examples in which the hamilton circuit consists of 4 vertices only. PR-5 , PR-6 , PR-7 , PR-8 and PR-9 are important examples where joining of partial circuits are not allowed. A main point is that only PR-1 , PR-2 , PR-3 and PR-4 are the only type of joinings that are allowed and no other type of joinings are allowed.

A very brief algorithm which gives a brief description of the main important points of the process of finding the minimum weight hamilton circuit is given below .

**ALGORITHM SECTION**

Beginning of Algorithm

Step-1.

Take the partial circuits of each vertex of the graph.

Step-2.

Sort the partial circuits of each vertex in ascending order according to their weights.

Step-3.

Put the sorted partial circuits present under each vertex into the appropriate Level numbers.

Step-4.

Sort the partial circuits under each level numbers in descending order according to their weights.

Step-5.

Carry out the process for finding the hamilton circuit as shown in Section #1.8 for the example in the document. The hamilton circuit obtained in this step of the algorithm is assumed to be the minimum weight hamilton circuit.

Step-6.

To find out if there are lesser weight hamilton circuits than the hamilton circuit obtained in Step-5 , further processing is to be done which is as follows. Group the partial circuits of the graph (the partial circuits which are present in Section #1.2 in this example ) together and sort them in ascending order according to their weights as done in Section #1.10 in this example. ( Please note that in Section #1.9, it is not necesssary to sort the partial circuits in ascending order, as all the partial circuits have to be processed anyway , but because if it is sorted, minimum weight hamilton circuits will be got quicker. But even if it is quicker, still all the partial circuits have to be processed. So it is not a necessity to sort the partial circuits in Section #1.9 ).

Step-7.

Take each necessary partial circuit from the sorted group (as given in Section #1.10 of this example ) and carry out the same process that is done in Step-5 for each of the necessary partial circuit that is present in Section #1.10.

Step-8.

From the hamilton circuit obtained in Step-5 and all the other hamilton circuits obtained from the necessary partial circuits as done in Step-7, find the minimum weight hamilton circuit among them ( as shown in Section #1.12 for this example ). This minimum weight hamilton circuit is the final minimum weight hamilton circuit that is got by the algorithm.

End of Algorithm

**EXAMPLE SECTION**

Example 1

This example is taken from the Internet. The solution for the example is got in the process described from Section #1.1 to Section #1.12.

Section #1.1 (BEGIN)

In this section, the weights of the different edges connected to the different vertices of a 5 vertex graph is shown below. The minimum weight hamilton circuit of this graph has a weight of '16' as given in the internet.

Vertex a

w[a,b] = 1 ->{D1}

w[a,c] = 4 ->{D2}

w[a,d] = 4

w[a,e] = 3

Vertex b

w[b,a] = 1

w[b,c] = 2

w[b,d] = 2

w[b,e] = 4

Vertex c

w[c,a] = 4

w[c,b] = 2

w[c,d] = 6

w[c,e] = 5

Vertex d

w[d,a] = 4

w[d,b] = 2

w[d,c] = 6

w[d,e] = 7

Vertex e

w[e,a] = 3

w[e,b] = 4

w[e,c] = 5

w[e,d] = 7

->D1. This shows the heading marked 'Vertex a'.

->D2. This shows the weight of one of the edges ( namely edge [a,c] ) which is connected to Vertex a.

Section #1.1 (END)

Section #1.2 (BEGIN)

In this section a combination of the edges ( the edges are taken from Section #1.1 ) connected to a particular vertex is taken. For eg:- there are four edges connected to vertex a. So the number of combinations of the four edges connected to 'vertex a' by taking two edges at a time is C(4,2) = 4!/((4-2)!\*2!) = 6.

Vertex a

[b,a] + [a,c] = [b,a,c]

[b,a] + [a,d] = [b,a,d]

[b,a] + [a,e] = [b,a,e]

[c,a] + [a,d] = [c,a,d]

[c,a] + [a,e] = [c,a,e]

[d,a] + [a,e] = [d,a,e]

Vertex b

[a,b] + [b,c] = [a,b,c]

[a,b] + [b,d] = [a,b,d]

[a,b] + [b,e] = [a,b,e]

[c,b] + [b,d] = [c,b,d]

[c,b] + [b,e] = [c,b,e]

[d,b] + [b,e] = [d,b,e]

Vertex c

[a,c] + [c,b] = [a,c,b]

[a,c] + [c,d] = [a,c,d]

[a,c] + [c,e] = [a,c,e]

[b,c] + [c,d] = [b,c,d]

[b,c] + [c,e] = [b,c,e]

[d,c] + [c,e] = [d,c,e]

Vertex d

[a,d] + [d,b] = [a,d,b]

[a,d] + [d,c] = [a,d,c]

[a,d] + [d,e] = [a,d,e]

[b,d] + [d,c] = [b,d,c]

[b,d] + [d,e] = [b,d,e]

[c,d] + [d,e] = [c,d,e]

Vertex e

[a,e] + [e,b] = [a,e,b]

[a,e] + [e,c] = [a,e,c]

[a,e] + [e,d] = [a,e,d]

[b,e] + [e,c] = [b,e,c]

[b,e] + [e,d] = [b,e,d]

[c,e] + [e,d] = [c,e,d]

Section #1.2 (END)

Section #1.3 (BEGIN)

In this section, the weights of the partial circuits( these partial circuits were obtained in Section #1.2 ) of a particular vertex are given below.

Vertex a

w[b,a,c] = 1+4 = 5

w[b,a,d] = 1+4 = 5

w[b,a,e] = 1+3 = 4

w[c,a,d] = 4+4 = 8

w[c,a,e] = 4+3 = 7

w[d,a,e] = 4+3 = 7

Vertex b

w[a,b,c] = 1+2 = 3

w[a,b,d] = 1+2 = 3

w[a,b,e] = 1+4 = 5

w[c,b,d] = 2+2 = 4

w[c,b,e] = 2+4 = 6

w[d,b,e] = 2+4 = 6

Vertex c

w[a,c,b] = 4+2 = 6

w[a,c,d] = 4+6 = 10

w[a,c,e] = 4+5 = 9

w[b,c,d] = 2+6 = 8

w[b,c,e] = 2+5 = 7

w[d,c,e] = 6+5 = 11

Vertex d

w[a,d,b] = 4+2 = 6

w[a,d,c] = 4+6 = 10

w[a,d,e] = 4+7 = 11

w[b,d,c] = 2+6 = 8

w[b,d,e] = 2+7 = 9

w[c,d,e] = 6+7 = 13

Vertex e

w[a,e,b] = 3+4 = 7

w[a,e,c] = 3+5 = 8

w[a,e,d] = 3+7 = 10

w[b,e,c] = 4+5 = 9

w[b,e,d] = 4+7 = 11

w[c,e,d] = 5+7 = 12

Section #1.3 (END)

Section #1.4 (BEGIN)

In this section, the partial circuits ( ie:- the partial circuits present in Section #1.2 ) under each vertex are sorted in 'Ascending order' according to their weights.

Vertex a ( Sorted in ascending order )

[b,a] + [a,e] = [b,a,e] w[b,a,e] = 1+3 = 4

[b,a] + [a,c] = [b,a,c] w[b,a,c] = 1+4 = 5

[b,a] + [a,d] = [b,a,d] w[b,a,d] = 1+4 = 5

[c,a] + [a,e] = [c,a,e] w[c,a,e] = 4+3 = 7

[d,a] + [a,e] = [d,a,e] w[d,a,e] = 4+3 = 7

[c,a] + [a,d] = [c,a,d] w[c,a,d] = 4+4 = 8

Vertex b ( Sorted in ascending order )

[a,b] + [b,c] = [a,b,c] w[a,b,c] = 1+2 = 3

[a,b] + [b,d] = [a,b,d] w[a,b,d] = 1+2 = 3

[c,b] + [b,d] = [c,b,d] w[c,b,d] = 2+2 = 4

[a,b] + [b,e] = [a,b,e] w[a,b,e] = 1+4 = 5

[c,b] + [b,e] = [c,b,e] w[c,b,e] = 2+4 = 6

[d,b] + [b,e] = [d,b,e] w[d,b,e] = 2+4 = 6

Vertex c ( Sorted in ascending order )

[a,c] + [c,b] = [a,c,b] w[a,c,b] = 4+2 = 6

[b,c] + [c,e] = [b,c,e] w[b,c,e] = 2+5 = 7

[b,c] + [c,d] = [b,c,d] w[b,c,d] = 2+6 = 8

[a,c] + [c,e] = [a,c,e] w[a,c,e] = 4+5 = 9

[a,c] + [c,d] = [a,c,d] w[a,c,d] = 4+6 = 10

[d,c] + [c,e] = [d,c,e] w[d,c,e] = 6+5 = 11

Vertex d ( Sorted in ascending order )

[a,d] + [d,b] = [a,d,b] w[a,d,b] = 4+2 = 6

[b,d] + [d,c] = [b,d,c] w[b,d,c] = 2+6 = 8

[b,d] + [d,e] = [b,d,e] w[b,d,e] = 2+7 = 9

[a,d] + [d,c] = [a,d,c] w[a,d,c] = 4+6 = 10

[a,d] + [d,e] = [a,d,e] w[a,d,e] = 4+7 = 11

[c,d] + [d,e] = [c,d,e] w[c,d,e] = 6+7 = 13

Vertex e ( Sorted in ascending order )

[a,e] + [e,b] = [a,e,b] w[a,e,b] = 3+4 = 7

[a,e] + [e,c] = [a,e,c] w[a,e,c] = 3+5 = 8

[b,e] + [e,c] = [b,e,c] w[b,e,c] = 4+5 = 9

[a,e] + [e,d] = [a,e,d] w[a,e,d] = 3+7 = 10

[b,e] + [e,d] = [b,e,d] w[b,e,d] = 4+7 = 11

[c,e] + [e,d] = [c,e,d] w[c,e,d] = 5+7 = 12

Section #1.4 (END)

Section #1.5 (BEGIN)

Partial circuits from Section #1.4 are taken and written in this section. Here the partial circuits are marked with level numbers in order to determine to which the Level number the partial circuits will be assigned. The lowest weight partial circuit under a particular vertex will always go to Level number 1, and similarly the next higher weight partial circuits under a particular vertex will go the higher level numbers. So the marking is as follows.

Vertex a ( Sorted in ascending order )

[b,a] + [a,e] = [b,a,e] w[b,a,e] = 1+3 = 4 ->L1 ->{D3}

[b,a] + [a,c] = [b,a,c] w[b,a,c] = 1+4 = 5 ->L2 ->{D4}

[b,a] + [a,d] = [b,a,d] w[b,a,d] = 1+4 = 5 ->L3 ->{D5}

[c,a] + [a,e] = [c,a,e] w[c,a,e] = 4+3 = 7 ->L4 ->{D6}

[d,a] + [a,e] = [d,a,e] w[d,a,e] = 4+3 = 7 ->L5 ->{D7}

[c,a] + [a,d] = [c,a,d] w[c,a,d] = 4+4 = 8 ->L6 ->{D8}

Vertex b ( Sorted in ascending order )

[a,b] + [b,c] = [a,b,c] w[a,b,c] = 1+2 = 3 ->L1 ->{D9}

[a,b] + [b,d] = [a,b,d] w[a,b,d] = 1+2 = 3 ->L2 ->{D10}

[c,b] + [b,d] = [c,b,d] w[c,b,d] = 2+2 = 4 ->L3

[a,b] + [b,e] = [a,b,e] w[a,b,e] = 1+4 = 5 ->L4

[c,b] + [b,e] = [c,b,e] w[c,b,e] = 2+4 = 6 ->L5

[d,b] + [b,e] = [d,b,e] w[d,b,e] = 2+4 = 6 ->L6

Vertex c ( Sorted in ascending order )

[a,c] + [c,b] = [a,c,b] w[a,c,b] = 4+2 = 6 ->L1

[b,c] + [c,e] = [b,c,e] w[b,c,e] = 2+5 = 7 ->L2

[b,c] + [c,d] = [b,c,d] w[b,c,d] = 2+6 = 8 ->L3

[a,c] + [c,e] = [a,c,e] w[a,c,e] = 4+5 = 9 ->L4

[a,c] + [c,d] = [a,c,d] w[a,c,d] = 4+6 = 10 ->L5

[d,c] + [c,e] = [d,c,e] w[d,c,e] = 6+5 = 11 ->L6

Vertex d ( Sorted in ascending order )

[a,d] + [d,b] = [a,d,b] w[a,d,b] = 4+2 = 6 ->L1

[b,d] + [d,c] = [b,d,c] w[b,d,c] = 2+6 = 8 ->L2

[b,d] + [d,e] = [b,d,e] w[b,d,e] = 2+7 = 9 ->L3

[a,d] + [d,c] = [a,d,c] w[a,d,c] = 4+6 = 10 ->L4

[a,d] + [d,e] = [a,d,e] w[a,d,e] = 4+7 = 11 ->L5

[c,d] + [d,e] = [c,d,e] w[c,d,e] = 6+7 = 13 ->L6

Vertex e ( Sorted in ascending order )

[a,e] + [e,b] = [a,e,b] w[a,e,b] = 3+4 = 7 ->L1

[a,e] + [e,c] = [a,e,c] w[a,e,c] = 3+5 = 8 ->L2

[b,e] + [e,c] = [b,e,c] w[b,e,c] = 4+5 = 9 ->L3

[a,e] + [e,d] = [a,e,d] w[a,e,d] = 3+7 = 10 ->L4

[b,e] + [e,d] = [b,e,d] w[b,e,d] = 4+7 = 11 ->L5

[c,e] + [e,d] = [c,e,d] w[c,e,d] = 5+7 = 12 ->L6

->D3. [b,a,e] is the lowest weight partial circuit in vertex a. So it is grouped in Level1 as indicated by '->L1'.

->D4. [b,a,c] is the next higher weight partial circuit in vertex a. So it is grouped in Level2 as indicated by '->L2'.

->D5. [b,a,d] is the next higher weight partial circuit in vertex a. So it is grouped in Level3 as indicated by '->L3'.

->D6. [c,a,e] is the next higher weight partial circuit in vertex a. So it is grouped in Level4 as indicated by '->L4'.

->D7. [d,a,e] is the next higher weight partial circuit in vertex a. So it is grouped in Level5 as indicated by '->L5'.

->D8. [c,a,d] is the next higher weight partial circuit in vertex a. So it is grouped in Level6 as indicated by '->L6'.

->D9. [a,b,c] is the lowest weight partial circuit in vertex b. So it is grouped in Level1 as indicated by '->L1'.

->D10. [a,b,d] is the next higher weight in vertex b. So it is grouped in Level2 as indicated by '->L2'.

In the same way, all the other partial circuits are grouped in the various levels as given in the next section.

Section #1.5 (END)

Section #1.6 (BEGIN)

This section consists of the different Levels where the partial circuits ( the partial circuits are got from Section #1.5 ) which were marked in Section #1.5 are grouped together. Note that the group of partial circuits under Level1 is written at the beginning and the all the higher Level number groups are written subsequently below each other with the Level numbers of each level having an ascending order. For eg:- Level1 group is written first, then Level2 group , then Level3 group and so on until the last Level number group ( in this example the Last Level number is Level6 ).

Level1

[b,a] + [a,e] = [b,a,e] w[b,a,e] = 1+3 = 4

[a,b] + [b,c] = [a,b,c] w[a,b,c] = 1+2 = 3

[a,c] + [c,b] = [a,c,b] w[a,c,b] = 4+2 = 6

[a,d] + [d,b] = [a,d,b] w[a,d,b] = 4+2 = 6

[a,e] + [e,b] = [a,e,b] w[a,e,b] = 3+4 = 7

Level2

[b,a] + [a,c] = [b,a,c] w[b,a,c] = 1+4 = 5

[a,b] + [b,d] = [a,b,d] w[a,b,d] = 1+2 = 3

[b,c] + [c,e] = [b,c,e] w[b,c,e] = 2+5 = 7

[b,d] + [d,c] = [b,d,c] w[b,d,c] = 2+6 = 8

[a,e] + [e,c] = [a,e,c] w[a,e,c] = 3+5 = 8

Level3

[b,a] + [a,d] = [b,a,d] w[b,a,d] = 1+4 = 5

[c,b] + [b,d] = [c,b,d] w[c,b,d] = 2+2 = 4

[b,c] + [c,d] = [b,c,d] w[b,c,d] = 2+6 = 8

[b,d] + [d,e] = [b,d,e] w[b,d,e] = 2+7 = 9

[b,e] + [e,c] = [b,e,c] w[b,e,c] = 4+5 = 9

Level4

[c,a] + [a,e] = [c,a,e] w[c,a,e] = 4+3 = 7

[a,b] + [b,e] = [a,b,e] w[a,b,e] = 1+4 = 5

[a,c] + [c,e] = [a,c,e] w[a,c,e] = 4+5 = 9

[a,d] + [d,c] = [a,d,c] w[a,d,c] = 4+6 = 10

[a,e] + [e,d] = [a,e,d] w[a,e,d] = 3+7 = 10

Level5

[d,a] + [a,e] = [d,a,e] w[d,a,e] = 4+3 = 7

[c,b] + [b,e] = [c,b,e] w[c,b,e] = 2+4 = 6

[a,c] + [c,d] = [a,c,d] w[a,c,d] = 4+6 = 10

[a,d] + [d,e] = [a,d,e] w[a,d,e] = 4+7 = 11

[b,e] + [e,d] = [b,e,d] w[b,e,d] = 4+7 = 11

Level6

[c,a] + [a,d] = [c,a,d] w[c,a,d] = 4+4 = 8

[d,b] + [b,e] = [d,b,e] w[d,b,e] = 2+4 = 6

[d,c] + [c,e] = [d,c,e] w[d,c,e] = 6+5 = 11

[c,d] + [d,e] = [c,d,e] w[c,d,e] = 6+7 = 13

[c,e] + [e,d] = [c,e,d] w[c,e,d] = 5+7 = 12

Section #1.6 (END)

Section #1.7 (BEGIN)

In this section , the partial circuits under each Level (The Levels are taken from Section #1.6 ) are sorted in 'Descending order' of their weights.

Level1 ( sorted in descending order )

[a,e] + [e,b] = [a,e,b] w[a,e,b] = 3+4 = 7

[a,c] + [c,b] = [a,c,b] w[a,c,b] = 4+2 = 6

[a,d] + [d,b] = [a,d,b] w[a,d,b] = 4+2 = 6

[b,a] + [a,e] = [b,a,e] w[b,a,e] = 1+3 = 4

[a,b] + [b,c] = [a,b,c] w[a,b,c] = 1+2 = 3

Level2 ( sorted in descending order )

[b,d] + [d,c] = [b,d,c] w[b,d,c] = 2+6 = 8

[a,e] + [e,c] = [a,e,c] w[a,e,c] = 3+5 = 8

[b,c] + [c,e] = [b,c,e] w[b,c,e] = 2+5 = 7

[b,a] + [a,c] = [b,a,c] w[b,a,c] = 1+4 = 5

[a,b] + [b,d] = [a,b,d] w[a,b,d] = 1+2 = 3

Level3 ( sorted in descending order )

[b,d] + [d,e] = [b,d,e] w[b,d,e] = 2+7 = 9

[b,e] + [e,c] = [b,e,c] w[b,e,c] = 4+5 = 9

[b,c] + [c,d] = [b,c,d] w[b,c,d] = 2+6 = 8

[b,a] + [a,d] = [b,a,d] w[b,a,d] = 1+4 = 5

[c,b] + [b,d] = [c,b,d] w[c,b,d] = 2+2 = 4

Level4 ( sorted in descending order )

[a,d] + [d,c] = [a,d,c] w[a,d,c] = 4+6 = 10

[a,e] + [e,d] = [a,e,d] w[a,e,d] = 3+7 = 10

[a,c] + [c,e] = [a,c,e] w[a,c,e] = 4+5 = 9

[c,a] + [a,e] = [c,a,e] w[c,a,e] = 4+3 = 7

[a,b] + [b,e] = [a,b,e] w[a,b,e] = 1+4 = 5

Level5 ( sorted in descending order )

[a,d] + [d,e] = [a,d,e] w[a,d,e] = 4+7 = 11

[b,e] + [e,d] = [b,e,d] w[b,e,d] = 4+7 = 11

[a,c] + [c,d] = [a,c,d] w[a,c,d] = 4+6 = 10

[d,a] + [a,e] = [d,a,e] w[d,a,e] = 4+3 = 7

[c,b] + [b,e] = [c,b,e] w[c,b,e] = 2+4 = 6

Level6 ( sorted in descending order )

[c,d] + [d,e] = [c,d,e] w[c,d,e] = 6+7 = 13

[c,e] + [e,d] = [c,e,d] w[c,e,d] = 5+7 = 12

[d,c] + [c,e] = [d,c,e] w[d,c,e] = 6+5 = 11

[c,a] + [a,d] = [c,a,d] w[c,a,d] = 4+4 = 8

[d,b] + [b,e] = [d,b,e] w[d,b,e] = 2+4 = 6

Section #1.7 (END)

Section #1.8 (BEGIN)

Now in order to find the minimum weight hamilton circuit, the partial circuits which are necessary for forming the minimum weight hamilton circuit are found from the Level groups given in Section #1.7. The partial circuits are taken one by one for checking starting from the beginning of Level1 and proceeding downwards towards the last partial circuit of the last Level until a hamilton circuit is found.

1) Take [a,e,b] from Level1. Since hamilton circuit rule is not violated, [a,e,b] is taken for forming the hamilton circuit. So the partial circuit is [a,e,b].

2) Take [a,c,b] from Level1. [a,c,b] does not fit with [a,e,b] since [a,c,b] does not satisfy PR-1 , PR-2 or PR-3 properties of the joining of partial circuits. Also PR-4 property is not satisfied here, since a 5 vertex hamilton circuit is required here and not a 4 vertex hamilton circuit ( 'PR-1' , 'PR-2' , PR-3' and 'PR-4' are properties of the joining of partial circuits as given in the explanation examples given after the notation explanations ). So [a,c,b] is not taken.

3) Take [a,d,b] from Level1. [a,d,b] does not fit with [a,e,b] , since [a,d,b] does not satisfy PR-1 , PR-2 or PR-3 properties. So [a,d,b] is not taken.

4) Take [b,a,e] from Level1. [b,a,e] does not fit with [a,e,b] , since [b,a,e] does not satisfy PR-1 , PR-2 or PR-3 properties. So [b,a,e] is not taken.

5) Take [a,b,c] from Level1. [a,b,c] does not fit with [a,e,b] , since [a,b,c] does not satisfy PR-1 , PR-2 or PR-3 properties. So [a,b,c] is not taken.

6) Take [b,d,c] from Level2. [b,d,c] satisfies PR-1 property. [b,d,c] fits with [a,e,b] to form the partial circuit [a,e,b,d,c].

7) Take [a,e,c] from Level2. [a,e,c] does not fit with [a,e,b,d,c] , since [a,e,c] does not satisfy PR-1 , PR-2 or PR-3 properties. So [a,e,c] is not taken.

8) Take [b,c,e] from Level2. [b,c,e] does not fit with [a,e,b,d,c] , since [b,c,e] does not satisfy PR-1 , PR-2 or PR-3 properties. So [b,c,e] is not taken.

9) Take [b,a,c] from Level2. [b,a,c] does not fit with [a,e,b,d,c] , since [b,a,c] does not satisfy PR-1 , PR-2 or PR-3 properties. So [b,a,c] is not taken.

10) Take [a,b,d] from Level2. [a,b,d] does not fit with [a,e,b,d,c] , since [a,b,d] does not satisfy PR-1 , PR-2 or PR-3 properties. So [a,b,d] is not taken.

11) Take [b,d,e] from Level3. [b,d,e] does not fit with [a,e,b,d,c] , since [b,d,e] does not satisfy PR-1 , PR-2 or PR-3 properties. So [b,d,e] is not taken.

12) Take [b,e,c] from Level3. [b,e,c] does not fit with [a,e,b,d,c] , since [b,e,c] does not satisfy PR-1 , PR-2 or PR-3 properties. So [b,e,c] is not taken.

13) Take [b,c,d] from Level3. [b,c,d] does not fit with [a,e,b,d,c] , since [b,c,d] does not satisfy PR-1 , PR-2 or PR-3 properties. So [b,c,d] is not taken.

14) Take [b,a,d] from Level3. [b,a,d] does not fit with [a,e,b,d,c] , since [b,a,d] does not satisfy PR-1 , PR-2 or PR-3 properties. So [b,a,d] is not taken.

15) Take [c,b,d] from Level3. [c,b,d] does not fit with [a,e,b,d,c] , since [c,b,d] does not satisfy PR-1 , PR-2 or PR-3 properties. So [c,b,d] is not taken.

16) Take [a,d,c] from Level4. [a,d,c] does not fit with [a,e,b,d,c] , since [a,d,c] does not satisfy PR-1 , PR-2 or PR-3 properties. So [a,d,c] is not taken.

17) Take [a,e,d] from Level4. [a,e,d] does not fit with [a,e,b,d,c] , since [a,e,d] does not satisfy PR-1 , PR-2 or PR-3 properties. So [a,e,d] is not taken.

18) Take [a,c,e] from Level4. [a,c,e] does not fit with [a,e,b,d,c] , since [a,c,e] does not satisfy PR-1 , PR-2 or PR-3 properties. So [a,c,e] is not taken.

19) Take [c,a,e] from Level4. [c,a,e] satisfies PR-2 property. [c,a,e] fits with [a,e,b,d,c] to form the hamilton circuit [a,e,b,d,c,a].

Therefore the hamilton circuit which is assumed to be of minimum weight is [a,e,b,d,c,a].

So [a,e,b,d,c,a] = [a,e,b] + [b,d,c] + [c,a,e]

Weight of [a,e,b,d,c,a] ie:- w[a,e,b,d,c,a] = w[a,e] + w[e,b] + w[b,d] + w[d,c] + w[c,a] = 3 + 4 + 2 + 6 + 4 = 19.

In order to know if there are lesser weight hamilton circuits , group the partial circuits of the different vertices present in Section #1.2 into one group. This group is written in the next section ie:- in Section #1.9.

Section #1.8 (END)

Section #1.9 (BEGIN)

Group the partial circuits present in Section #1.2 into one group here. The group is given below.

[b,a] + [a,c] = [b,a,c] w[b,a,c] = 1+4 = 5

[b,a] + [a,d] = [b,a,d] w[b,a,d] = 1+4 = 5

[b,a] + [a,e] = [b,a,e] w[b,a,e] = 1+3 = 4

[c,a] + [a,d] = [c,a,d] w[c,a,d] = 4+4 = 8

[c,a] + [a,e] = [c,a,e] w[c,a,e] = 4+3 = 7

[d,a] + [a,e] = [d,a,e] w[d,a,e] = 4+3 = 7

[a,b] + [b,c] = [a,b,c] w[a,b,c] = 1+2 = 3

[a,b] + [b,d] = [a,b,d] w[a,b,d] = 1+2 = 3

[a,b] + [b,e] = [a,b,e] w[a,b,e] = 1+4 = 5

[c,b] + [b,d] = [c,b,d] w[c,b,d] = 2+2 = 4

[c,b] + [b,e] = [c,b,e] w[c,b,e] = 2+4 = 6

[d,b] + [b,e] = [d,b,e] w[d,b,e] = 2+4 = 6

[a,c] + [c,b] = [a,c,b] w[a,c,b] = 4+2 = 6

[a,c] + [c,d] = [a,c,d] w[a,c,d] = 4+6 = 10

[a,c] + [c,e] = [a,c,e] w[a,c,e] = 4+5 = 9

[b,c] + [c,d] = [b,c,d] w[b,c,d] = 2+6 = 8

[b,c] + [c,e] = [b,c,e] w[b,c,e] = 2+5 = 7

[d,c] + [c,e] = [d,c,e] w[d,c,e] = 6+5 = 11

[a,d] + [d,b] = [a,d,b] w[a,d,b] = 4+2 = 6

[a,d] + [d,c] = [a,d,c] w[a,d,c] = 4+6 = 10

[a,d] + [d,e] = [a,d,e] w[a,d,e] = 4+7 = 11

[b,d] + [d,c] = [b,d,c] w[b,d,c] = 2+6 = 8

[b,d] + [d,e] = [b,d,e] w[b,d,e] = 2+7 = 9

[c,d] + [d,e] = [c,d,e] w[c,d,e] = 6+7 = 13

[a,e] + [e,b] = [a,e,b] w[a,e,b] = 3+4 = 7

[a,e] + [e,c] = [a,e,c] w[a,e,c] = 3+5 = 8

[a,e] + [e,d] = [a,e,d] w[a,e,d] = 3+7 = 10

[b,e] + [e,c] = [b,e,c] w[b,e,c] = 4+5 = 9

[b,e] + [e,d] = [b,e,d] w[b,e,d] = 4+7 = 11

[c,e] + [e,d] = [c,e,d] w[c,e,d] = 5+7 = 12

Section #1.9 (END)

Section #1.10 (BEGIN)

Sort the group in Section #1.9 according to their weights in ascending order. The sorted group is given below.

[a,b] + [b,c] = [a,b,c] w[a,b,c] = 1+2 = 3

[a,b] + [b,d] = [a,b,d] w[a,b,d] = 1+2 = 3

[b,a] + [a,e] = [b,a,e] w[b,a,e] = 1+3 = 4

[c,b] + [b,d] = [c,b,d] w[c,b,d] = 2+2 = 4

[b,a] + [a,c] = [b,a,c] w[b,a,c] = 1+4 = 5

[b,a] + [a,d] = [b,a,d] w[b,a,d] = 1+4 = 5

[a,b] + [b,e] = [a,b,e] w[a,b,e] = 1+4 = 5

[c,b] + [b,e] = [c,b,e] w[c,b,e] = 2+4 = 6

[d,b] + [b,e] = [d,b,e] w[d,b,e] = 2+4 = 6

[a,c] + [c,b] = [a,c,b] w[a,c,b] = 4+2 = 6

[a,d] + [d,b] = [a,d,b] w[a,d,b] = 4+2 = 6

[c,a] + [a,e] = [c,a,e] w[c,a,e] = 4+3 = 7

[d,a] + [a,e] = [d,a,e] w[d,a,e] = 4+3 = 7

[b,c] + [c,e] = [b,c,e] w[b,c,e] = 2+5 = 7

[a,e] + [e,b] = [a,e,b] w[a,e,b] = 3+4 = 7

[c,a] + [a,d] = [c,a,d] w[c,a,d] = 4+4 = 8

[b,c] + [c,d] = [b,c,d] w[b,c,d] = 2+6 = 8

[b,d] + [d,c] = [b,d,c] w[b,d,c] = 2+6 = 8

[a,e] + [e,c] = [a,e,c] w[a,e,c] = 3+5 = 8

[a,c] + [c,e] = [a,c,e] w[a,c,e] = 4+5 = 9

[b,d] + [d,e] = [b,d,e] w[b,d,e] = 2+7 = 9

[b,e] + [e,c] = [b,e,c] w[b,e,c] = 4+5 = 9

[a,c] + [c,d] = [a,c,d] w[a,c,d] = 4+6 = 10

[a,d] + [d,c] = [a,d,c] w[a,d,c] = 4+6 = 10

[a,e] + [e,d] = [a,e,d] w[a,e,d] = 3+7 = 10

[d,c] + [c,e] = [d,c,e] w[d,c,e] = 6+5 = 11

[a,d] + [d,e] = [a,d,e] w[a,d,e] = 4+7 = 11

[b,e] + [e,d] = [b,e,d] w[b,e,d] = 4+7 = 11

[c,e] + [e,d] = [c,e,d] w[c,e,d] = 5+7 = 12

[c,d] + [d,e] = [c,d,e] w[c,d,e] = 6+7 = 13

Section #1.10 (END)

Section #1.11 (BEGIN)

The sorted group from Section #1.10 is written here. Here each partial circuit is marked with necessary partial circuit number.

[a,b] + [b,c] = [a,b,c] w[a,b,c] = 1+2 = 3 ->{NPC-1}

[a,b] + [b,d] = [a,b,d] w[a,b,d] = 1+2 = 3 ->{NPC-2}

[b,a] + [a,e] = [b,a,e] w[b,a,e] = 1+3 = 4 ->{NPC-3}

[c,b] + [b,d] = [c,b,d] w[c,b,d] = 2+2 = 4 ->{NPC-4}

[b,a] + [a,c] = [b,a,c] w[b,a,c] = 1+4 = 5 ->{NPC-5}

[b,a] + [a,d] = [b,a,d] w[b,a,d] = 1+4 = 5 ->{NPC-6}

[a,b] + [b,e] = [a,b,e] w[a,b,e] = 1+4 = 5 ->{NPC-7}

[c,b] + [b,e] = [c,b,e] w[c,b,e] = 2+4 = 6 ->{NPC-8}

[d,b] + [b,e] = [d,b,e] w[d,b,e] = 2+4 = 6 ->{NPC-9}

[a,c] + [c,b] = [a,c,b] w[a,c,b] = 4+2 = 6 ->{NPC-10}

[a,d] + [d,b] = [a,d,b] w[a,d,b] = 4+2 = 6 ->{NPC-11}

[c,a] + [a,e] = [c,a,e] w[c,a,e] = 4+3 = 7 ->{NPC-12}

[d,a] + [a,e] = [d,a,e] w[d,a,e] = 4+3 = 7 ->{NPC-13}

[b,c] + [c,e] = [b,c,e] w[b,c,e] = 2+5 = 7 ->{NPC-14}

[a,e] + [e,b] = [a,e,b] w[a,e,b] = 3+4 = 7 ->{NPC-15}

[c,a] + [a,d] = [c,a,d] w[c,a,d] = 4+4 = 8 ->{NPC-16}

[b,c] + [c,d] = [b,c,d] w[b,c,d] = 2+6 = 8 ->{NPC-17}

[b,d] + [d,c] = [b,d,c] w[b,d,c] = 2+6 = 8 ->{NPC-18}

[a,e] + [e,c] = [a,e,c] w[a,e,c] = 3+5 = 8 ->{NPC-19}

[a,c] + [c,e] = [a,c,e] w[a,c,e] = 4+5 = 9 ->{NPC-20}

[b,d] + [d,e] = [b,d,e] w[b,d,e] = 2+7 = 9 ->{NPC-21}

[b,e] + [e,c] = [b,e,c] w[b,e,c] = 4+5 = 9 ->{NPC-22}

[a,c] + [c,d] = [a,c,d] w[a,c,d] = 4+6 = 10 ->{NPC-23}

[a,d] + [d,c] = [a,d,c] w[a,d,c] = 4+6 = 10 ->{NPC-24}

[a,e] + [e,d] = [a,e,d] w[a,e,d] = 3+7 = 10 ->{NPC-25}

[d,c] + [c,e] = [d,c,e] w[d,c,e] = 6+5 = 11 ->{NPC-26}

[a,d] + [d,e] = [a,d,e] w[a,d,e] = 4+7 = 11 ->{NPC-27}

[b,e] + [e,d] = [b,e,d] w[b,e,d] = 4+7 = 11 ->{NPC-28}

[c,e] + [e,d] = [c,e,d] w[c,e,d] = 5+7 = 12 ->{NPC-29}

[c,d] + [d,e] = [c,d,e] w[c,d,e] = 6+7 = 13 ->{NPC-30}

Section #1.11 (END)

Section #1.12 (BEGIN)

In this section, each necessary partial circuit present in Section #1.11 is used in finding the hamilton circuits.

Here the process of finding the hamilton circuits begins with 'NPC-1' .

->NPC-1.

[NPC-1-BEGIN]

Take [a,b,c] as a necessary partial circuit. Since hamilton circuit rule is not violated, [a,b,c] is taken for forming the hamilton circuit. So the partial circuit is [a,b,c].

Now use the same process that is done in Section #1.8.

1) Take [a,e,b] from Level1. [a,e,b] satisfies PR-3 property. So [a,e,b] fits with [a,b,c] to form [a,e,b,c].

2) Take [a,c,b] from Level1. [a,c,b] does not satisfy PR-4 property since a 5 vertex hamilton circuit is required here. So [a,c,b] is not taken.

3) Take [a,d,b] from Level1. [a,d,b] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,d,b] is not taken.

4) Take [b,a,e] from Level1. [b,a,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,a,e] is not taken.

5) Take [a,b,c] from Level1. [a,b,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,b,c] is not taken.

6) Take [b,d,c] from Level2. [b,d,c] satisfies PR-3 property. So [b,d,c] is joined with [a,e,b,c] to form [a,e,b,d,c].

7) Take [a,e,c] from Level2. [a,e,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,e,c] is not taken.

8) Take [b,c,e] from Level2. [b,c,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,c,e] is not taken.

9) Take [b,a,c] from Level2. [b,a,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,a,c] is not taken.

10) Take [a,b,d] from Level2. [a,b,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,b,d] is not taken.

11) Take [b,d,e] from Level3. [b,d,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,d,e] is not taken.

12) Take [b,e,c] from Level3. [b,e,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,e,c] is not taken.

13) Take [b,c,d] from Level3. [b,c,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,c,d] is not taken.

14) Take [b,a,d] from Level3. [b,a,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,a,d] is not taken.

15) Take [c,b,d] from Level3. [c,b,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [c,b,d] is not taken.

16) Take [a,d,c] from Level4. [a,d,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,d,c] is not taken.

17) Take [a,e,d] from Level4. [a,e,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,e,d] is not taken.

18) Take [a,c,e] from Level4. [a,c,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,c,e] is not taken.

19) Take [c,a,e] from Level4. [c,a,e] satisfies PR-2 property. So [c,a,e] is joined with [a,e,b,d,c] to form [a,e,b,d,c,a].

So [a,e,b,d,c,a] = [a,b,c] + [a,e,b] + [b,d,c] + [c,a,e]

w[a,e,b,d,c,a] = w[e,b] + w[b,d] + w[d,c] + w[c,a] + w[a,e] = 4 + 2 + 6 + 4 + 3 = 19.

[NPC-1-END]

->NPC-2.

[NPC-2-BEGIN]

Take [a,b,d] as a necessary partial circuit. Since hamilton circuit rule is not violated, [a,b,d] is taken for forming the hamilton circuit. So the partial circuit is [a,b,d].

Use the same process that is done in Section #1.8.

1) Take [a,e,b] from Level1. [a,e,b] satisfies PR-3 property. So [a,e,b] fits with [a,b,d] to form [a,e,b,d].

2) Take [a,c,b] from Level1. [a,c,b] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,c,b] is not taken.

3) Take [a,d,b] from Level1. [a,d,b] does not satisfy PR-4 property since a 5 vertex hamilton circuit is required. So [a,d,b] is not taken.

4) Take [b,a,e] from Level1. [b,a,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,a,e] is not taken.

5) Take [a,b,c] from Level1. [a,b,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,b,c] is not taken.

6) Take [b,d,c] from Level2. [b,d,c] satisfies PR-2 property. So [b,d,c] is joined with [a,e,b,d] to form [a,e,b,d,c].

7) Take [a,e,c] from Level2. [a,e,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,e,c] is not taken.

8) Take [b,c,e] from Level2. [b,c,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,c,e] is not taken.

9) Take [b,a,c] from Level2. [b,a,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,a,c] is not taken.

10) Take [a,b,d] from Level2. [a,b,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,b,d] is not taken.

11) Take [b,d,e] from Level3. [b,d,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,d,e] is not taken.

12) Take [b,e,c] from Level3. [b,e,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,e,c] is not taken.

13) Take [b,c,d] from Level3. [b,c,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,c,d] is not taken.

14) Take [b,a,d] from Level3. [b,a,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,a,d] is not taken.

15) Take [c,b,d] from Level3. [c,b,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [c,b,d] is not taken.

16) Take [a,d,c] from Level4. [a,d,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,d,c] is not taken.

17) Take [a,e,d] from Level4. [a,e,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,e,d] is not taken.

18) Take [a,c,e] from Level4. [a,c,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,c,e] is not taken.

19) Take [c,a,e] from Level4. [c,a,e] satisfies PR-2 property. So [c,a,e] fits with [a,e,b,d,c] to form [a,e,b,d,c,a].

[a,e,b,d,c,a] = [a,b,d] + [a,e,b] + [b,d,c] + [c,a,e]  
w[a,e,b,d,c,a] = w[e,b] + w[b,d] + w[d,c] + w[c,a] + w[a,e] = 4 + 2 + 6 + 4 + 3 = 19

[NPC-2-END]

->NPC-3.

[NPC-3-BEGIN]

Take [b,a,e] as a necessary partial circuit. Since hamilton circuit rule is not violated, [b,a,e] is taken for forming the hamilton circuit. So the partial circuit is [b,a,e].

Use the same process that is done in Section #1.8.

1) Take [a,e,b] from Level1. If [a,e,b] is joined with [b,a,e] , a 3 vertex hamilton circuit will be obtained. But a 5 vertex hamilton circuit is required here and not a 3 vertex hamilton circuit. So

[a,e,b] is not taken.

2) Take [a,c,b] from Level1. [a,c,b] satisfies PR-3 property. So [a,c,b] fits with [b,a,e] to form [b,c,a,e].

3) Take [a,d,b] from Level1. [a,d,b] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,d,b] is not taken.

4) Take [b,a,e] from Level1. [b,a,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,a,e] is not taken.

5) Take [a,b,c] from Level1. [a,b,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,b,c] is not taken.

6) Take [b,d,c] from Level2. [b,d,c] satisfies PR-3 property. So [b,d,c] fits with [b,c,a,e] to form [b,d,c,a,e].

7) Take [a,e,c] from Level2. [a,e,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,e,c] is not taken.

8) Take [b,c,e] from Level2. [b,c,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,c,e] is not taken.

9) Take [b,a,c] from Level2. [b,a,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,a,c] is not taken.

10) Take [a,b,d] from Level2. [a,b,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,b,d] is not taken.

11) Take [b,d,e] from Level3. [b,d,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,d,e] is not taken.

12) Take [b,e,c] from Level3. [b,e,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,e,c] is not taken.

13) Take [b,c,d] from Level3. [b,c,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,c,d] is not taken.

14) Take [b,a,d] from Level3. [b,a,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,a,d] is not taken.

15) Take [c,b,d] from Level3. [c,b,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [c,b,d] is not taken.

16) Take [a,d,c] from Level4. [a,d,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,d,c] is not taken.

17) Take [a,e,d] from Level4. [a,e,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,e,d] is not taken.

18) Take [a,c,e] from Level4. [a,c,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,c,e] is not taken.

19) Take [c,a,e] from Level4. [c,a,e] is already present in [b,d,c,a,e]. Therefore there is no need to take [c,a,e].

20) Take [a,b,e] from Level4. [a,b,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,b,e] is not taken.

21) Take [a,d,e] from Level5. [a,d,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,d,e] is not taken.

22) Take [b,e,d] from Level5. [b,e,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,e,d] is not taken.

23) Take [a,c,d] from Level5. [a,c,d] is already present in [b,d,c,a,e]. Therefore there is no need to take [a,c,d].

24) Take [d,a,e] from Level5. [d,a,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [d,a,e] is not taken.

25) Take [c,b,e] from Level5. [c,b,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [c,b,e] is not taken.

26) Take [c,d,e] from Level6. [c,d,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [c,d,e] is not taken.

27) Take [c,e,d] from Level6. [c,e,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [c,e,d] is not taken.

28) Take [d,c,e] from Level6. [d,c,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [d,c,e] is not taken.

29) Take [c,a,d] from Level6. [c,a,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [c,a,d] is not taken.

30) Take [d,b,e] from Level6. [d,b,e] satisfies PR-2 property. So [d,b,e] fits with [b,d,c,a,e] to form [b,d,c,a,e,b].

[b,d,c,a,e,b] = [b,a,e] + [a,c,b] + [b,d,c] + [d,b,e]

w[b,d,c,a,e,b] = w[d,c] + w[c,a] + w[a,e] + w[e,b] + w[b,d] = 6 + 4 + 3 + 4 + 2 = 19

[NPC-3-END]

->NPC-4.

[NPC-4-BEGIN]

Take [c,b,d] as a necessary partial circuit. Since hamilton circuit rule is not violated, [c,b,d] is taken for forming the hamilton circuit. So the partial circuit is [c,b,d].

Use the same process that is done in Section #1.8.

1) Take [a,e,b] from Level1. [a,e,b] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,e,b] is not taken.

2) Take [a,c,b] from Level1. [a,c,b] satisfies PR-2 property. So [a,c,b] fits with [c,b,d] to form [a,c,b,d].

3) Take [a,d,b] from Level1. [a,d,b] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,d,b] is not taken.

4) Take [b,a,e] from Level1. [b,a,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,a,e] is not taken.

5) Take [a,b,c] from Level1. [a,b,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,b,c] is not taken.

6) Take [b,d,c] from Level2. [b,d,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,d,c] is not taken.

7) Take [a,e,c] from Level2. [a,e,c] satisfies PR-3 property. So [a,e,c] fits with [a,c,b,d] to form [a,e,c,b,d].

8) Take [b,c,e] from Level2. [b,c,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,c,e] is not taken.

9) Take [b,a,c] from Level2. [b,a,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,a,c] is not taken.

10) Take [a,b,d] from Level2. [a,b,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,b,d] is not taken.

11) Take [b,d,e] from Level3. [b,d,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,d,e] is not taken.

12) Take [b,e,c] from Level3. [b,e,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,e,c] is not taken.

13) Take [b,c,d] from Level3. [b,c,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,c,d] is not taken.

14) Take [b,a,d] from Level3. [b,a,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,a,d] is not taken.

15) Take [c,b,d] from Level3. [c,b,d] is already present in [a,c,b,d]. Therefore there is no need to take [c,b,d].

16) Take [a,d,c] from Level4. [a,d,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,d,c] is not taken.

17) Take [a,e,d] from Level4. [a,e,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,e,d] is not taken.

18) Take [a,c,e] from Level4. [a,c,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,c,e] is not taken.

19) Take [c,a,e] from Level4. [c,a,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [c,a,e] is not taken.

20) Take [a,b,e] from Level4. [a,b,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,b,e] is not taken.

21) Take [a,d,e] from Level5. [a,d,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,d,e] is not taken.

22) Take [b,e,d] from Level5. [b,e,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,e,d] is not taken.

23) Take [a,c,d] from Level5. [a,c,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,c,d] is not taken.

24) Take [d,a,e] from Level5. [d,a,e] satisfies PR-2 property. So [d,a,e] fits with [a,e,c,b,d] to form [a,e,c,b,d,a].

[a,e,c,b,d,a] = [c,b,d] + [a,c,b] + [a,e,c] + [d,a,e]

w[a,e,c,b,d,a] = w[a,e] + w[e,c] + w[c,b] + w[b,d] + w[d,a] = 3 + 5 + 2 + 2 + 4 = 16

[NPC-4-END]

->NPC-5.

[NPC-5-BEGIN]

Take [b,a,c] as a necessary partial circuit. Since hamilton circuit rule is not violated, [b,a,c] is taken for forming the hamilton circuit. So the partial circuit is [b,a,c].

Use the same process that is done in Section #1.8.

1) Take [a,e,b] from Level1. [a,e,b] satisfies PR-3 property. So [a,e,b] fits with [b,a,c] to form [b,e,a,c].

2) Take [a,c,b] from Level1. Since a 5 vertex hamilton circuit is required and not a 4 vertex hamilton circuit, [a,c,b] is not taken.

3) Take [a,d,b] from Level1. [a,d,b] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,d,b] is not taken.

4) Take [b,a,e] from Level1. [b,a,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,a,e] is not taken.

5) Take [a,b,c] from Level1. [a,b,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,b,c] is not taken.

6) Take [b,d,c] from Level2. [b,d,c] satisfies PR-1 property. So [b,d,c] fits with [b,e,a,c] to form [b,e,a,c,d,b].

[b,e,a,c,d,b] = [b,a,c] + [a,e,b] + [b,d,c]

w[b,e,a,c,d,b] = w[e,a] + w[a,c] + w[c,d] + w[d,b] + w[b,e] = 3 + 4 + 6 + 2 + 4 = 19

[NPC-5-END]

->NPC-6.

[NPC-6-BEGIN]

Take [b,a,d] as a necessary partial circuit. Since hamilton circuit rule is not violated, [b,a,d] is taken for forming the hamilton circuit. So the partial circuit is [b,a,d].

Use the same process that is done in Section #1.8.

1) Take [a,e,b] from Level1. [a,e,b] satisfies PR-3 property. So [a,e,b] fits with [b,a,d] to form [b,e,a,d].

2) Take [a,c,b] from Level1. [a,c,b] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,c,b] is not taken.

3) Take [a,d,b] from Level1. [a,d,b] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,d,b] is not taken.

4) Take [b,a,e] from Level1. [b,a,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,a,e] is not taken.

5) Take [a,b,c] from Level1. [a,b,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,b,c] is not taken.

6) Take [b,d,c] from Level2. [b,d,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,d,c] is not taken.

7) Take [a,e,c] from Level2. [a,e,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,e,c] is not taken.

8) Take [b,c,e] from Level2. [b,c,e] satisfies PR-3 property. So [b,c,e] fits with [b,e,a,d] to form [b,c,e,a,d].

9) Take [b,a,c] from Level2. [b,a,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,a,c] is not taken.

10) Take [a,b,d] from Level2. [a,b,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,b,d] is not taken.

11) Take [b,d,e] from Level3. [b,d,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,d,e] is not taken.

12) Take [b,e,c] from Level3. [b,e,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,e,c] is not taken.

13) Take [b,c,d] from Level3. [b,c,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,c,d] is not taken.

14) Take [b,a,d] from Level3. [b,a,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,a,d] is not taken.

15) Take [c,b,d] from Level3. [c,b,d] satisfies PR-2 property. So [c,b,d] fits with [b,c,e,a,d] to form [b,c,e,a,d,b].

[b,c,e,a,d,b] = [b,a,d] + [a,e,b] + [b,c,e] + [c,b,d]

w[b,c,e,a,d,b] = w[c,e] + w[e,a] + w[a,d] + w[d,b] + w[b,c] = 5 + 3 + 4 + 2 + 2 = 16

[NPC-6-END]

->NPC-7.

[NPC-7-BEGIN]

Take [a,b,e] as a necessary partial circuit. Since hamilton circuit rule is not violated, [a,b,e] is taken for forming the hamilton circuit. So the partial circuit is [a,b,e].

Use the same process that is done in Section #1.8.

1) Take [a,e,b] from Level1. [a,e,b] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,e,b] is not taken.

2) Take [a,c,b] from Level1. [a,c,b] satisfies PR-3 property. So [a,c,b] fits with [a,b,e] to form [a,c,b,e].

3) Take [a,d,b] from Level1. [a,d,b] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,d,b] is not taken.

4) Take [b,a,e] from Level1. [b,a,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,a,e] is not taken.

5) Take [a,b,c] from Level1. [a,b,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,b,c] is not taken.

6) Take [b,d,c] from Level2. [b,d,c] satisfies PR-3 property. So [b,d,c] fits with [a,c,b,e] to form [a,c,d,b,e].

7) Take [a,e,c] from Level2. [a,e,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,e,c] is not taken.

8) Take [b,c,e] from Level2. [b,c,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,c,e] is not taken.

9) Take [b,a,c] from Level2. [b,a,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,a,c] is not taken.

10) Take [a,b,d] from Level2. [a,b,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,b,d] is not taken.

11) Take [b,d,e] from Level3. [b,d,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,d,e] is not taken.

12) Take [b,e,c] from Level3. [b,e,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,e,c] is not taken.

13) Take [b,c,d] from Level3. [b,c,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,c,d] is not taken.

14) Take [b,a,d] from Level3. [b,a,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [b,a,d] is not taken.

15) Take [c,b,d] from Level3. [c,b,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [c,b,d] is not taken.

16) Take [a,d,c] from Level4. [a,d,c] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,d,c] is not taken.

17) Take [a,e,d] from Level4. [a,e,d] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,e,d] is not taken.

18) Take [a,c,e] from Level4. [a,c,e] does not satisfy PR-1 , PR-2 or PR-3 property. So [a,c,e] is not taken.

19) Take [c,a,e] from Level4. [c,a,e] satisfies PR-2 property. So [c,a,e] fits with [a,c,d,b,e] to form [a,c,d,b,e,a].

[a,c,d,b,e,a] = [a,b,e] + [a,c,b] + [b,d,c] + [c,a,e]

w[a,c,d,b,e,a] = w[c,d] + w[d,b] + w[b,e] + w[e,a] + w[a,c] = 6 + 2 + 4 + 3 + 4 = 19

[NPC-7-END]

From the next necessary partial circuit onwards, only the hamilton circuit result for the necessary partial circuit is written in order to make the document as brief as possible.

->NPC-8.

[NPC-8-BEGIN]

Take [c,b,e] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [d,b,e,a,c,d].

[d,b,e,a,c,d] = [c,b,e] + [a,e,b] + [b,d,c] + [c,a,e]

w[d,b,e,a,c,d] = w[d,b] + w[b,e] + w[e,a] + w[a,c] + w[c,d] = 2 + 4 + 3 + 4 + 6 = 19

[NPC-8-END]

->NPC-9.

[NPC-9-BEGIN]

Take [d,b,e] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [b,d,c,a,e,b].

[b,d,c,a,e,b] = [d,b,e] + [a,e,b] + [b,d,c] + [c,a,e]

w[b,d,c,a,e,b] = w[b,d] + w[d,c] + w[c,a] + w[a,e] + w[e,b] = 2 + 6 + 4 + 3 + 4 = 19

[NPC-9-END]

->NPC-10.

[NPC-10-BEGIN]

Take [a,c,b] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [e,c,d,b,a,e].

[e,c,d,b,a,e] = [a,c,b] + [b,d,c] + [a,e,c] + [a,b,d]

w[e,c,d,b,a,e] = w[e,c] + w[c,d] + w[d,b] + w[b,a] + w[a,e] = 5 + 6 + 2 + 1 + 3 = 17

[NPC-10-END]

->NPC-11.

[NPC-11-BEGIN]

Take [a,d,b] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [d,a,e,c,b,d].

[d,a,e,c,b,d] = [a,d,b] + [a,e,c] + [b,c,e]

w[d,a,e,c,b,d] = w[a,d] + w[d,b] + w[b,c] + w[c,e] + w[e,a] = 4 + 2 + 2 + 5 + 3 = 16

[NPC-11-END]

->NPC-12.

[NPC-12-BEGIN]

Take [c,a,e] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [a,c,d,b,e,a].

[a,c,d,b,e,a] = [c,a,e] + [a,e,b] + [b,d,c]

w[a,c,d,b,e,a] = w[c,a] + w[a,e] + w[e,b] + w[b,d] + w[d,c] = 4 + 3 + 4 + 2 + 6 = 19

[NPC-12-END]

->NPC-13.

[NPC-13-BEGIN]

Take [d,a,e] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [a,e,c,b,d,a].

[a,e,c,b,d,a] = [d,a,e] + [a,e,b] + [b,c,e] + [c,b,d]

w[a,e,c,b,d,a] = w[a,e] + w[e,c] + w[c,b] + w[b,d] + w[d,a] = 3 + 5 + 2 + 2 + 4 = 16

[NPC-13-END]

->NPC-14.

[NPC-14-BEGIN]

Take [b,c,e] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [c,e,a,d,b,c].

[c,e,a,d,b,c] = [b,c,e] + [a,d,b] + [a,e,c]

w[c,e,a,d,b,c] = w[c,e] + w[e,a] + w[a,d] + w[d,b] + w[b,c] = 5 + 3 + 4 + 2 + 2 = 16

[NPC-14-END]

->NPC-15.

[NPC-15-BEGIN]

Take [a,e,b] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [a,e,b,d,c,a].

[a,e,b,d,c,a] = [a,e,b] + [b,d,c] + [c,a,e]

w[a,e,b,d,c,a] = w[a,e] + w[e,b] + w[b,d] + w[d,c] + w[c,a] = 3 + 4 + 2 + 6 + 4 = 19

[NPC-15-END]

->NPC-16.

[NPC-16-BEGIN]

Take [c,a,d] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [e,a,d,b,c,e].

[e,a,d,b,c,e] = [c,a,d] + [a,c,b] + [a,e,c] + [c,b,d]

w[e,a,d,b,c,e] = w[e,a] + w[a,d] + w[d,b] + w[b,c] + w[c,e] = 3 + 4 + 2 + 2 + 5 = 16

[NPC-16-END]

->NPC-17.

[NPC-17-BEGIN]

Take [b,c,d] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [b,c,d,a,e,b].

[b,c,d,a,e,b] = [b,c,d] + [a,e,b] + [a,d,c]

w[b,c,d,a,e,b] = w[c,d] + w[d,a] + w[a,e] + w[e,b] + w[b,c] = 6 + 4 + 3 + 4 + 2 = 19

[NPC-17-END]

->NPC-18.

[NPC-18-BEGIN]

Take [b,d,c] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [b,d,c,a,e,b].

[b,d,c,a,e,b] = [b,d,c] + [a,e,b] + [c,a,e]

w[b,d,c,a,e,b] = w[b,d] + w[d,c] + w[c,a] +w[a,e] + w[e,b] = 2 + 6 + 4 + 3 + 4 = 19

[NPC-18-END]

->NPC-19.

[NPC-19-BEGIN]

Take [a,e,c] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [a,e,c,b,d,a].

[a,e,c,b,d,a] = [a,e,c] + [a,d,b] + [b,c,e]

w[a,e,c,b,d,a] = w[a,e] + w[e,c] + w[c,b] + w[b,d] + w[d,a] = 3 + 5 + 2 + 2 + 4 = 16

[NPC-19-END]

->NPC-20.

[NPC-20-BEGIN]

Take [a,c,e] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [a,c,e,b,d,a].

[a,c,e,b,d,a] = [a,c,e] + [a,d,b] + [b,e,c]

w[a,c,e,b,d,a] = w[a,c] + w[c,e] + w[e,b] + w[b,d] + w[d,a] = 4 + 5 + 4 + 2 + 4 = 19

[NPC-20-END]

->NPC-21.

[NPC-21-BEGIN]

Take [b,d,e] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [b,d,e,a,c,b].

[b,d,e,a,c,b] = [b,d,e] + [a,c,b] + [a,e,d]

w[b,d,e,a,c,b] = w[b,d] + w[d,e] + w[e,a] + w[a,c] + w[c,b] = 2 + 7 + 3 + 4 + 2 = 18

[NPC-21-END]

->NPC-22.

[NPC-22-BEGIN]

Take [b,e,c] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [b,e,c,a,d,b].

[b,e,c,a,d,b] = [b,e,c] + [a,d,b] + [a,c,e]

w[b,e,c,a,d,b] = w[b,e] + w[e,c] + w[c,a] + w[a,d] + w[d,b] = 4 + 5 + 4 + 4 + 2 = 19

[NPC-22-END]

->NPC-23.

[NPC-23-BEGIN]

Take [a,c,d] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [a,c,d,b,e,a].

[a,c,d,b,e,a] = [a,c,d] + [a,e,b] + [b,d,c]

w[a,c,d,b,e,a] = w[a,c] + w[c,d] + w[d,b] + w[b,e] + w[e,a] = 4 + 6 + 2 + 4 + 3 = 19

[NPC-23-END]

->NPC-24.

[NPC-24-BEGIN]

Take [a,d,c] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [a,d,c,b,e,a].

[a,d,c,b,e,a] = [a,d,c] + [a,e,b] + [b,c,d]

w[a,d,c,b,e,a] = w[a,d] + w[d,c] + w[c,b] + w[b,e] + w[e,a] = 4 + 6 + 2 + 4 + 3 = 19

[NPC-24-END]

->NPC-25.

[NPC-25-BEGIN]

Take [a,e,d] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [a,e,d,b,c,a].

[a,e,d,b,c,a] = [a,e,d] + [a,c,b] + [b,d,e]

w[a,e,d,b,c,a] = w[a,e] + w[e,d] + w[d,b] + w[b,c] + w[c,a] = 3 + 7 + 2 + 2 + 4 = 18

[NPC-25-END]

->NPC-26.

[NPC-26-BEGIN]

Take [d,c,e] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [d,c,e,a,b,d].

[d,c,e,a,b,d] = [d,c,e] + [b,a,e] + [b,d,c]

w[d,c,e,a,b,d] = w[d,c] + w[c,e] + w[e,a] + w[a,b] + w[b,d] = 6 + 5 + 3 + 1 + 2 = 17

[NPC-26-END]

->NPC-27.

[NPC-27-BEGIN]

Take [a,d,e] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [a,d,e,b,c,a].

[a,d,e,b,c,a] = [a,d,e] + [a,c,b] + [b,e,d]

w[a,d,e,b,c,a] = w[a,d] + w[d,e] + w[e,b] + w[b,c] + w[c,a] = 4 + 7 + 4 + 2 + 4 = 21

[NPC-27-END]

->NPC-28.

[NPC--BEGIN]

Take [b,e,d] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [b,e,d,a,c,b].

[b,e,d,a,c,b] = [b,e,d] + [a,c,b] + [a,d,e]

w[b,e,d,a,c,b] = w[b,e] + w[e,d] + w[d,a] + w[a,c] + w[c,b] = 4 + 7 + 4 + 4 + 2 = 21

[NPC-28-END]

->NPC-29.

[NPC-29-BEGIN]

Take [c,e,d] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [c,e,d,a,b,c].

[c,e,d,a,b,c] = [c,e,d] + [a,b,c] + [b,a,d]

w[c,e,d,a,b,c] = w[c,e] + w[e,d] + w[d,a] + w[a,b] + w[b,c] = 5 + 7 + 4 + 1 + 2 = 19

[NPC-29-END]

->NPC-30.

[NPC-30-BEGIN]

Take [c,d,e] as a necessary partial circuit.

Use the same process that is done in Section #1.8.

The hamilton circuit is [c,d,e,a,b,c].

[c,d,e,a,b,c] = [c,d,e] + [b,a,e] + [a,b,c]

w[c,d,e,a,b,c] = w[c,d] + w[d,e] + w[e,a] + w[a,b] + w[b,c] = 6 + 7 + 3 + 1 + 2 = 19

[NPC-30-END]

All the necessary partial circuits present in Section #1.11 has been processed. Now compare the different hamilton circuits obtained.

The hamilton circuit obtained in Section #1.8 ie:- [a,e,b,d,c,a] has a weight of 19.

The lowest weight hamilton circuits obtained by processing the necessary partial circuits as given in this section are as follows.

( The results are written in the format of :-

line number) necessary partial circuit number ; necessary partial circuit ; hamilton circuit obtained from the necessary partial circuit ; weight of the hamilton circuit.

The values in the result are separated by a semicolon. )

1) NPC-4 ; [c,b,d] ; [a,e,c,b,d,a] ; 16.

2) NPC-6 ; [b,a,d] ; [b,c,e,a,d,b] ; 16.

3) NPC-11 ; [a,d,b] ; [d,a,e,c,b,d] ; 16.

4) NPC-13 ; [d,a,e] ; [a,e,c,b,d,a] ; 16.

5) NPC-14 ; [b,c,e] ; [c,e,a,d,b,c] ; 16.

6) NPC-16 ; [c,a,d] ; [e,a,d,b,c,e] ; 16.

7) NPC-19 ; [a,e,c] ; [a,e,c,b,d,a] ; 16.

Seven hamilton circuits formed from the necessary partial circuits have the least weight of 16. So the hamilton circuit ( for eg:- the hamilton circuit [a,e,c,b,d,a] formed from NPC-4 ( ie:- [c,b,d] ) ) with weight of 16 is the minimum weight hamilton circuit.

Section #1.12 (END)