Jie Yang

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Interests

My major interests lie in computer architecture, Field Programmable Gate Array (FPGA) and embedded systems.
During my undergraduate period, I focused my projects on FPGA and ARM+FPGA heterogeneous systems.
During my graduate studies, my research topic was data center network acceleration and I focused on middleware and RDMA congestion control.

Education

2015–2018 **M.Sc. Computer Science**, *Nanjing University*.
2010–2014 **B.Sc. Computer Science**, *Nanjing University*.

Scholarships and Awards

2012–2013 The Third Prize People Scholarship
2011–2012 National Endeavor Fellowship, The First Prize People Scholarship

Technical Skills

Languages Verilog HDL, C/C++, Java, , Python, Matlab

Project Experience

Project Experience

2016–present **Nanjing University**, Nanjing, China.

FPGA-based RDMA NIC

RDMA is a new trend of data center network. The project aims to build a RDMA research platform by implementing RDMA protocol on FPGA as Network Interface Controller(NIC). Based on Xilinx HLS and Microblaze, the throughput of RDMA NIC can reach line rate(10Gbps) on Xilinx Kintex7 chip, and it can also communicate with commercial RDMA NIC.

2015-3–2015-9 **Nanjing University**, Nanjing, China.

FPGA-based Software Define Middleware

Software Define Middleware(SDM) needs a uniform abstract language to run on different platforms, such as CPU, NPU and FPGA. I define a C-like pseudo language to implement SDM function, and it can be run on FPGA. C-like pseudo language is transformed in to Xilinx HLS by custom compiler, then in to verilog.

2012–2015 **Nanjing University**, Nanjing, China.

SimMIPS: a MIPS-based embedded system on FPGA

SimMIPS is an embedded system implemented on FPGA, including CPU, peripherals and multiple BUS interfaces. As a simplified version of MIPS32 4Kc processor, SimMIPS covers most instructions of MIPS32 Release 1 Instruction Set, and programmes or Operating System compiled by GNU GCC could be executed on SimMIPS. For more details, you can visit `https://github.com/jackyangNJ/SimMIPS`.

2013–2014 **Nanjing University**, Nanjing, China.

SmartCar: an intelligent navigation car in the library

SmartCar aims to navigate readers autonomously in the library. We implemented the control system on the platform *zrobot*, using C, Java and Verilog languages. To achieve autonomous navigation, we combined the traditional inertial navigation technology with image processing and added many sensors or devices to the car, such as acceleration sensor, gyroscope, USB camera, wireless network card, Hall sensors, etc. For more information, you can visit `https://github.com/jackyangNJ/SmartCar`.

2013 summer **Institute of Computing Technology**, *Chinese Academy of Sciences*, Beijing, China.

testing Xilinx soft processor MicroBlaze performance and building a prototype system

The project was to aid ICT research. My major work was to test the performance of soft processor MicroBlaze on Linux with Xilinx FPGA, and meanwhile I built a research prototype system, a network composed of a interconnect 3x3 mesh of nine MicroBlaze processors on one FPGA chip.