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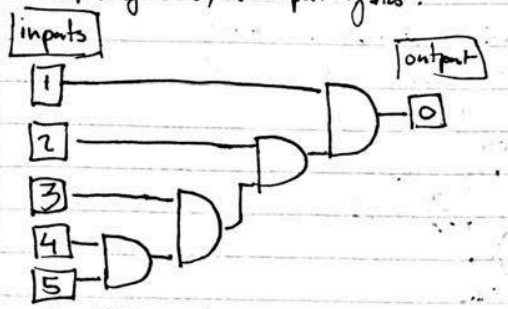
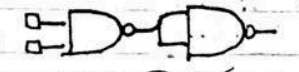
CMPE 12 HW2

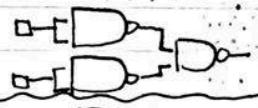
1. 5-input and gate w/ 2-input and gates.



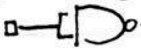
2. $2^5 = 32$ output lines
3. 1 output line and 4 select lines for the 16-input MUX
4. $\lceil 14/4 \rceil = 4$ nybbles of storage
5. AND =>



OR



NOT



6. Memory is stored at a specific address; the number of bits of information stored at each location is its addressability.

7.

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

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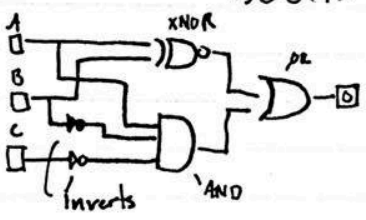
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

DNF

$\neg A \neg B \neg C + \neg A \neg B C + A \neg B \neg C + A B \neg C + A B C$

$\neg A \neg B (T) + A \neg B \neg C \quad + A B (T)$ ✓

$A \neg B \neg C (T)$



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a. 39 - 22 : 00100111 − 00010110 ⇒ 00100111 − 00010110 = 00010001 : 17

39: 32+4+2+1

22: 16+4+2

b. 25 - 14 : 00011001 − 00001110 ⇒ 00011001 − 00001110 = 00001011 : 11

25: 16+8+1

14: 8+4+2

c. 39 - 12 00100111 − 00001100 = 00011011 : 27

32+4+2+1 − 8+4

d. 18 - 11 00010010 − 00001011 = 00000111 = 7

16+2 − 8+2+1

e. 30 - 26 00011110 − 00011010 = 00000100 = 4

16+8+4+2 − 16+8+2