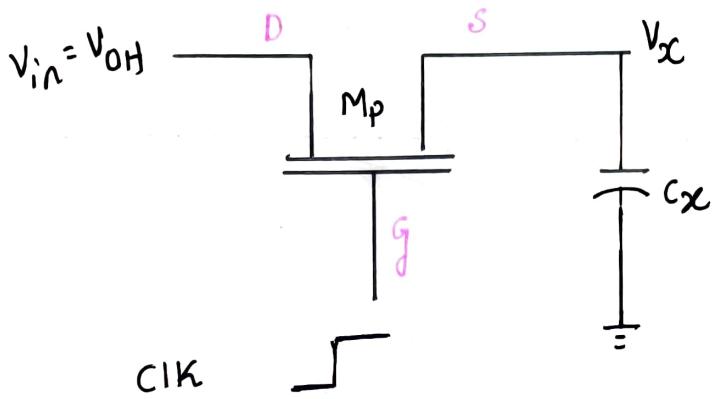


# Basic principles of Pass transistor circuits

## I Logic 1 transfer



→ assume  $V_x(t) = 0$  @  $t=0$

→  $V_{in} = V_{OH}$  applied at input terminal

→  $V_{in} = V_{OH} = V_{DD}$

→ When gate signal goes from 0 to 1

→  $V_{DS} = V_{GS}$

→  $\therefore M_p$  operates in saturation.

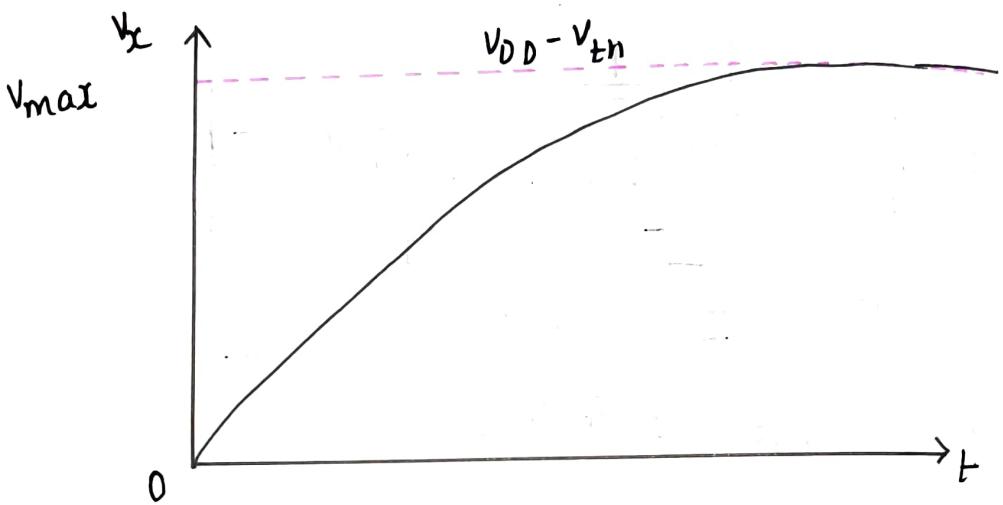
→  $V_{DS} > V_{GS} - V_t$

$$\therefore C_x \frac{dV_x}{dt} = \frac{K_n}{2} \left[ V_{DD} - V_x - V_{Tn} \right]^2$$

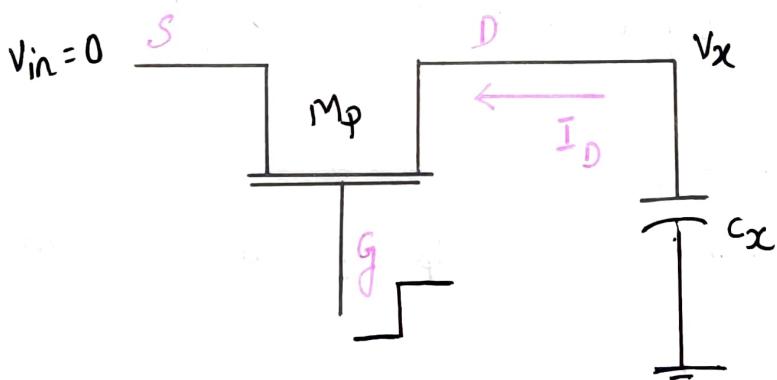
$$\int_0^t dt = \frac{2C_x}{K_n} \int_0^{V_x} \frac{dV_x}{\left( V_{DD} - V_x - V_{Tn} \right)^2}$$

$$t = \frac{2C_x}{K_n} \left[ \frac{1}{V_{DD} - V_x - V_{TN}} \right]_0^{V_x}$$

$$t = \frac{2C_x}{K_n} \left[ \left( \frac{1}{V_{DD} - V_x - V_{TN}} \right) - \left( \frac{1}{V_{DD} - V_{TN}} \right) \right]$$



Logic 0 Transfer :-



- assume soft node voltage is equal to Logic 1
- Logic 0 is applied to  $\text{I/P}$  node
- $V_{in} = 0$
- When gate signal goes from 0 to  $V_{DD}$

→ M<sub>P</sub> starts Conducting

→  $V_{GS} = V_{DD}$

$V_{DS} = V_{max} = V_{DD} - V_{Tn}$

$V_{DS} < V_{GS} - V_{Tn}$  → Operates in Linear region

→  $-C_x \frac{dV_x}{dt} = \frac{k_n}{2} \left[ 2(V_{DD} - V_{Tn})V_x - V_x^2 \right]$

$$dt = -\frac{2C_x}{k_n} \cdot \frac{dV_x}{2(V_{DD} - V_{Tn})V_x - V_x^2}$$

$$\frac{dV_x}{2(V_{DD} - V_{Tn})V_x - V_x^2} = \frac{dV_x}{V_x [2(V_{DD} - V_{Tn}) - V_x]} = \frac{A}{V_x} + \frac{B}{2(V_{DD} - V_{Tn}) - V_x}$$

1  $dV_x = A(2(V_{DD} - V_{Tn}) - V_x) + B V_x$

$$A = \frac{1}{2(V_{DD} - V_{Tn})}$$

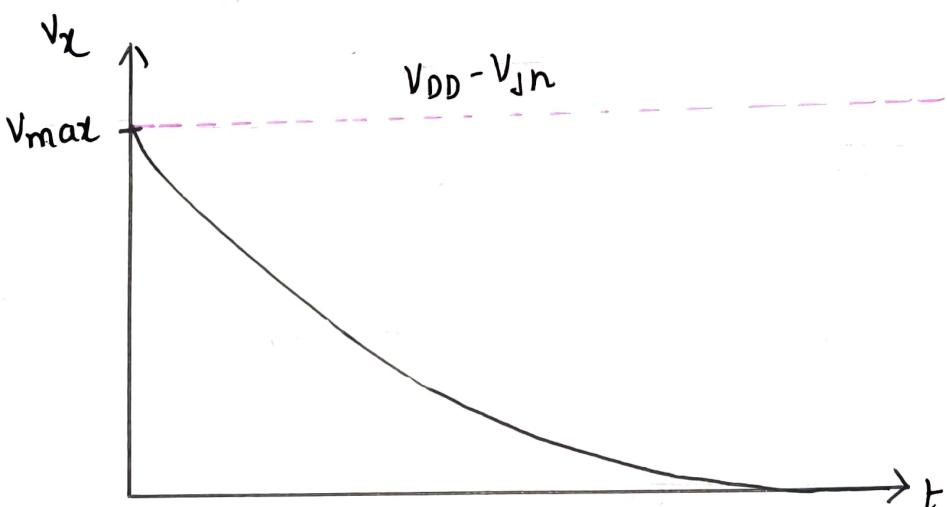
$$B = \frac{1}{2(V_{DD} - V_{Tn})}$$

$$\int dt = -\frac{2C_x}{k_n} \int \frac{\frac{1}{2(V_{DD} - V_{Tn})}}{V_x} + \frac{\frac{1}{2(V_{DD} - V_{Tn})}}{2(V_{DD} - V_{Tn}) - V_x} dV_x$$

$$= -\frac{2C_X}{K_n^2(V_{DD} - V_{Jn})} \left[ \ln(v_x) - \ln\left(2(V_{DD} - V_{Jn}) - v_x\right) \right]$$

$$= \frac{C_X}{K_n(V_{DD} - V_{Jn})} \left[ \ln\left(\frac{(2(V_{DD} - V_{Jn}) - v_x)}{v_x}\right) \right] \begin{matrix} v_x \\ v_{DD} - v_{Jn} \end{matrix}$$

$$t = \frac{C_X}{K_n(V_{DD} - V_{Jn})} \left[ \ln\left(\frac{2(V_{DD} - V_{Jn}) - v_x}{v_x}\right) \right]$$



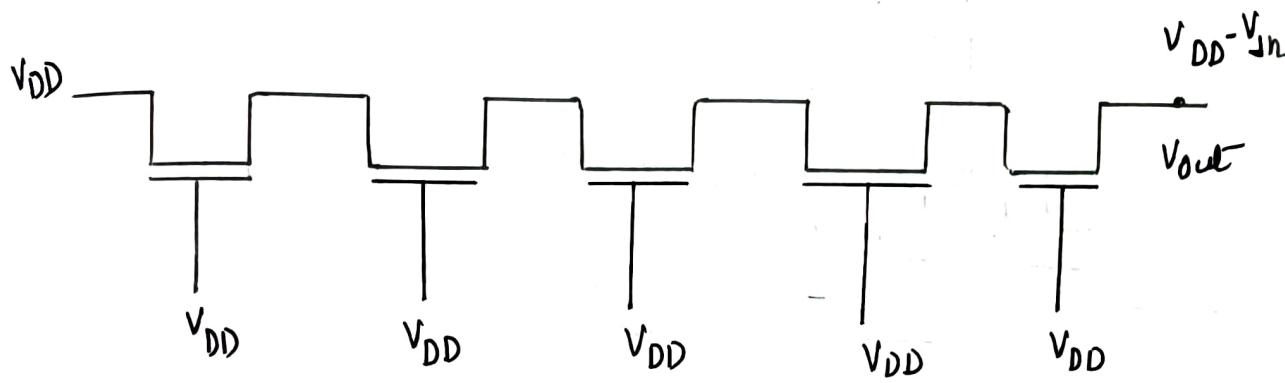
Rise time

$$t_{90\%} = \frac{C_X}{K_n(V_{DD} - V_{Jn})} \left[ \ln\left(\frac{2(V_{DD} - V_{Jn}) - 0.9(V_{DD} - V_{Jn})}{0.9(V_{DD} - V_{Jn})}\right) \right]$$

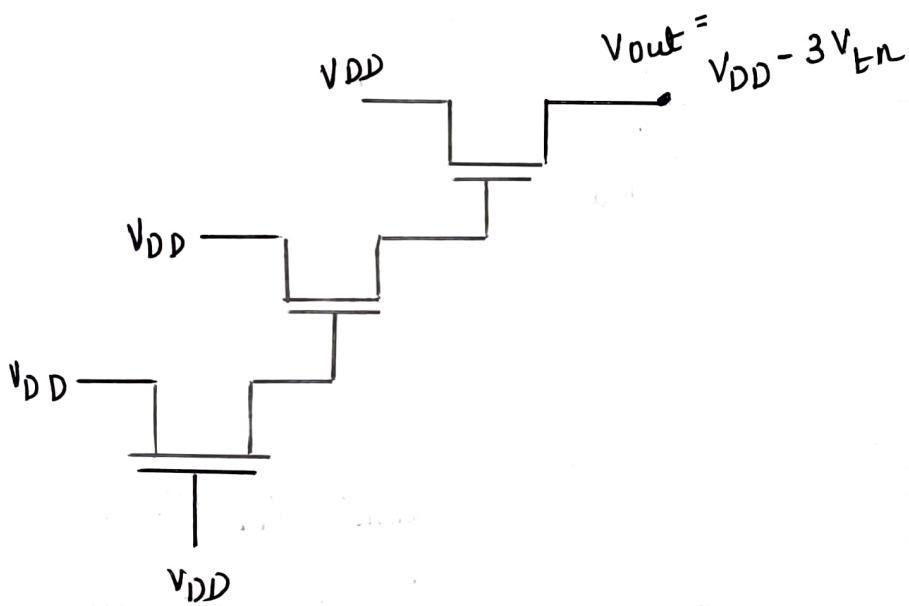
$$= \frac{C_X}{K_n(V_{DD} - V_{Jn})} \left[ \ln\left(\frac{1.1}{0.9}\right) \right]$$

$$t_{10\%} = \frac{C_X}{K_n(V_{DD} - V_{Jn})} \ln\left(\frac{1.9}{0.1}\right)$$

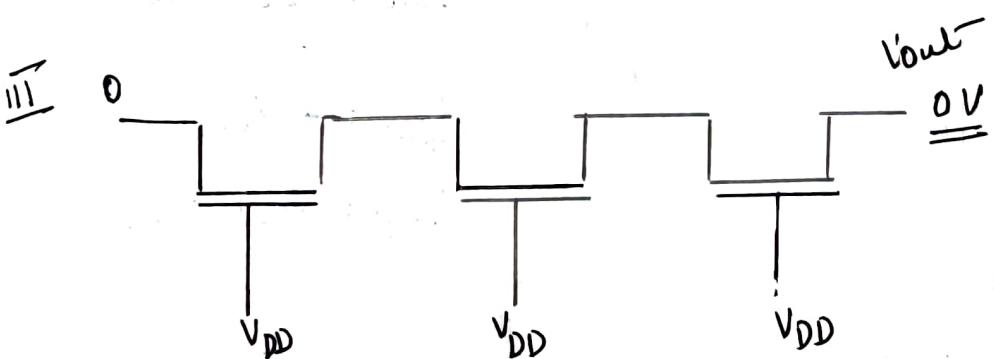
I



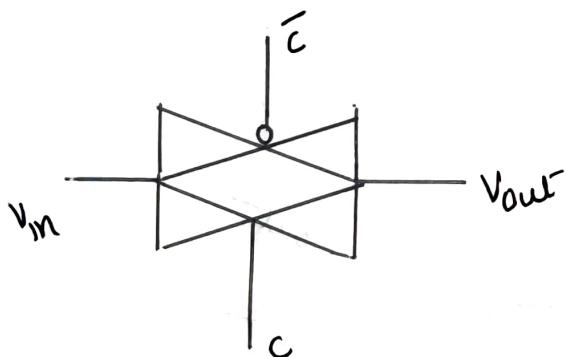
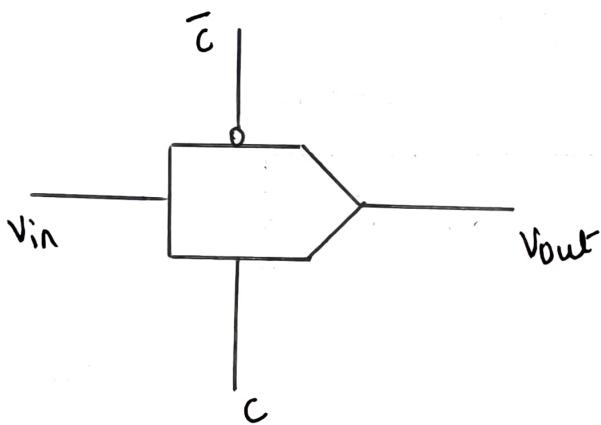
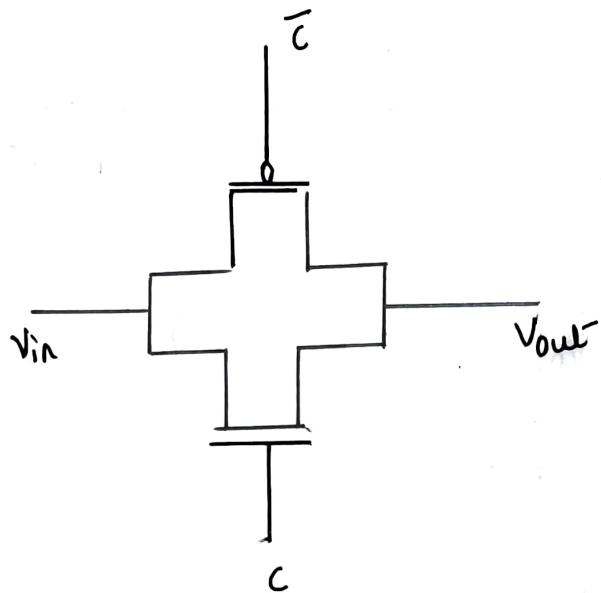
II



III



Transmission gates : TG

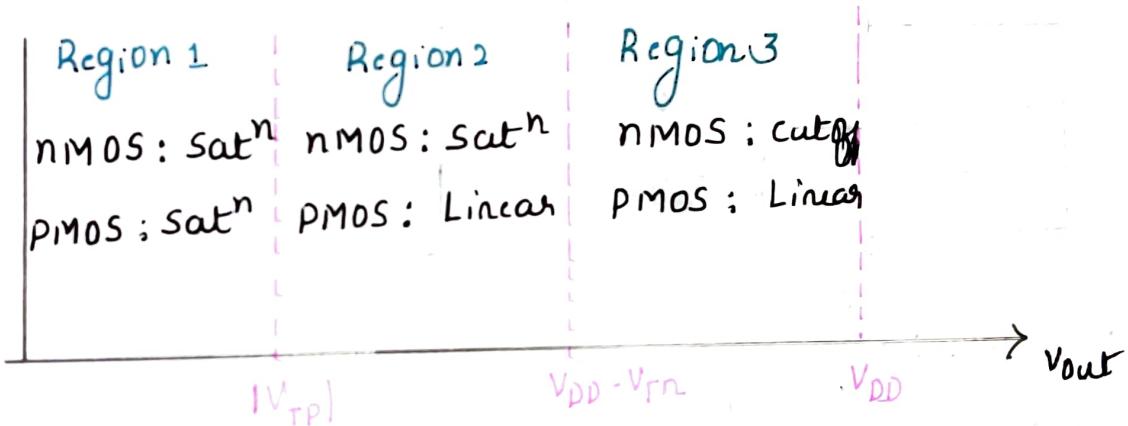
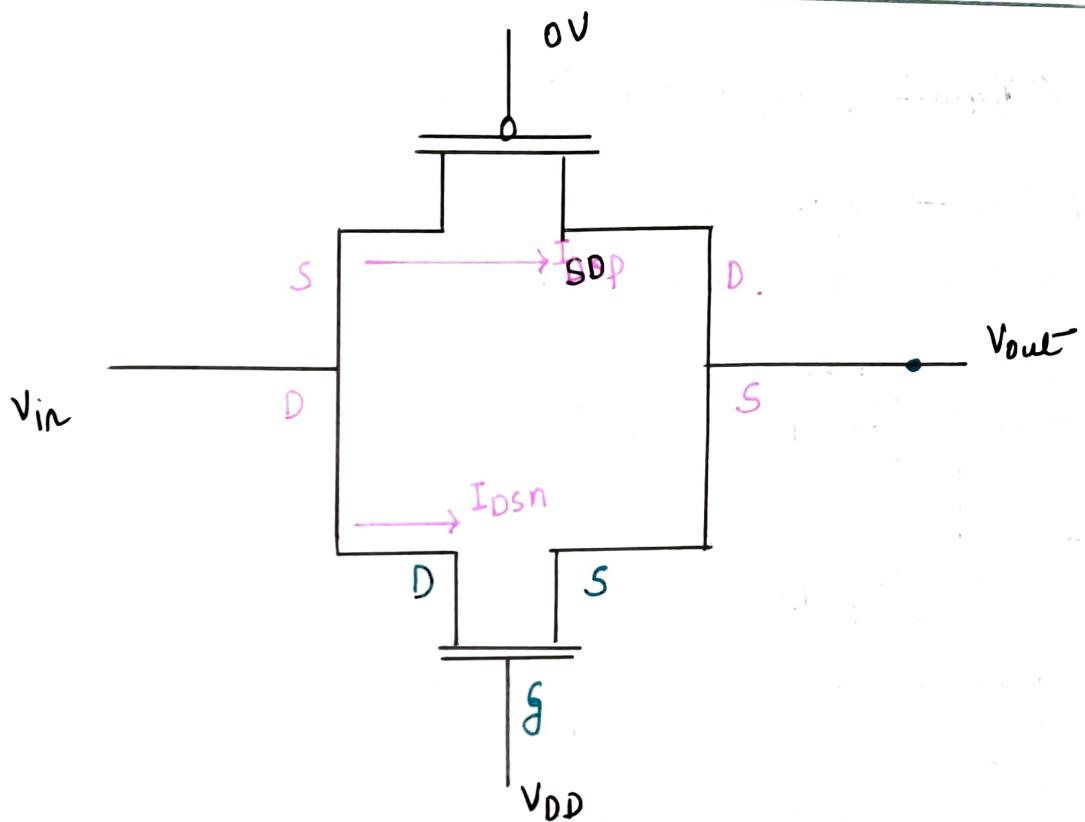


$$V_{GSn} = V_{DD} - V_{out}$$

$$V_{DSn} = V_{DD} - V_{out}$$

$$V_{GSp} = -V_{DD}$$

$$V_{DSP} = V_{out} - V_{DD}$$



$$I_D = I_{DSn} + I_{DSP}$$

$$R_{cq,n} = \frac{V_{DD} - V_{out}}{I_{DSn}}$$

$$R_{cq,p} = \frac{V_{DD} - V_{out}}{I_{SDP}}$$

## Region 1

nMOS  $\rightarrow$  Saturation

PMOS  $\rightarrow$  Saturation

$$I_{DSn} = \frac{K_n}{2} \left[ V_{DD} - V_{out} - V_{tn} \right]^2$$

$$I_{SDP} = \frac{K_p}{2} \left[ V_{DD} - V_{tp} \right]^2$$

$$R_{eqn} = \frac{2(V_{DD} - V_{out})}{K_n(V_{DD} - V_{out} - V_{tn})^2}$$

$$R_{eqp} = \frac{2(V_{DD} - V_{out})}{K_p(V_{DD} - V_{tp})^2}$$

## Region 2 :-

nMOS  $\rightarrow$  Saturation

PMOS  $\rightarrow$  Linear

$$I_{DSn} = \frac{K_n}{2} \left[ V_{DD} - V_{out} - V_{tn} \right]^2$$

$$I_{SDP} = \frac{K_p}{2} \left[ 2(V_{DD} - V_{tp})(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2 \right]$$

$$R_{eqn} = \frac{2(V_{DD} - V_{out})}{K_n(V_{DD} - V_{out} - V_{tn})^2}$$

$$R_{eqp} = \frac{2(V_{DD} - V_{out})}{K_p(2(V_{DD} - V_{tp})(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2)}$$

2

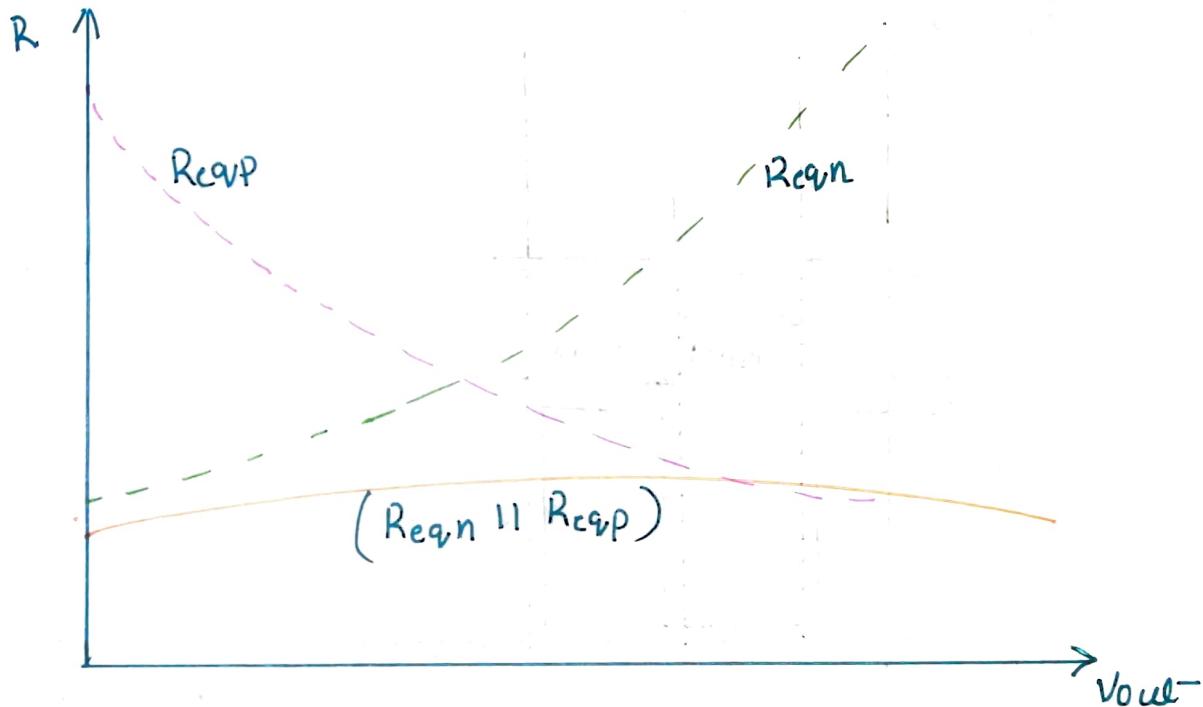
$$R_{eqp} = \frac{2}{K_p (2(v_{DD} - v_{tp}) - (v_{DD} - v_{out}))}$$

Region 3 :-

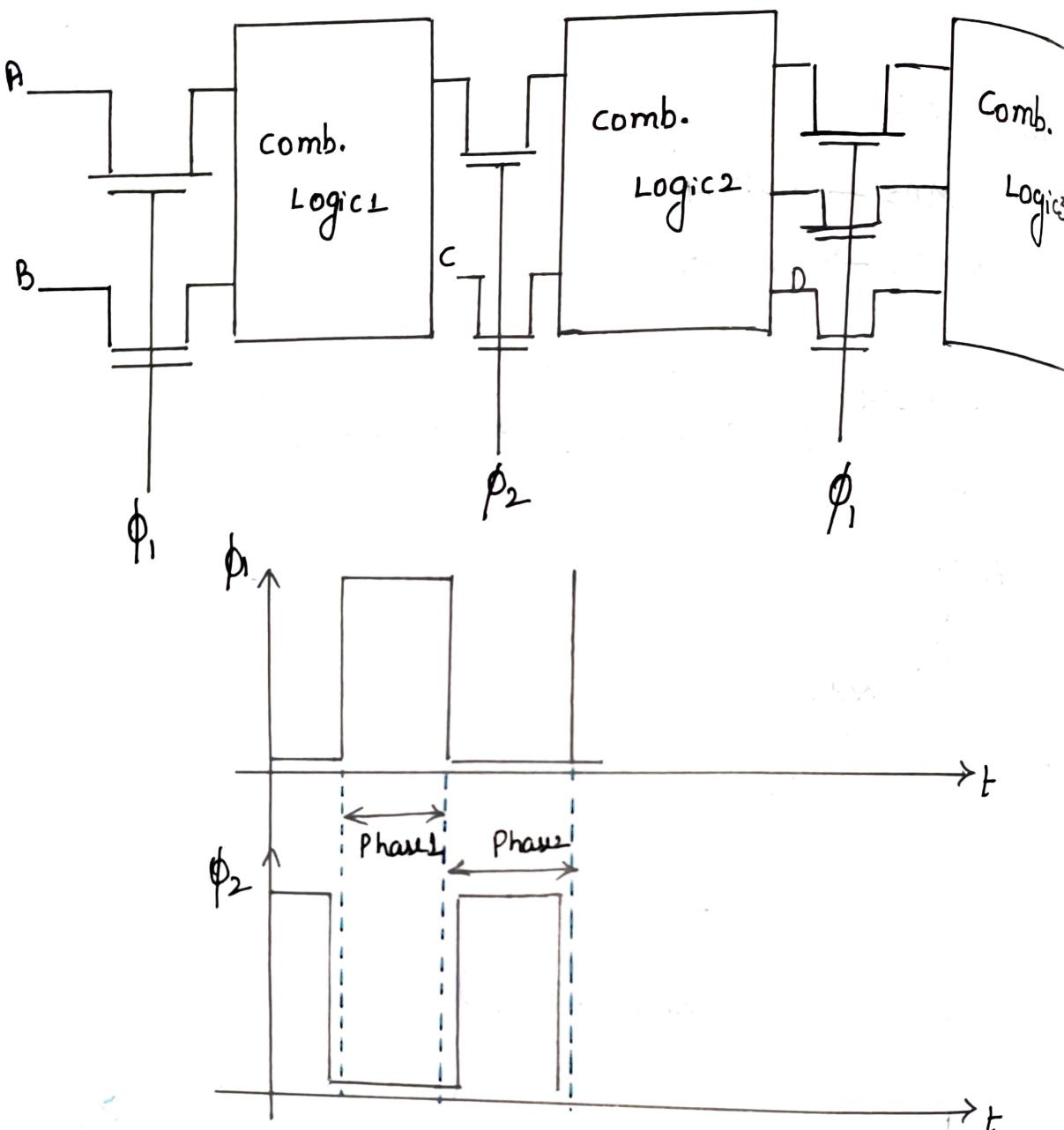
nMOS  $\rightarrow$  cut off

PMOS  $\rightarrow$  Linear

$$R_{eqp} = \frac{2}{K_p (2(v_{DD} - v_{tp}) - (v_{DD} - v_{out}))}$$



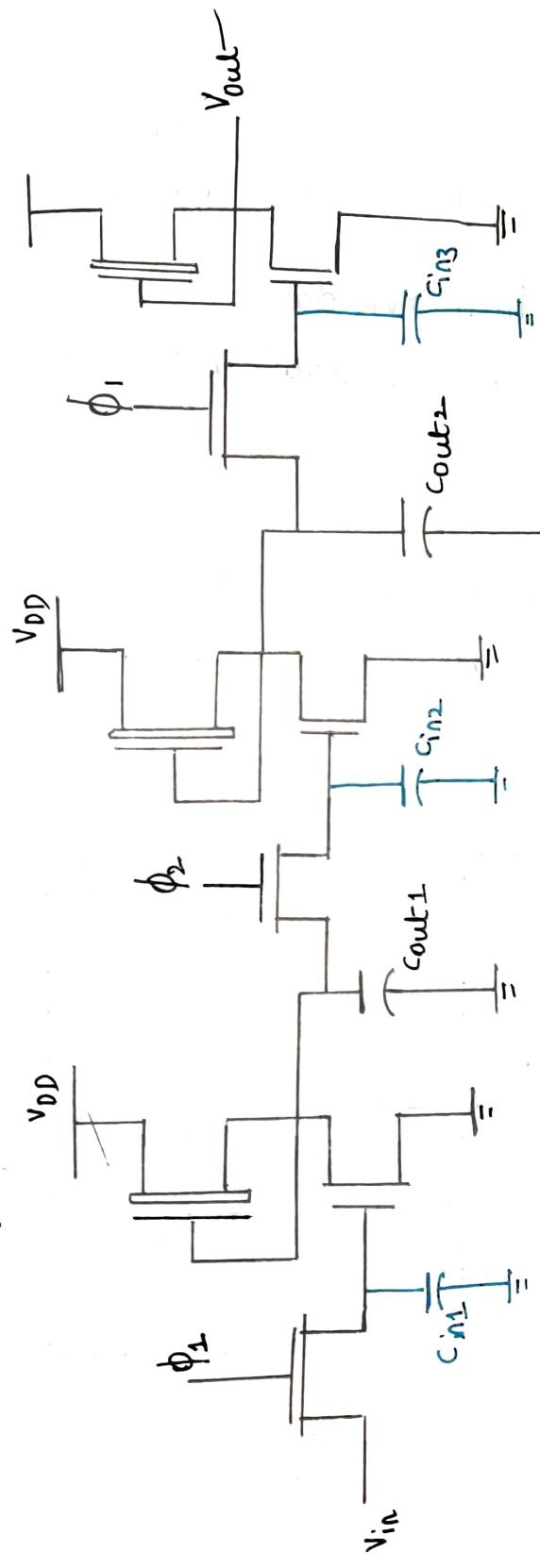
# Dynamic Pass Transistor circuits



non-overlapping clock signal used for two-phase operation.

- Generalised view of multistage synchronous circuit is as shown in figure.
- It consists of cascaded combinational logic stages which are interconnected through nMOS pass transistor

$\therefore$  NMOS - dynamic shift register with duplication load two phase clocking :-



$\rightarrow$  all  $1/p$  of each combinational block is driven by single clock signal.

$\rightarrow$  Here two-phase non-overlapping clocks are used.

- $\rightarrow$  When  $\phi_1 = 1$   $1/p$  levels of stage 1 are applied through the pass transistors
- $\rightarrow$  When  $\phi_2 = 1$  stage 2 process the data & stage 1 & stage 3 retain previously processed data
- $\rightarrow$  circuit of duplication local dynamic shift register circuit in which  $1/p$  data is inverted once shifted to next stage

→ Operation :-

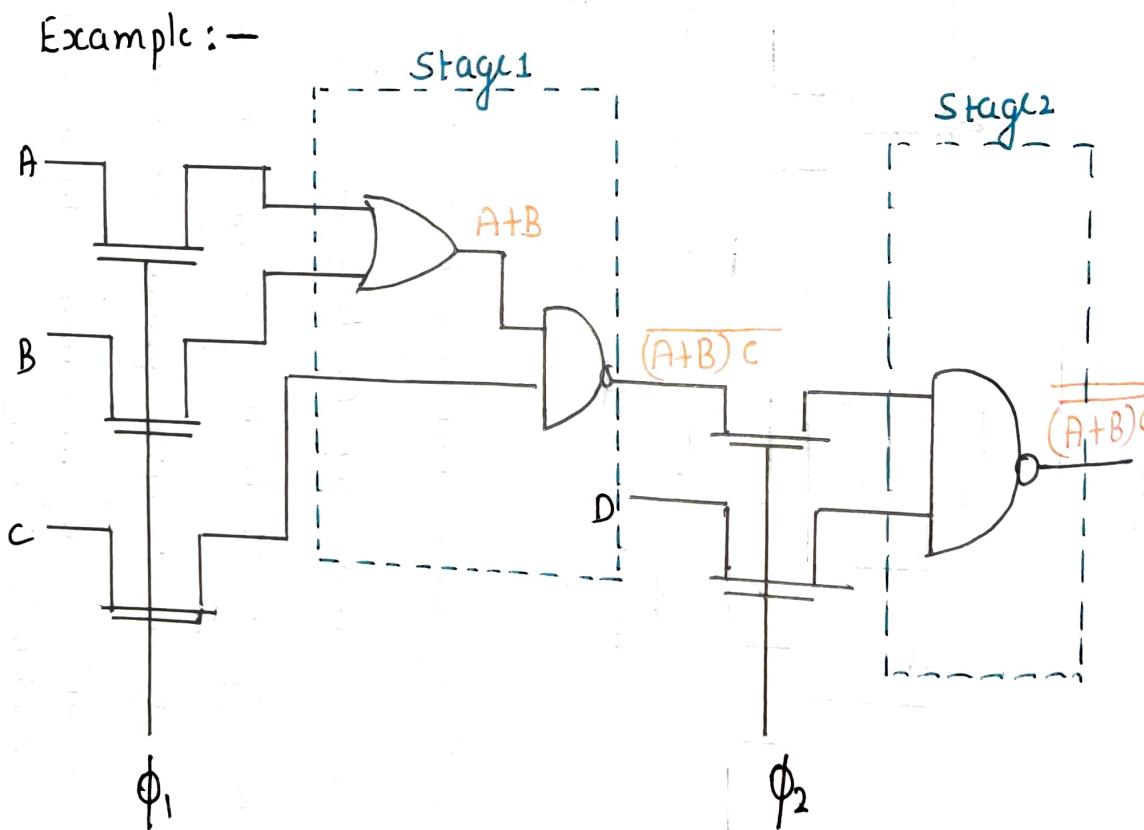
$$\rightarrow \phi_1 = 1 ; \quad C_{in1} = V_{in1}$$
$$C_{out1} = V_{in1}$$

$$\rightarrow \phi_2 = 1 \quad C_{in2} = V_{in1}' \quad \left. \begin{array}{l} \\ \end{array} \right\} \begin{array}{l} \text{stage 1 retain} \\ \text{Previous stage} \end{array}$$
$$C_{out} = V_{in1}$$

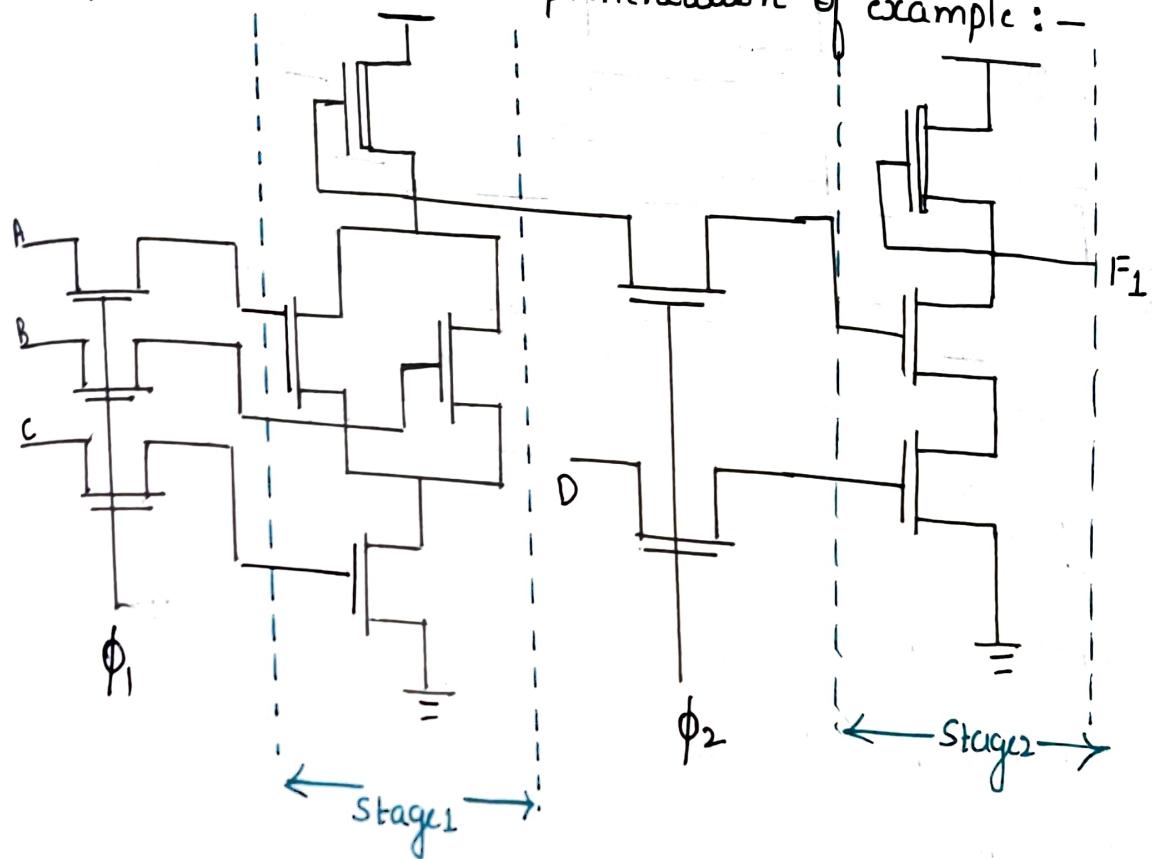
$\rightarrow \phi_1 = 1$       Stage 1 captures new data  
Stage 3 process the data o/p of Stage 2  
Stage 2 retains previous data

$\rightarrow$  Maximum clock frequency is determined by signal propagation delay through one inverter stage.

Example :-



Depletion load nmos implementation of example :-



Enhancement load dynamic shift register :-

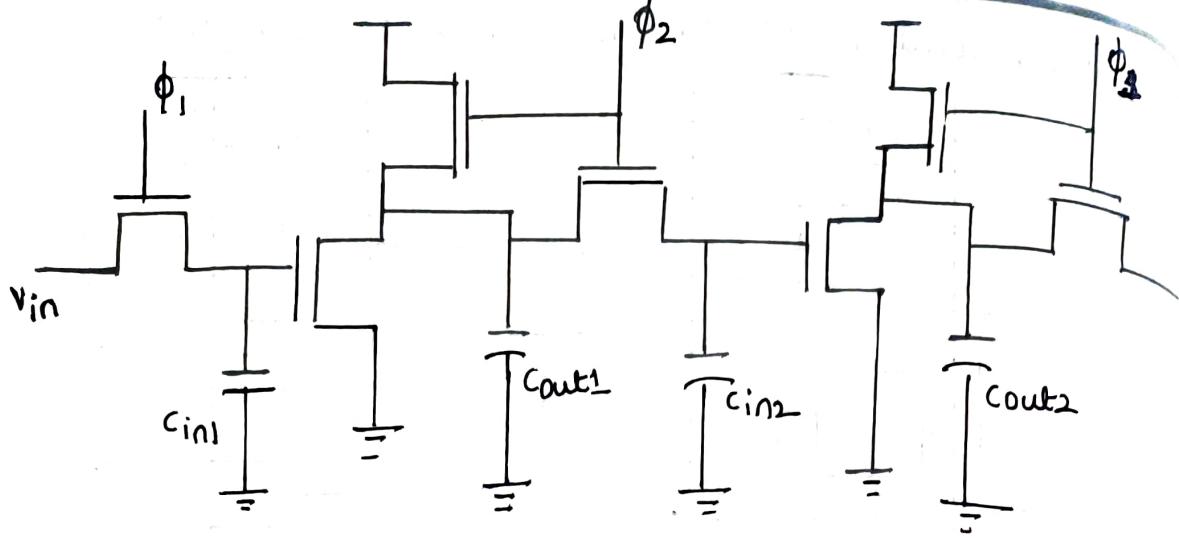
→ Instead of biasing load transistors with constant gate voltage apply clock signal to the gate of load MOS.

I Ratioed Logic

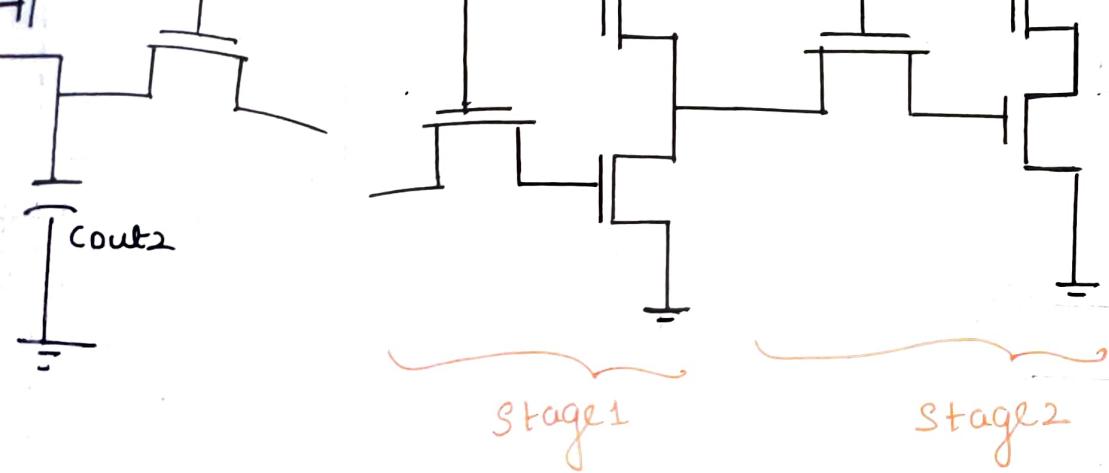
→ circuit diagram of enhancement load dynamic shift reg is shown in figure.

→ When  $\phi_1$  = active  $V_{in}$  is transferred to first stage s/p cap. circ through pass transistor.

→ In this phase enhancement type nmos load transistors of first stage inv is not yet active yet



- When  $\phi_1$  = active  $V_{in} = C_{in1}$
- In this phase enhancement load of first stage inverter is not yet active.
- During  $\phi_2$  = active  
Enhancement load and pass transistor of stage 2 are simultaneously switched on.
- Still Input logic is preserved in  $C_{in1}$  the o/p of the first inverter stage attains its valid logic.
- When  $\phi_1$  is active again the valid o/p level across  $C_{out2}$  is determined and is buffered in to  $C_{in2}$
- In this circuit the Valid low o/p voltage level  $V_{OL}$  of each stage is strictly determined by driver to load ratio
- ∴ This is called ratioed dynamic logic.



→ Ratioless logic

stage inverter

stage 2 are

of the first

1 across Cout2

→ Enhancement mode dynamic shift-registers (ratioless) is as depicted in figure.

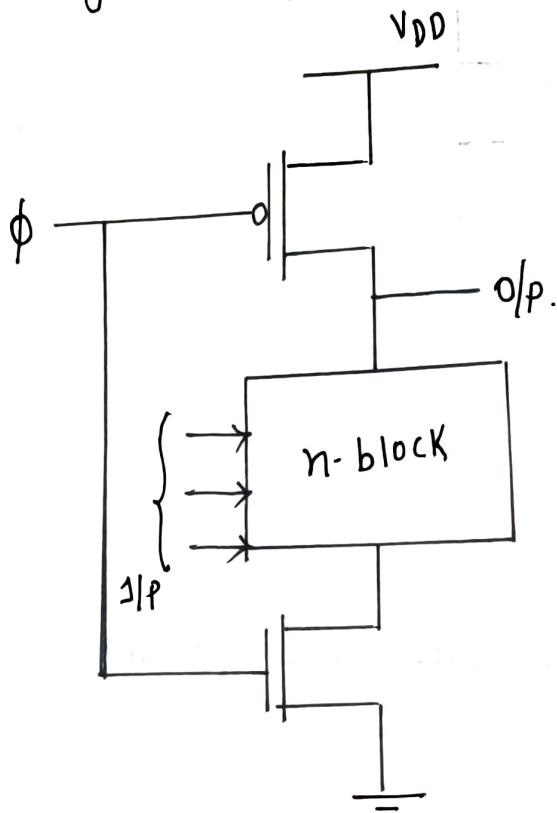
→ When  $\phi_1$  is active s/p is transferred in to first stage o/p cap.  $C_{in1}$  through pass transistor

→ At the same stage Enhancement mode nMOS inverter is active  $\therefore$  o/p of first stage attain its valid logic.

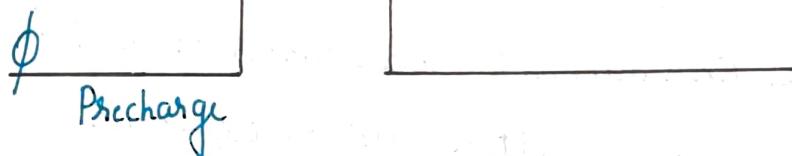
→ When  $\phi_2$  is active s/p pass transistor of stage 2 is turned on and logic level is transferred in to stage 2

$V_{OL}$  of each  
and ratio

## Dynamic Logic :-

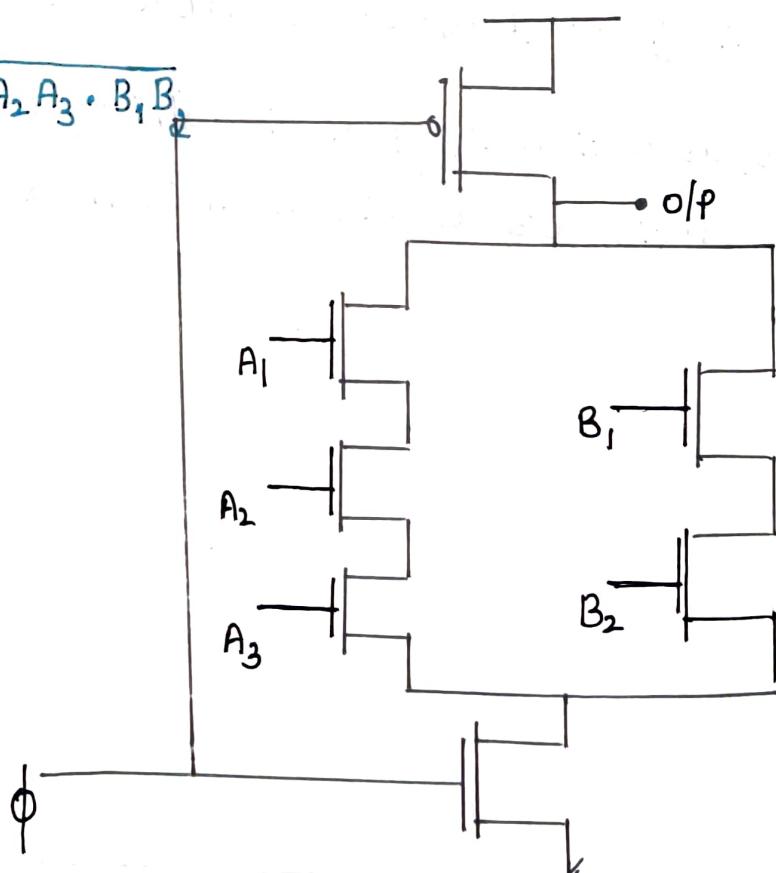


Evaluation

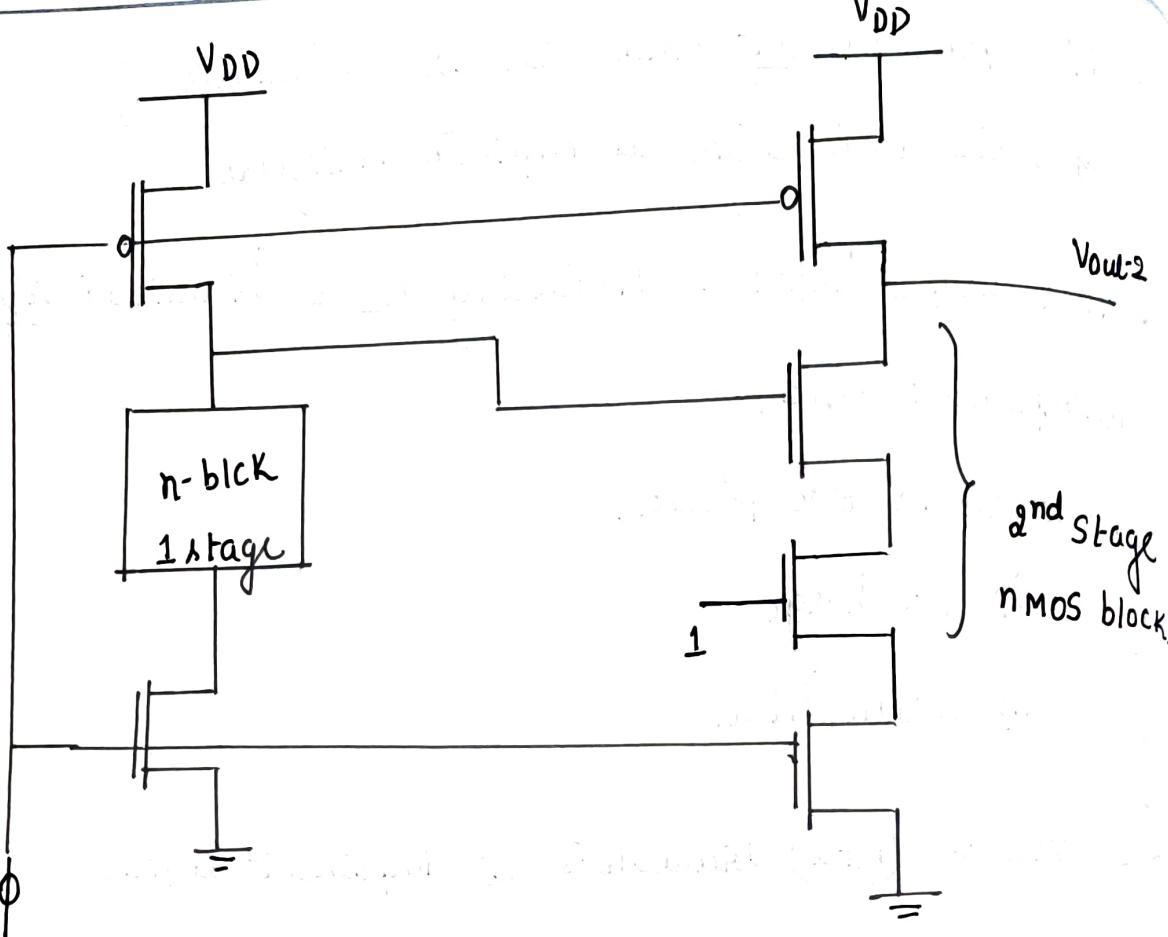


Ex:-

$$Y = \overline{A_1 A_2 A_3} \cdot \overline{B_1 B_2}$$

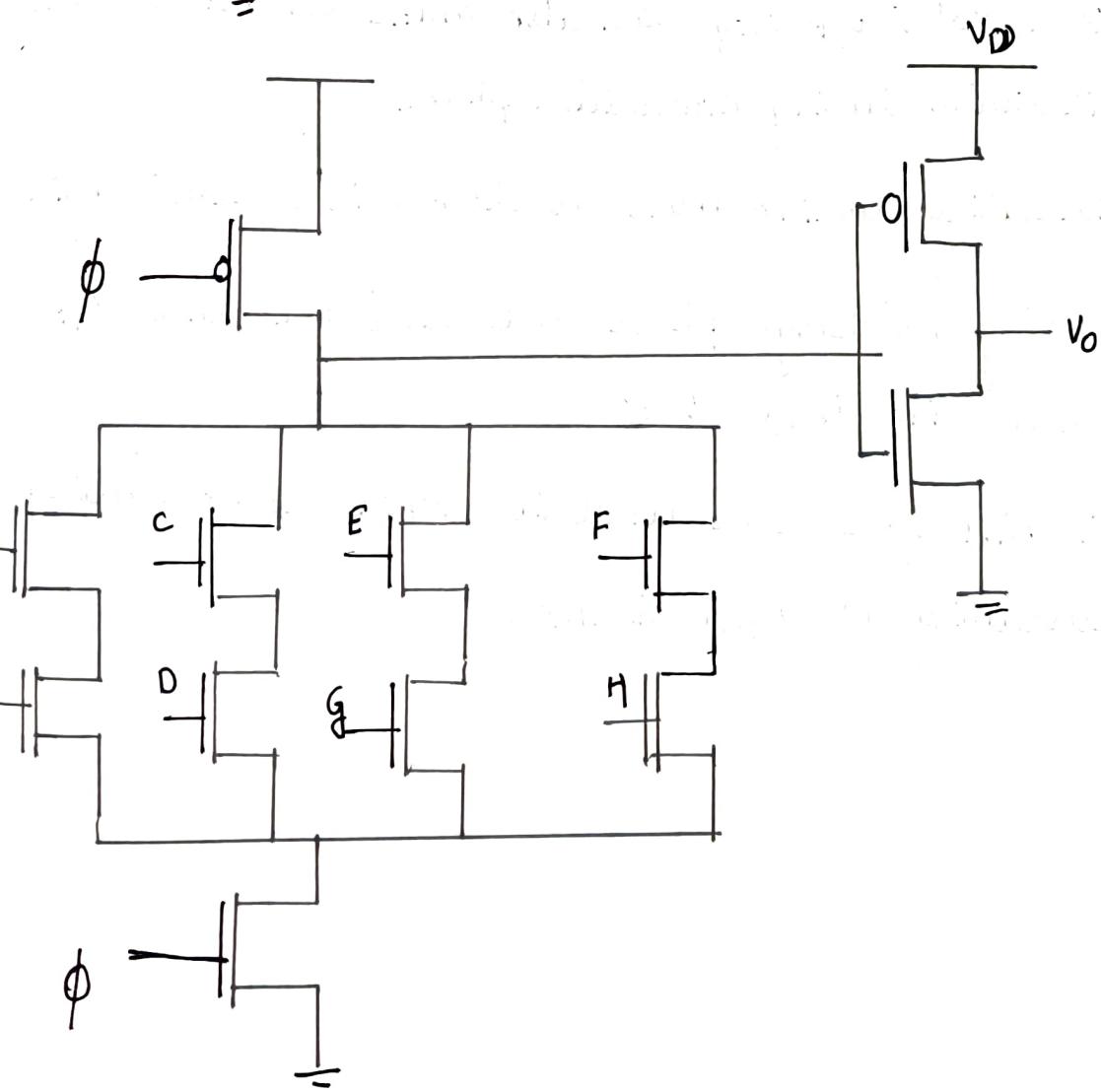
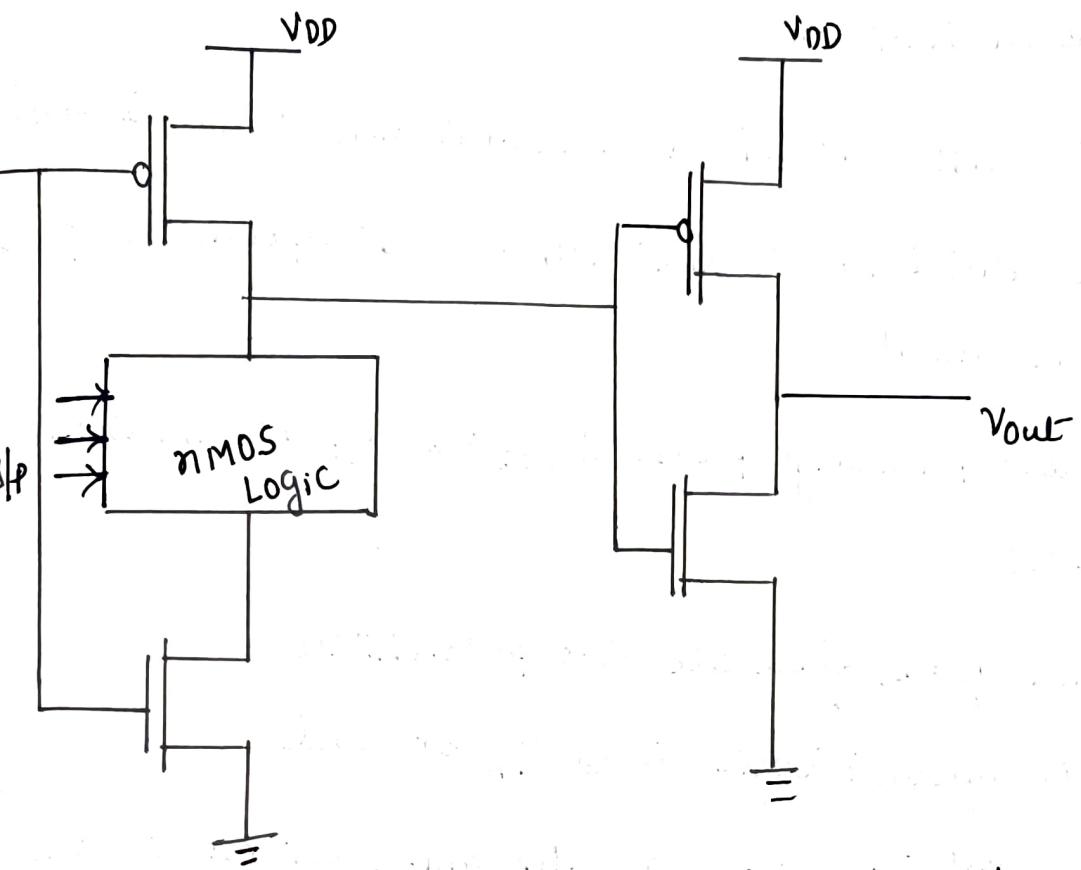


- The general st and example schematic of CMOS dynamic logic is depicted in figure.
- This Logic helps in reducing no of Transistor req to implement logic.
- It works in two phases.
  - i) Precharge
  - ii) Evaluation.
- It requires  $(n+2)$  transistors to implement logic.
- When  $\phi=0$  circuit operates in precharge mode
- In precharge mode O/p is initially precharged to Logic 1.
- When  $\phi=1$  circuit operates in Evaluation mode
- Here o/p will be computed based on s/p applied.
- It uses single phase clocking.
- The operation of single stage CMOS logic is straightforward
- cascading of CMOS dynamic logic is presenting significant problem.



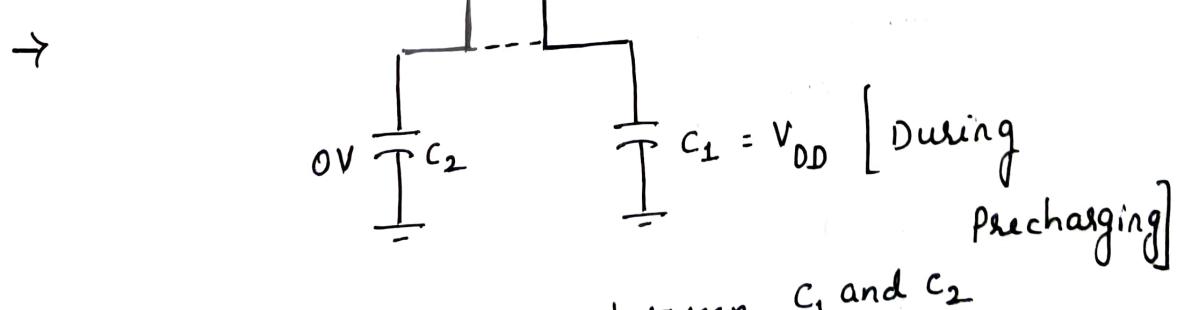
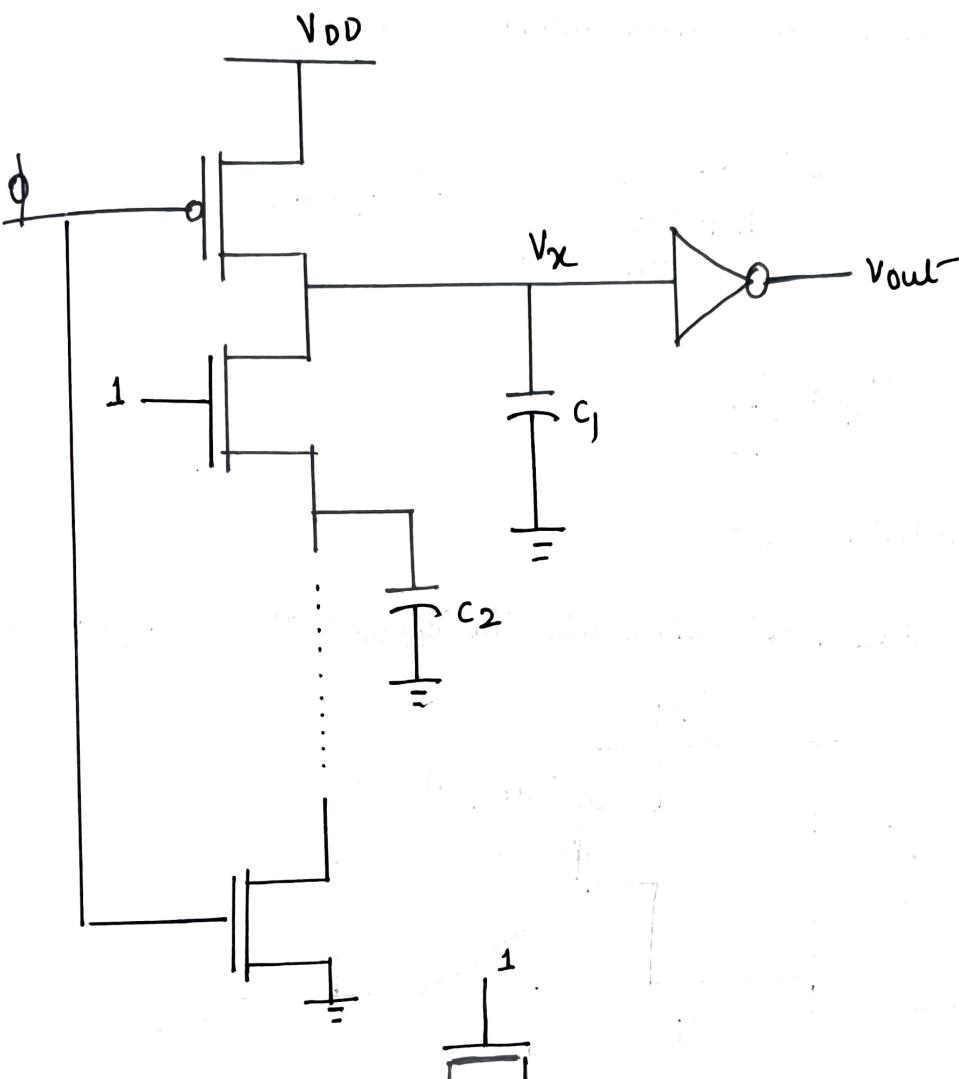
- assume during precharge state both  $V_{out1}$  &  $V_{out2} = V_{DD}$
- External s/p are applied during this phase.
- s/p of first stage are assumed such that  $V_{out1} = 0$
- During evaluation phase all stages evaluate concurrently
- $V_{out2}$  results in error result

# Domino CMOS logic :-



- Consider generalized circuit of domino CMOS logic shown in figure.
- The CMOS inverter is cascaded with dynamic logic
- The addition of inverters allow us to operate a no. of stages in cascade
- During precharge phase  $V_{out1} = 1$  o/p of CMOS inv  
 $V_{out2} = 0$
- When  $\phi = 1$ , there are two possibilities
- o/p of dynamic logic is @  $V_{DD}$  or gnd
- so inverter o/p  $V_{tg}$  can also make at most one transition during evaluation phase.
- cascading domino logic as shown in dynamic logic
- During precharge phase all the  $V_0 = 1$  and o/p of all the inv is @  $V_0 = 0$
- ∴ This st can be used to avoid error during cascading of dynamic CMOS.

- The main drawback of domino logic is it can generate only non inverting o/p.
- charge sharing between O/p & intermediate node of n-bit during evaluation phase results in error results



- charge will be sharing between  $C_1$  and  $C_2$

$$\rightarrow \text{if } C_1 = C_2$$

$$\rightarrow \left. \begin{array}{l} V_{C_1} = V_{DD} \\ V_{C_2} = 0 \end{array} \right\} \text{Initially}$$

$\rightarrow$  O/p node voltage after charge sharing

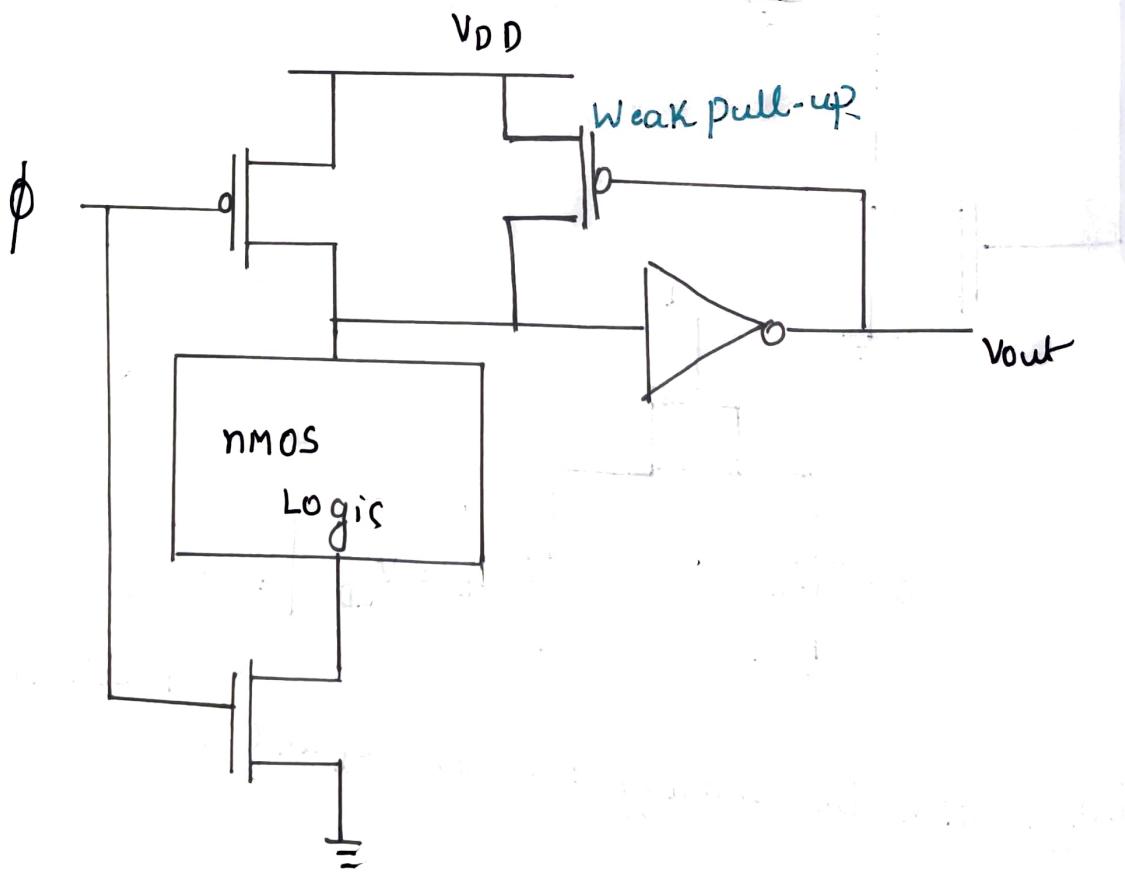
$$V_{C_1} = \frac{V_{DD}}{1 + \frac{C_2}{C_1}}$$

$\left. \begin{array}{l} \\ \end{array} \right\} \text{if } C_1 = C_2$

$$V_{C_1} = \frac{V_{DD}}{2}$$

$\rightarrow$  O/p results in error

$\rightarrow$  Measures taken to eliminate the effect of charge sharing



Multiple output domino CMOS gate realizing four functions :-  
 $C = C_1 + P C_2$

Multiple output domino cmos gate realizing four functions :-

$$\begin{aligned}
 C_1 &= g_1 + P_1 C_0 \\
 C_2 &= g_2 + P_2 g_1 + P_2 P_1 C_0 \\
 C_3 &= g_3 + P_3 g_2 + P_3 P_2 g_1 + \\
 &\quad P_3 P_2 P_1 C_0 \\
 C_4 &= g_4 + P_4 g_3 + P_4 P_3 g_2 + \\
 &\quad P_4 P_3 P_2 g_1 + P_4 P_3 P_2 P_1 C_0 \\
 &\quad \vdots
 \end{aligned}$$

