DIGITAL VLSI DESIGN

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Unit 2: Fabrication of MOSFETs & Circuit Design Process

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Complex Logic Circuits

The ability to realize complex logic functions using a small number of transistors is one of the most attractive features of nMOS and CMOS logic circuits.

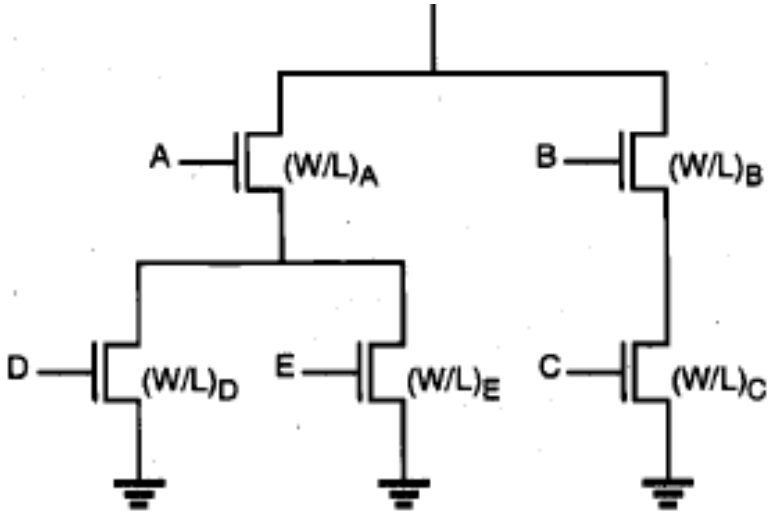
- Consider the following Boolean function as an example.

$$Z=\overline{A(D+E)+BC}$$

- Inspection of the circuit topology reveals the simple design principle of the pull-down network:
- * OR operations are performed by parallel-connected drivers.
- * AND operations are performed by series-connected drivers.
- * Inversion is provided by the nature of MOS circuit operation.

Complex Logic Circuits

Pull Down Network



- The realization of the n-net, or pull-down network, is based on the same basic design principles examined earlier.
- The pMOS pull-up network, on the other hand, must be the dual network of the n-net.
- This means that all parallel connections in the nMOS pull-down network will correspond to a series connection in the pMOS pull-up network, and all series connections in the pull-down network correspond to a parallel connection in the pull-up network.

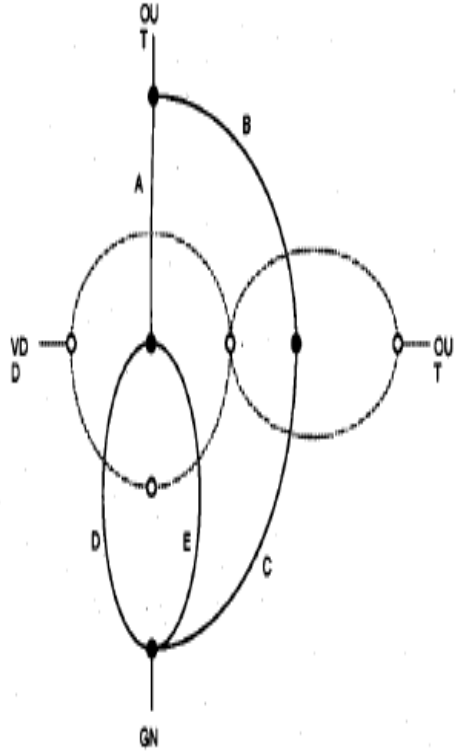
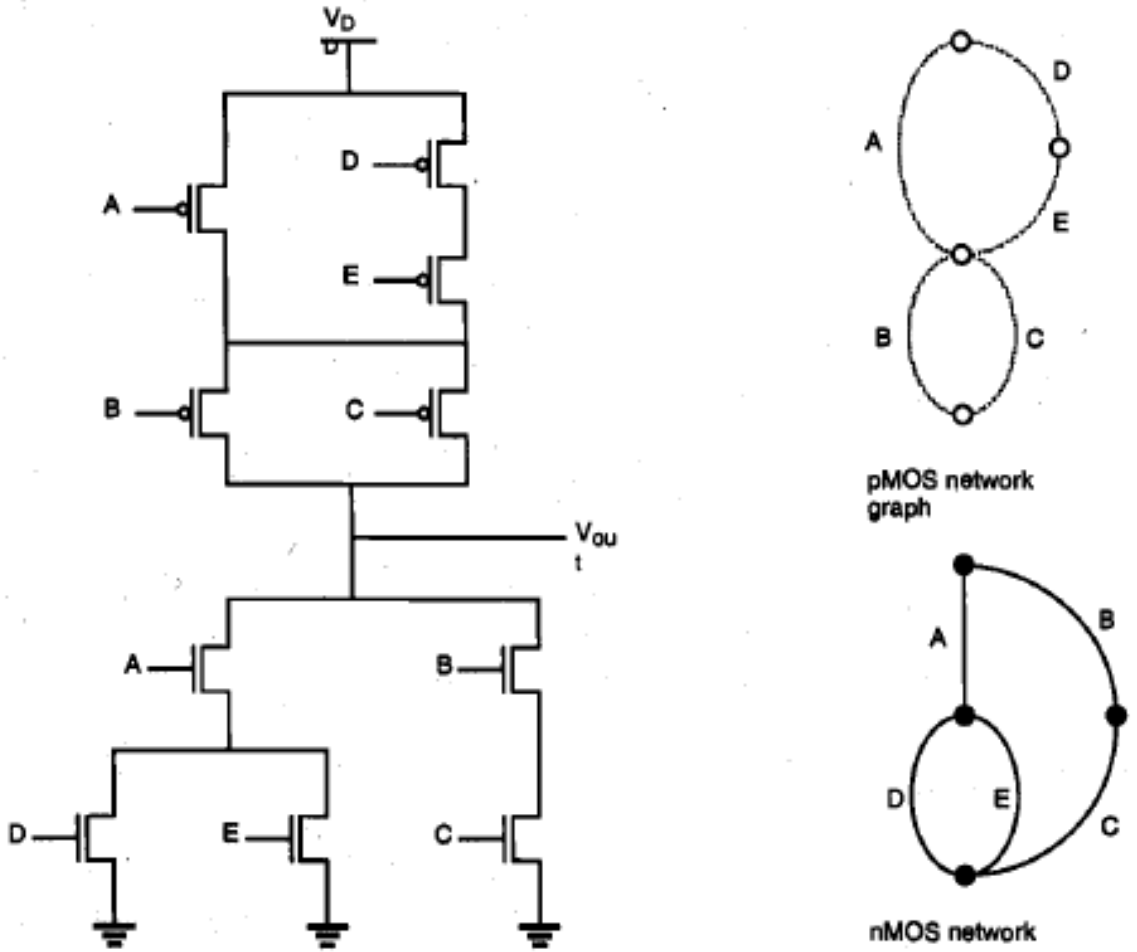


Figure 7.18. Construction of the dual pull-up graph from the pull-down graph, using the dual-graph concept.

Complex Logic Circuits

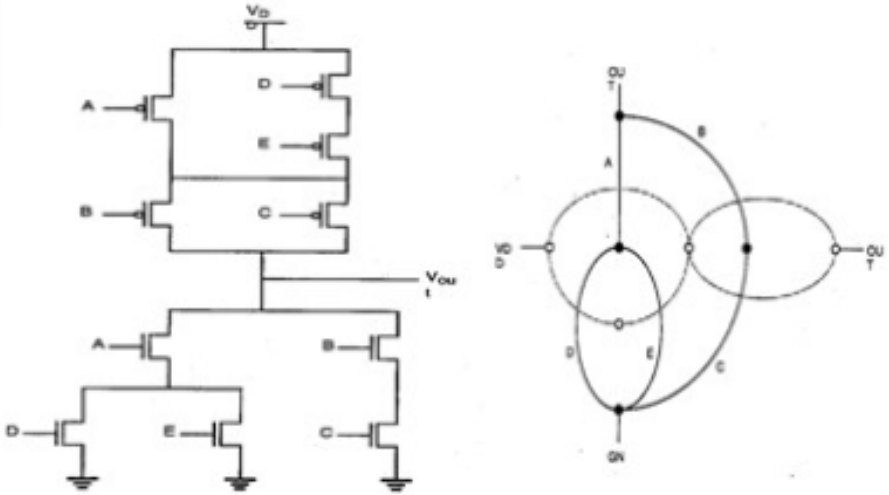


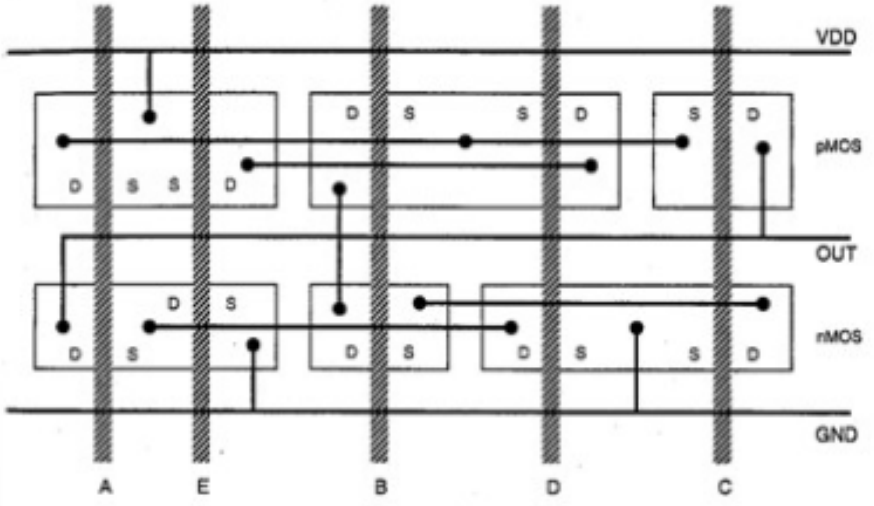
pMOS network graph

nMOS network

Figure 7.19. A complex CMOS logic gate realizing the Boolean function $Vout = \overline{A(D+E)+BC}$

Layout Technique using Euler Graph Method





- Euler Graph Technique can be used to determine if any complex CMOS gate can be physically laid out in an optimum fashion
  - –Start with either NMOS or PMOS tree (NMOS for this example) and connect lines for transistor segments, labeling devices, with vertex points as circuit nodes.
  - –Next place a new vertex within each confined area on the pull-down graph and connect neighboring vertices with new lines, making sure to cross each edge of the pull-down tree only once.
  - –The new graph represents the pull-up tree and is the dual of the pull-down tree.
- The stick diagram at the left (done with arbitrary gate ordering) gives a very non-optimum layout for the CMOS gate above.

THANK YOU

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