DIGITAL VLSI DESIGN

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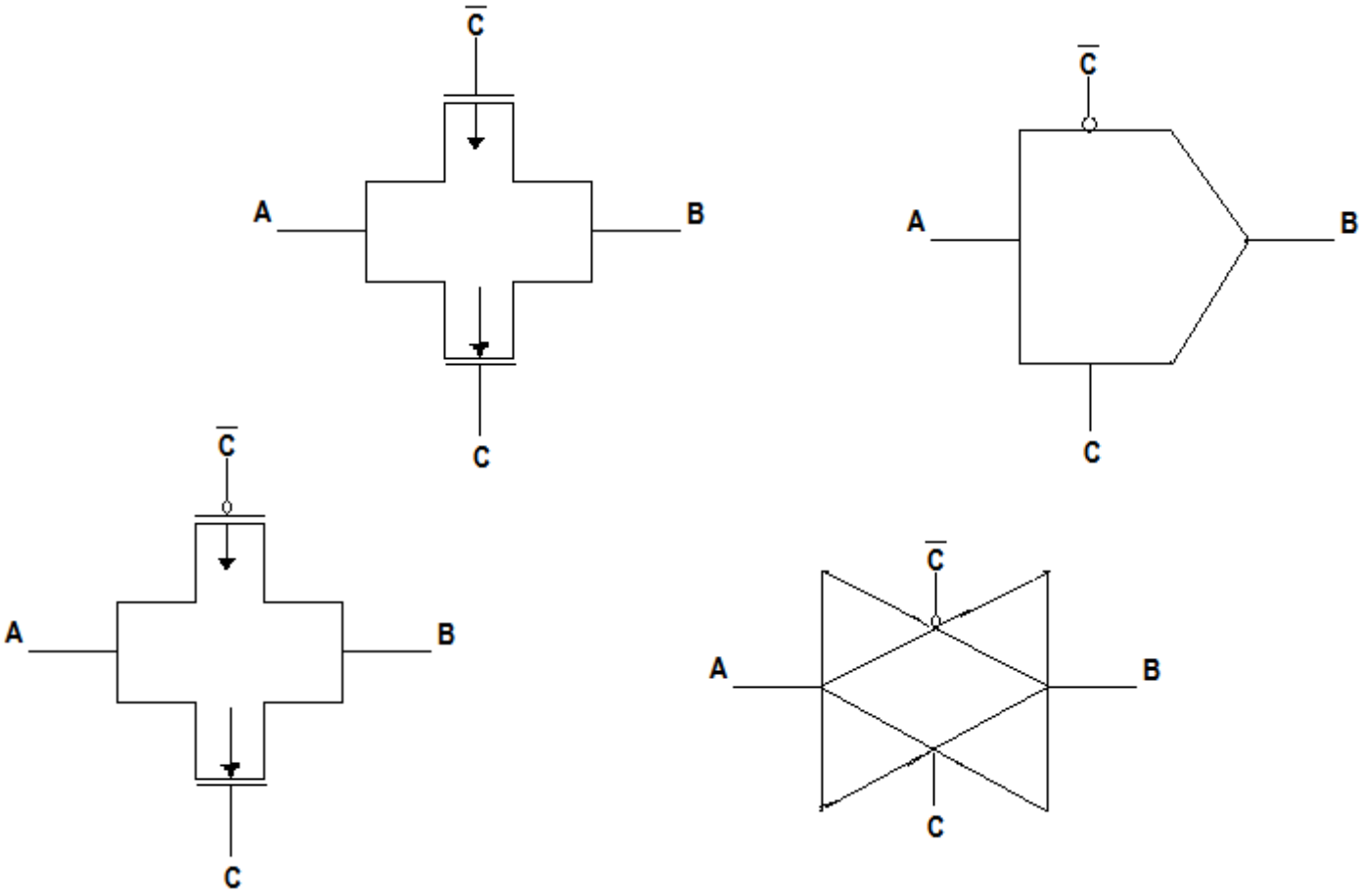
Dynamic Logic Circuit & Semiconductor Memories

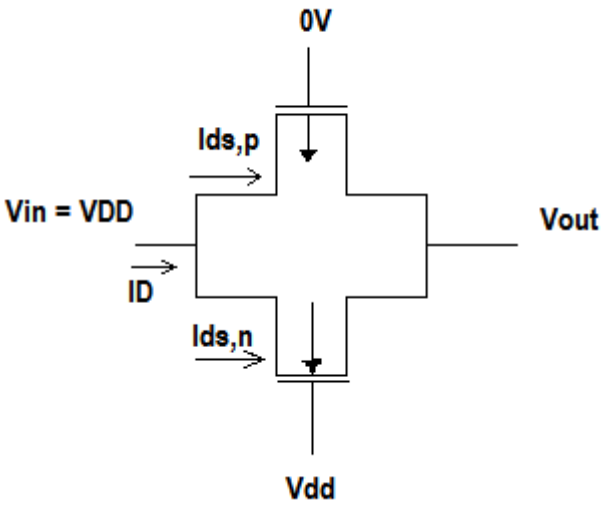
Unit 5: Dynamic Logic Circuit & Semiconductor Memories				
46-47	R1: Chap7 (7.5), R1: Chap9 (9.2, 9.4 and 9.6) R1: Chap 10 (10.1, 10.3 & 10.4)	CMOS Transmission Gates, Pass Gates (7.5, 9.2)	19 %	100%
48-49		Synchronous Dynamic Circuit Techniques (9.4)		
50 - 51		High Performance CMOS Dynamic circuits, Domino Logic (only till MODL) (9.6)		
52 – 56		Introduction, Basic SRAM and DRAM cell (10.1, 10.3 & 10.4)		

Reference Books:

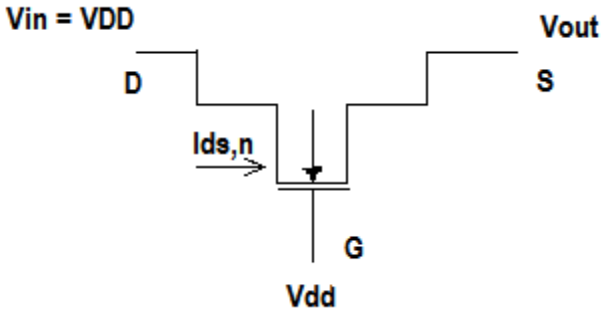
R1: CMOS Digital Integrated Circuits Analysis And Design, **Sung-Mo (Steve) Kang,**

Four different representations of the CMOS transmission gate (TG)





- substrate of the nMOS transistor is connected to GND
- the substrate of the pMOS transistor is connected to VDD
- Substrate-bias effect for both transistors must take into account



- Node A is input and Node B is output
- When control signal C=1 i.e., VDD
- Vin = VDD

- The Vds and Vgs of nMOS transistor is
- Vds, n = Vd – Vs, **Vds, n = Vdd – Vout**
- Vgs, n = Vg – Vs , **Vgs, n = Vdd – Vout**

- Thus, the nMOS
  - **Turned off** for **Vgs < Vtn**

$$\mathbf{Vdd - Vout < Vtn}$$

$$\mathbf{Vout > Vdd - Vtn}$$

- Operates in **saturation mode** for

$$\mathbf{Vout < Vdd - Vtn}$$

The Vds and Vgs of pMOS transistor is

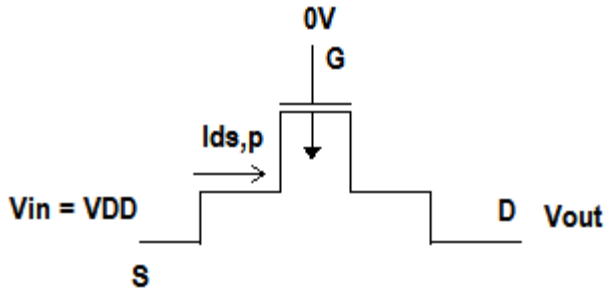
Vds, p = Vd – Vs, **Vds, p =Vout –Vdd**

Vgs, p = Vg – Vs , **Vgs, n = – Vdd**

pMOS operates in **linear region** for

Vds > Vgs – |Vt,p|

Vout > |Vt,p|



pMOS operates in **saturation mode** for

Vds < Vgs – |Vt,p| , thus Vout < |Vt,p|

Three operating regions for the CMOS transmission gate, depending on the output voltage level

- The total current flowing through TG,

$$I_D = I_{DS,n} + I_{DS,p}$$

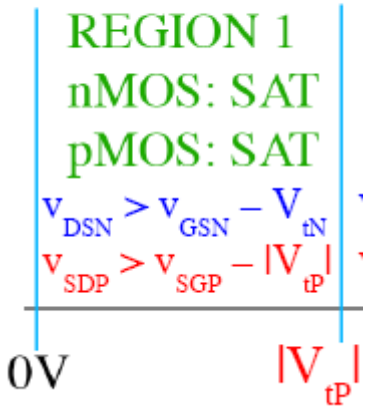
- Equivalent resistance for each transistor is

$$R_{eq,n} = \frac{V_{DD} - V_{out}}{I_{DS,n}} \quad \text{and} \quad R_{eq,p} = \frac{V_{DD} - V_{out}}{I_{DS,p}}$$

- The total equivalent resistance of the CMOS TG is the parallel equivalent of these two resistances.

Region 1

- The output voltage is smaller than $v_I = V_{DD}$ value of pMOS
- Vout < |Vtp|.
- Both transistors are in saturation



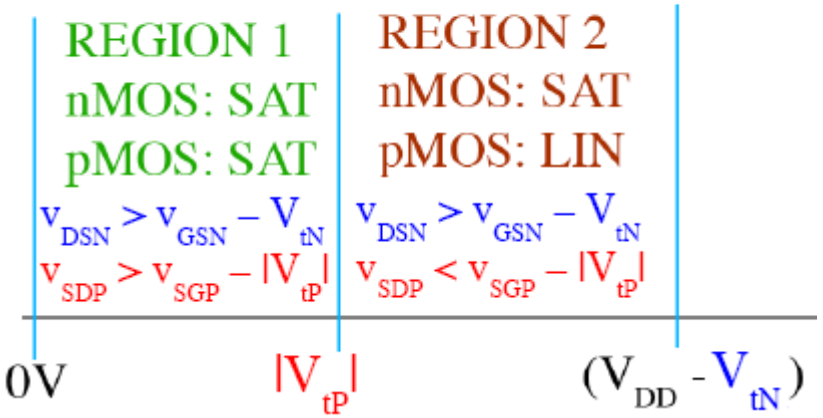
$$R_{eq,n} = \frac{2(V_{DD} - V_{out})}{K_n(V_{DD} - V_{out} - V_{t,n})^2}$$

$$R_{eq,p} = \frac{2(V_{DD} - V_{out})}{K_p(V_{DD} - |V_{t,p}|)^2}$$

Region 2

$$v_I = V_{DD}$$

$$R_{eq,n} = \frac{2(V_{DD} - V_{out})}{K_n(V_{DD} - V_{out} - V_{t,n})^2}$$

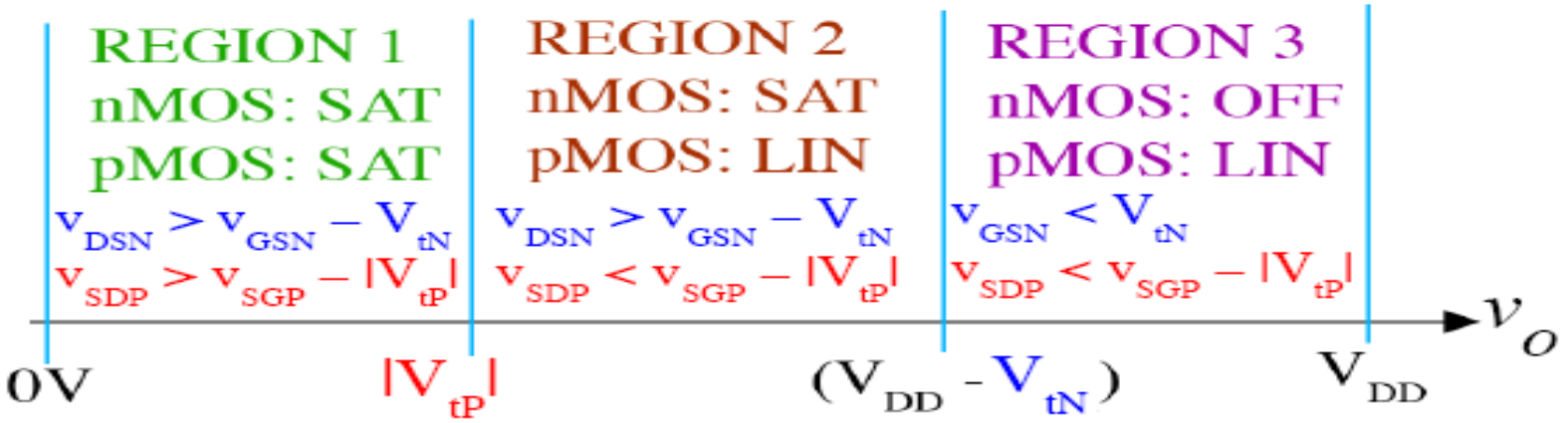


$$R_{eq,p} = \frac{2(V_{DD} - V_{out})}{K_p[2(V_{DD} - |V_{T,p}|)(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2]}$$

$$R_{eq,p} = \frac{2}{K_p[2(V_{DD} - |V_{T,p}|) - (V_{DD} - V_{out})]}$$

Region 3

$$v_I = V_{DD}$$

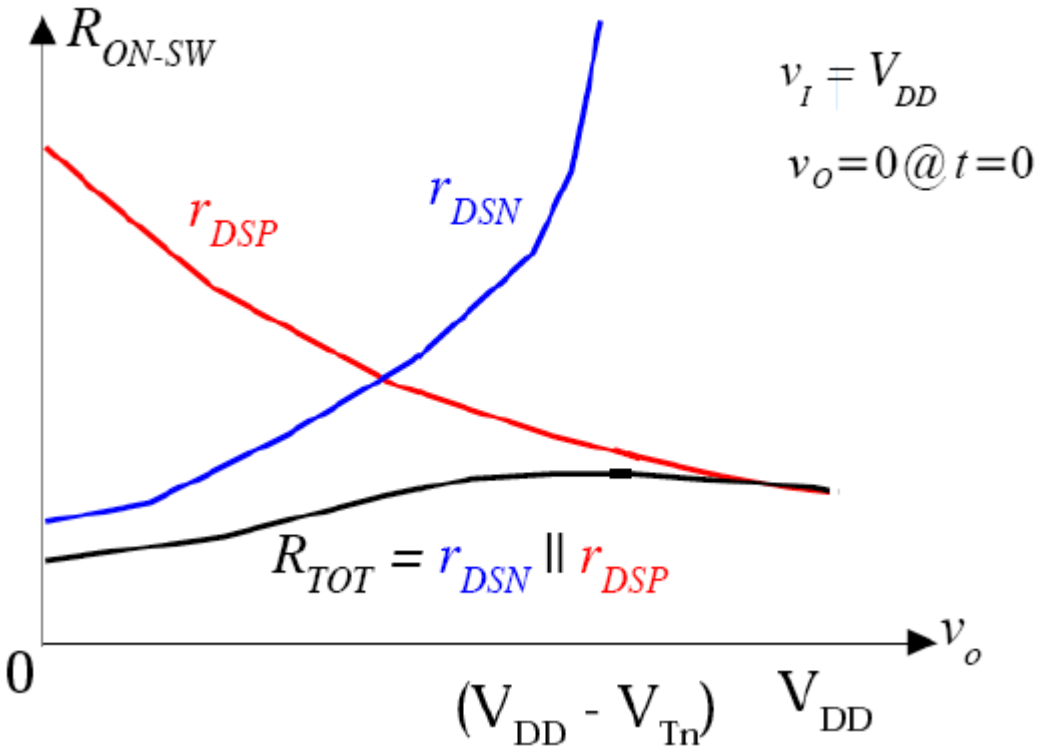


REGION 3
nMOS: OFF
pMOS: LIN

$$r_{DSN} = \infty$$

$$r_{DSP} = \frac{2}{k_p\left[2\left(V_{DD} - |V_{Tp}|\right) - \left(V_{DD} - V_{out}\right)\right]}$$

Equivalent resistance of the CMOS transmission gate as a function of output voltage.



- the total equivalent resistance of the TG remains relatively constant, i.e., its value is almost independent of the output voltage.
- Whereas the equivalent resistances of both nMOS and pMOS are strongly dependent on output voltage

CMOS transmission Gate

A CMOS pass gate which is turned on by a logic-high control signal can be replaced by its simple equivalent resistance for dynamic analysis, as shown in Fig. 7.36

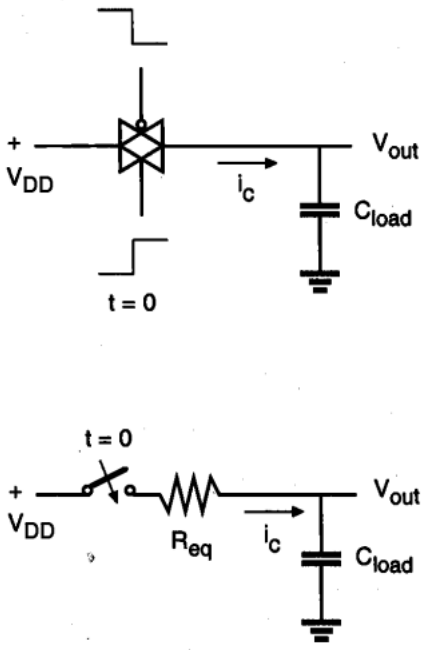
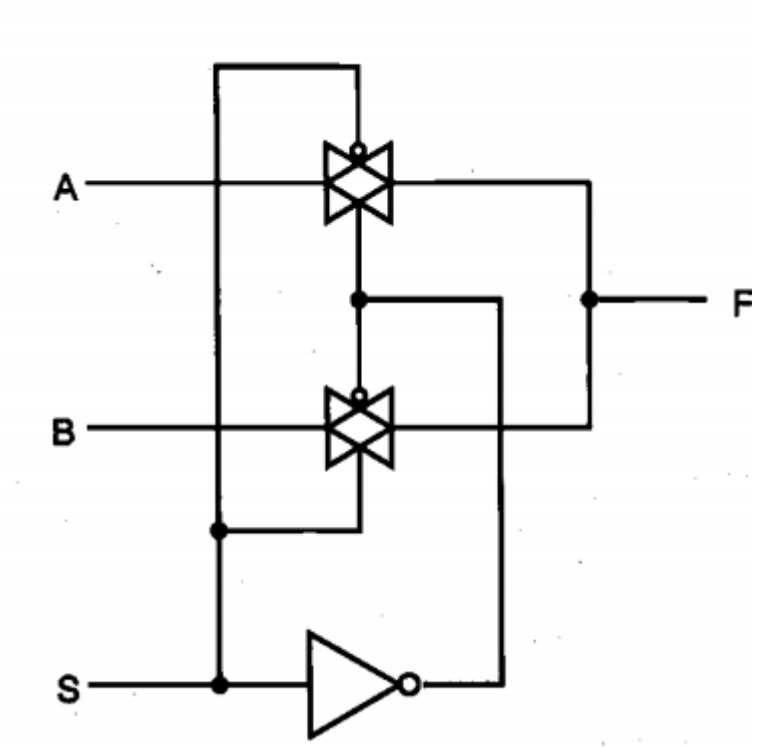
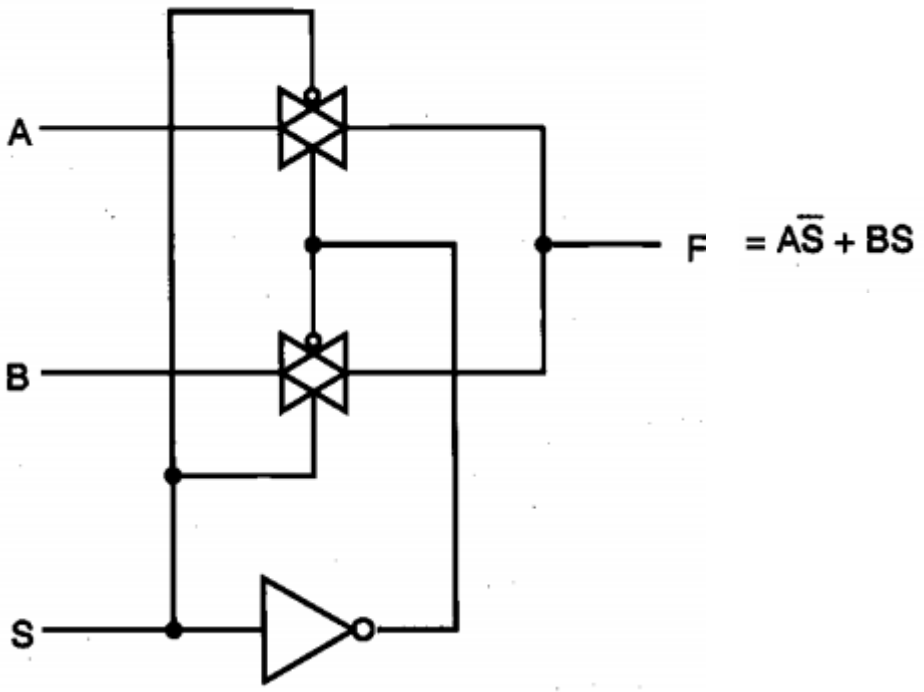
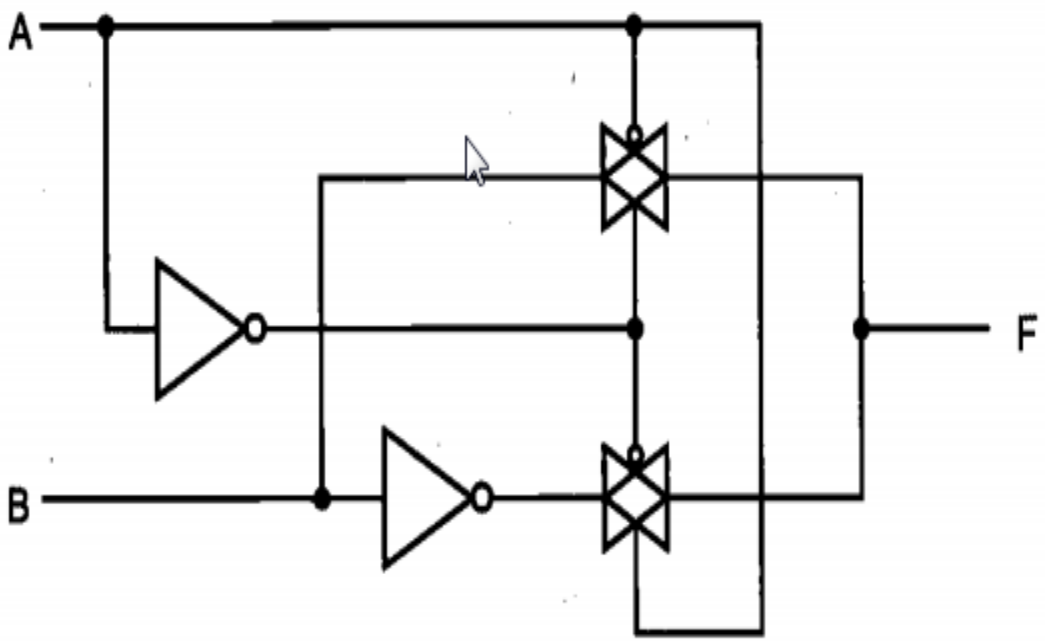


Figure 7.36. Replacing the CMOS TG with its resistor equivalent for transient analysis.

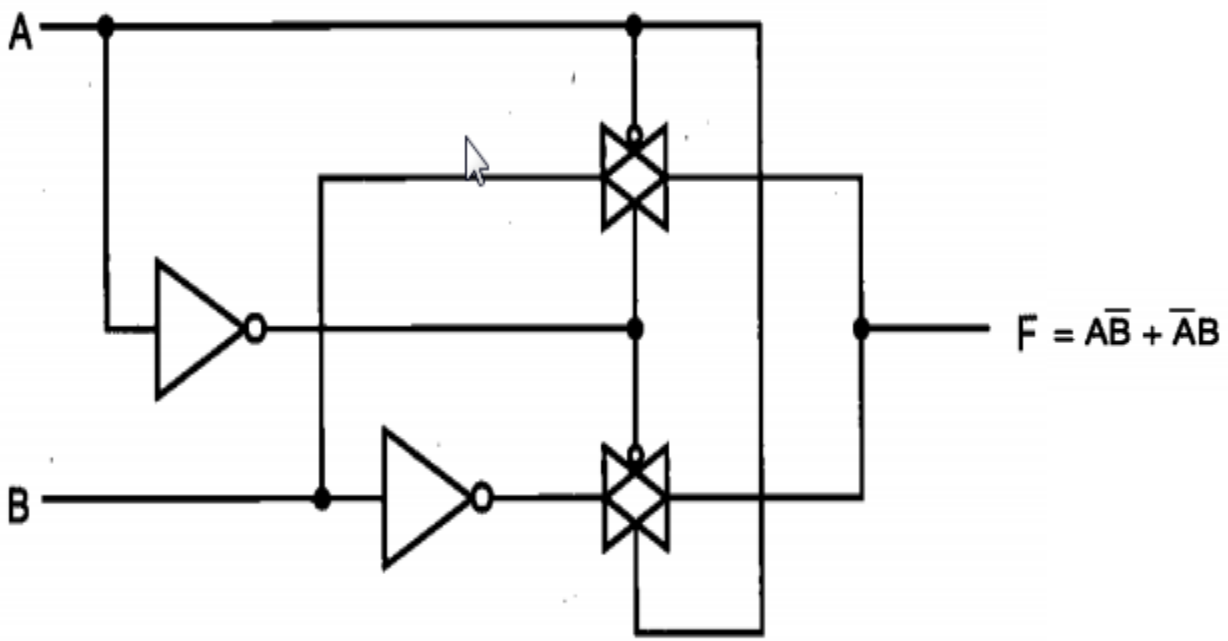

A
B
S
F

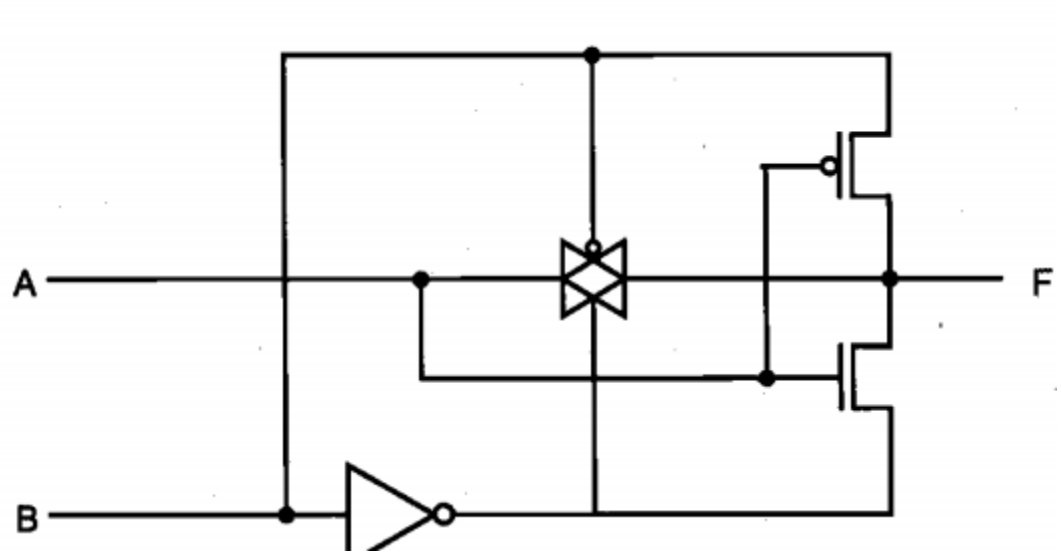
Two-input multiplexor circuit implemented using two CMOS TGs.



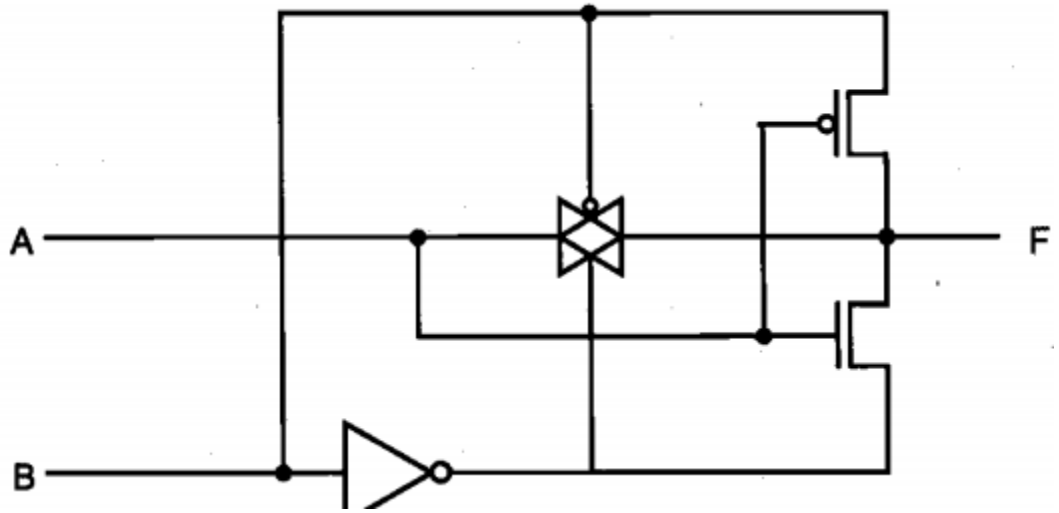

A
B
F

Eight-transistor CMOS TG implementation of the XOR function.




A
B
F

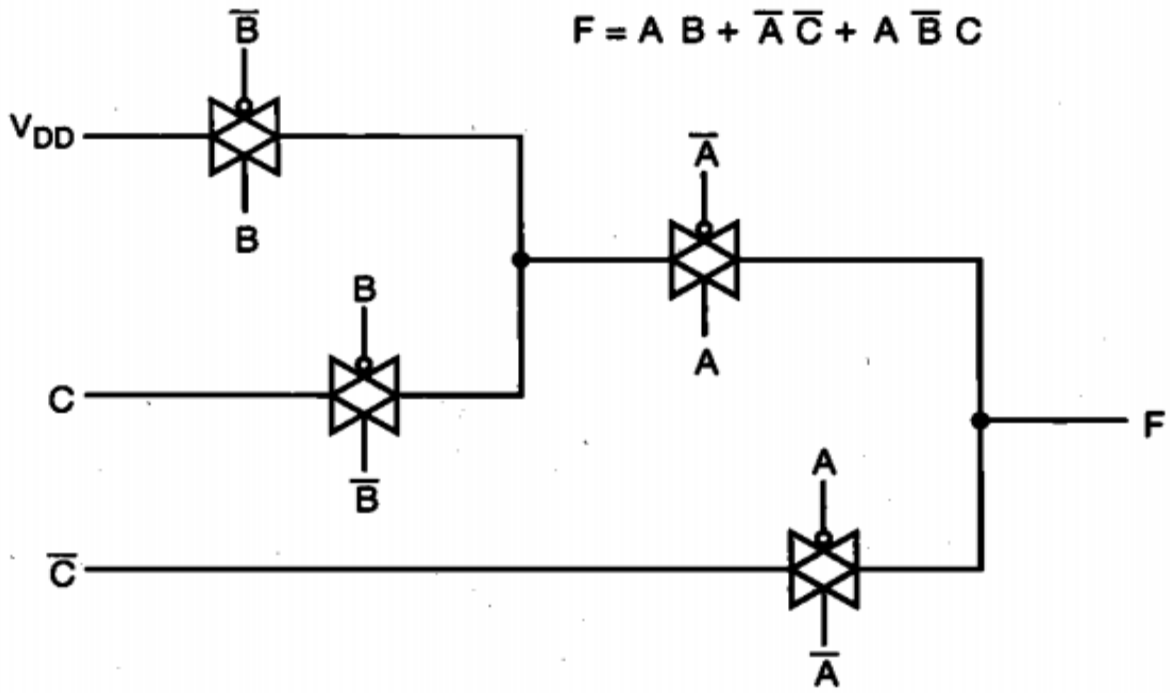
Six-transistor CMOS TG implementation of the XOR function.



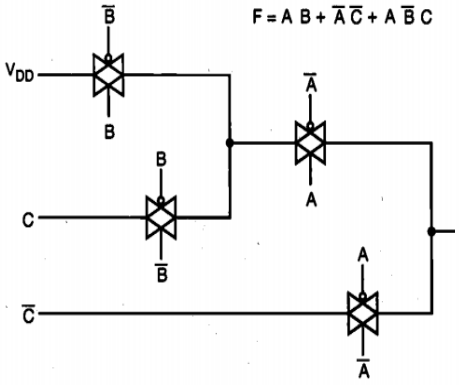
Implement the given function using TG

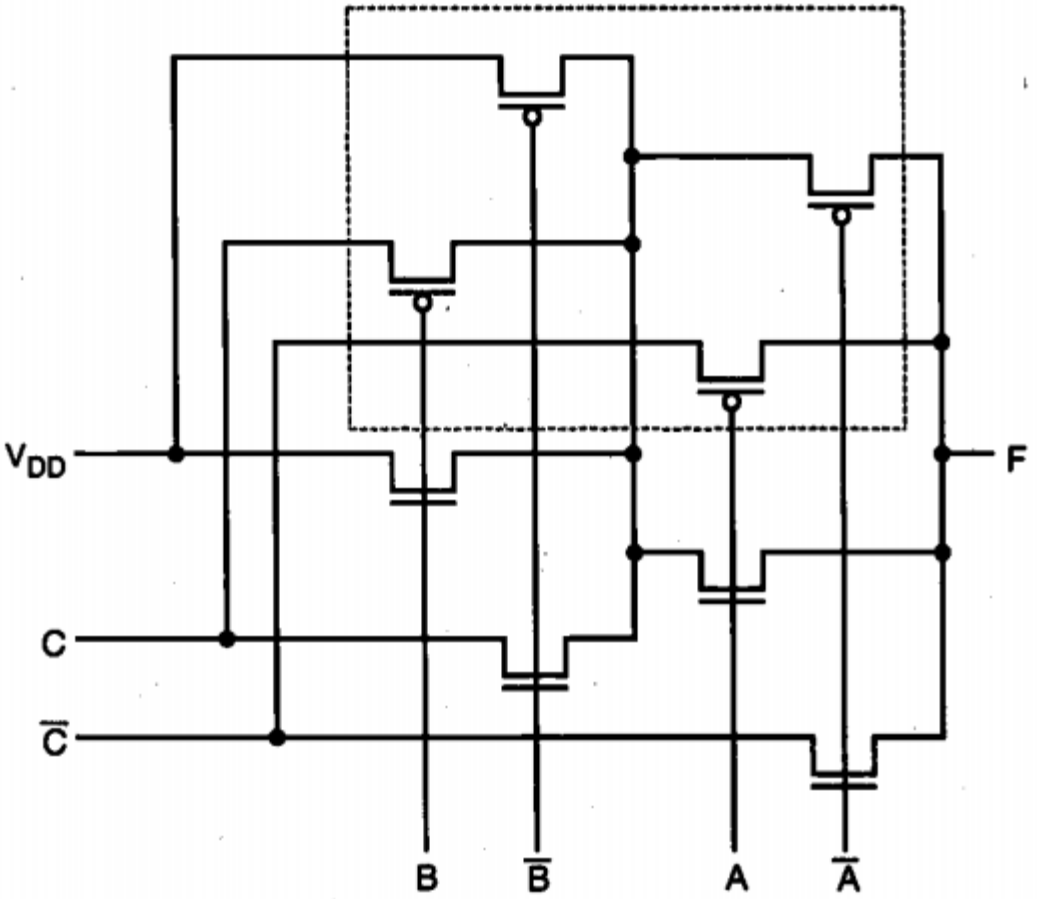
$$F = A\,B + \overline{A}\,\overline{C} + A\,\overline{B}\,C$$

Implement the given function using TG



Implement the given function using TG





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Basic Principles of Pass Transistor Circuits

Static v.s. Dynamic

- **Static Logic Gates**
  - Valid logic levels are steady-state operating points
  - Outputs are generated in response to input voltage levels after a certain time delay, and it can preserve its output levels as long as there is power.
  - All gate output nodes have a conducting path to V_{DD} or ***GND***, except when input changes are occurring.
- **Dynamic Logic Gates**
  - The operation depends on temporary storage of charge in parasitic node capacitances.
  - The stored charge **does not remain indefinitely**, so must be **updated** or **refreshed**. This requires establishment of an update or recharge path to the capacitance frequently enough to preserve valid voltage levels.

Static v.s. Dynamic

- **Advantages of Dynamic Logic Gates**
  - Allow implementation of simple sequential circuits with memory functions.
  - Use of common clock signals throughout the system ***enables the synchronization*** of various circuit blocks.
  - Implementation of complex circuits requires a ***smaller silicon area*** than static circuits.
  - Often consumes ***less dynamic power*** than static designs, due to smaller parasitic capacitances.

Basic Principles of Pass Transistor Circuits
Logic "1" Transfer

- The Pass transistor MP is driven by the parasitic capacitance C_x, depending on the input signal V_{in}.
- There are two possible operations when CK = 1:
  - Charging-up the capacitance C_x to a logic-high level
  - Charging-down the capacitance C_x to a logic-low level
- If $CK = 0$: MP is off, C_x is unchanged.
- In either case, the output of the depletion – load nMOS inverter assumes a logic-low or logic-high level, depending on V_x.

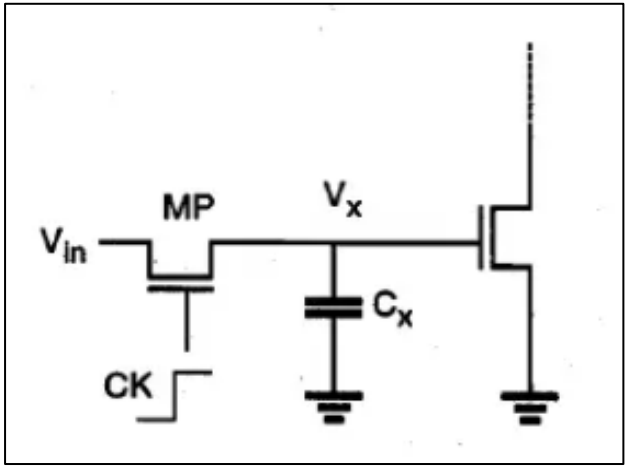


Fig.1 : The basic building block of nMOS dynamic logic, which consists of an nMOS pass transistor driving the gate of another nMOS transistor.

Basic Principles of Pass Transistor Circuits
Logic "1" Transfer

- Pass transistor MP provides the only current path to the intermediate capacitive node (soft node) X.
- When clock signal is inactive (CK = 0), the pass transistor ceases to conduct.
- Output of the inverter is determined by the charge stored by the capacitor C_x.
- Two events to examine:
  - Charge-up (logic-1 transfer) event
  - Charge-down (logic-0 transfer) event

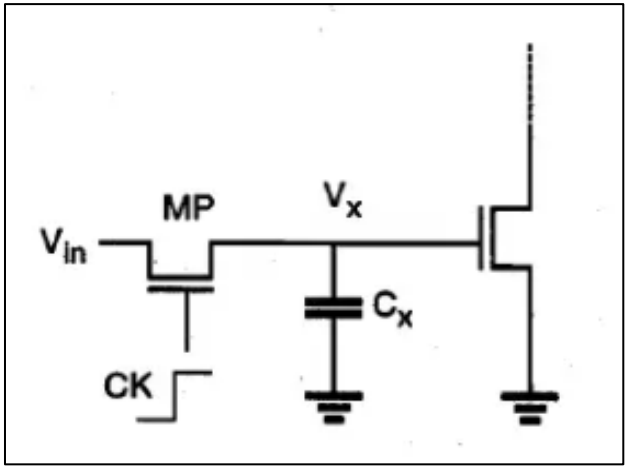
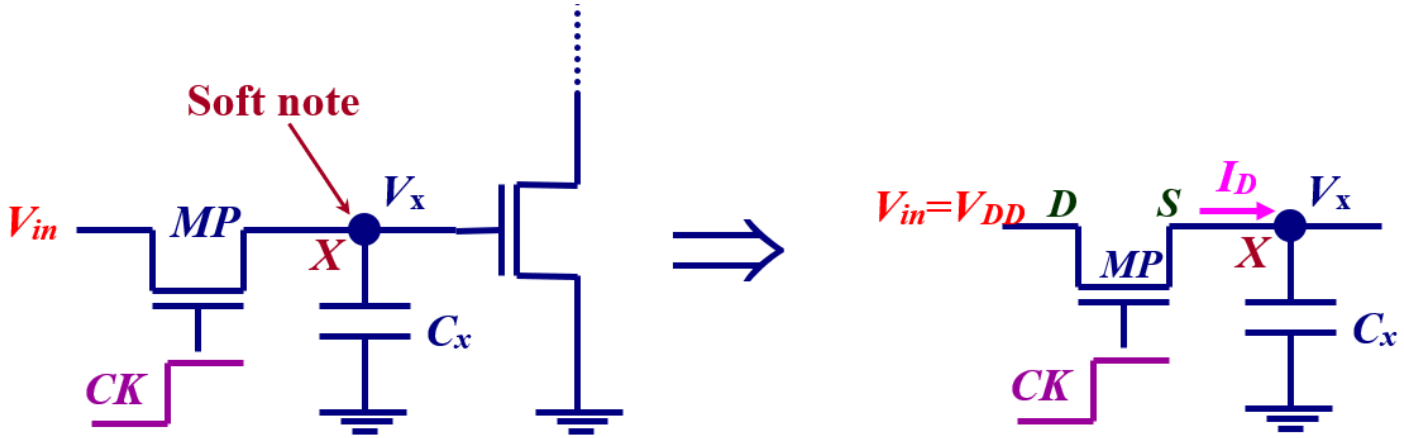


Fig.1 : The basic building block of nMOS dynamic logic, which consists of an nMOS pass transistor driving the gate of another nMOS transistor.

Basic Principles of Pass Transistor Circuits
Logic "1" Transfer

- **Logic "1" Transfer:** $V_X(t=0)=0V$, $V_{in}=V_{OH}=V_{DD}$, $CK=0 \rightarrow V_{DD}$



- $V_{GS} = V_{DD} - V_X$, $V_{DS} = V_{DD} - V_X = V_{GS}$.
- Therefore, $V_{DS} > V_{GS} - V_{T,MP} \Rightarrow$ **MP** is in saturation.

$$C_X \frac{dV_X}{dt} = \frac{k_n}{2}\left(V_{DD} - V_X - V_{T,MP}\right)^2$$

- Note that the $V_{T,MP}$ is subject to substrate bias effect and therefore, depends on the voltage level V_X. We will neglect the substrate bias effect for simplicity.

Basic Principles of Pass Transistor Circuits
Logic "1" Transfer

- Integrating the above equation with ***t*** from 0 → ***t*** and V_X from 0 → V_X, we have

$$\int_0^t dt = \frac{2C_X}{k_n}\int_0^{V_X}\frac{dV_X}{\left(V_{DD}-V_X-V_{T,MP}\right)^2}$$

$$= \frac{2C_X}{k_n}\left.\frac{1}{V_{DD}-V_X-V_{T,MP}}\right|_0^{V_X}$$

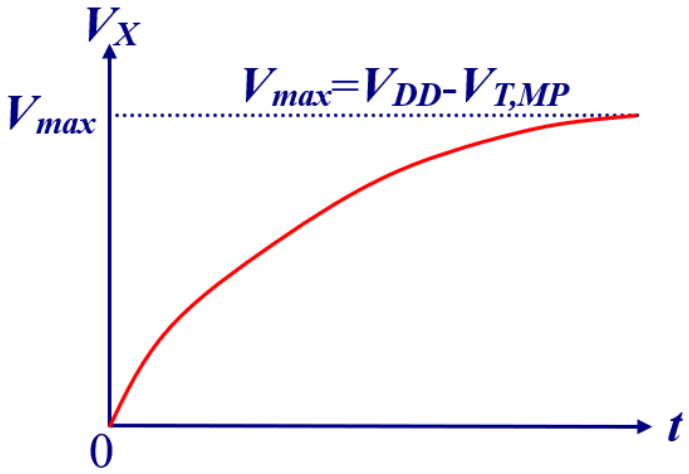
- Therefore,

$$t = \frac{2C_X}{k_n}\left(\frac{1}{V_{DD}-V_X-V_{T,MP}} - \frac{1}{V_{DD}-V_{T,MP}}\right)$$

- and,

$$V_X(t) = \left(V_{DD}-V_{T,MP}\right)\frac{\frac{k_n\left(V_{DD}-V_{T,MP}\right)}{2C_X}t}{1+\frac{k_n\left(V_{DD}-V_{T,MP}\right)}{2C_X}t}$$

Basic Principles of Pass Transistor Circuits Logic "1" Transfer



- V_X rises from 0V and approaches a limit value $V_{max} = V_X(t)|_{t=\infty} = V_{DD}-V_{T,MP}$, but it can not exceed this value, since the pass transistor will turn off at this point ($V_{GS}=V_{T,MP}$). Therefore, it transfers a ***"weak logic 1"***.
- The actual V_{max} by taking the body effect into account is,

$$V_{max} = V_{DD} - V_{T0,MP} - \gamma\left(\sqrt{|2\phi_F| + V_{max}} - \sqrt{|2\phi_F|}\right)$$

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Logic “1” Transfer

- Voltage obtained at node X following a logic “1” transfer is lower than V_{DD}.
- If zero-bias threshold voltage is used, then rise time of voltage V_x will be underestimated and actual charge-up time will be longer than predicted.
- There is significant implication for circuit design with the fact that node voltage V_x has an upper limit of $V_{max} = (V_{DD} - V_{T,n})$
- To understand this, consider two cases:
  - Logic “1” at the input node is being transferred through a chain of cascaded pass transistors.
  - Output of each pass transistor drives the gate of another pass transistor.

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Logic "1" Transfer

Case 1: Logic "1" at the input node is being transferred through a chain of cascaded pass transistors

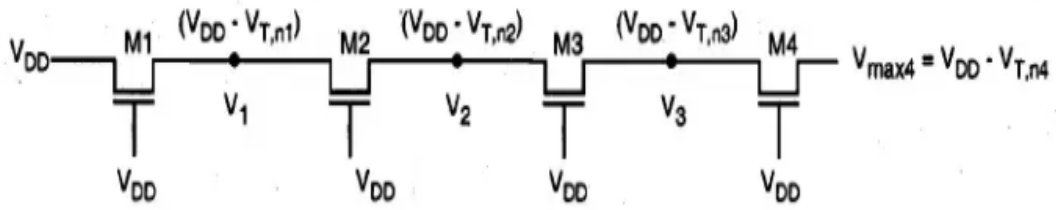

Fig. 7: Node voltages in a pass transistor chain during the logic "1" transfer

- Initially assume all internal node voltages V_1 through V_4 are zero
- M1 operates in saturation with $V_{DS1} > V_{GS1} - V_{T,n1}$
- $\therefore V_1$ cannot exceed $V_{max1} = (V_{DD} - V_{T,n1})$
- Assume all pass transistors are identical, M2 operates at the saturation boundary, $\therefore V_{max2} = \left(V_{DD} - V_{T,n2}\right)$
- With $V_{T,n1} = V_{T,n2} = V_{T,n3} = \cdots$, the node voltage at the end of the pass transistor chain will become one threshold voltage lower than V_{DD} regardless of the number of pass transistors in the chain.

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Logic “1” Transfer

Case 2: Output of each pass transistor drives the gate of another pass transistor

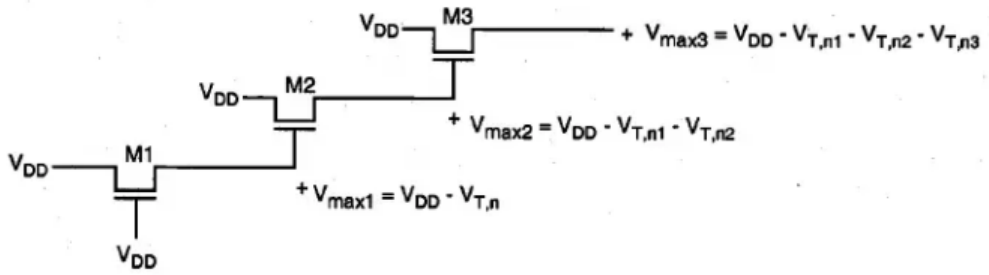

Fig. 8: Node voltages during the logic “1” transfer, when each pass transistor is driving another pass transistor.

- Here Output of M1 can reach $V_{max1} = (V_{DD} - V_{T,n1})$
- This voltage drives the gate of the second pass transistor and upper limit of V_2 is $V_{max2} = V_{DD} - V_{T,n1} - V_{T,n2}$
- Each stage causes a significant loss of voltage level.

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Logic "1" Transfer

Case 2: Output of each pass transistor drives the gate of another pass transistor

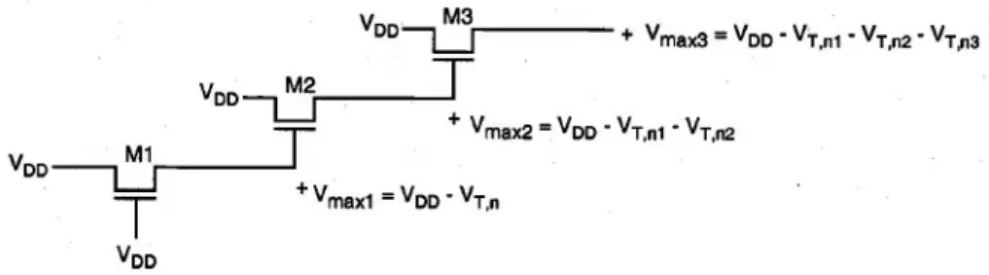

Fig. 8: Node voltages during the logic "1" transfer, when each pass transistor is driving another pass transistor.

- The amount of voltage drop at each stage taking into account the corresponding substrate bias effect can be approximated as

$$V_{T,n1} = V_{T0,n} - \gamma\left(\sqrt{|2\varphi_F| + V_{max1}} - \sqrt{|2\varphi_F|}\right)$$

$$V_{T,n2} = V_{T0,n} - \gamma\left(\sqrt{|2\varphi_F| + V_{max2}} - \sqrt{|2\varphi_F|}\right) \quad (6)$$

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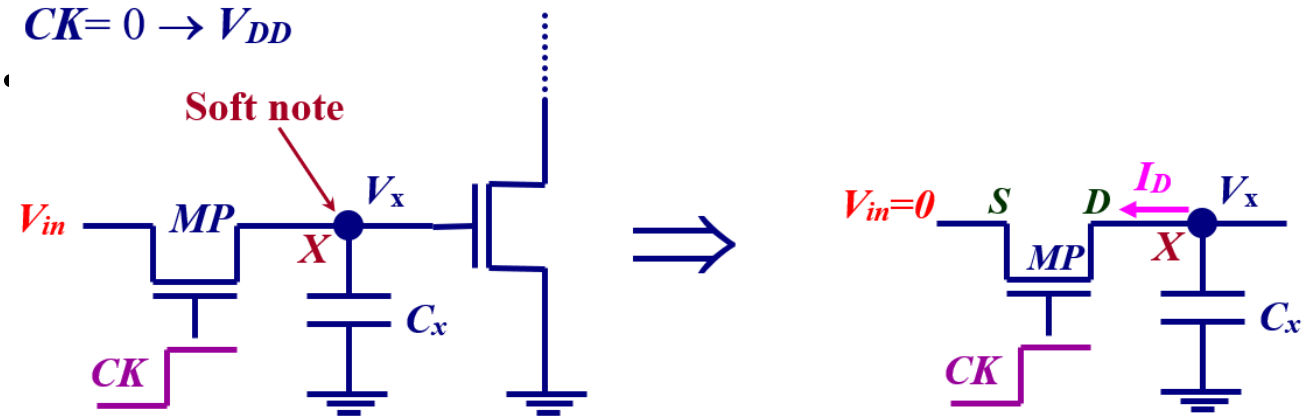
Basic Principles of Pass Transistor Circuits
Logic "0" Transfer

- **Logic "0" Transfer:** $V_X(t=0)=V_{max}= V_{DD} - V_{T,MP}$, $V_{in}=V_{OL}=0V$,



- $V_{GS} = V_{DD}$, $V_{DS} = V_{max} = V_{DD} - V_{T,MP}$.
- Therefore, $V_{DS} \leq V_{GS} - V_{T,MP} \Rightarrow$ **MP** is in linear region.

$$-C_X \frac{dV_X}{dt} = \frac{k_n}{2}\left[2\left(V_{DD} - V_{T,MP}\right)V_X - V_X^2\right]$$

- Note that the V_{SB}=0. Hence, there is no body effect for **MP** ($V_{T,MP}= V_{T0,MP}$). But the initial condition $V_X(t=0)=V_{DD} - V_{T,MP}$ contains the threshold voltage with body effect. To simplify the expressions, we will use $V_{T,MP}$ in the following.

Basic Principles of Pass Transistor Circuits
Logic "0" Transfer

- MP in linear region discharges C_x

$$-C_x \frac{dV_x}{dt} = \frac{k_n}{2}\left(2(V_{DD} - V_{T,n})V_x - V_x^2\right)$$

$$dt = -\frac{2C_x}{k_n} \cdot \frac{dV_x}{2(V_{DD} - V_{T,n})V_x - V_x^2}$$

Integrating both sides

$$\int_0^t dt = -\frac{2C_x}{k_n} \int_{V_{DD}-V_{T,n}}^{V_x} \left(\frac{\frac{1}{2(V_{DD} - V_{T,n})}}{2(V_{DD} - V_{T,n}) - V_x} + \frac{\frac{1}{2(V_{DD} - V_{T,n})}}{V_x} \right) dV_x$$

$$t = \frac{C_x}{k_n(V_{DD} - V_{T,n})} \left[ln\left(\frac{2(V_{DD} - V_{T,n}) - V_x}{V_x} \right) \right] |_{V_{DD}-V_{T,n}}^{V_x}$$

The fall-time expression for the node voltage V_x is

$$t = \frac{C_x}{k_n(V_{DD} - V_{T,n})} \left[ln\left(\frac{2(V_{DD} - V_{T,n}) - V_x}{V_x} \right) \right]$$

Basic Principles of Pass Transistor Circuits
Logic "0" Transfer

- Voltage drops from logic-high level of V_{max} to 0V.
- The applied input voltage level (logic "0") can be transferred to the soft node without any modification during this event.
- Fall-time can be calculated using two time points $t_{90\%}$ and $t_{10\%}$.

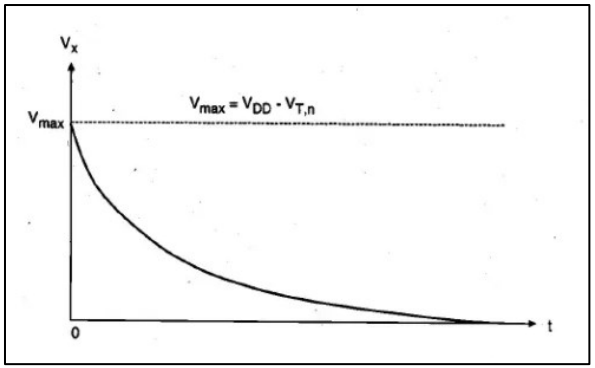


Fig. 5: Variation of V_x as a function of time during logic "0" transfer.

Basic Principles of Pass Transistor Circuits
Logic "0" Transfer

- Fall-time (τ_{fall}) for soft node voltage V_x:

Assume two points $t_{90\%}$ and $t_{10\%}$ as the times at which node voltage is 0.9 V_{max} and 0.1 V_{max}.

$$t_{90\%} = \frac{C_x}{k_n(V_{DD} - V_{T,n})} \ln\left(\frac{(2 - 0.9)(V_{DD} - V_{T,n})}{0.9(V_{DD} - V_{T,n})}\right)$$

$$= \frac{C_x}{k_n(V_{DD} - V_{T,n})} \ln\frac{1.1}{0.9}$$

$$t_{10\%} = \frac{C_x}{k_n(V_{DD} - V_{T,n})} \ln\frac{1.9}{0.1}$$

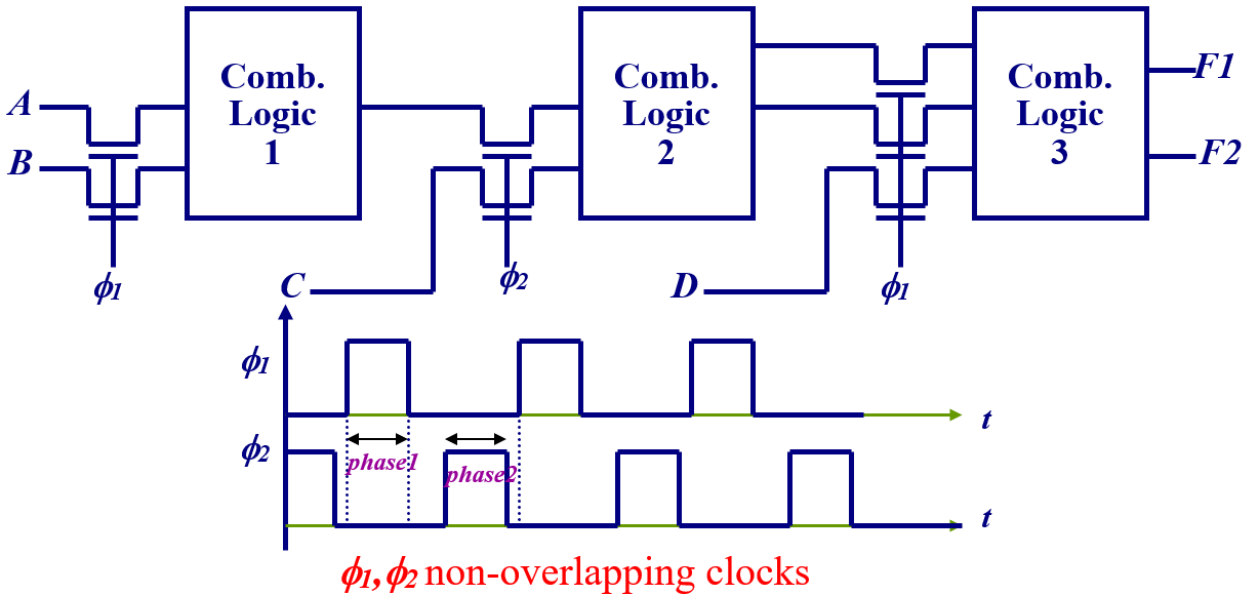
$$\tau_{fall} = t_{90\%} - t_{10\%} = \frac{C_x}{k_n(V_{DD} - V_{T,n})} [\ln(19) - \ln(1.22)]$$

$$= 2.74 \frac{C_x}{k_n(V_{DD} - V_{T,n})}$$

The transient charge-up and charge down events which are responsible for logic "1" transfer and logic "0" transfer during the active clock phase, i.e., when CK = 1.
When Ck = 0 the storage of logic levels at the soft node X

Synchronous Dynamic Circuit Techniques – Dynamic Pass Transistor Circuits

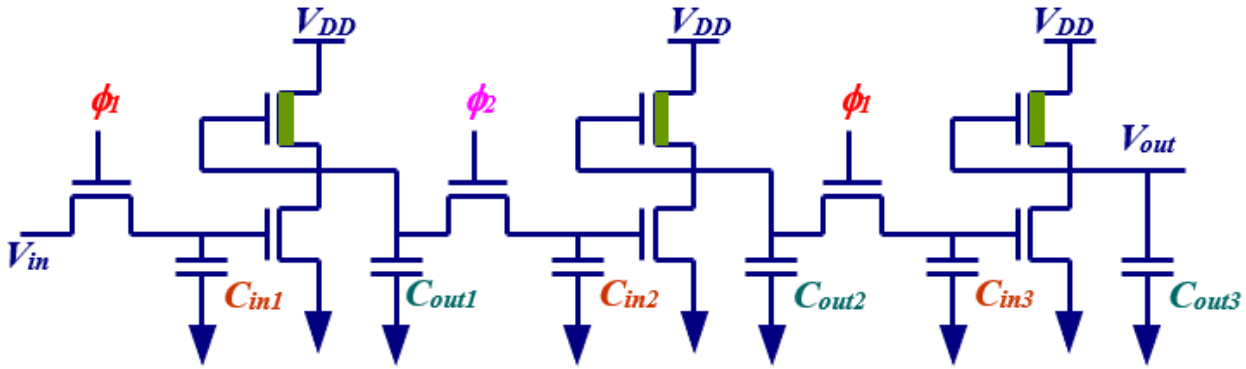
- The multi-stage synchronous circuit is shown below. The circuit consists of **cascaded combinational logic stages interconnected through nMOS pass transistors**. Its operation depends on temporary charge storage in the parasitic input capacitances.



- Logic levels are stored on input capacitances during the inactive clock phase.

Dynamic Pass Transistor Circuits
Two-Phase Clock Dynamic Shift Register

- **Depletion-Load Dynamic Shift Register**

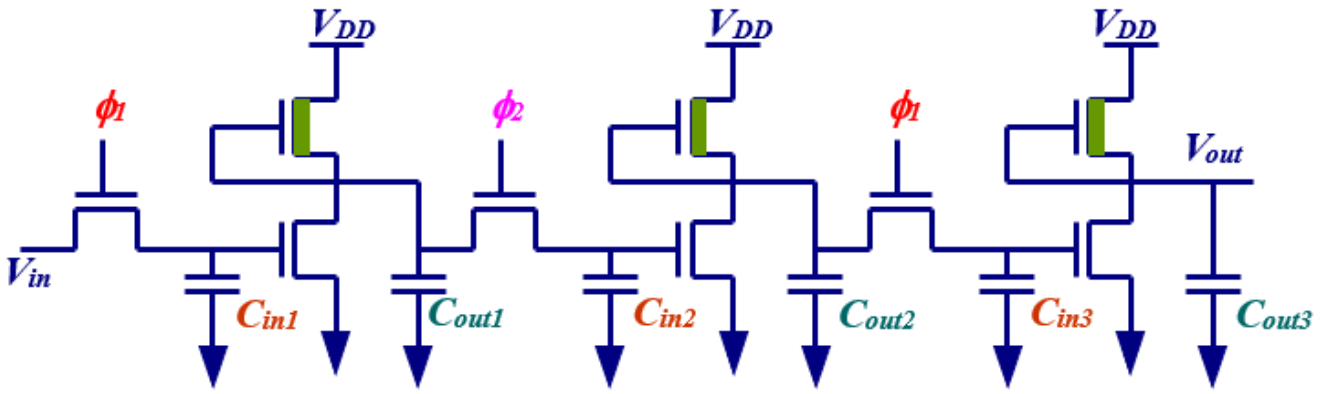


The operation of the shift register circuit is as follows.

- During the active phase of Φ1 the input voltage level Vin is transferred into the input capacitance Cin1.
- Thus, the valid output voltage level of the first stage is determined as the inverse of the current input during this cycle.
- When Φ 2 becomes active during the next phase, the output voltage level of the first stage is transferred into the second stage input capacitance Cin 2, and the valid output voltage level of the second stage is determined.
- During the active Φ 2 phase, the first-stage input capacitance continues to retain its previous level via charge storage. When Φ 1 becomes active again, the original data bit written into the register during the previous cycle is transferred into the third stage, and the first stage can now accept the next data bit

Dynamic Pass Transistor Circuits
Two-Phase Clock Dynamic Shift Register

- **Depletion-Load Dynamic Shift Register**



- The max clock frequency is determined by signal propagation delay through **one inverter** stage.
- One half-period of the clock signal must be long enough to allow C_{in} to charge up or down, and C_{out} to charge to the new value.
- The logic-high input value is one V_{T0} lower than V_{DD}.

Dynamic Pass Transistor Circuits
Two-Phase Clock Dynamic Shift Register

- The same operation principle used in the simple shift register circuit can easily be extended to synchronous complex logic.

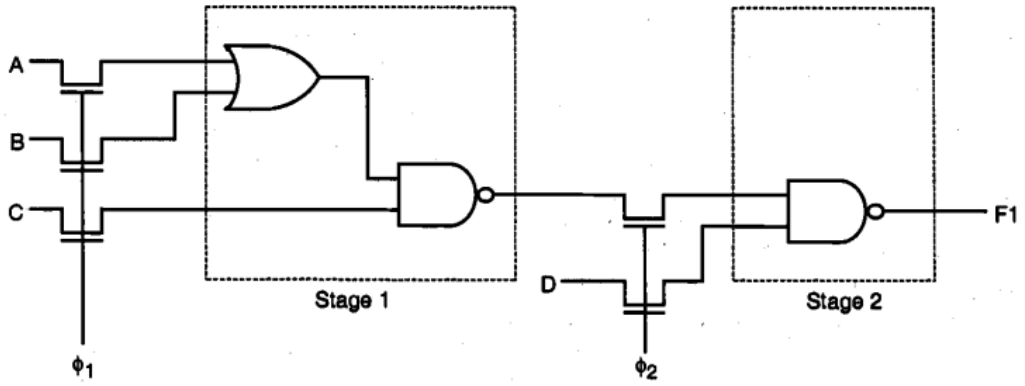


Figure 9.17. A two-stage synchronous complex logic circuit example.

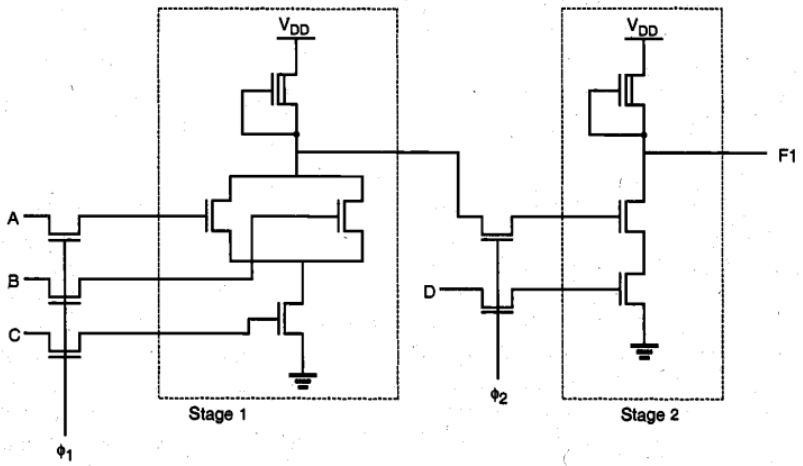
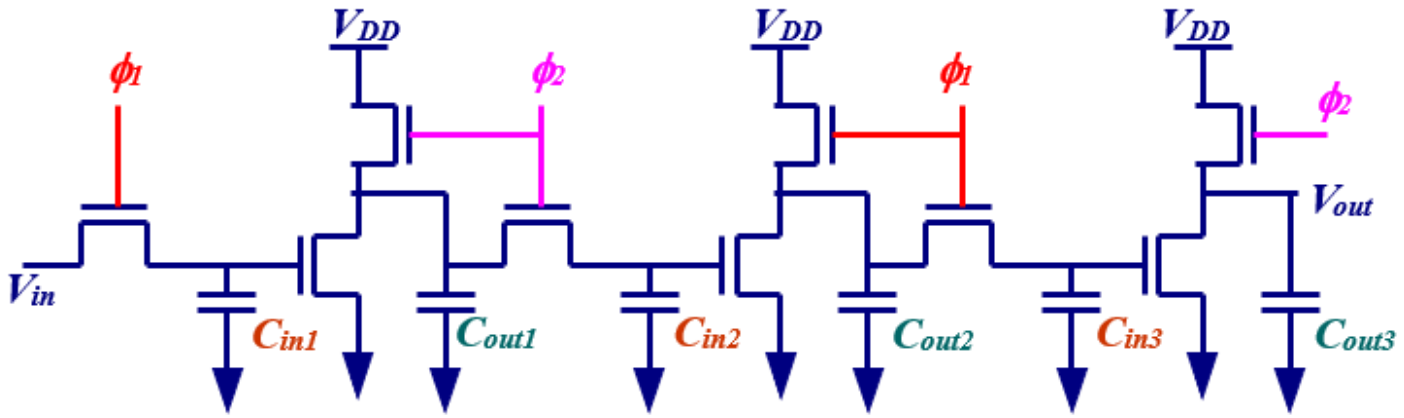
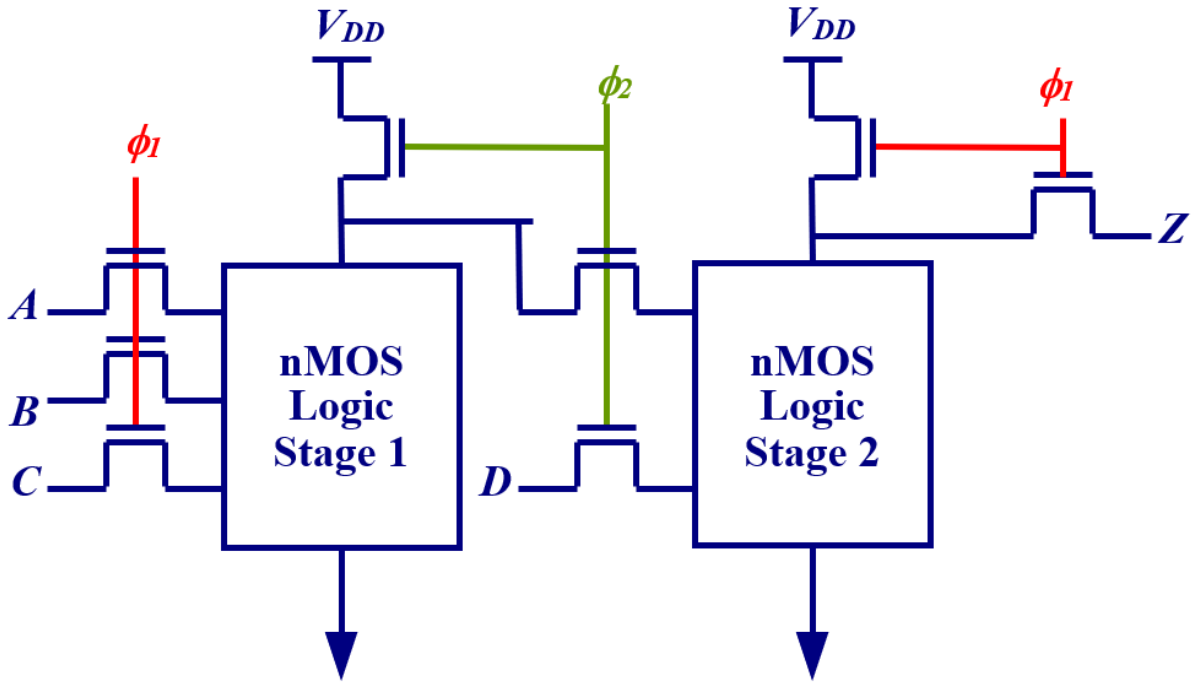


Figure 9.18. Depletion-load nMOS implementation of synchronous complex logic.

- **Enhancement-Load Dynamic Shift Register 1**
  - Instead of biasing load transistors with a constant gate voltage, a clock signal is applied to the gate of the load transistor ⇒ ***power dissipation and silicon area are reduced.***
  - The power supply current flows ***only when the load devices are activated by the clock signal***, the power consumption is **lower** than the depletion-load nMOS logic.



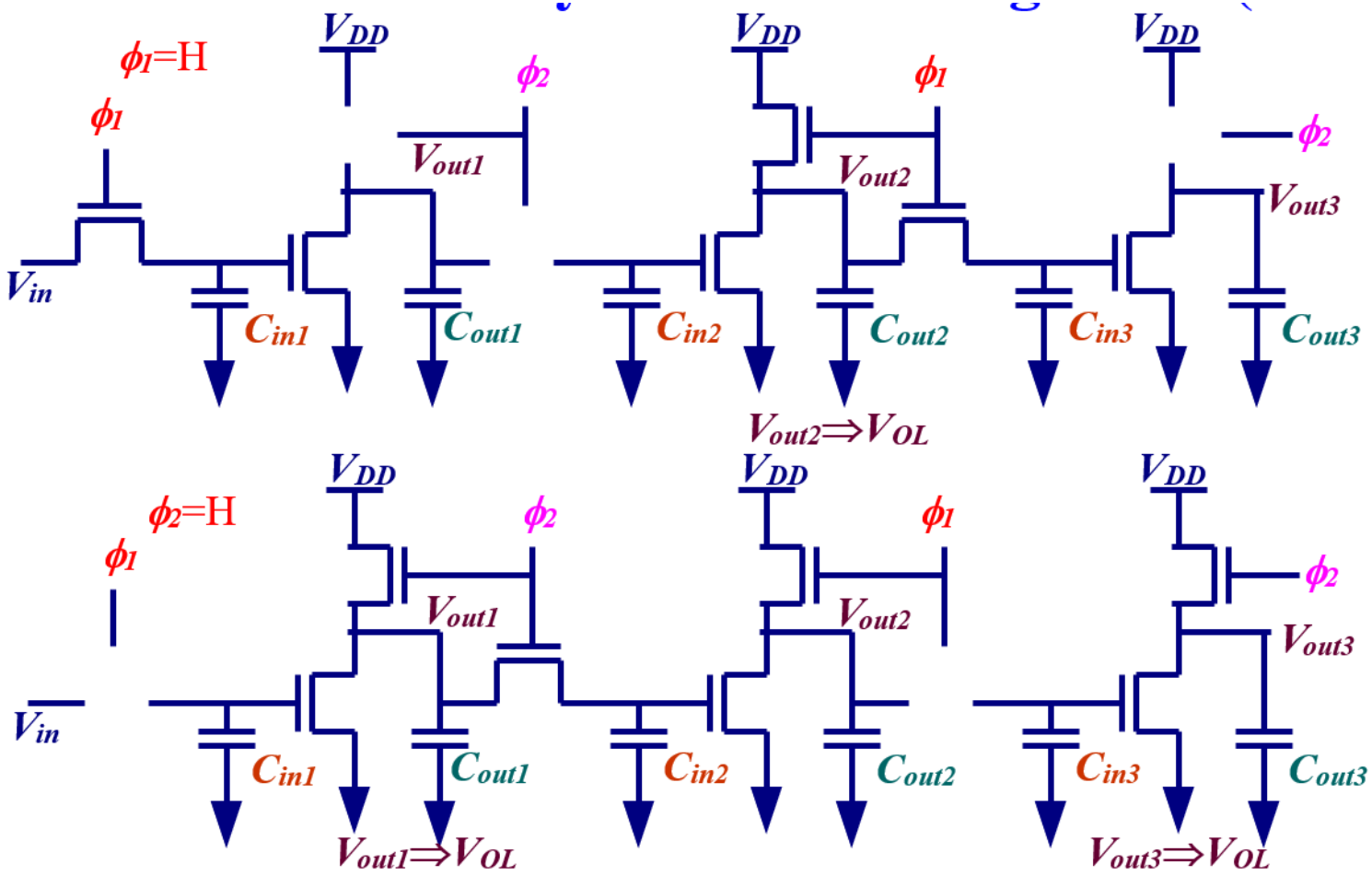
- **Enhancement-Load Dynamic Shift Register 1**



General Circuit Structure of Ratioed Synchronous Dynamic Circuit

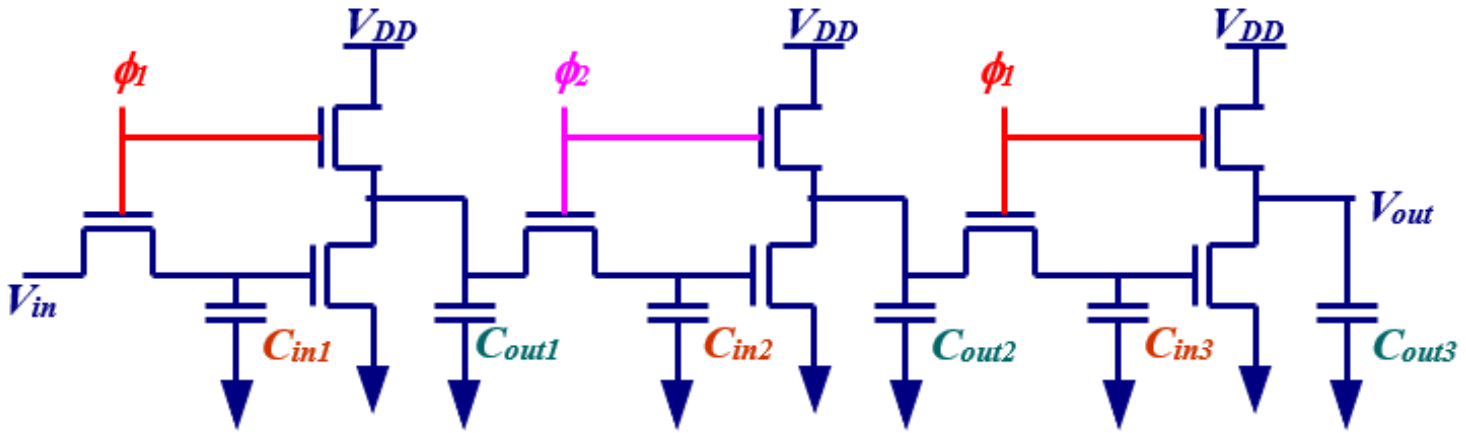
Dynamic Pass Transistor Circuits
Enhancement-Load Dynamic Shift Register

- **Enhancement-Load Dynamic Shift Register 1**

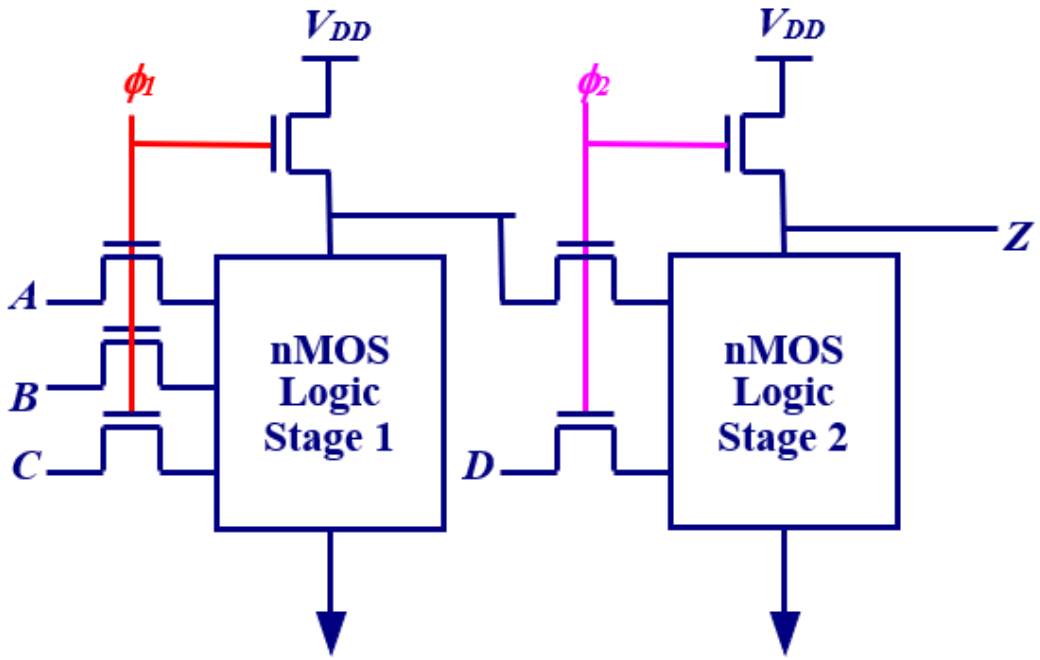


- $V_{OL} \rightarrow k_{driver}/k_{load} \Rightarrow$ ***Ratioed Dynamic Logic.***
- C_{out1}, C_{in2} & C_{out2}, C_{in3} interact $\Rightarrow$ ***Charge Sharing***

- **Enhancement-Load Dynamic Shift Register 2**
  - The ***input pass transistor*** and the ***load transistor*** are driven by the same clock phase.
  - The valid low-output voltage level V_{OL}=0V can be achieved regardless of the driver-to-load ratio, this circuit is a ***ratioless dynamic logic***.

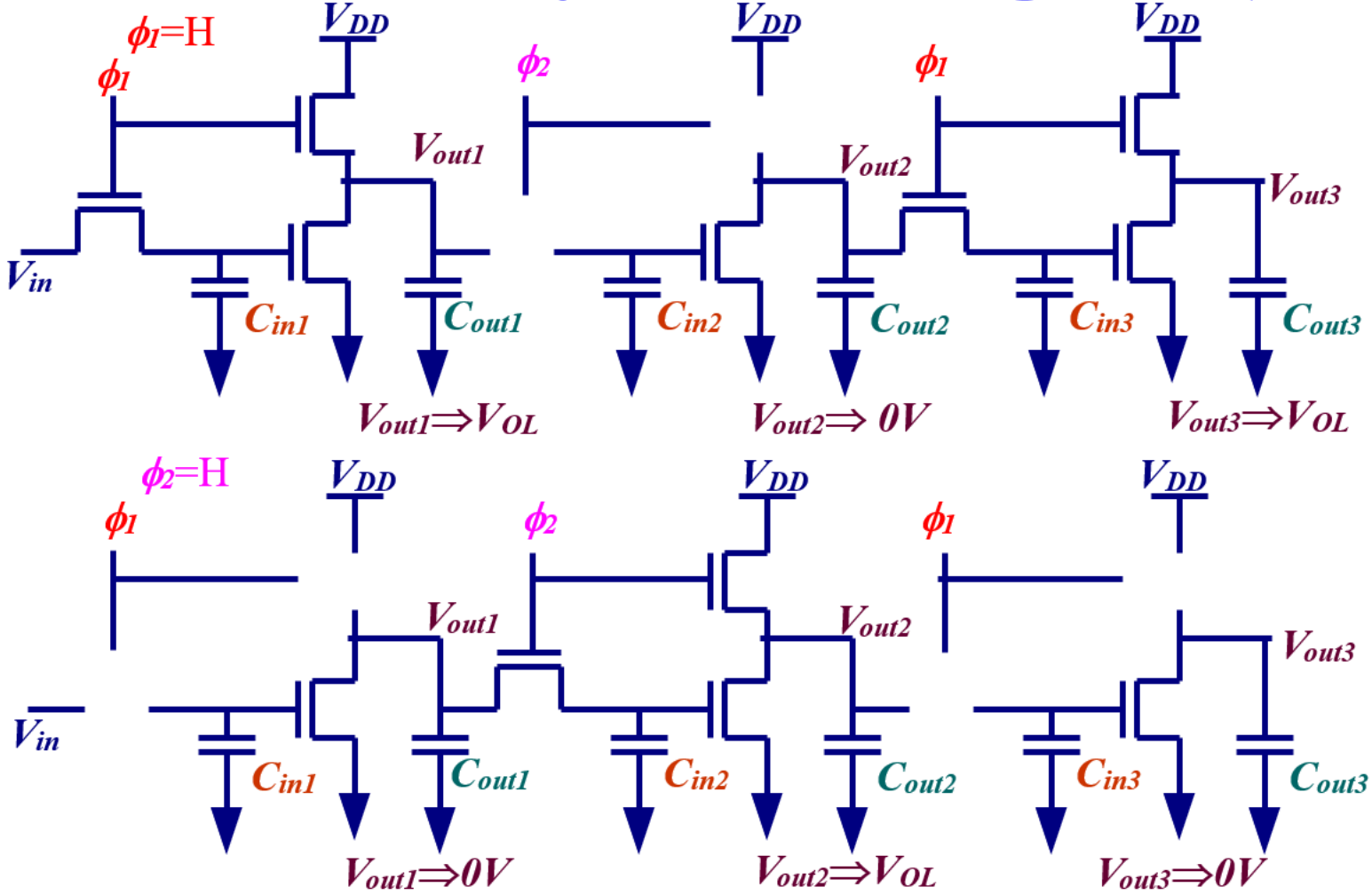


Enhancement-Load Dynamic Shift Register 2(Cont.)
General Structure



General Circuit Structure of Ratioless Synchronous Dynamic Circuit

Enhancement-Load Dynamic Shift Register 2 (Cont.)



- $V_{OL} \rightarrow 0V \Rightarrow$ ***Ratioless Dynamic Logic.***
- $C_{ini} << C_{outi-1}$ for i=2,3 $\Rightarrow$ ***Minimum Charge Sharing***

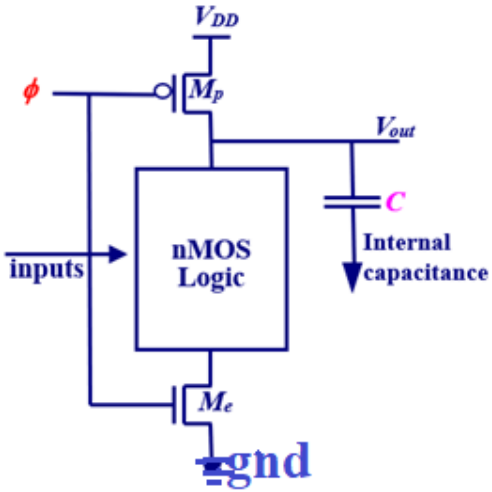
Dynamic CMOS Logic Circuits

- A dynamic logic gate uses clocking and charge storage properties of MOSFETs to implement logic operations.
- The clock provides a synchronized data flow which makes the technique useful in designing sequential networks.
- The characterizing feature of a dynamic logic gate is that the result of a calculation is valid only for a short period of time.
- While this makes the circuits more difficult to design and use they require fewer transistors and may be faster than static cascades.
- The circuit operation is based on **first Precharging** the output node capacitance and subsequently, **Evaluating** the output level according to the applied inputs
- Both of these operations are scheduled by a single clock signal, which drives one nMOS and one pMOS transistor in each dynamic stage.

Dynamic CMOS Logic Circuits

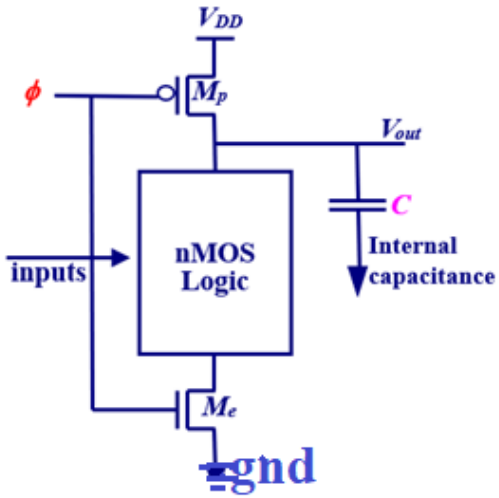
- the clock drives a complementary pair of transistors Me and Mp
- These control the operation of the circuit and provide synchronization.
- Logic is implemented using an nMOS logic between output node and ground.
- Clock signal defines two distinct modes of operation during every cycle.
- When Φ = 0
  - The circuit is in Precharge with Mp ON and Me OFF
  - Establishes a path between Vdd and output, and allowing C to charge to Vdd.
  - Mp is called – Precharge Transistor
  - Since the bottom of the nMOS logic array is not connected to Gnd,

(because Me is OFF) the inputs have no effect.



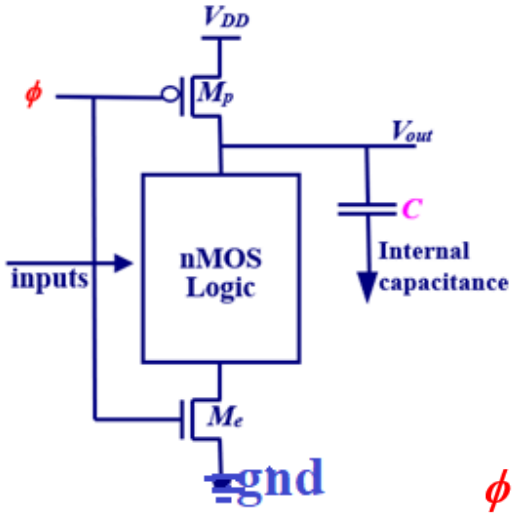
Dynamic CMOS Logic Circuits

- When Φ = 1
  - The circuit is into the evaluation mode with Mp - OFF and Me - ON
  - Establishes a path between Gnd and output
  - The inputs are valid and control the switching in the nMOS logic array;
  - Me is called – Evaluate Transistor
  - **If the nMOS logic block act like a closed switch between GND and output, the C discharge through the logic array and Me,**
  - **final result of the V_{out}= 0V**
  - **If the inputs cause the block to behave like an open switch (i.e., no connection between output and gnd) , the charge on C is held V_{DD} (which is charged during Precharge cycle)**

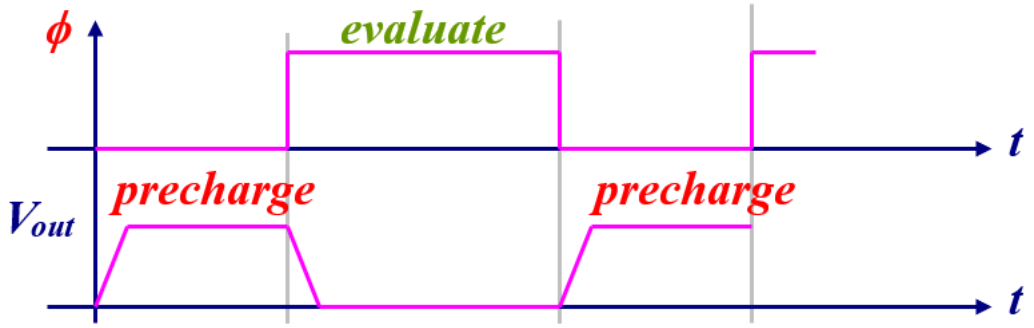


Dynamic CMOS Logic Circuits

- Dynamic CMOS Precharge-Evaluate Logic Reduced Transistor Count

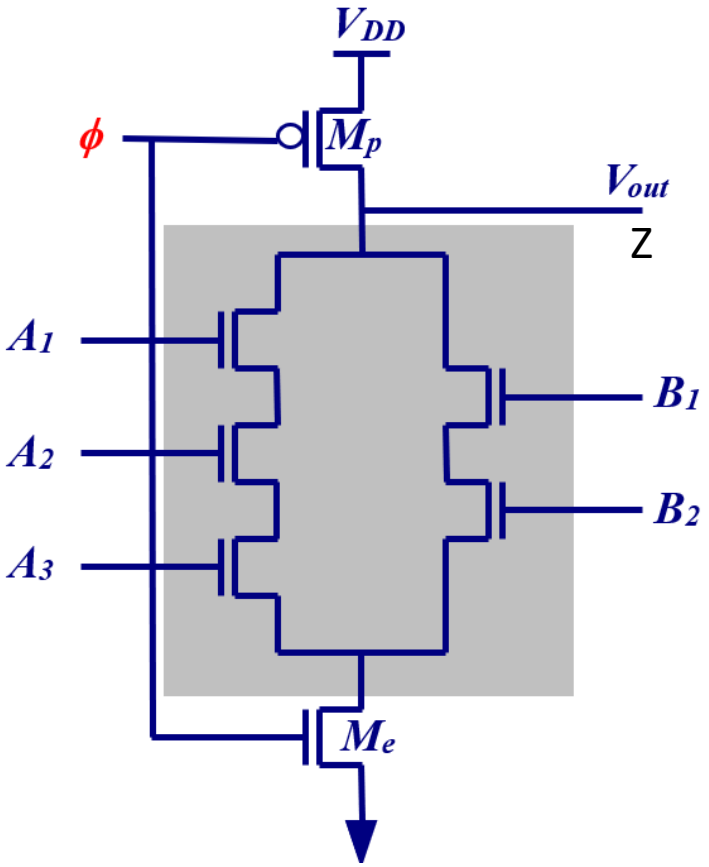


- ϕ=0 $\Rightarrow$ C ***precharges*** to V_{DD} (output is not available during precharge)
- ϕ =1 $\Rightarrow$ C ***selectively*** discharges to 0 (output is only available after discharge is complete)



Dynamic CMOS Logic Circuits

- Dynamic CMOS Precharge-Evaluate Logic an Example

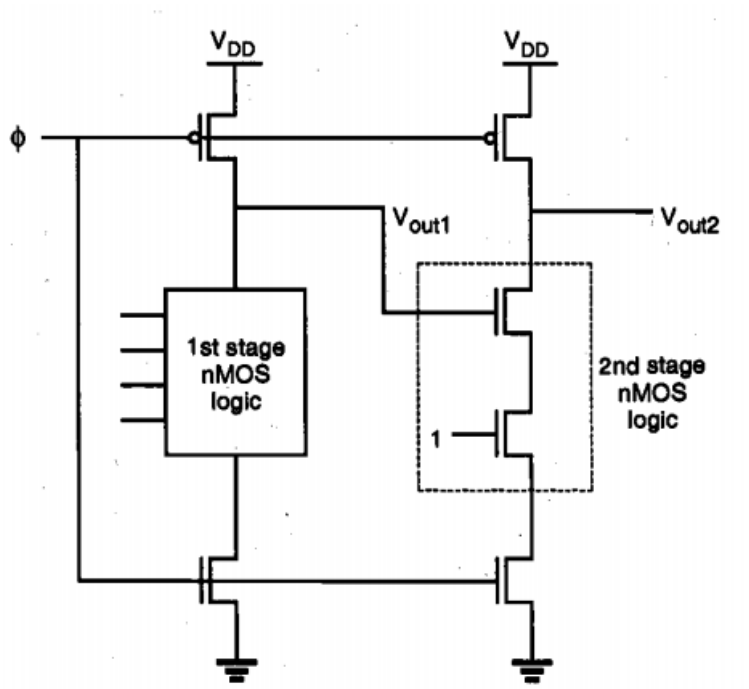


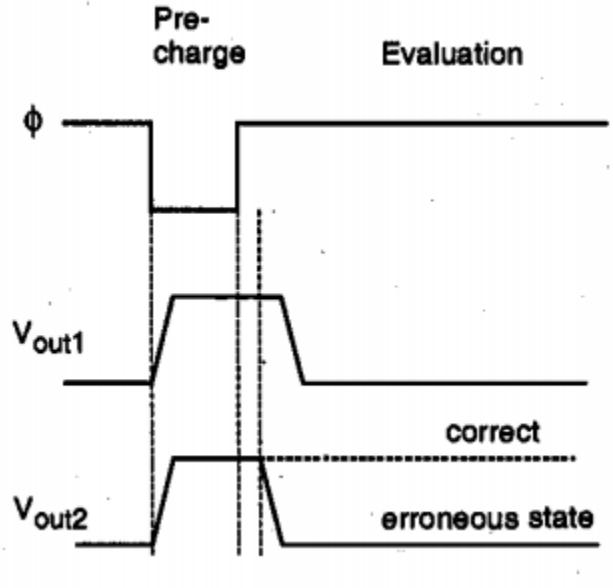
Z is high when $\phi=0$

$$Z=\overline{(A_1A_2A_3+B_1B_2)}$$

Dynamic CMOS Logic Circuits

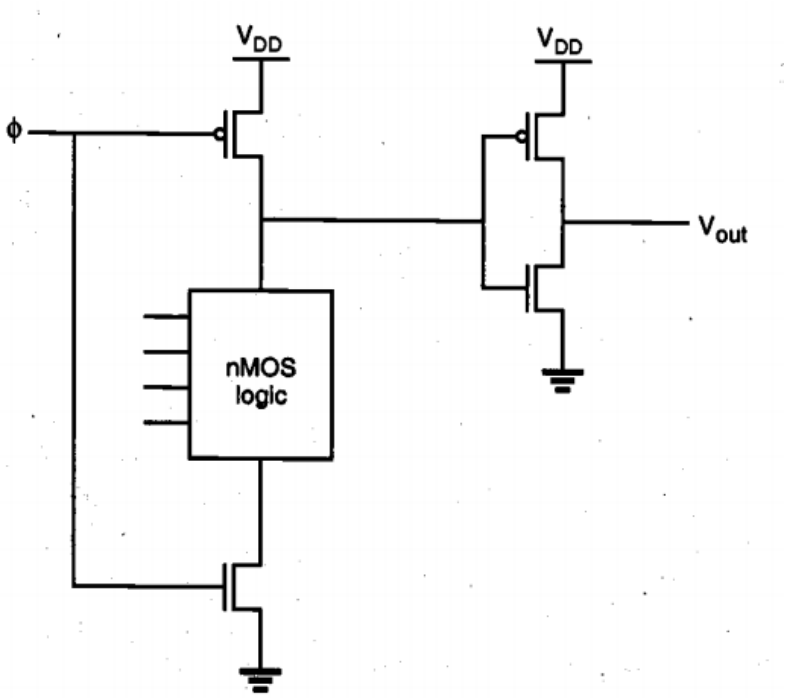
- Illustration of the cascading problem in dynamic CMOS logic





High Performance Dynamic CMOS Circuits
Domino CMOS Logic

- A dynamic CMOS logic stage, is cascaded with a static CMOS inverter stage.



Cascaded domino CMOS logic gates

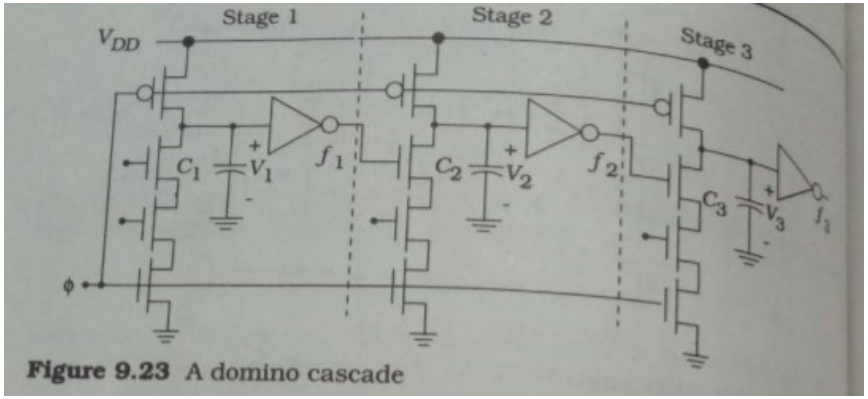
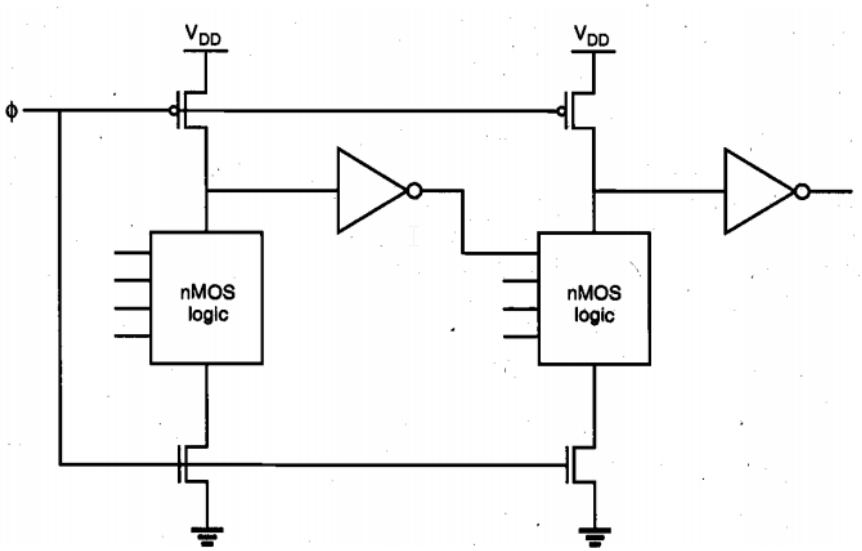
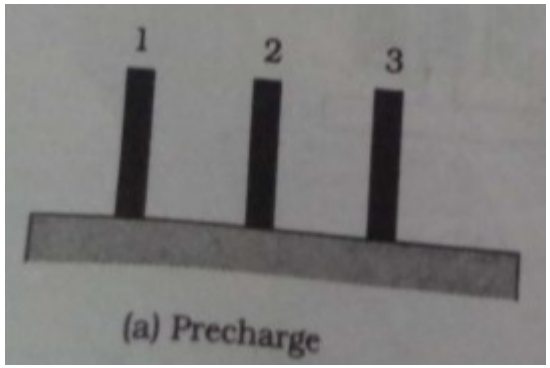
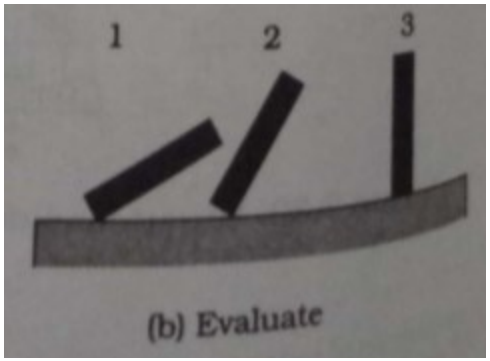


Figure 9.23 A domino cascade



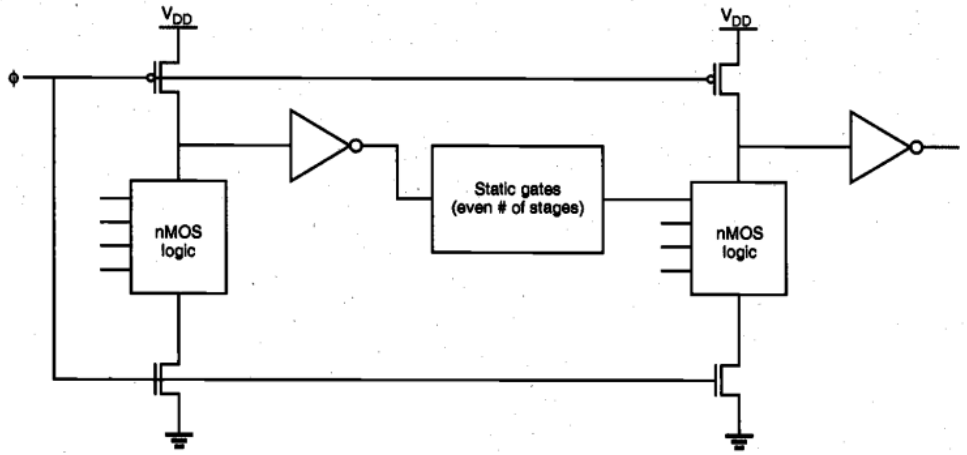




Domino CMOS Logic

The Limitations

The static CMOS and domino gates can be used together, **The limitation:** ***the number of inverting static logic stages in cascade must be even***, to let the inputs of next domino stage can have only 0 to 1 transitions during the evaluation.



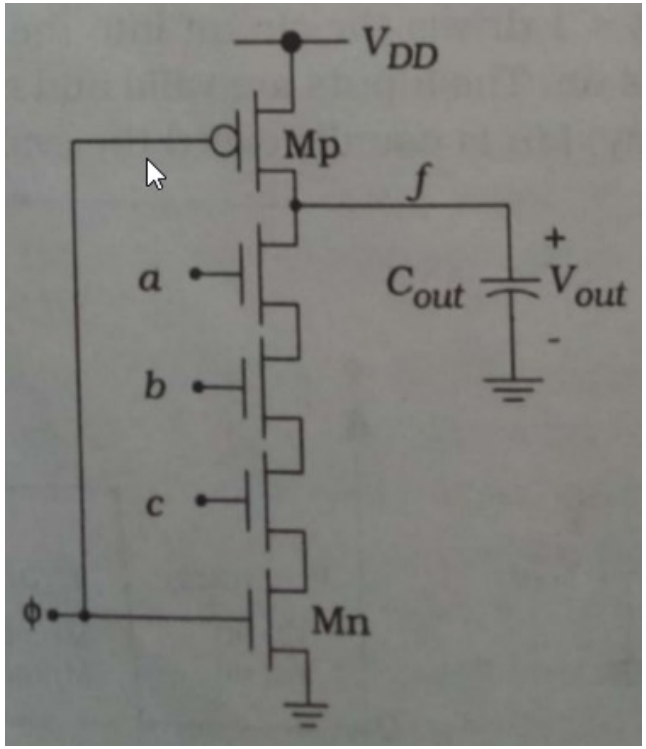
- Can implement only ***non-inverting logic***
- suffer from ***charge sharing*** during the evaluation which may cause erroneous outputs.

Dynamic CMOS Logic Circuits

- Charge sharing between the output capacitance Cout and an intermediate node capacitance during the evaluation cycle may reduce the output voltage level
- Example $f = \overline{a.b.c}$
- The origin of the charge sharing problem is the parasitic

Node capacitance between C1 and C2 between the FETs as

Shown in the fig



Dynamic CMOS Logic Circuits

- The origin of the charge sharing problem is the parasitic node capacitance between C1 and C2 between the FETs as shown in the fig.

➢ When Type equation here.Φ = 0, Mp on and

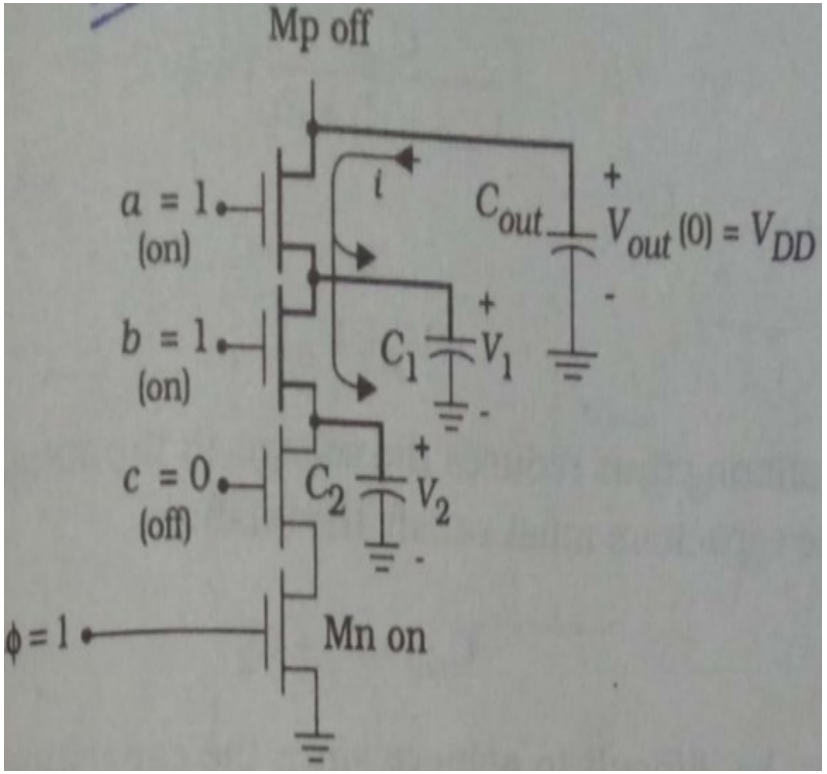
Mn off output node is precharge to Vdd.

➢ Φ = 1, Mp is off, isolating the output node from

Power supply Vdd.

➢ The initial voltage on Cout at the start of the

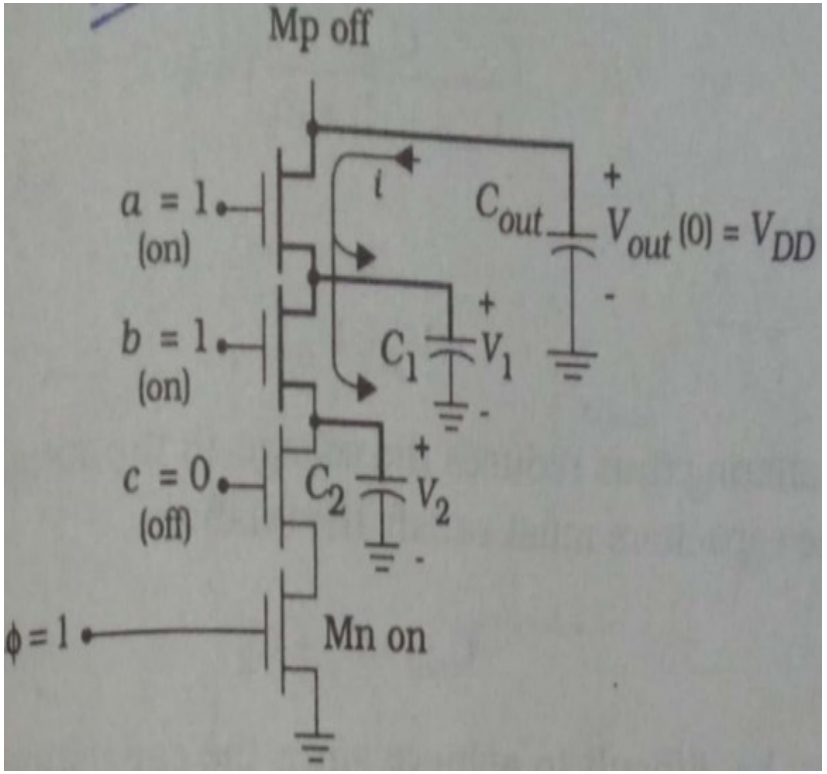
Evaluation is Vout = Vdd.



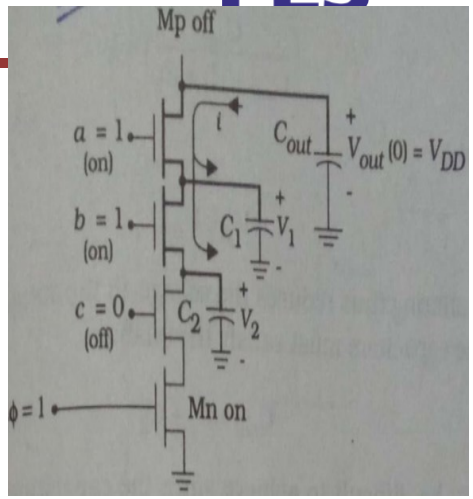
Dynamic CMOS Logic Circuits

- Assuming that the capacitor voltages V1 and V2 are both 0V at this time, the total charge on the circuit is $Q = C_{out}V_{DD}$
- The worst –case charge sharing condition for this circuit is when the input are at (a,b,c) =(1,1,0)
- With c = 0, there is no discharge path to Gnd
- So Vout should remain high.
- Since a and b input FETs are ON,

Cout is Electrically connected to C1 and C2 as Shown in fig.



Dynamic CMOS Logic Circuits



- i flows because Vout > V1 and V2
- Means charge transfer from Cout to C1 and C2
- Vout decreases while V1 and V2 increases.

The current flow ceases when the voltages are equal with a final value. $Vout = V1 = V2 = Vf$

The total charge Q = CV on the circuit is then distributed according to

$$Q = Cout\ Vout + C1\ V1 + C2V2$$

$$Q = (Cout\ + C1\ + C2)\ \text{Vf}$$

Applying the principle of conservation of charge, this must be equal to the initial charge in the system.

$$Q = (C_{out} + C_1 + C_2)V_f = C_{out}V_{DD}$$

$$V_f = \left(\frac{C_{out}}{C_{out} + C_1 + C_2}\right)V_{DD}$$

Dynamic CMOS Logic Circuits

- Applying the principle of conservation of charge, this must be equal to the initial charge in the system.

$$Q = (C_{out} + C_1 + C_2)V_f = C_{out}V_{DD}$$

$$V_f = \left(\frac{C_{out}}{C_{out} + C_1 + C_2}\right)V_{DD}$$

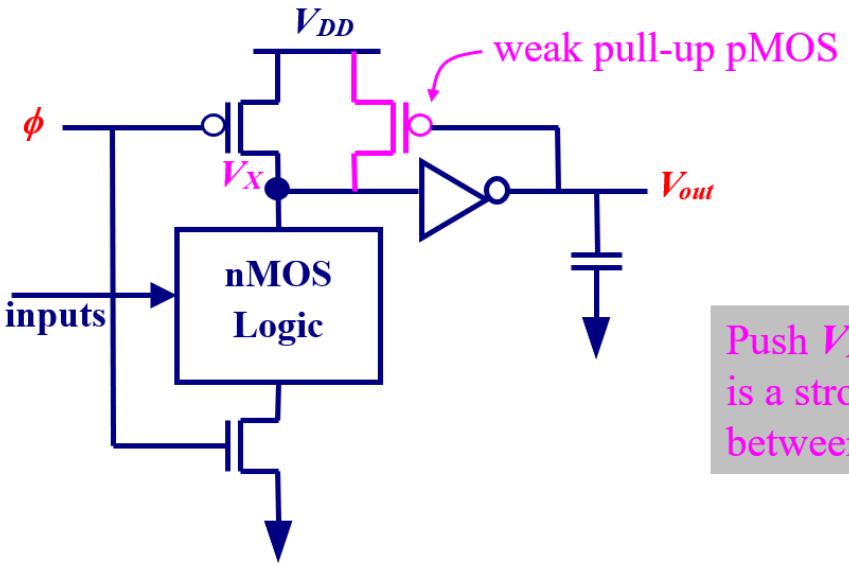
- If $\left(\frac{C_{out}}{C_{out} + C_1 + C_2}\right) < 1$

- Thus charge sharing reduces the voltage on the output node. To keep Vout high the Cout >> C1 + C2
- This is difficult to achieve since the capacitance values are determined by the layout dimensions.
- After charge sharing problem, the output node is still subject to charge leakage, which continues to drop the output voltage with time.

Domino CMOS Logic

Reduce Charge Sharing Degradation of V_X

- A weak pMOS pull-up device in a feedback loop can be used to prevent the loss of output voltage level due to charge sharing and charge leakage. (*Charge Keeper circuit*)
- A weak PMOS pull-up device with a small (W/L) ratio to the dynamic CMOS stage output is connected as Shown in the figure .
- Which essentially forces a high output level unless there is a strong pull-down path between the output and the ground

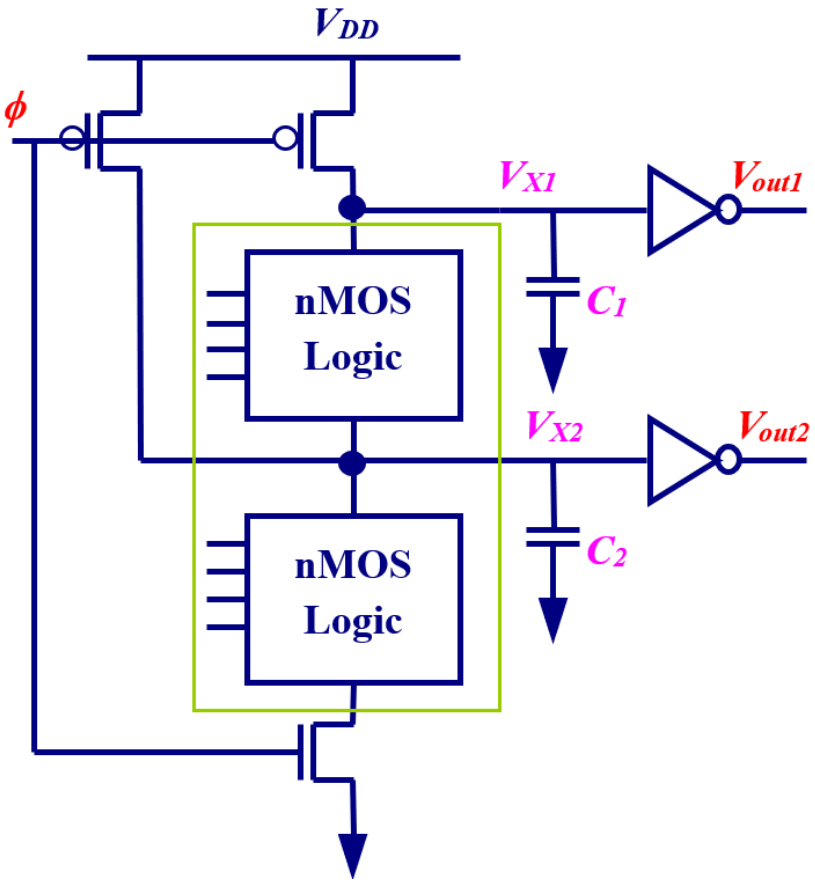


Push V_X to V_{DD} unless there is a strong pull-down path between V_{out} and ground

Domino CMOS Logic

Another solution for charge sharing problems

- Use ***separate pMOS*** transistors to precharge all intermediate nodes in nMOS pull-down tree which have a ***large parasitic capacitance***.
- Effectively eliminate all charge sharing problems during evaluation
- Allow implementation of **multiple-output** domino structures.
- Can cause additional delay since the nMOS tree need to drain a larger charge to pull down V_X



Domino CMOS Logic

Multiple Output Domino Logic (MODL)

- Realization of multiple functions using a single domino CMOS logic gate.
- The four functions to be realized are listed in the following.

$$C_1 = G_1 + P_1 C_0$$
$$C_2 = G_2 + P_2 G_1 + P_2 P_1 C_0$$
$$C_3 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 C_0$$
$$C_4 = G_4 + P_4 G_3 + P_4 P_3 G_2 + P_4 P_3 P_2 G_1 + P_4 P_3 P_2 P_1 C_0$$

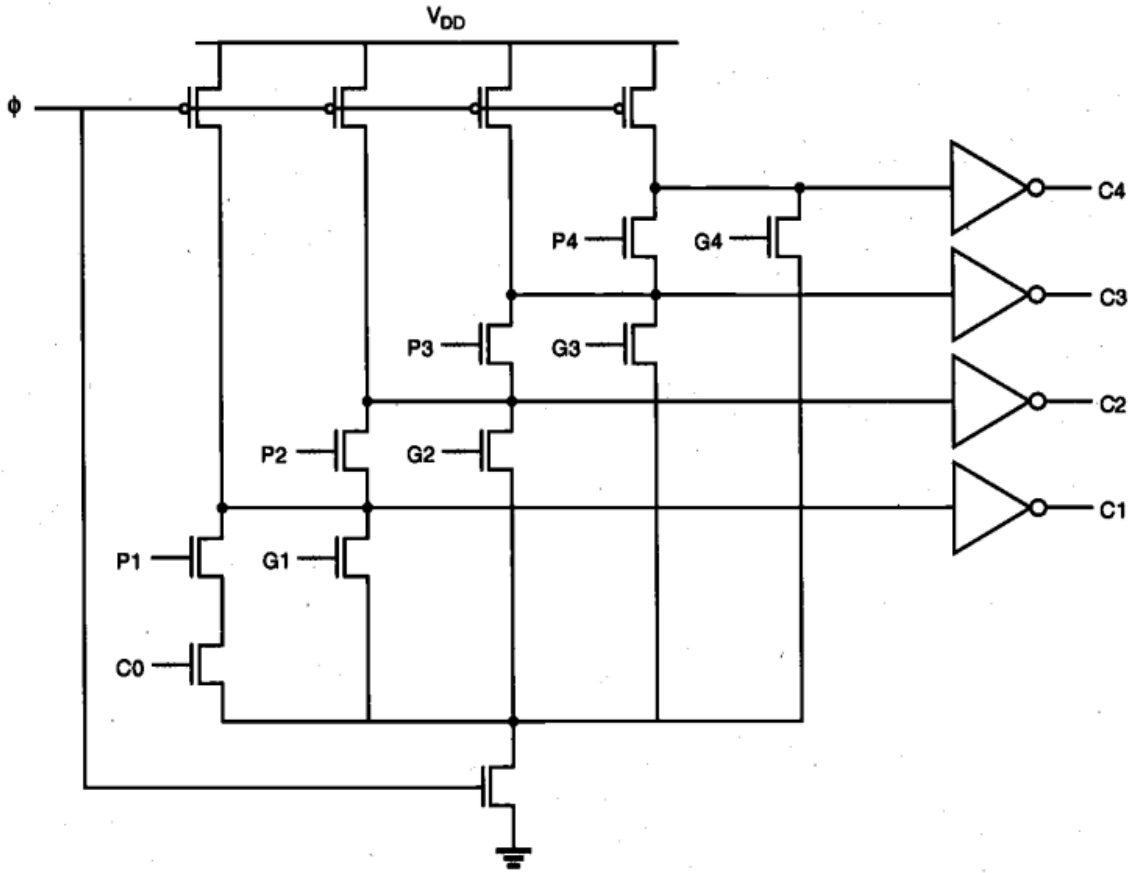
- the functions C1 through C4 are the four carry terms to be used in a four-stage carry-lookahead adder, where the variables Gi and Pi are defined as

  Gi = Ai * Bi

  Pi = Ai Bi

Domino CMOS Logic

Multiple Output Domino Logic (MODL)

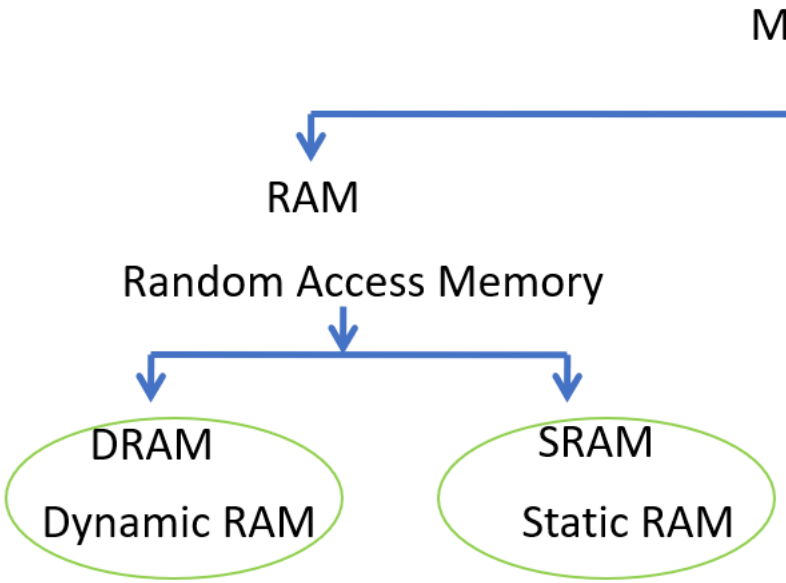


$$C_1 = G_1 + P_1C_0$$
$$C_2 = G_2 + P_2G_1 + P_2P_1C_0$$
$$C_3 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1C_0$$
$$C_4 = G_4 + P_4G_3 + P_4P_3G_2 + P_4P_3P_2G_1 + P_4P_3P_2P_1C_0$$

UNIT 5

Semiconductor Memories

Semiconductor Memories



ROM

Read Only Memory

- Mask (Fuse) ROM
- PROM
- EPROM
- EEPROM
- Flash
- Ferroelectric RAM (FRAM)

DRAM – Dynamic Random Access Memories

DRAM Cells

Concept of storage :

DRAM Cells store the information on the Capacitor.

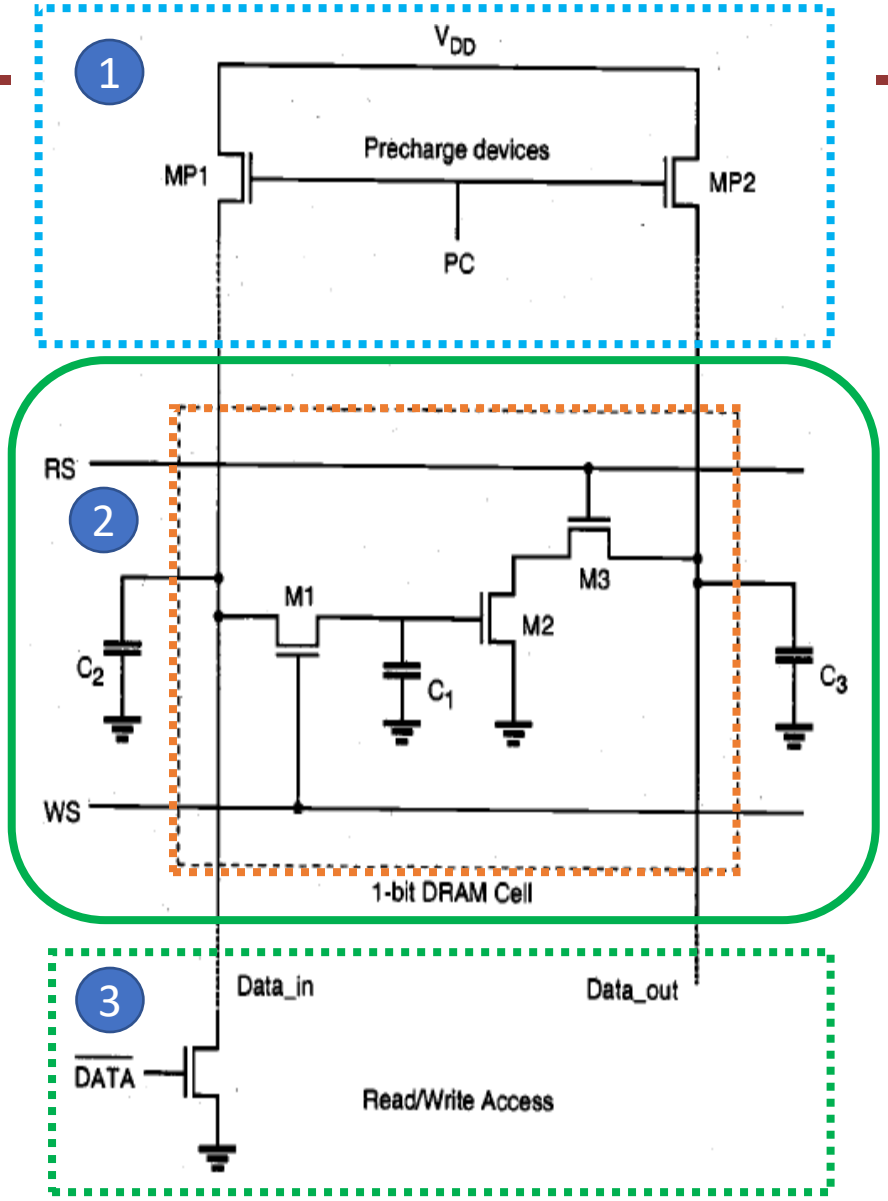
Advantage:

DRAM cells have high density since they are smaller.

Disadvantage:

- The “read’ operation is destructive in the case of DRAM.
- The cells have to be periodically refreshed due to its nature of dynamic (capacitive storage).

Operation of 3T DRAM Cell



Complete DRAM Circuitry

A typical 3T DRAM is shown

Consisting of -

(1) The column pull up precharge transistors

(3) The column read/write circuitry

The binary information is stored in the form of charge in the parasitic node capacitance C1.

The storage transistor M2 is turned on and off depending on the charge stored in C1.

The pass transistors M1 and M3 act as access switches for data read and write operations

Fig: 3T DRAM cell with pull up and read/write circuitry

Operation of 3T DRAM Cell

DRAM Bit lines, Word lines & Precharge event

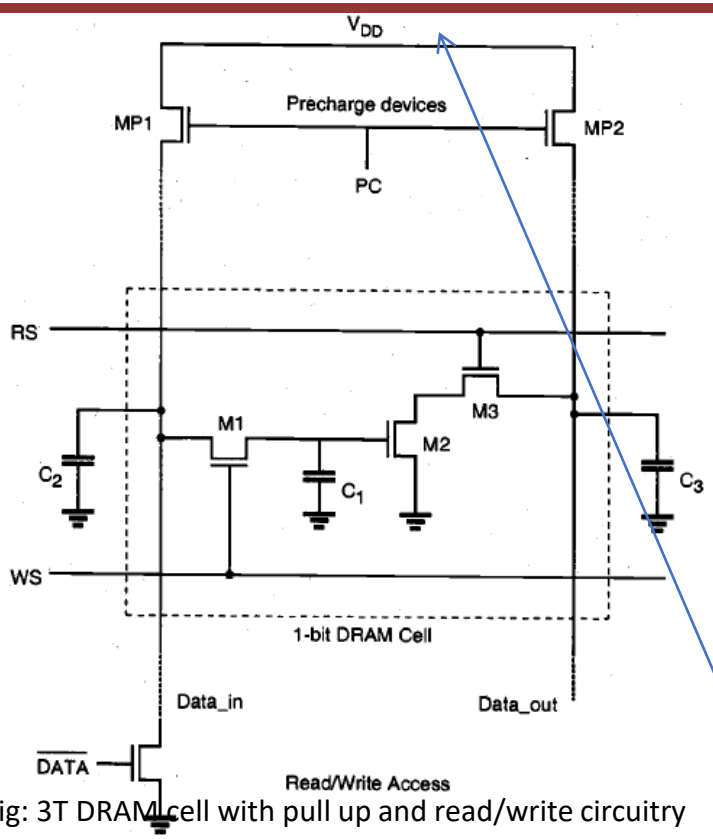


Fig: 3T DRAM cell with pull up and read/write circuitry

The cell has two separate bit lines for "data read" and "data write".

It also has two separate word lines to control the access transistors (M1 & M3).

The operation of the 3T DRAM and its peripheral circuitry is based on a two-phase non-overlapping clock scheme.

The precharge events are driven by Phi1 clock signal, whereas the "read" and "write" events are driven by phi2 clock signal.

Column capacitances C2 and C3 are being charged-up through MP1 and MP2 during the precharge cycle

- Every "data read" and "data write" operation is preceded by a precharge cycle which is initiated with the precharge signal PC going high.
- During the precharge cycle, the column pull-up transistors are activated and the corresponding column capacitances C2 and c3 are charged up to logic-high level.
- Note that the capacitors C2 and C3 are at least one order of magnitude larger than the internal storage capacitance C1.

Operation of 3T DRAM Cell

Write "1" Operation

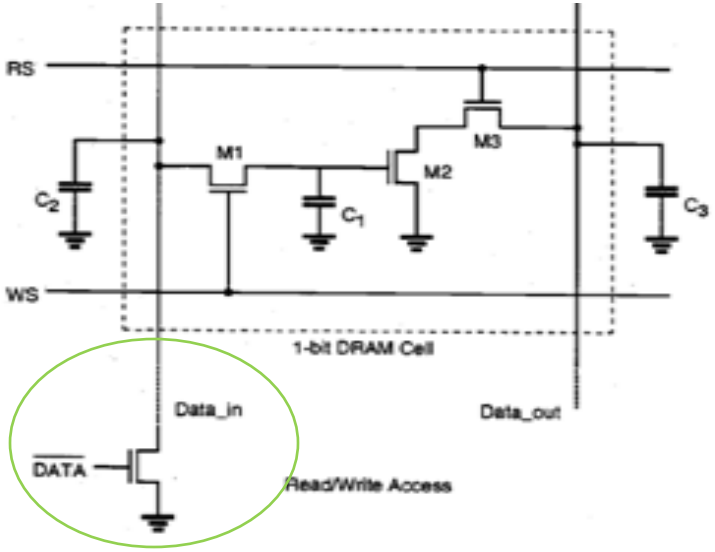


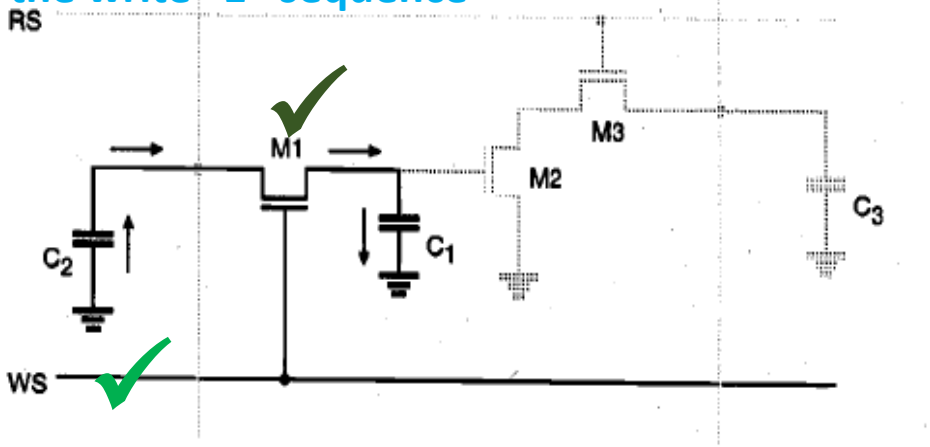
Fig: 3T DRAM cell with read/write circuitry

For write "1" operation -

Data' = Logic-level low, hence the transistor is OFF.

The voltage level on the column Data_in remains high.

Charge sharing between C2 and C1 during the write "1" sequence



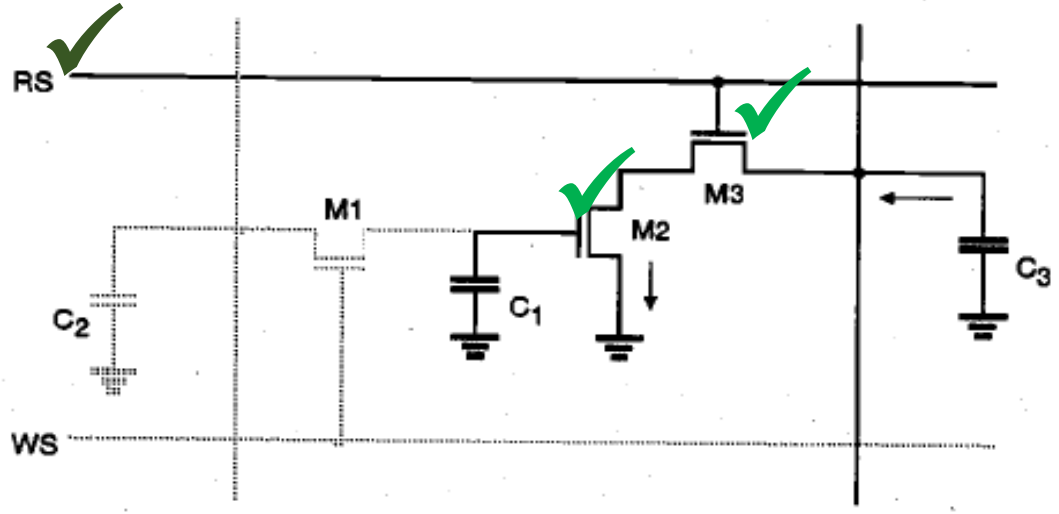
✔ The "write signal" WS is pulled high during the active phase of Phi2 Clock signal. As a result M1 is turned ON.

✔ With M1 conducting, the charge on C2 is shared with C1.

Note: *Since the capacitance C2 is very large compared to C1, the storage node capacitance C1 attains approximately the same logic level as the column capacitance C2 at the end of the charge-sharing process .*

Operation of 3T DRAM Cell

Read "1" Operation



For read "1" operation –

✓ The "read select" signal RS must be pulled high during the active phase of Phi2 clock signal, following a precharge cycle.

✓ The read access transistor M3 = ON, M2 = ON since C1 is charged to Logic 1 (storing bit 1)

• Since M2 and M3 is ON the capacitance C3 discharges to ground through M3 and M2

• The falling column voltage is interpreted by the "data read " / Data_out circuitry as a stored logic "1"

Operation of 3T DRAM Cell
Write "0" Operation

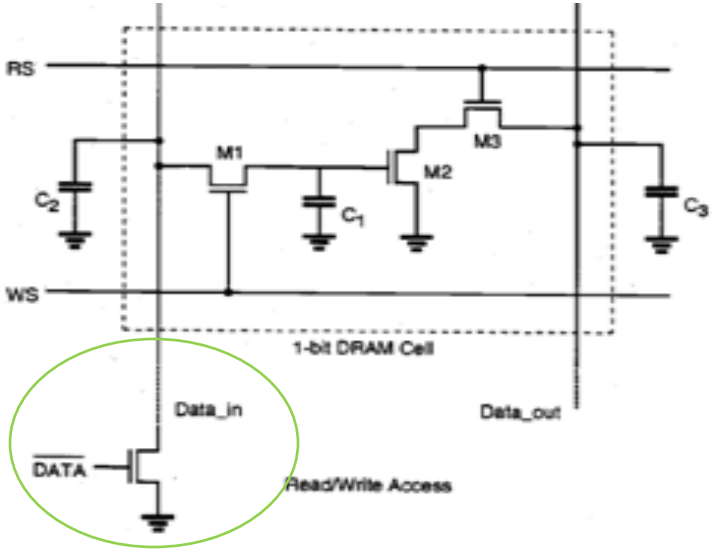


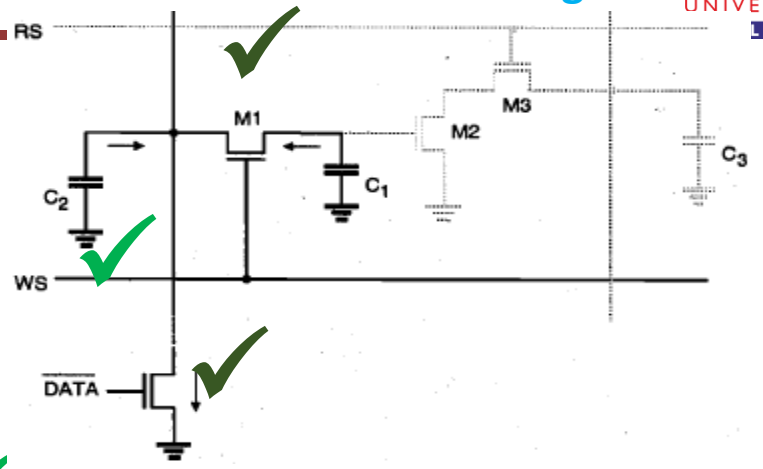
Fig: 3T DRAM cell with read/write circuitry

For write "0" operation -

Data' = Logic-level high, hence the transistor is ON.

The voltage level on the column Data_in is pulled to logic level 0 .

Both C1 and C2 are discharged via M1 and the data write transistor during the write "0"



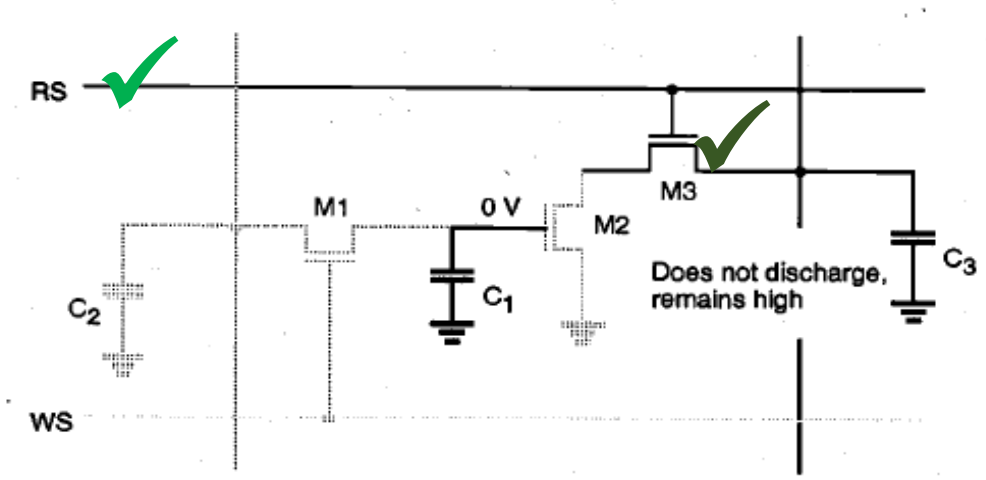
✔ The "write signal" WS is pulled high during the active phase of Phi2 Clock signal. As a result M1 is turned ON.

✔ With M1 conducting, the charge on C2, as well as C1 is pulled to logic level "0" through M1 and the data write transistor.

Thus, at the end of the write "0" sequence, the storage capacitance C1 contains a very low charge, and the transistor M2 is turned OFF since its gate voltage is approximately 0.

Operation of 3T DRAM Cell

Read "0" Operation



For read "0" operation –

✓ The "read select" signal RS must be pulled high during the active phase of Phi2 clock signal, following a precharge cycle.

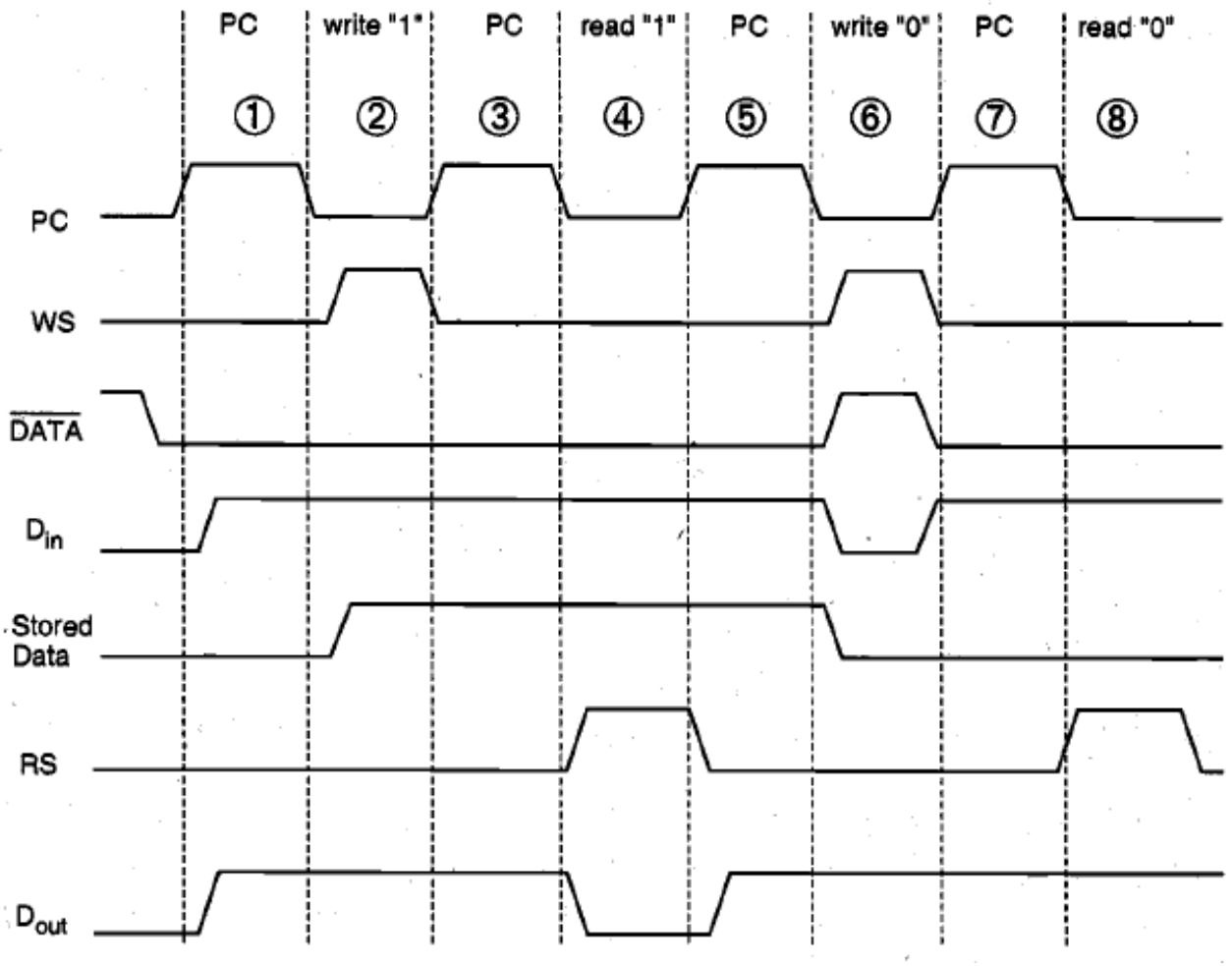
✓ The read access transistor M3 = ON, M2 = OFF since C1 is charged to Logic 0 (storing bit 0)

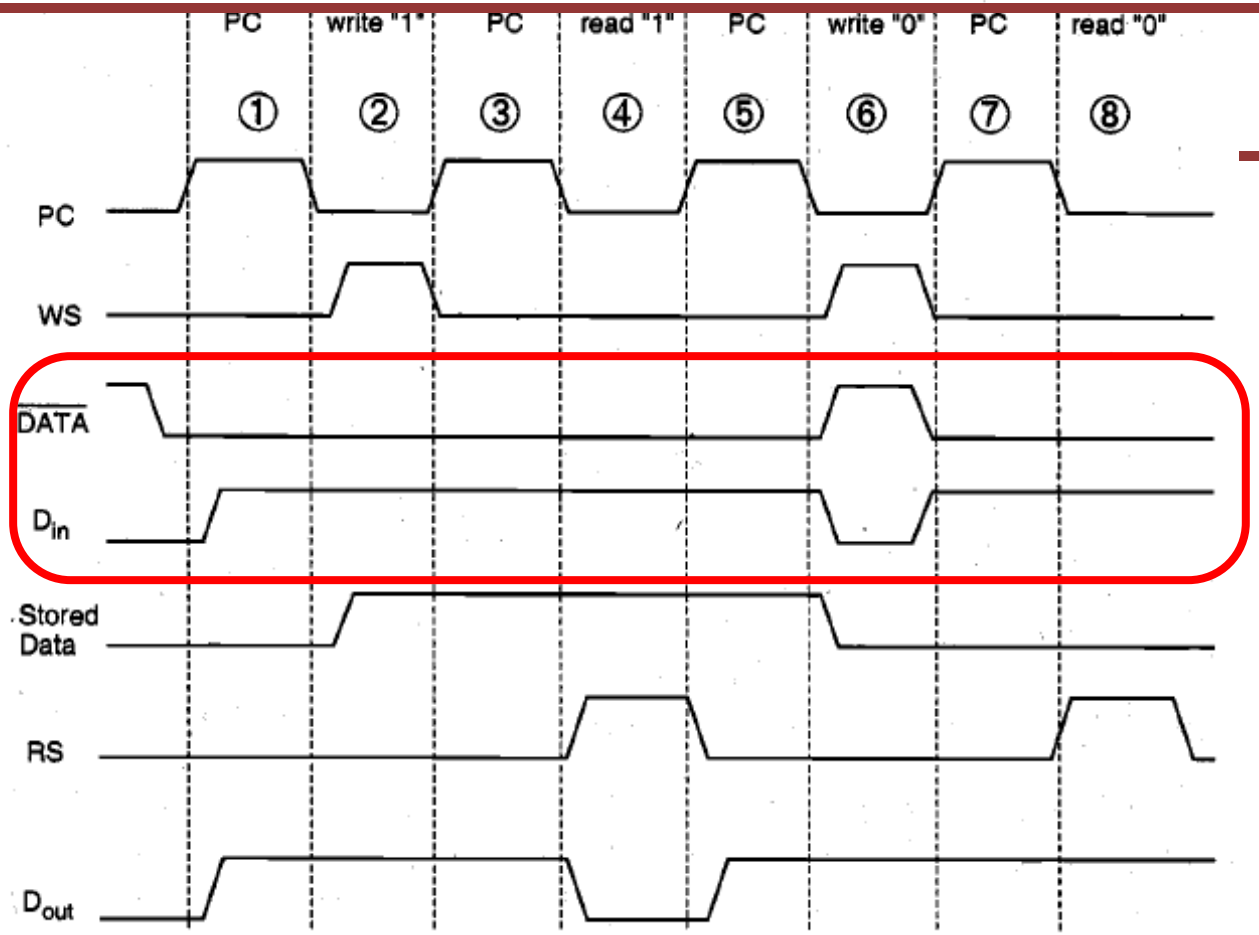
• Since M2 is OFF ,there is no conducting path between the column capacitor C2 and the ground. Hence C3 cannot discharge.

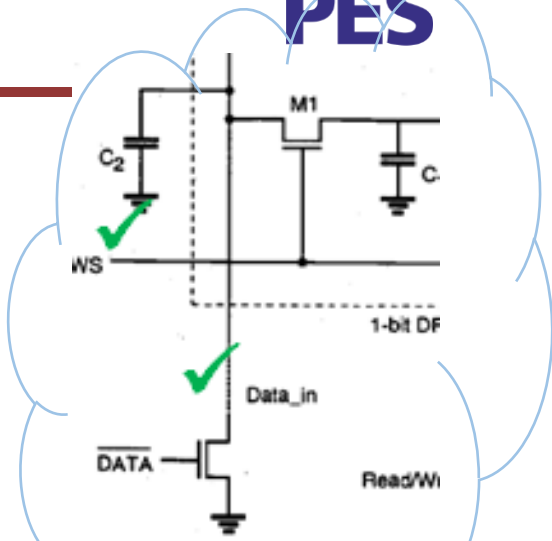
• The logic-high level on the column voltage is interpreted by the "data read " / Data_out circuitry as a stored logic "0"

Operation of 3T DRAM Cell

The typical voltage waveforms associated with the 3T DRAM cell during a sequence of four consecutive operations : write “1”, read “1”, write”0” and read”0”.



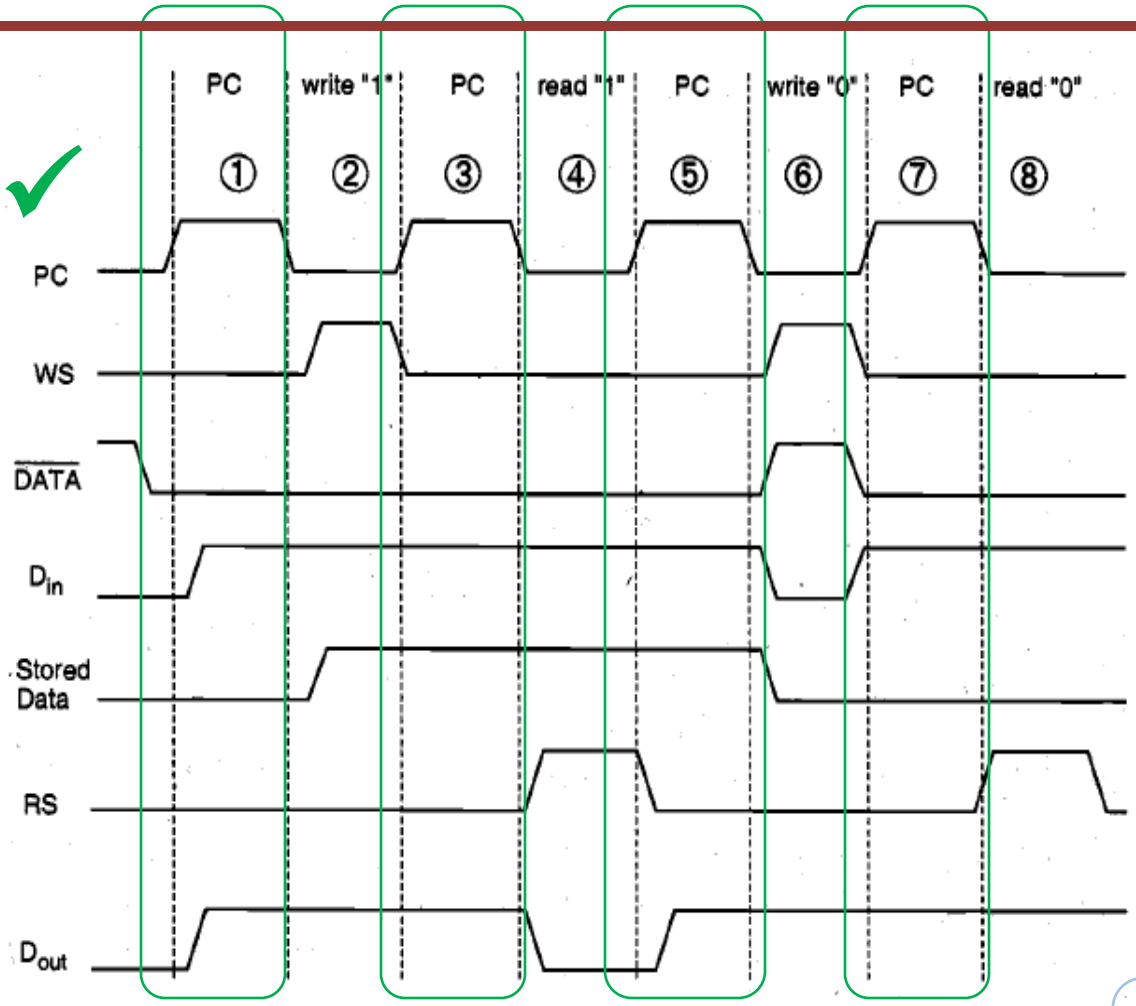


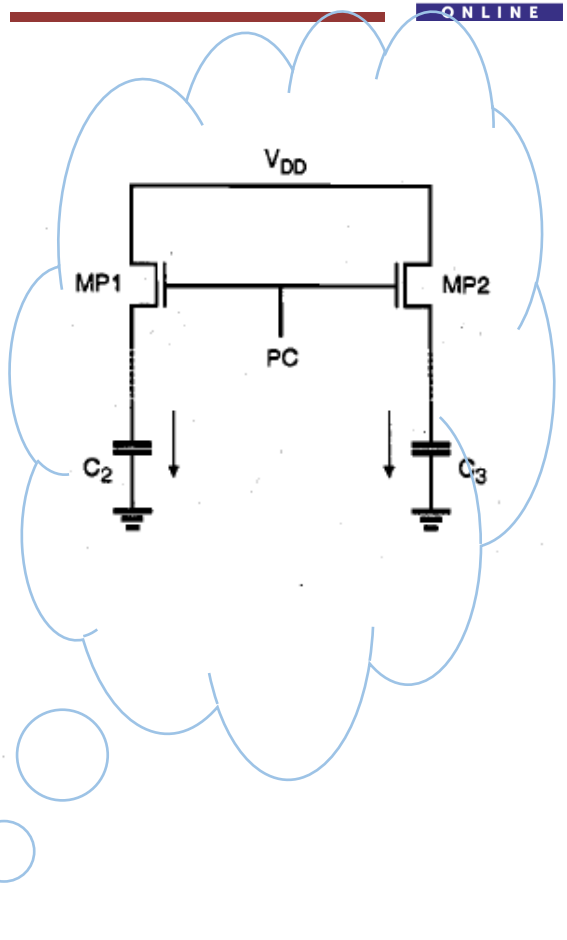


Note : The data' and the data in signals are always complementary

When data' = 0, the data write transistor is OFF and the data in/ Din = 1

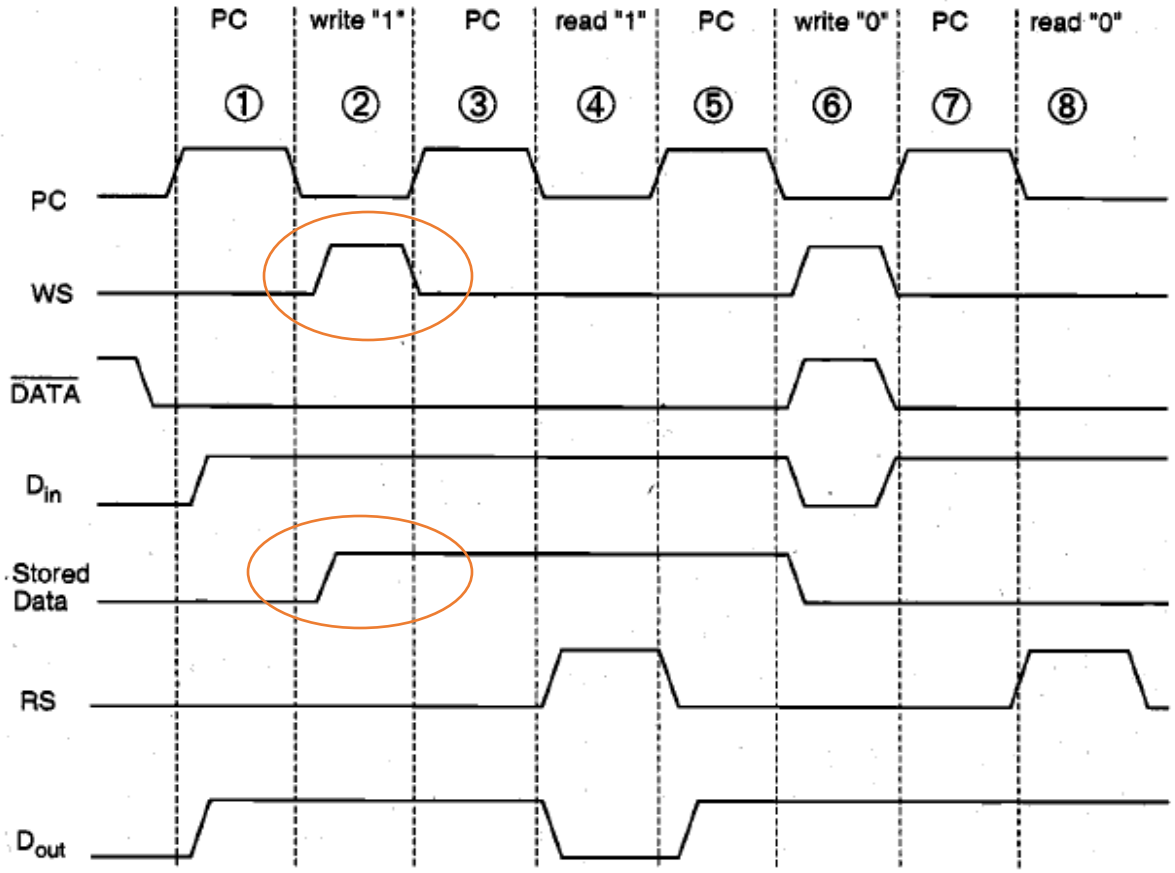
When data' = 1, the data write transistor is ON and the data in/ Din = 0





Every "data read" and "data write" operation is preceded by a precharge cycle which is initiated with the precharge signal PC going high.

Write “1” Operation



For write “1” operation -

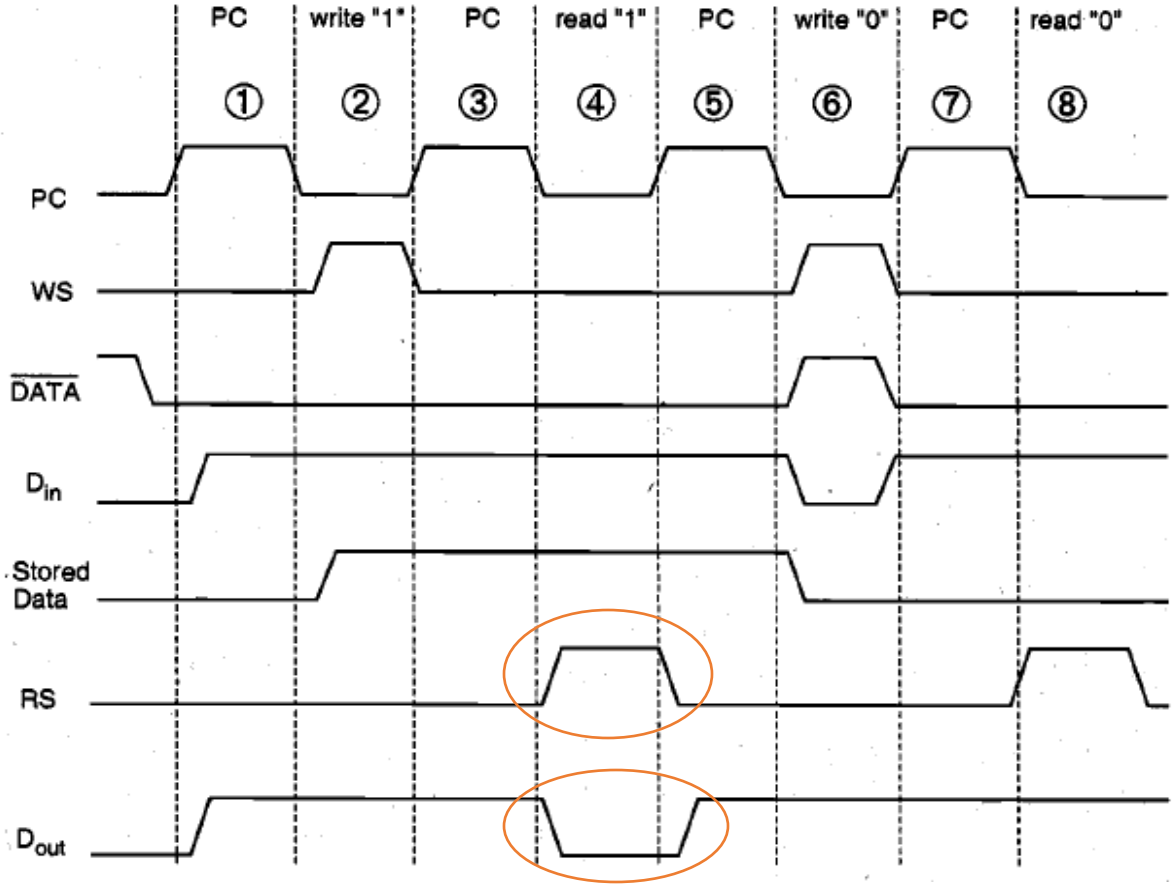
Data’ = Logic-level low, hence the transistor is OFF.

The voltage level on the column Data_in remains high.

✔ The “write signal” WS is pulled high during the active phase of Phi2 Clock signal. As a result M1 is turned ON.

✔ With M1 conducting, the charge on C2 is shared with C1.

Read "1" Operation



For read "1" operation –

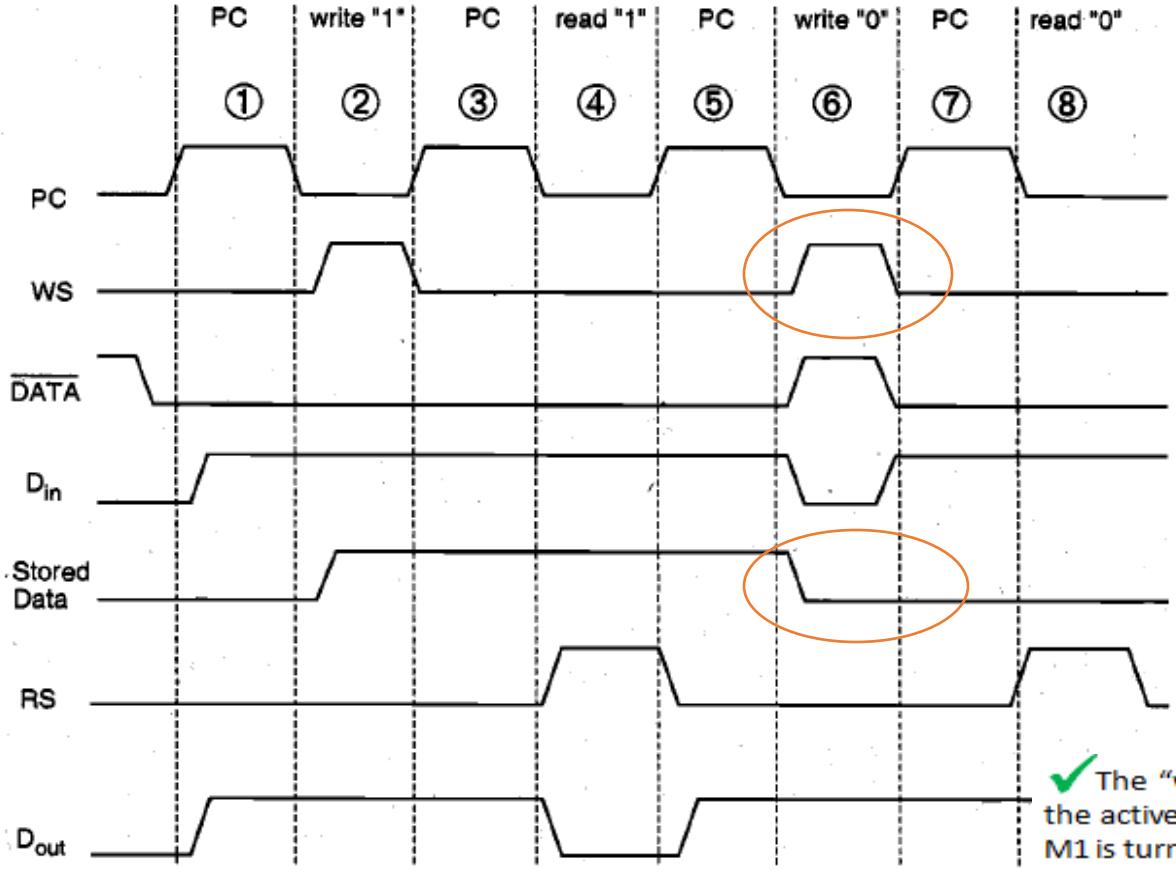
✔ The "read select" signal RS must be pulled high during the active phase of Phi2 clock signal, following a precharge cycle.

✔ The read access transistor M3 = ON, M2 = ON since C1 is charged to Logic 1 (storing bit 1)

- Since M2 and M3 is ON the capacitance C3 discharges to ground through M3 and M2

- The falling column voltage is interpreted by the "data read " / Data_out circuitry as a stored logic "1"

Write “0” Operation



For write “0” operation -

Data’ = Logic-level high, hence the transistor is ON.

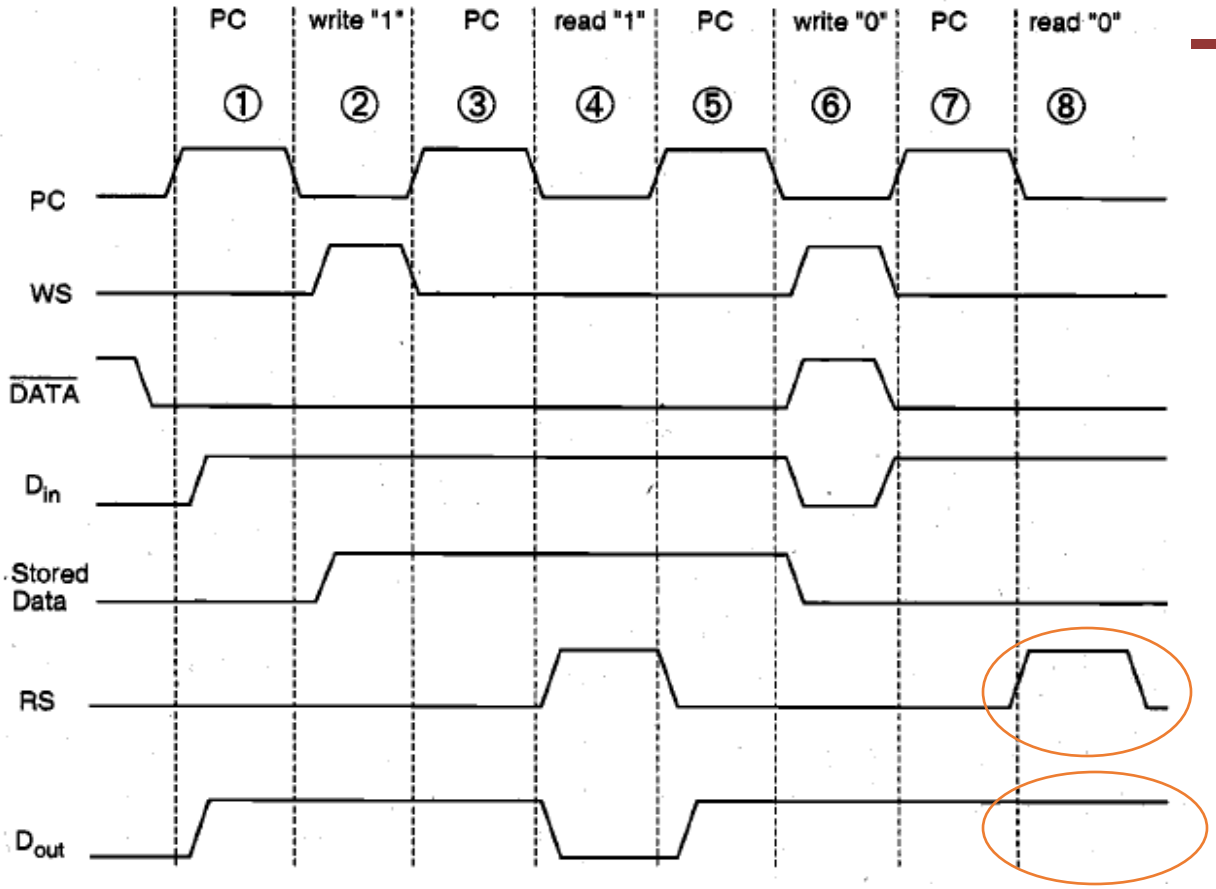
The voltage level on the column Data_in is pulled to logic level 0 .

✔ The “write signal” WS is pulled high during the active phase of Phi2 Clock signal. As a result M1 is turned ON.

✔ With M1 conducting, the charge on C2, as well as C1 is pulled to logic level “0” through M1 and the data write transistor.

Thus, at the end of the write “0” sequence, the storage capacitance C1 contains a very low charge, and the transistor M2 is turned OFF since its gate voltage is approximately 0.

Read "0" Operation



For read "0" operation –

✔ The "read select" signal RS must be pulled high during the active phase of Phi2 clock signal, following a precharge cycle.

✔ The read access transistor M3 = ON, M2 = OFF since C1 is charged to Logic 0 (storing bit 0)

- Since M2 is OFF ,there is no conducting path between the column capacitor C2 and the ground. Hence C3 cannot discharge.

- The logic-high level on the column voltage is interpreted by the "data read " / Data_out circuitry as a stored logic "0"

Refresh Operation in DRAM cell

Disadvantage of DRAM cell: (requirement of a Refresh Operation)

- The charge stored in C1 cannot be held indefinitely, the drain junction leakage current of the write access transistor M1 is the main reason for the gradual depletion of the stored charge on C1.

- In order to refresh the data stored in the DRAM cells before they are altered due to leakage, the data must be periodically read, inverted (since the data output level reflects the inverse of the stored data), and then written back into the same cell location.

- The refresh operation is performed for all the storage cells in the DRAM array every 2 to 4ms.

Operation of 1T DRAM Cell

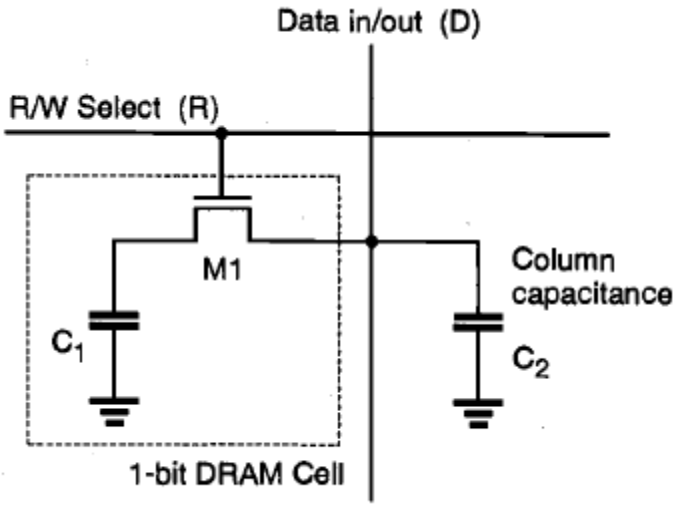


Fig : Typical 1T DRAM cell with its access lines

- Currently, 1T cell is most widely used storage structure in the DRAM industry

- It has a single access transistor M1 and a storage capacitor C1

Working of 1T DRAM cell

The bit line is precharged to ½ VDD initially

To Write "1" :
Date in/out = Logic 1
R/W select = Logic high, M1 is ON
C1 (storage Capacitor) = Logic 1
To Write "0" :
Date in/out = Logic 0
R/W select = Logic high, M1 is ON
C1 (storage Capacitor) = Logic 0
To Read "0" or "1" :
C2 is precharged to ½ VDD
R/W select = Logic high, M1 is ON
The charge sharing takes place between C1 and C2
If C1 had Logic 0, there is a fall in C2 which is detected by the sense amplifier as Logic 0 being stored in the DRAM Cell.
If C1 had Logic 1, there is a rise in C2 which is detected by the sense amplifier as Logic 1 being stored in the DRAM Cell.

SRAM – Static Random Access Memories

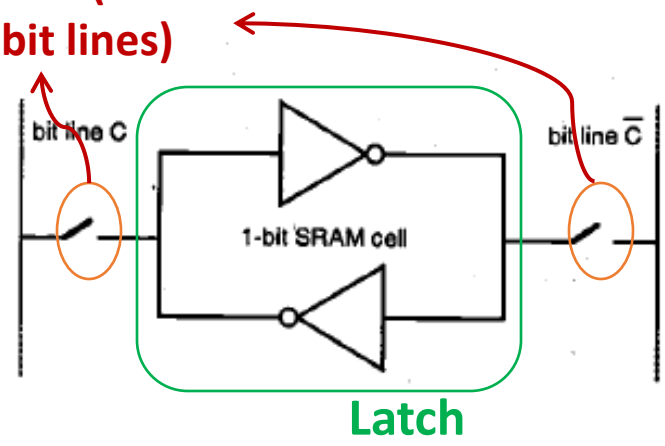


Fig: Symbolic representation of the two-inverter latch circuit with access switches

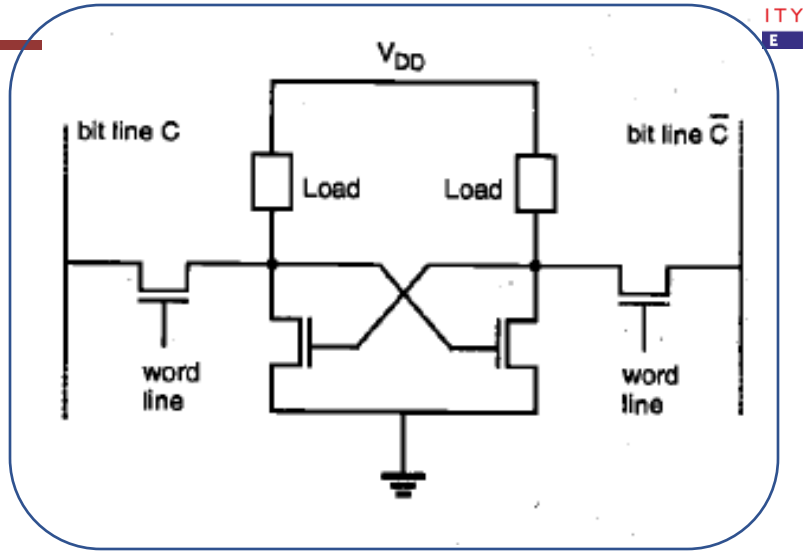


Fig: Generic circuit topology of the MOS static RAM cell

- The generic structure of the MOS static RAM cell, consisting of two cross-coupled inverters and two access transistors is shown above.

- The load devices may be Polysilicon resistors, depletion – type nMOS transistors, or pMOS transistors, depending on the type of the memory cell.

- The pass gates acting as data access switches are enhancement type nMOS transistors.

SRAM – Static Random Access Memories

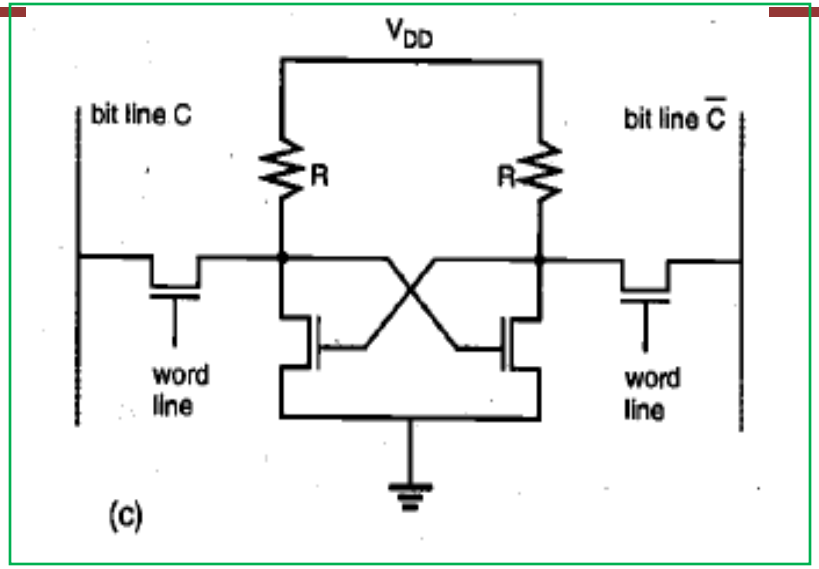


Fig : Resistive Load SRAM Cell

- The use of resistive – load inverters with undoped polysilicon resistors in the latch structure typically results in a significantly more compact cell size.

- The cell will have only 4 transistors. If multiple polysilicon layers are available, one layer can be used for the gates of the enhancement type nMOS transistors, while another can be used for the load resistors and interconnects.

Design Constraint :

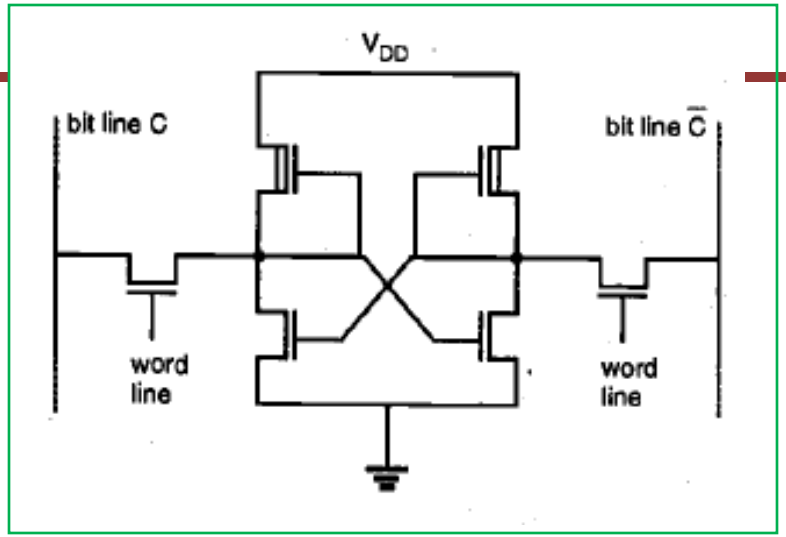
- The resistance value should be low to attain acceptable noise margins and output pull-up times.

- The resistance value should be a higher value in order to reduce the amount of standby current being drawn by each memory cell.

Trade –off :

Thus, there is a trade-off between the high resistance required for low power and the requirement to provide wider noise margin and high speed.

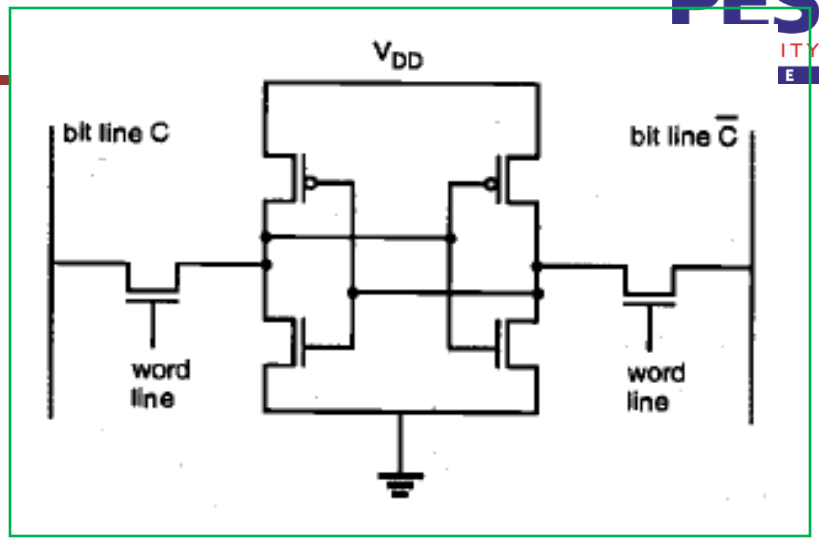
SRAM – Static Random Access Memories



Depletion load nMOS SRAM cell

• The 6T depletion – load nMOS SRAM can be easily implemented with one polysilicon and one metal layer, and the cell size tends to be relatively small, especially with the use of buried metal-diffusion contacts.

• The static power consumption of the depletion –load SRAM cell, however, makes it an unsuitable candidate for high density SRAM arrays.



Full CMOS SRAM cell

• The Full CMOS SRAM cells are currently most popular due to the lowest static power dissipation among the various circuit configurations and compatibility with current logic process.

• The CMOS cell offers superior noise margins and switching speed as well.

Full CMOS SRAM cell

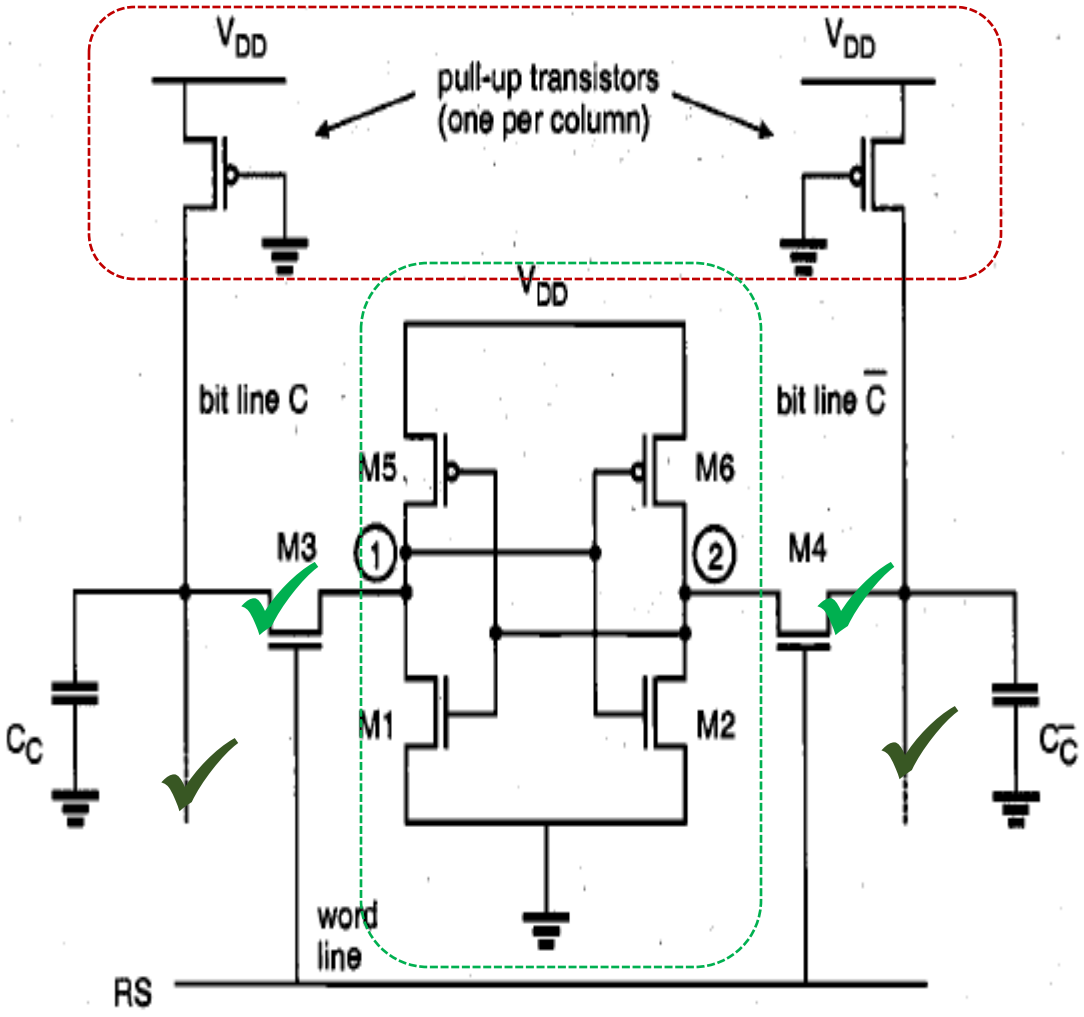
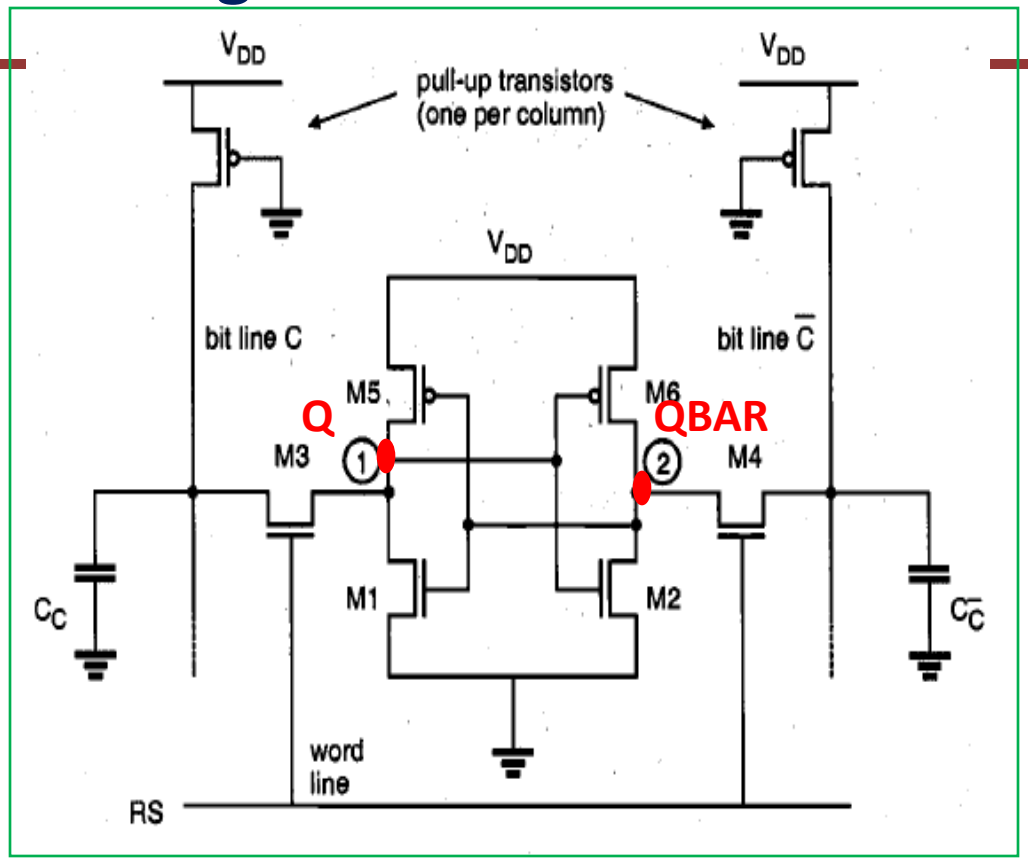


Fig: Circuit topology of the CMOS SRAM cell

- The circuit structure of full CMOS static RAM along with the pMOS column pull-up transistors on the complementary bit lines is shown.
- The memory cell consist of a simple CMOS latch (two inverters connected back to back).
- It has two access transistors (M3 & M4) connected to the complementary bit lines with their gates connected to word line (RS) i.e., Row Select.
- The access transistors are turned on whenever a word line (row) is activated for read or write operation, connecting the cell to the complementary bit- line columns.
- The two complementary bit lines are bit line c and bit line c'

Working of Full CMOS SRAM



- To write into the SRAM cell, bit line C and bit line C' will act as input lines.

- To read from the SRAM cell, bit line C and bit line C' will act as output lines.

Write operation

To write "1" :

Make bit line C = VDD
Make bit line C' = 0
Make RS (Word line) = VDD

CC = VDD, CC' = 0,
M3 & M4 = ON,
Q = VDD and QBAR = 0

To write "0" :

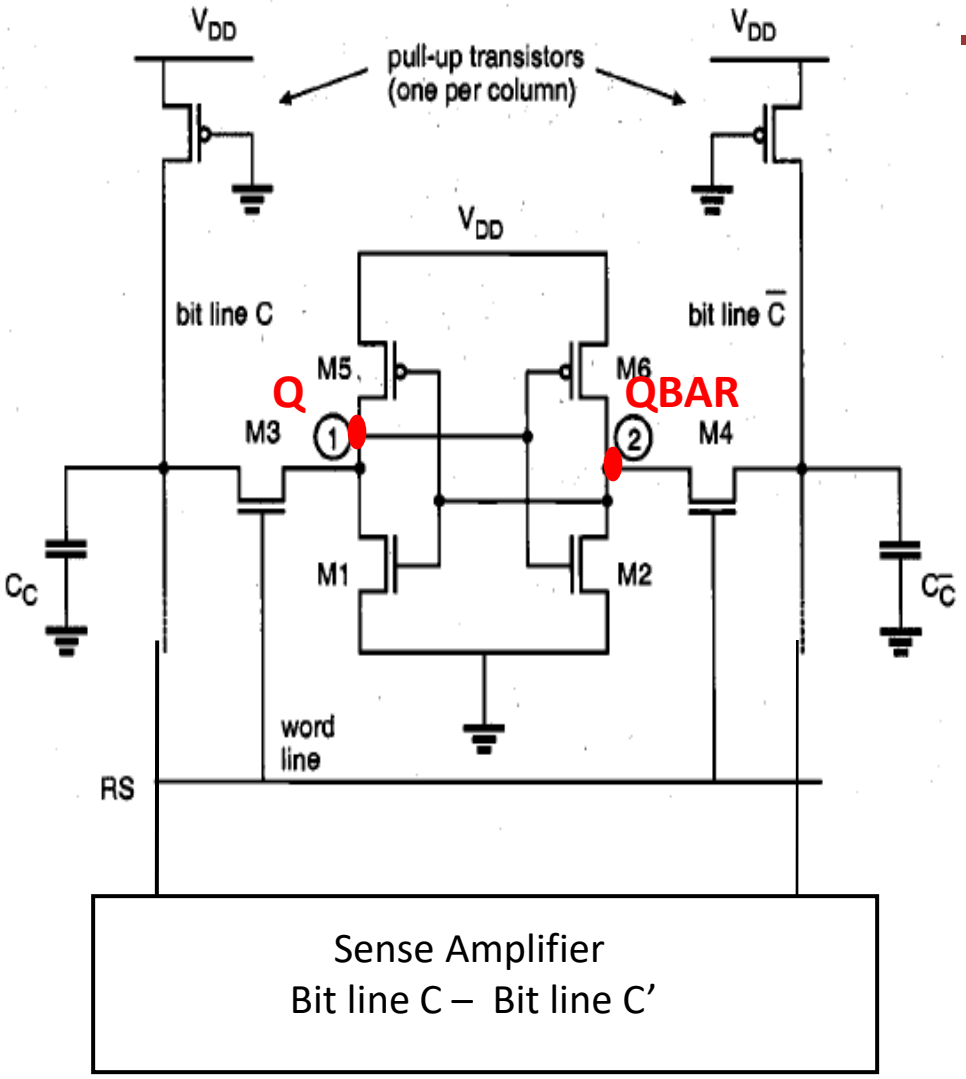
Make bit line C = 0
Make bit line C' = VDD
Make RS (Word line) = VDD

CC = 0, CC' = VDD,
M3 & M4 = ON,
Q = 0 and QBAR = VDD

Hold operation

Make RS (Word line) = 0,
M3 & M4 = OFF
The bit stored in the cell remains unchanged indefinitely

Working of Full CMOS SRAM



Read Operation

Read "1" operation

Precharge the bit line C and the bit line C' to VDD.

Make RS (Word Line) = VDD.

M3 and M4 = ON.

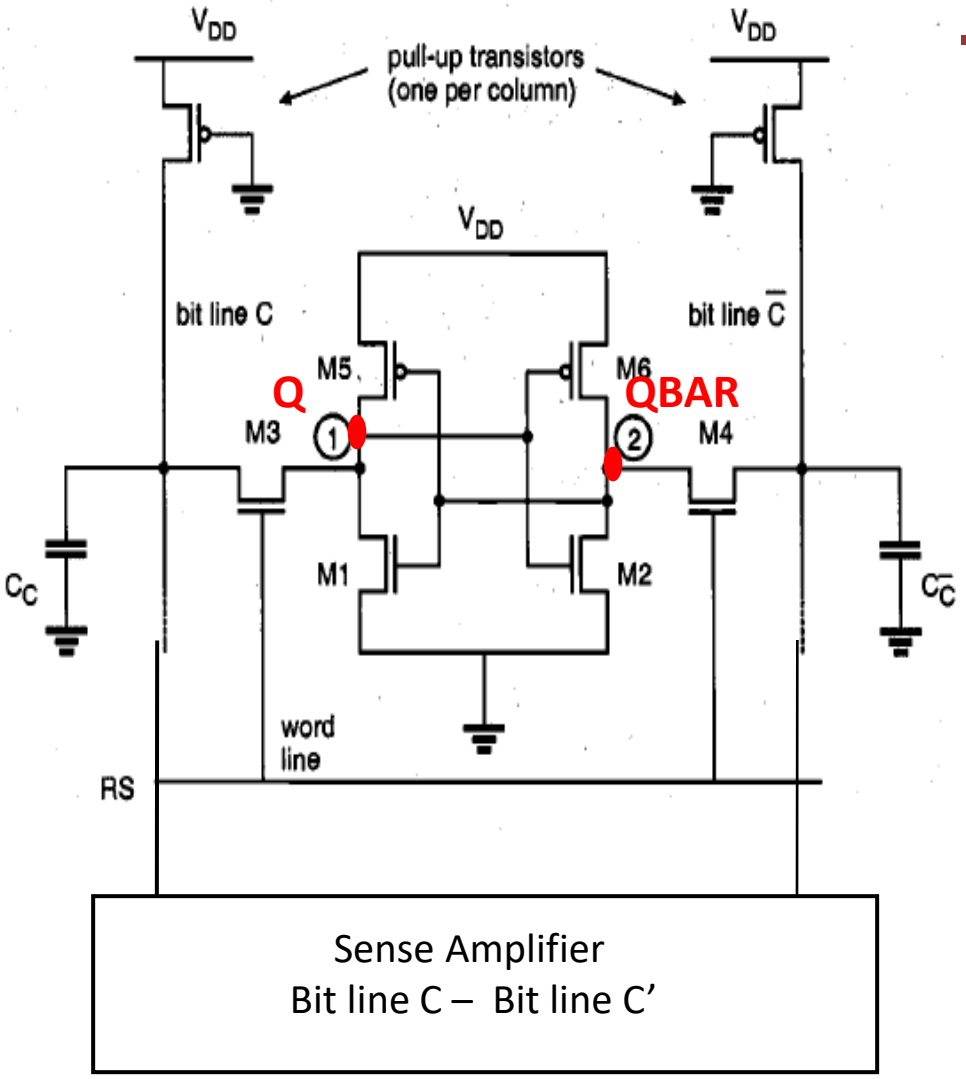
If Q = VDD & QBAR = 0, a bit 1 is stored in the cell (M2 is ON and M1 is OFF). Hence Bit line C' discharges to ground through M4 and M2.

The output of the sense amplifier –

Bit line C – Bit line C'
VDD – 0 = VDD*
Hence a bit 1 is stored

* General case for understanding purpose

Working of Full CMOS SRAM



Read Operation

Read "0" operation

Precharge the bit line C and the bit line C' to VDD.

Make RS (Word Line) = VDD.

M3 and M4 = ON.

If Q = 0 & QBAR = VDD, a bit 0 is stored in the cell (M1 is ON and M2 is OFF). Hence Bit line C discharges to ground through M3 and M1.

The output of the sense amplifier –

Bit line C – Bit line C'
0 – VDD = - VDD*
Hence a bit 0 is stored

* General case for understanding purpose

CMOS SRAM Cell Design Strategy

The two basic requirements which dictate the (W/L) ratios are :

(a) The data-read operation should not destroy the stored information in the SRAM Cell.

(b) The cell should not allow the modification of the stored information during the data-write phase.

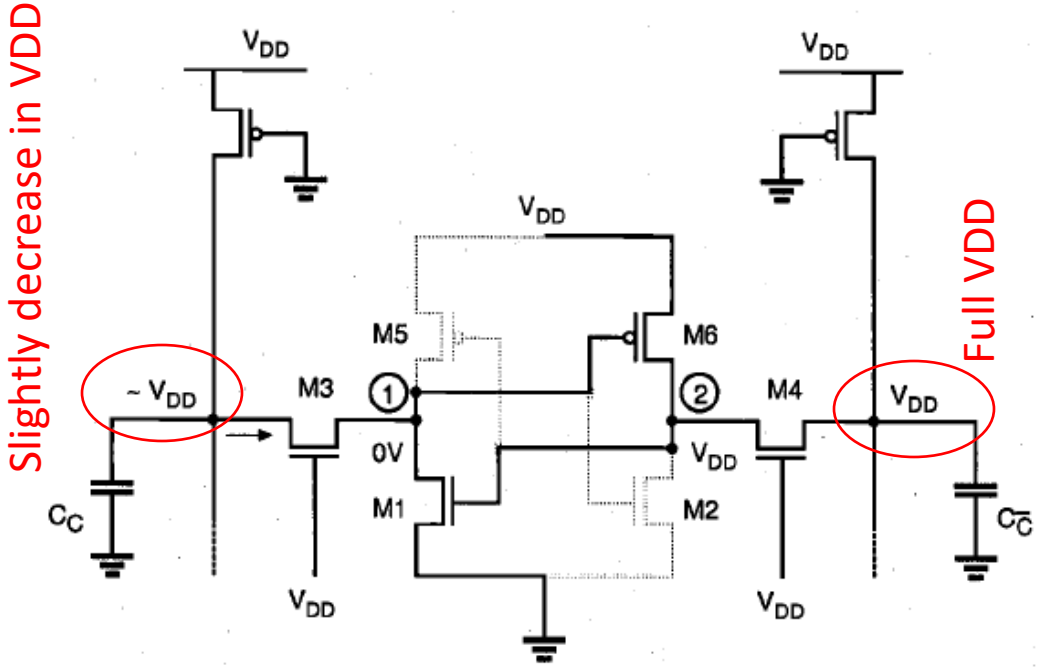


Fig : Voltage levels in the SRAM cell at the beginning of the "read" operation

Case : read "0"

M2 & M5 = OFF, M1 and M6 = ON
M1 & M6 = Linear Mode

Thus, the internal node voltages V1 = 0 & V2 = VDD before M3 & M4 are turned ON

When M3 & M4 are turned ON, There is no change in column C' and no current will flow through M4.

CMOS SRAM Cell Design Strategy

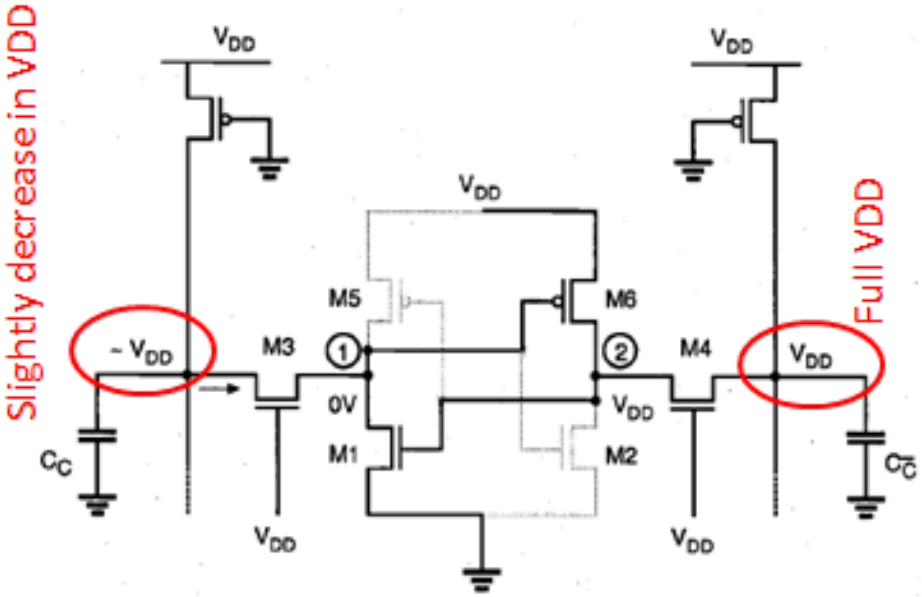


Fig : Voltage levels in the SRAM cell at the beginning of the "read" operation

- M3 & M1 will conduct a nonzero current and the voltage level of Column C will begin to drop slightly.

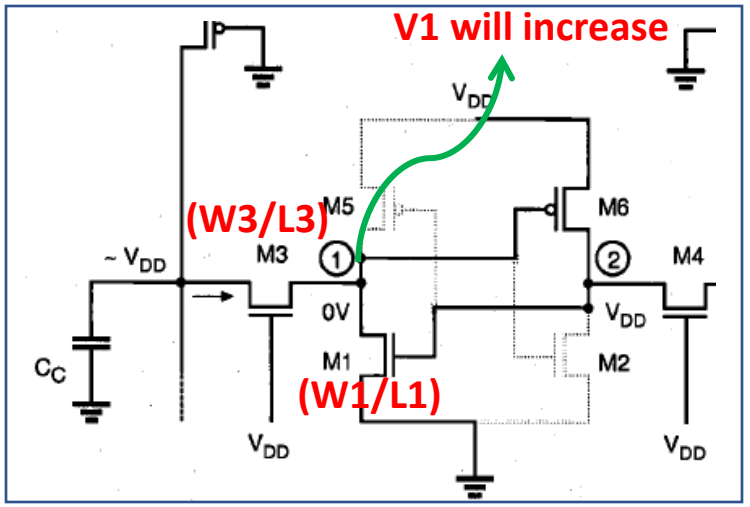
Note: The column capacitance Cc is typically very large; therefore, the amount of decrease in the column voltage is limited to a few hundred millivolts during the read phase.

Case : read "0"

Design Strategy :

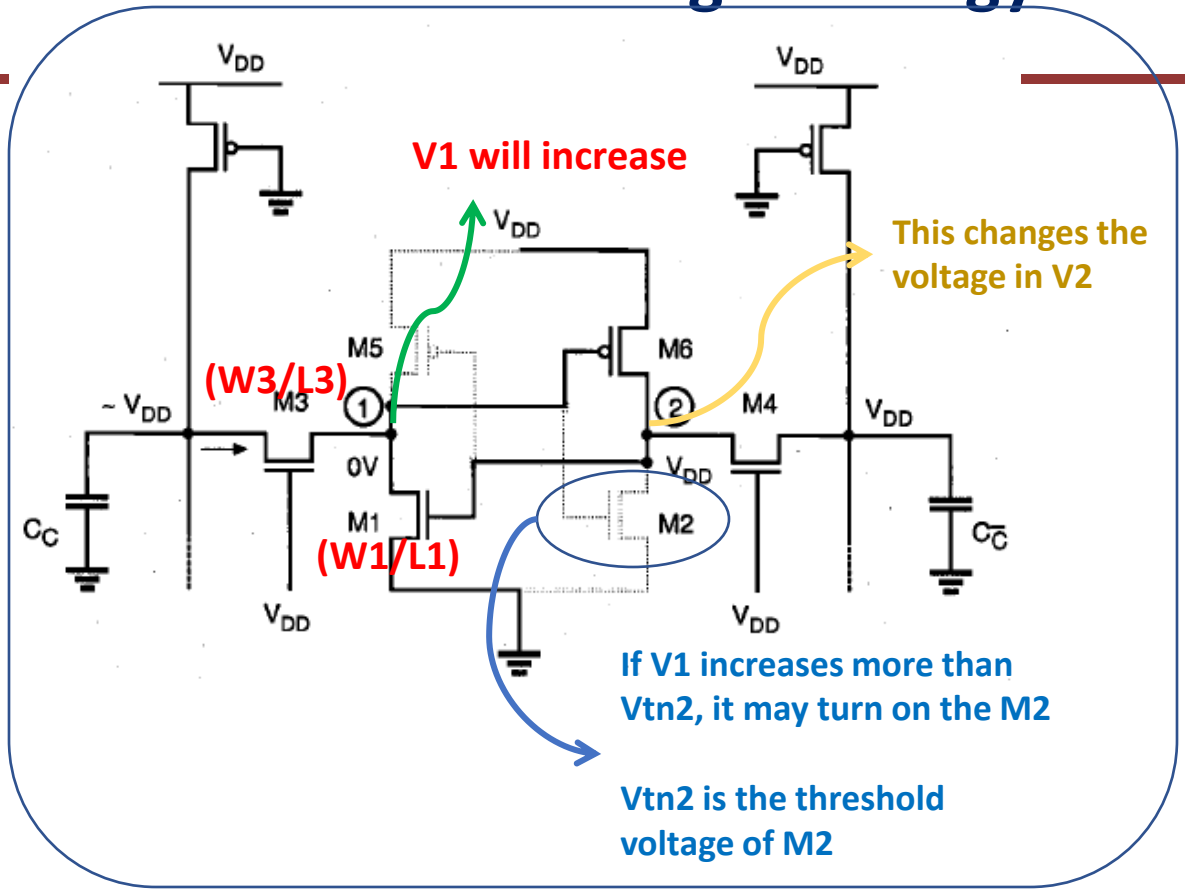
While M1 & M3 are slowly discharging the column capacitance, the node voltage of V1 will increase from its initial value of 0V.

Especially if the (W/L) ratio of the access transistor M3 is large compared to (W/L) of M1.



If W3/L3 > W1/l1 , V1 will increase because M3 will have less resistance compared to M1 (since resistance is proportional to (L/W).

CMOS SRAM Cell Design Strategy



Important Note:

The read circuitry is a sense amplifier which is responsible for detecting the small change in the bit line voltages drops and amplifying that value to output the bit stored.

Hence the design should be done in a very careful manner.

- If W3/L3 > W1/l1 , V1 will increase because M3 will have less resistance compared to M1 (since resistance is proportional to (L/W).

- If the node voltage V1 increases more than Vtn2 (Threshold voltage of M2 Transistor), it may turn ON the M2 MOSFET leading to unintended change of the stored state.

CMOS SRAM Cell Design Strategy

The Key design issue for the data-read operation is then to guarantee that the ***voltage V1 does not exceed the threshold of M2***, so that the transistor M2 remains turned OFF during the read phase.

$$V_{1,max} \leq V_{T,2} \qquad (1)$$

We can assume that after the access transistors are turned on, the column voltage Vc remains approximately equal to VDD. Hence , M3 operates in saturation while M1 operates in the linear region.

$$\frac{k_{n,3}}{2}\left(V_{DD}-V_1-V_{T,n}\right)^2 = \frac{k_{n,1}}{2}\left(2\left(V_{DD}-V_{T,n}\right)V_1-V_1^2\right) \qquad (2)$$

Substitute V1 as VT,n in equation 2 (from equation 1) and simplifying the equation

$$\frac{k_{n,3}}{k_{n,1}} = \frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_1} < \frac{2\left(V_{DD}-1.5V_{T,n}\right)V_{T,n}}{\left(V_{DD}-2V_{T,n}\right)^2}$$

To summarize, the transistor M2 will remain in cut-off during the read "0" operation if the condition in equation 1 is satisfied.

A symmetrical condition also dictates the aspect ratios of M2 and M4.

CMOS SRAM Cell Design Strategy

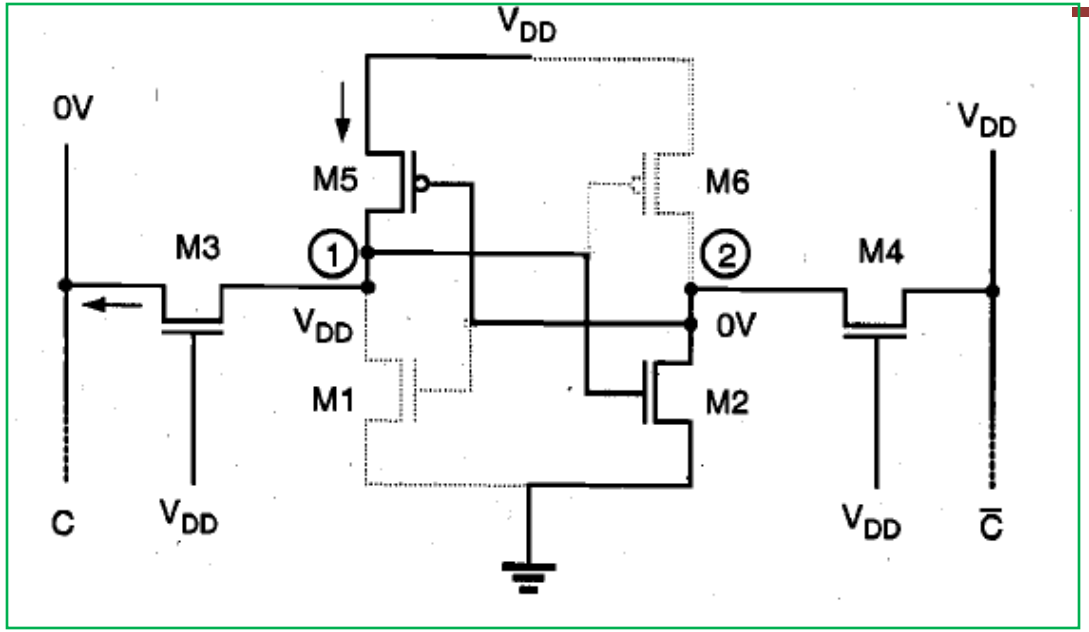


Fig : Voltage levels in the SRAM cell at the beginning of the 'Write" operation

Case : write "0"

Consider the write "0" operation, assuming that a logic "1" is stored in the SRAM Cell initially.

Initial Conditions : M1 & M6 = OFF, M2 & M5 = ON (Linear Mode)
Thus, the internal node voltages are V1 = VDD and V2 = 0 V before the access transistors are turned ON.

Design Strategy :

To write "0", M3 and M4 are turned ON.

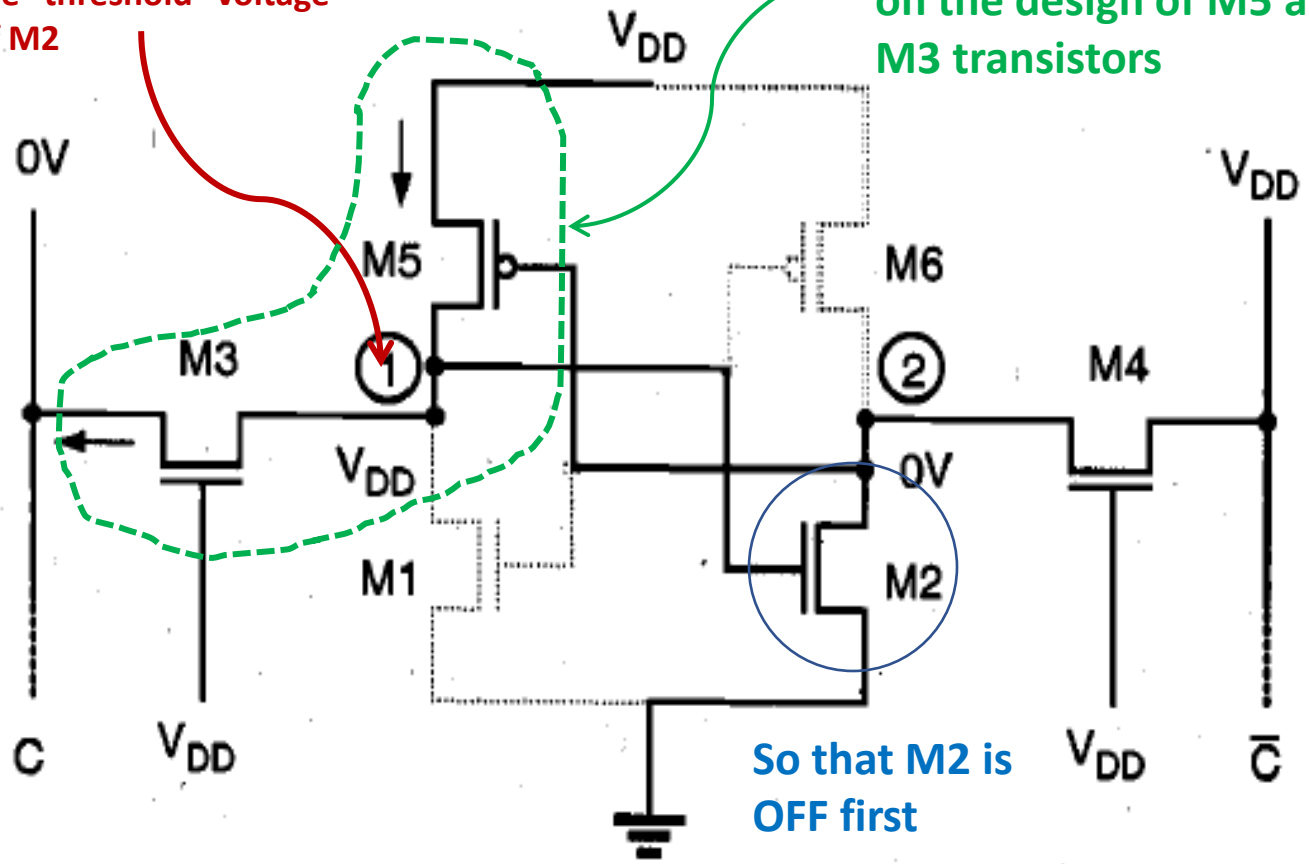
To change the stored information i.e., to force V1 to 0V and V2 to VDD, the node voltage V1 must be reduced below the threshold voltage of M2.

So that M2 turns OFF first.

CMOS SRAM Cell Design Strategy

We have to make this node voltage less than the threshold voltage of M2

Making the node voltage V1 = 0V entirely depends on the design of M5 and M3 transistors



So that M2 is OFF first

When V1 = Vtn, the transistor M3 operates in linear region and M5 operates in the saturation mode

$$\frac{k_{p,5}}{2}\left(0 - V_{DD} - V_{T,p}\right)^2 = \frac{k_{n,3}}{2}\left(2\left(V_{DD} - V_{T,n}\right)V_{T,n} - V_{T,n}^2\right) \quad (3)$$

Rearranging the conditions, results in

$$\frac{k_{p,5}}{k_{n,3}} < \frac{2\left(V_{DD} - 1.5\,V_{T,n}\right)V_{T,n}}{\left(V_{DD} + V_{T,p}\right)^2}$$

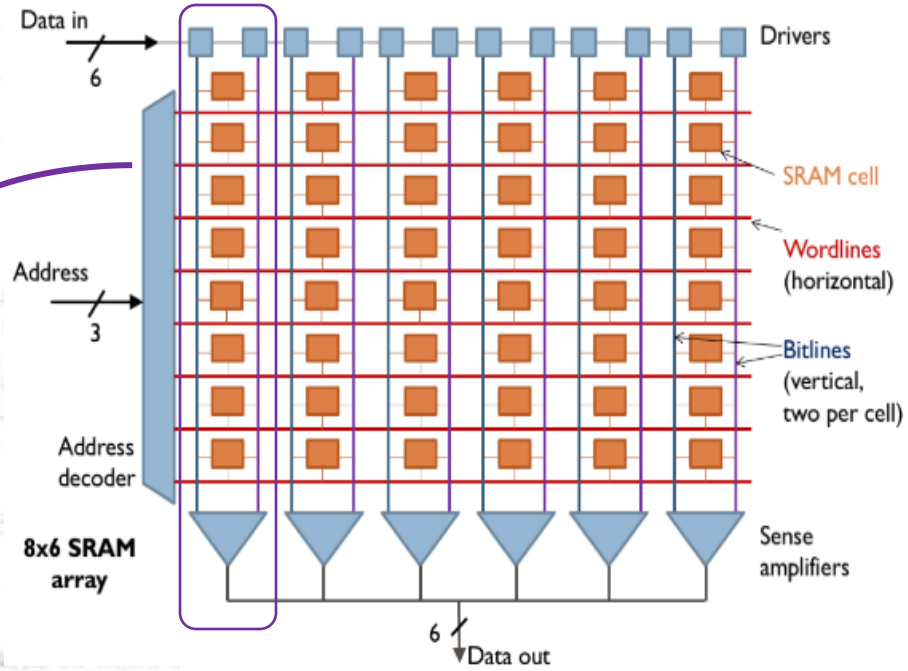
$$\frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_3} < \frac{\mu_n}{\mu_p} \cdot \frac{2\left(V_{DD} - 1.5\,V_{T,n}\right)V_{T,n}}{\left(V_{DD} + V_{T,p}\right)^2}$$

To summarize, the transistor M2 will be forced into cut-off mode during the write"0" operation if the above conditions are satisfied.

This will guarantee that M1 subsequently turns ON , charging the stored information.
Note: a symmetrical condition also dictates the aspect ratios of M6 and M4.

Operation of SRAM

SRAM Memory Block



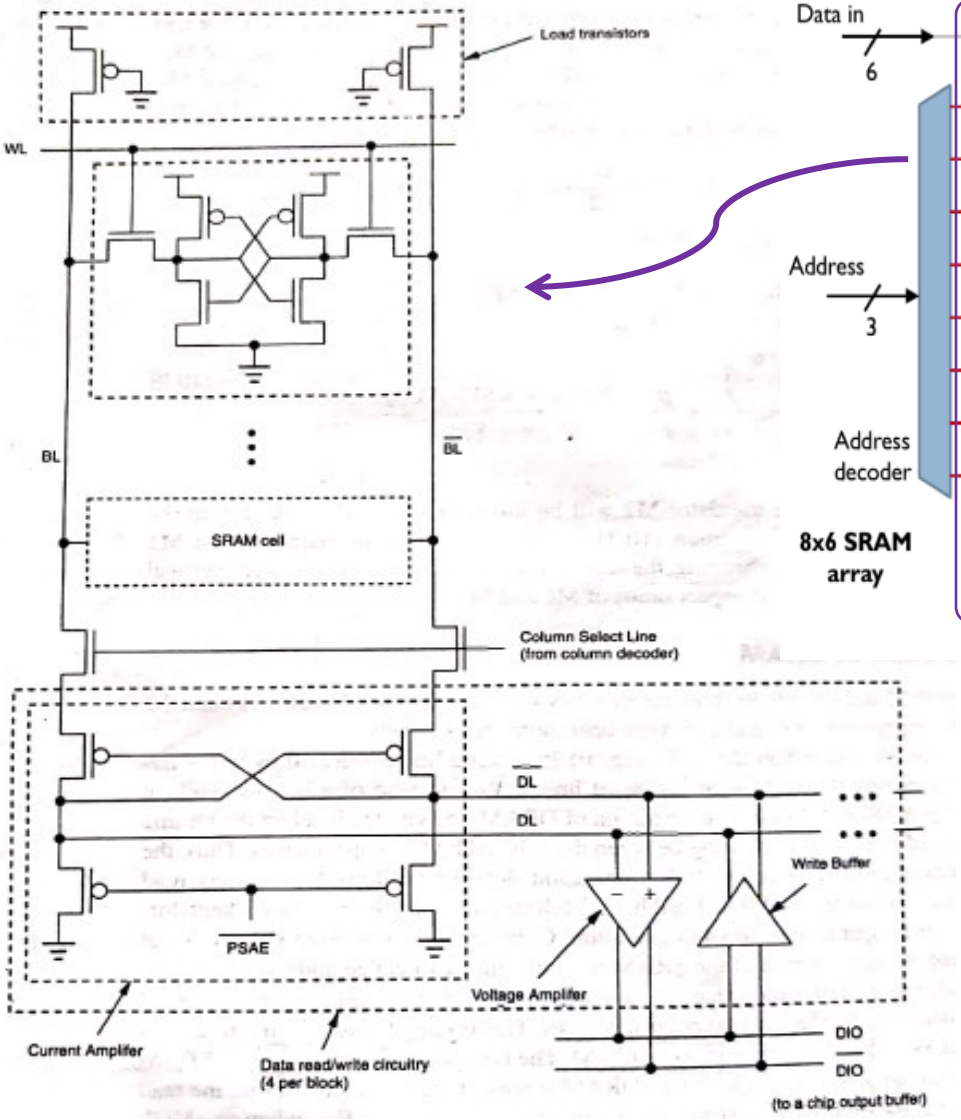
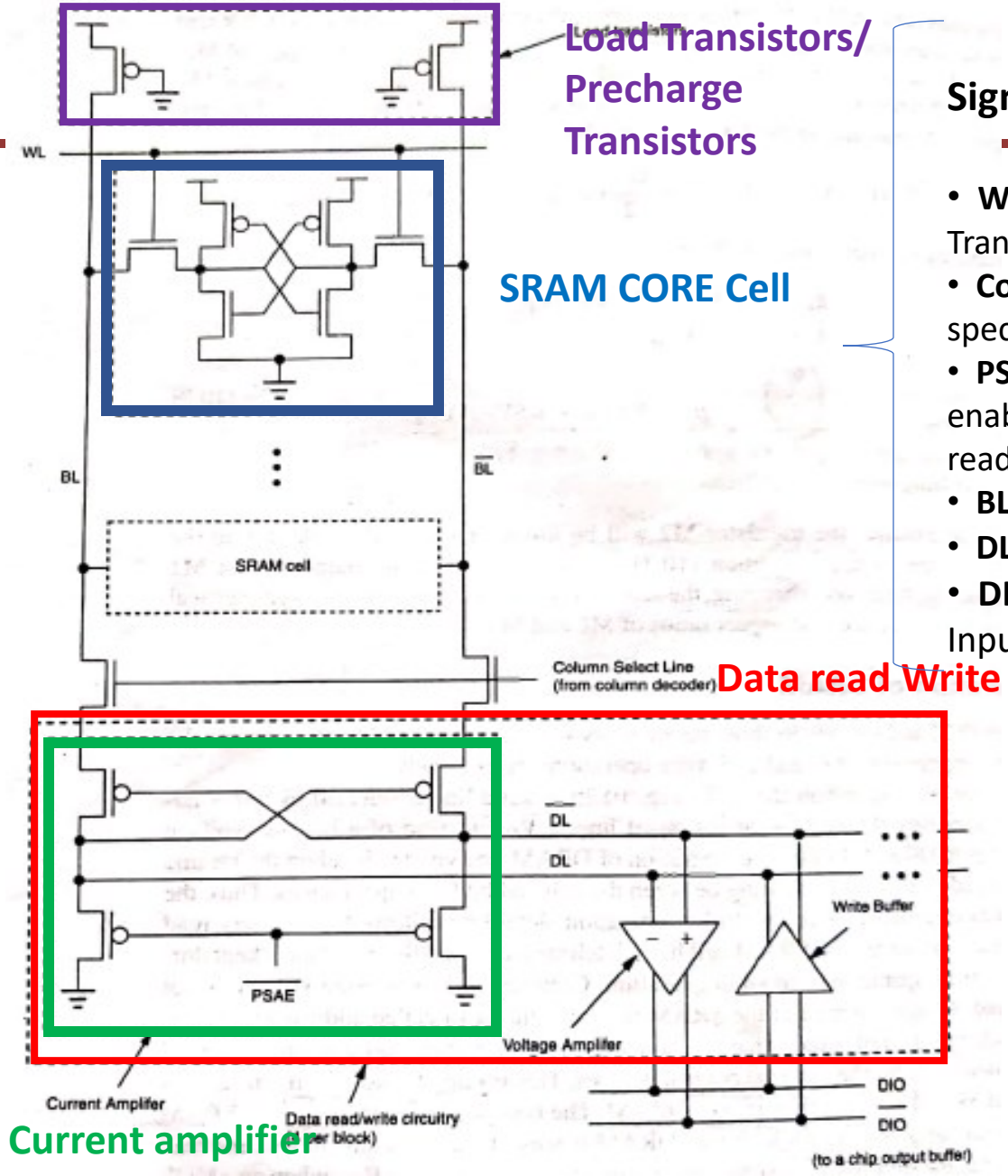


Fig : memory structure of SRAM with read/write circuitry

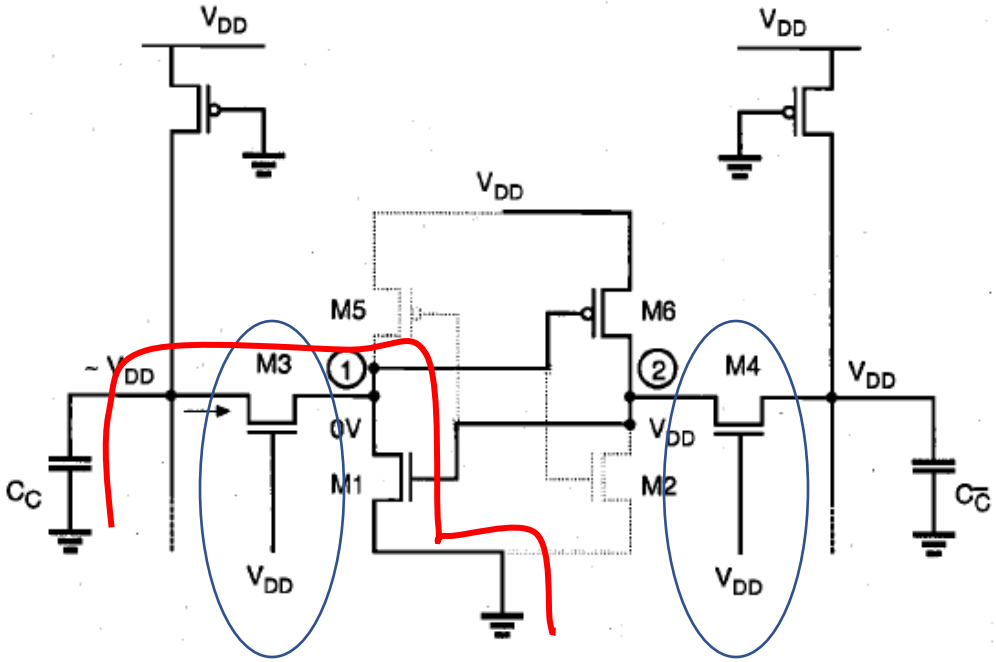


Signals associated with the SRAM

- **Word Line (WL)** – To turn ON the access Transistors (also acts as Row select).
- **Column Select Line (CSL)** – To select the specific column in the array.
- **PSAE' (PMOS Sense Amplifier Enable)** – To enable the current sense amplifier during the read operation
- **BL & BL'** – Bit Line and Bit Line'
- **DL & DL'** – Data Line & Data Line'
- **DIO & DIO'** – Data Input / Output & Data Input / Output'

SRAM – Read Operation

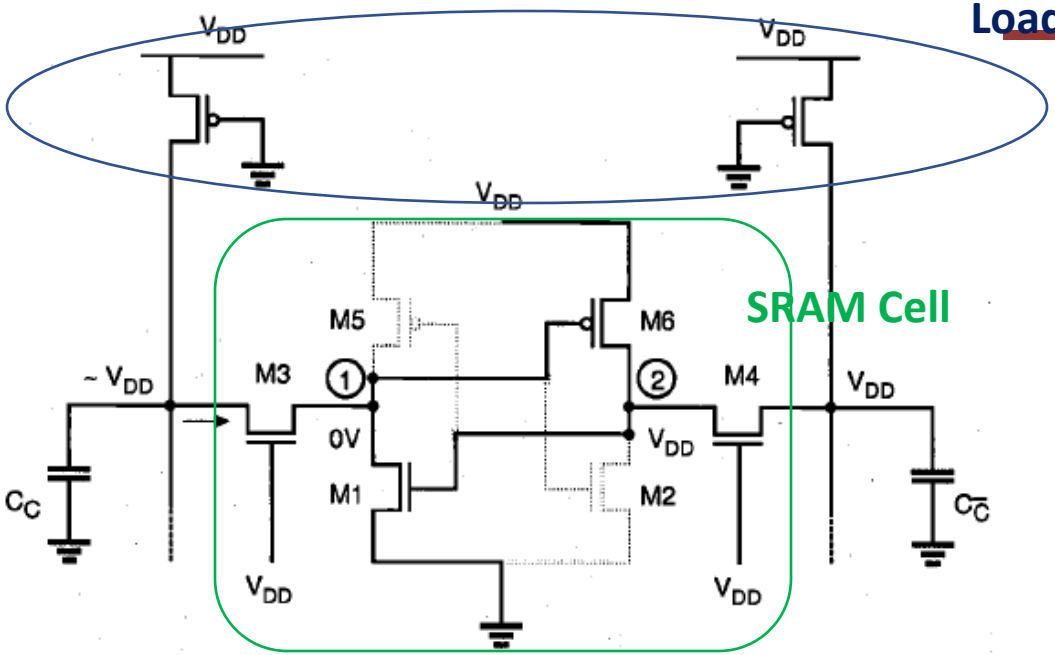
When the Word Line is enabled, one of the bit lines is discharged through an nMOS transistor connected to a “0” node of the cell.



The access transistors are turned ON (Word line is Enabled)

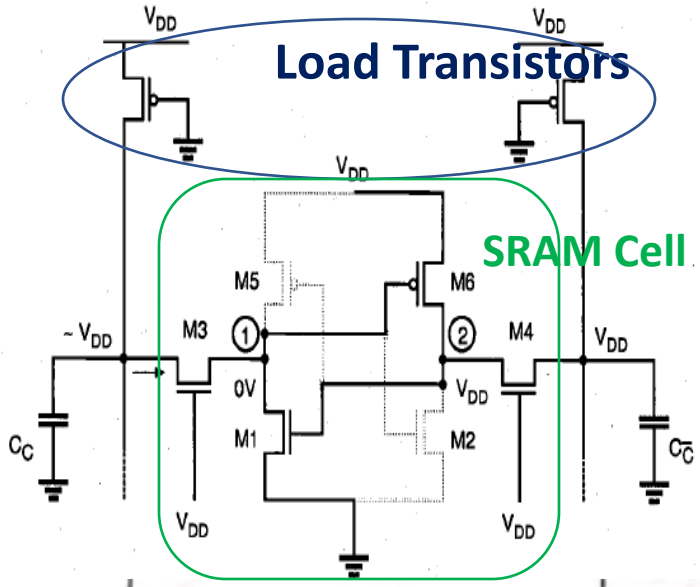
One of the bit line discharges through the nMOS (Here Cc discharges through M3 and M1)

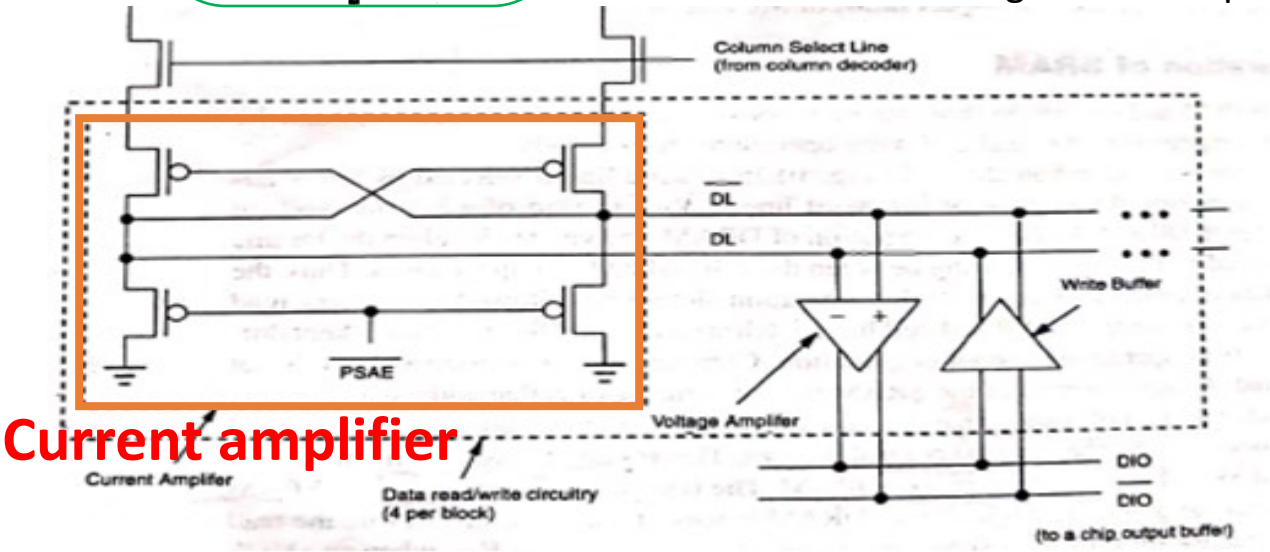
SRAM – Read Operation



The current driving capability of the cell is very small (tens of uA) and the voltage change on the bit line is just tens of mV when the load transistor is turned ON.

SRAM – Read Operation



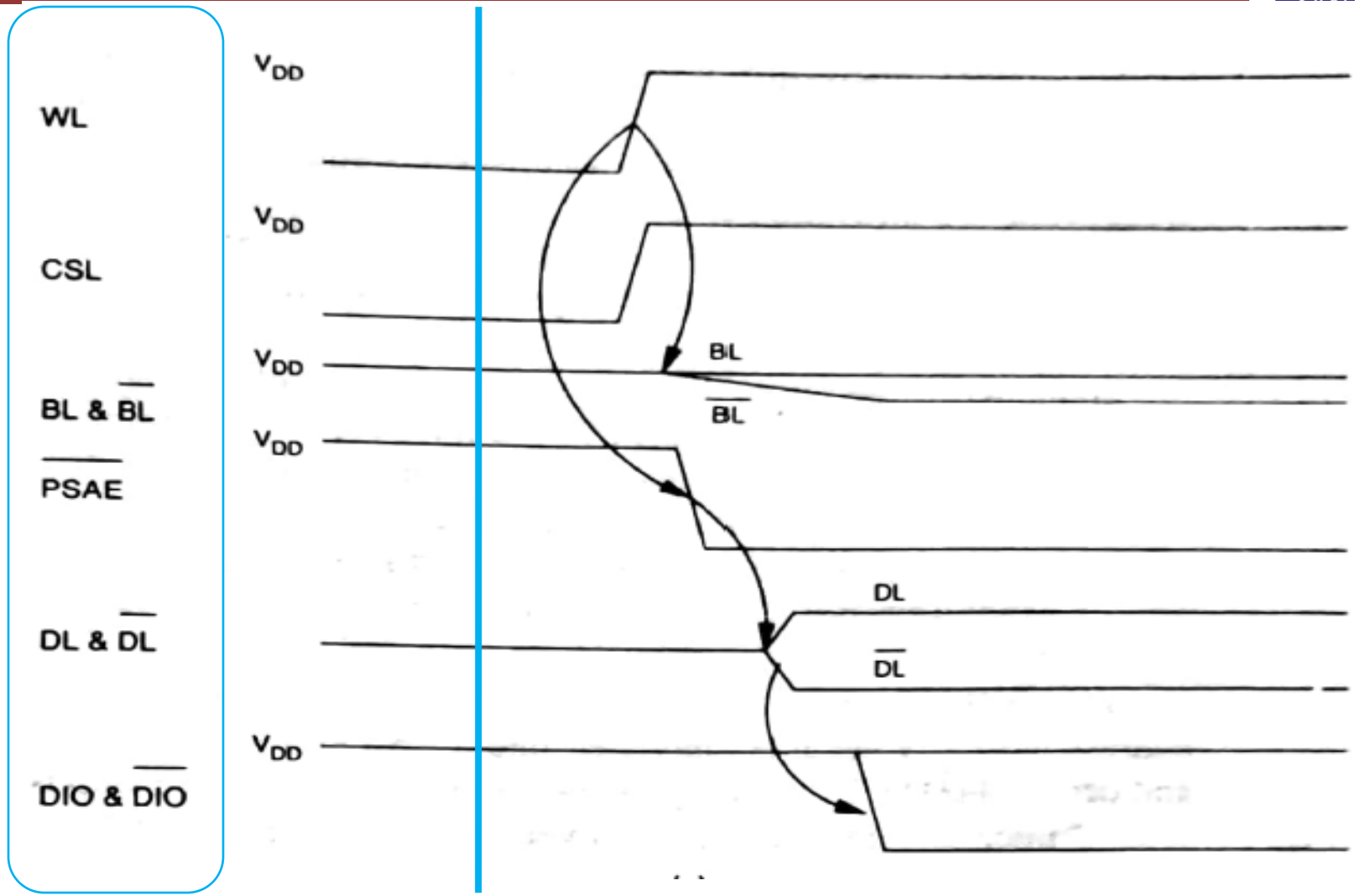


- The sense amplifier to detect the voltage difference on the bit lines is shared by multiple bit lines and the connection of the sense amplifier to a bit line pair is controlled by a column selection line.

- Typically a multi-stage amplifier is used to improve the read speed

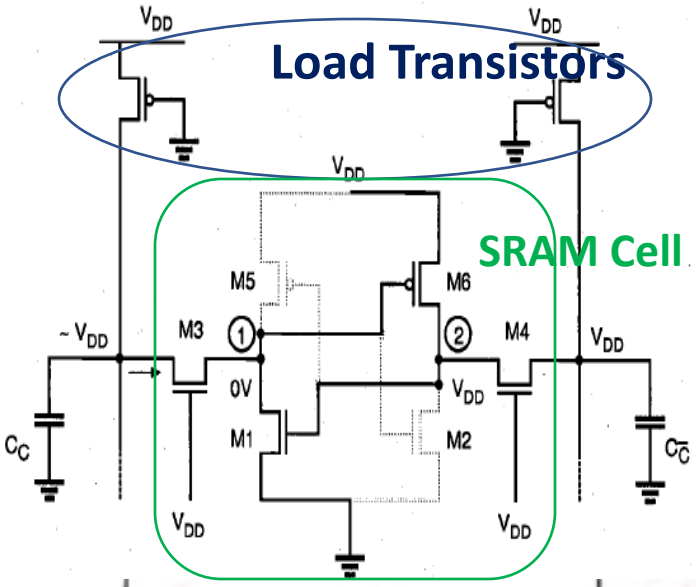
- A high gain voltage or current – mode amplifier is used as a first stage amplifier and a voltage – mode amplifier to generate CMOS level signals (DIO & DIO') with a large current driving capability is used as the last stage of the amplifiers.

SRAM – Read Operation



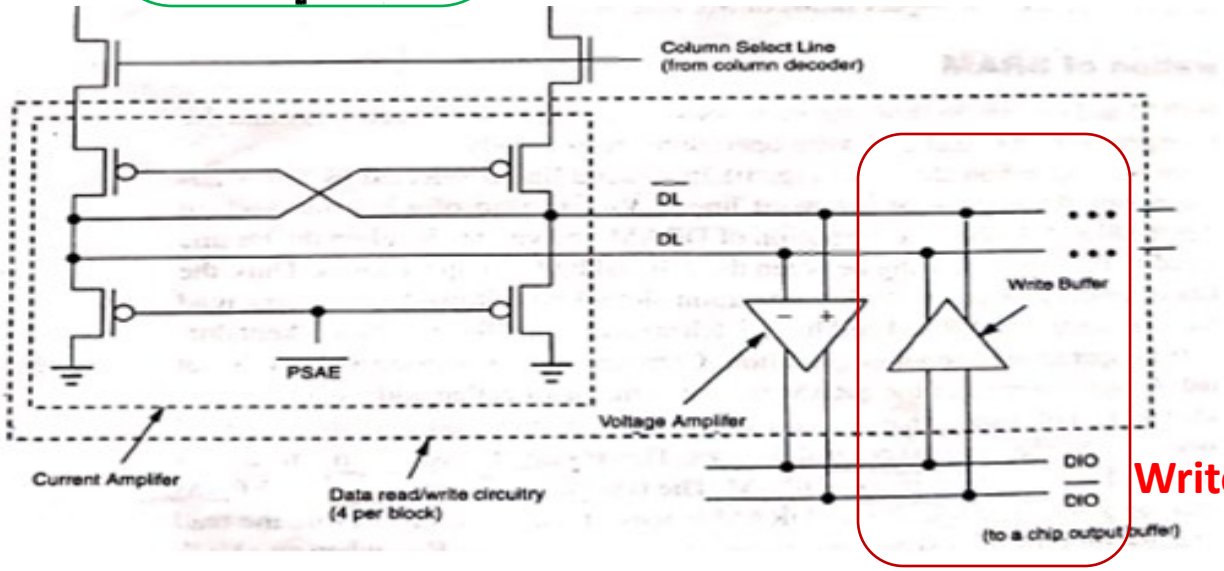
SRAM – Write Operation

- In the write operation, data to be written into a cell and provided by external devices and DIO & DIO' and DL & DL' lines are set according to the data.



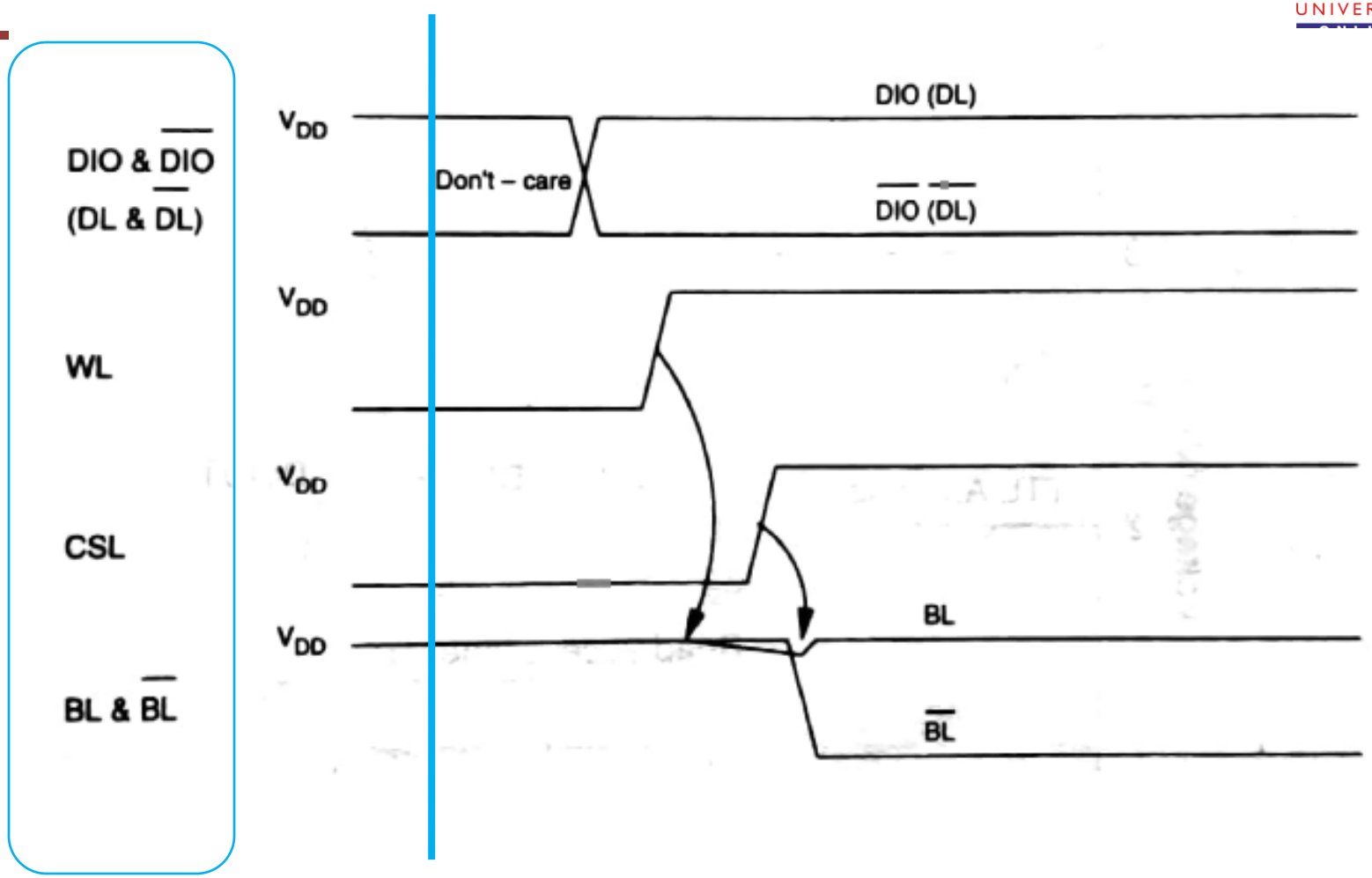
- A word line is selected by a row address and one of the bit lines is discharged as in the read operation.

- When the column gates are opened , the write buffer starts to write data into the cell. Since the write buffer has much larger current driving capability than that of the cell, the write operation take less time than the read operation.



Write Buffer

SRAM – Write Operation



THANK YOU

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