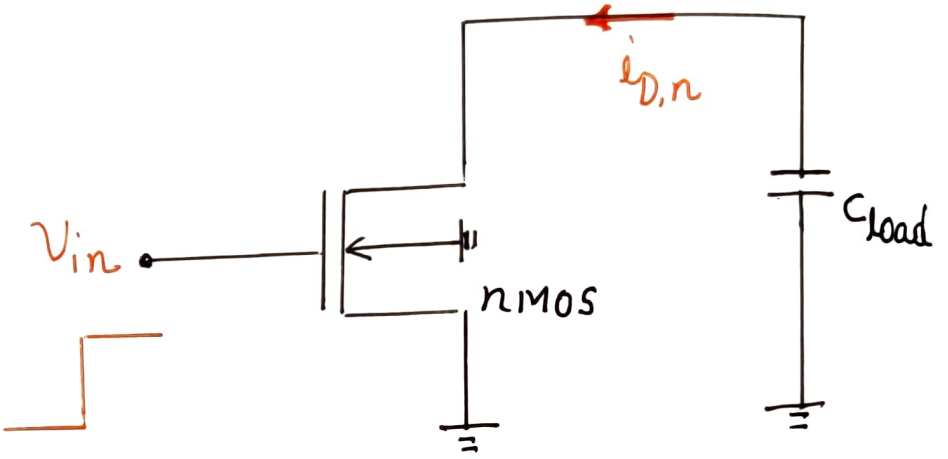
Calculation of delay :-

Equivalint CMOS circuit during high-to-low Output transition



→ W.K.T.

current and vtg are relatiol in capacitor is given by

$$i = C \frac{dV}{dt}$$

→ In a CMOS inverter

$$i_{D,p} - i_{Dn} = C_{load} \frac{dV_{out}}{dt}$$

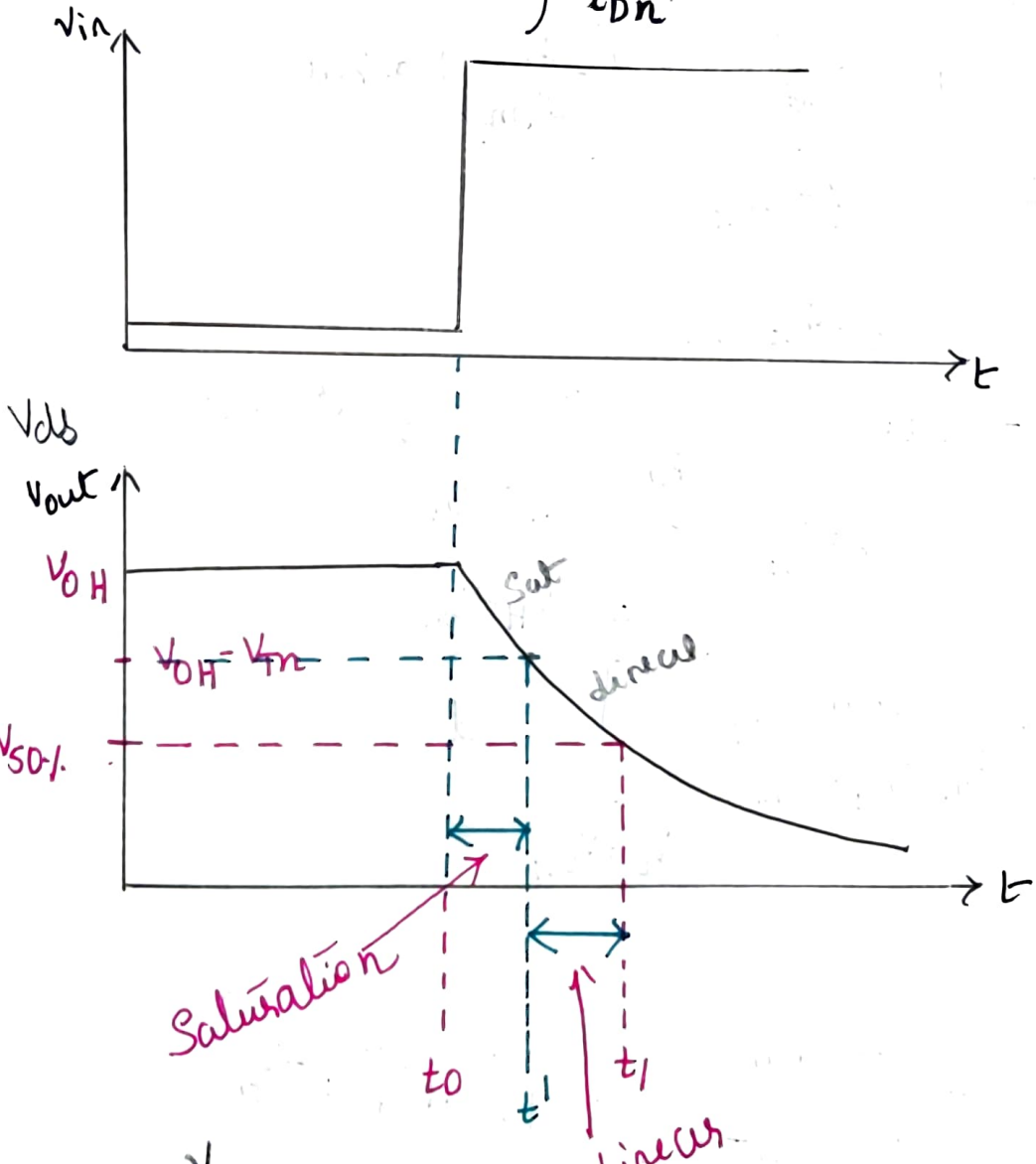
→ In a high to low transition

$$v_{in} = V_{OH}$$

$$\therefore i_{D,p} = 0$$

$$\therefore C_{load} \frac{dV_{out}}{dt} = -i_{Dn}$$

$$dt = -C_{load} \int \frac{1}{i_{Dn}} dV_{out}$$



$V_{ds} > V_{gs} - V_{tn}$

$> v_{in} - V_{th}$

$V_{OH} - V_{th}$

→ From to to t_1' nMOS is operating in Saturation region

$$I_{D,n} = \frac{K_n}{2}(V_{in} - V_{tn})^2$$

$$= \frac{K_n}{2}\left[V_{OH} - V_{tn}\right]^2$$

$$\therefore \int_{t=t_0}^{t=t'} dt = C_{load} \int_{V_0 = V_{OH}}^{V_0 = V_{OH} - V_{Tn}} \left(\frac{1}{I_{Dn}}\right) dV_{out}$$

$$= -C_{load} \int_{V_0 = V_{OH}}^{V_0 = V_{OH} - V_{Tn}} \frac{1}{\frac{K_n}{2}(V_{OH} - V_{tn})^2} dV_{out}$$

$$= -\frac{2C_{load}}{K_n(V_{OH} - V_{tn})^2} \int_{V_0 = V_{OH}}^{V_0 = V_{OH} - V_{tn}} dV_{out}$$

$$= -\frac{2C_{load}}{K_n(V_{OH} - V_{tn})^2} \left[\cancel{V_{OH}} - \cancel{V_{OH}} - V_{tn}\right]$$

$$= \frac{2C_{load}\, V_{tn}}{K_n(V_{OH} - V_{tn})^2}$$

@ $t = t'$ to $t = t_1$

$$\int_{t=t'}^{t=t_1} dt = -C_{load} \int_{V_{out}=V_{OH}-V_{tn}}^{V_{out}=V_{50}} \frac{1}{I_{Dn}} dV_{out}$$

→ In this region MOSFET Operating in Linear region

$$i_{dn} = \frac{1}{2} K_n \left[2(V_{in} - V_{tn}) V_{out} - V_{out}^2 \right]$$

$$= \frac{K_n}{2} \left[2 (V_{OH} - V_{tn}) V_{out} - V_{out}^2 \right]$$

$$\int_{t=t'}^{t=t_1} dt = -C_{load} \int_{V_{out}=V_{OH}-V_{tn}}^{V_{out}=V_{50}} \frac{1}{\frac{K_n}{2}\left(2(V_{OH}-V_{tn})V_{out} - V_{out}^2\right)} dV_{out}$$

$$= \frac{C_{load} 2}{K_n} \int_{V_{out}=V_{OH}-V_{tn}}^{V_{out}=V_{50}} \frac{1}{2(V_{OH}-V_{tn})V_{out} - V_{out}^2} dV_{out}$$

$$\int \frac{1}{2\alpha x - x^2}\,dx = \int \frac{1}{2\alpha x - x^2 + \alpha^2 - \alpha^2}\,dx$$

$$= \int \frac{1}{\alpha^2 - (x-\alpha)^2}\,dx$$

$$\int \frac{1}{\alpha^2 - (x-\alpha)^2}\,dx = \frac{1}{2\alpha} \ln\left[1 + \frac{x}{\alpha}\right] - \ln\left[1 - \frac{x}{\alpha}\right] = \ln\left[\frac{x}{2\alpha - x}\right]$$

$$\frac{1}{2\alpha} \ln\left(\frac{x}{2\alpha - x}\right)$$

$$\int \frac{1}{\alpha^2 - (x-\alpha)^2}\,dx = \frac{1}{2(V_{OH} - V_{Tn})} \cdot \ln\left[\frac{V_{out}}{2(V_{OH} - V_{Tn}) - V_{out}}\right]$$

$V_{out} = V_{50}$

$V_{out} = V_{OH} - V_{Tn}$

$$t_1 - t' = \frac{-2C_{load}}{2(V_{OH} - V_{tn})K_n} \cdot \ln\left[\frac{V_{out}}{2(V_{OH} - V_{Tn}) - V_{out}}\right]$$

$V_{out} = V_{50}$

$V_{out} = V_{OH} - V_{Tn}$

$$= \frac{C_{load}}{(V_{OH} - V_{tn})K_n} \ln\left[\frac{2(V_{OH} - V_{Tn}) - V_{out}}{V_{out}}\right]$$

$V_{out} = V_{50}$

$V_{out} = V_{OH} - V_{Tn}$

$$\frac{C_{load}}{(V_{OH} - V_{Tn})K_n} \ln\left[\frac{2(V_{OH} - V_{Tn}) - V_{50}}{V_{50}}\right] - \ln\left[\frac{2(V_{OH} - V_{Tn}) - (V_{OH} - V_{Tn})}{V_{OH} - V_{Tn}}\right]$$

0

$$= \frac{C_{load}}{K_n (V_{OH} - V_{Tn})} \ln \left[\frac{2(V_{OH} - V_{Tn}) - V_{50}}{V_{50}} \right]$$

$$\therefore \tau_{PHL} = \frac{2 C_{load} V_{Tn}}{K_n (V_{OH} - V_{Tn})^2} + \frac{C_{load}}{K_n (V_{OH} - V_{Tn})} \ln \left[\frac{2(V_{OH} - V_{Tn}) - V_{50}}{V_{50}} \right]$$

$$= \frac{C_{load}}{K_n (V_{OH} - V_{Tn})} \left[\frac{2 V_{Tn}}{V_{OH} - V_{Tn}} + \ln \left[\frac{2(V_{OH} - V_{Tn})}{V_{50}} - 1 \right] \right]$$

$$V_{50} = \frac{V_{OH} + V_{OL}}{2}$$

$$\therefore \tau_{PHL} = \frac{C_{load}}{K_n (V_{OH} - V_{Tn})} \left[\frac{2 V_{Tn}}{V_{OH} - V_{Tn}} + \ln \left[\frac{4(V_{OH} - V_{Tn})}{V_{OH} + V_{OL}} - 1 \right] \right]$$

→ For CMOS inverter

$$V_{OH} = V_{DD}$$

$$V_{OL} = 0$$

$$\tau_{PHL} = \frac{C_{load}}{K_n (V_{DD} - V_{Tn})} \cdot \left[\frac{2 V_{Tn}}{V_{DD} - V_{Tn}} + \ln \left(\frac{4(V_{DD} - V_{Tn})}{V_{DD}} - 1 \right) \right]$$

→ When input voltage switches from V_{OH} to V_{OL} nMOS transistor cut off

$$\tau_{PLH} = \frac{C_{load}}{K_p(V_{OH} - V_{OL} - |V_{TP}|)} \left[\frac{2|V_{TP}|}{V_{OH} - V_{OL} - |V_{TP}|} + \ln \left(\frac{2(V_{OH} - V_{OL} - |V_{TP}|}{V_{OH} - V_{SO}} \right. \right.$$

$V_{OH} = V_{DD}$

$V_{OL} = 0$

$$\tau_{PLH} = \frac{C_{load}}{K_p(V_{DD} - |V_{TP}|)} \left[\frac{2|V_{TP}|}{V_{DD} - |V_{TP}|} + \ln \left[\frac{4(V_{DD} - |V_{TP}|}{V_{DD}} - 1 \right] \right]$$

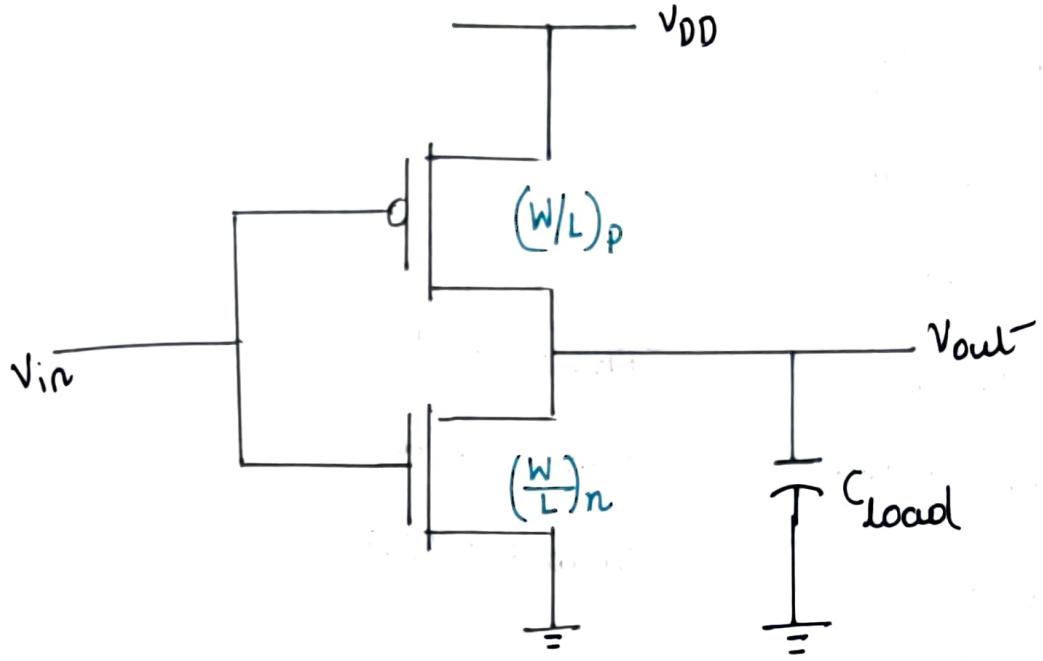
Comparing τ_{PHL} & τ_{PLH} equations

$\tau_{PHL} = \tau_{PLH}$ If $V_{T,n} = |V_{T,P}|$

$K_n = K_p$

$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p}$

Inverter Design with delay Constraints



→ The goal is to determine channel dimensions of NMOS & PMOS transistors

→ Design constraint of CMOS transistors are

noise margin
Silicon area
Power dissipation
Propagation delay

$$\left(\frac{W}{L}\right)_n = \frac{C_{load}}{\tau_{PHL}\,\mu_n C_{ox}(V_{DD}-V_{Tn})} \cdot \left[\frac{2V_{Tn}}{V_{DD}-V_{Tn}} + \ln\left(\frac{4(V_{DD}-V_{Tn})}{V_{DD}}-1\right)\right]$$

$$\left(\frac{W}{L}\right)_p = \frac{C_{load}}{\tau_{PLH}\,\mu_p C_{ox}(V_{DD}-V_{TP})} \cdot \left[\frac{2V_{TP}}{V_{DD}-|V_{TP}|} + \ln\left(\frac{4(V_{DD}-|V_{TP}|}{V_{DD}}-1\right)\right]$$

1. $\mu_n C_{ox} = 120 \frac{\mu A}{V^2}$

$\mu_p C_{ox} = 60 \frac{\mu A}{V^2}$

$L = 0.6\ \mu m$

$V_{Ton} = 0.8\ V$

$V_{Top} = -1\ V$

$W_{min} = 1.2\ \mu m$

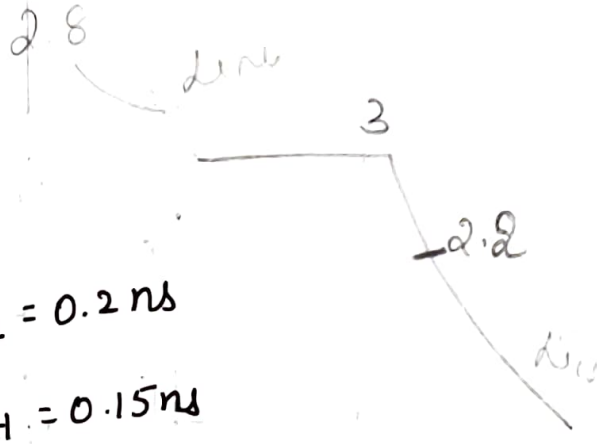
$V_{TH} = 1.5\ V$

$V_{DD} = 3V$

$\tau_{PHL} = 0.2\ ns$

$\tau_{PLH} = 0.15\ ns$

$C_{load} = 300\ fF$



$$\left(\frac{W}{L}\right)_n = \frac{C_{load}}{\tau_{PHL}\,\mu_n C_{ox}(V_{DD}-V_{Tn})}\left[\frac{2V_{Tn}}{V_{DD}-V_{Tn}} + \ln\left(\frac{4(V_{DD}-V_{tn})}{V_{DD}}\right.\right.$$

$$= \frac{300\times10^{-15}}{0.2\times10^{-9}\times120\times10^{-6}(3-0.8)}\left[\frac{2\times0.8}{3-0.8} + \ln\left(\frac{4(3-0.8)}{3}\right.\right.$$

$$= 7.9$$

$$\left(\frac{W}{L}\right)_p = \frac{C_{load}}{\tau_{PLH}\,\mu_p C_{ox}(V_{DD}-V_{TP})}\left[\frac{2V_{TP}}{V_{DD}-V_{TP}} + \ln\left(\frac{4(V_{DD}-V_{TP})}{V_{DD}}\right.\right.$$

$$= 25.2$$

$t = 0.35\,ns$

$2 \rightarrow 0.5V \longrightarrow$ nMOS operates in Linear

$$t = \frac{C_{load}}{K_n (V_{DD} - V_{TOn})} \ln \left[\frac{2(V_{OH} - V_{TOn}) - V_{out}}{V_{out}} \right]_2^{0.5}$$

$$0.35n = \frac{300 \times 10^{-15}}{120 \times 10^{-6} \left(\frac{W}{L}\right)_n [3 - 0.8]} \left[\ln \left[\frac{2(3-0.8) - 0.5}{0.5} \right] - \ln \left[\frac{2(3-0.8) - 2}{2} \right] \right)$$

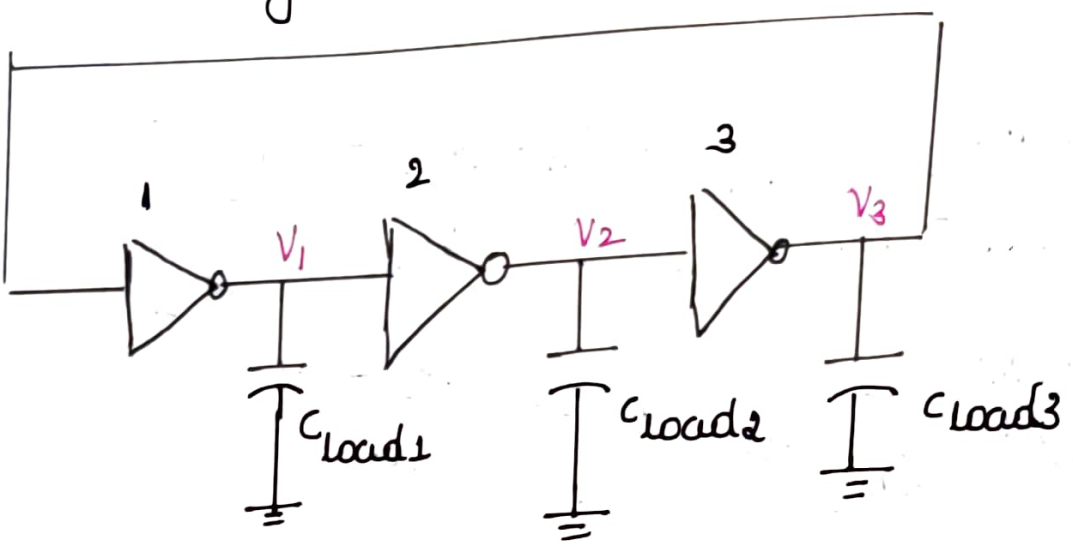
$$0.35 \times 10^{-9} = \frac{300 \times 10^{-15}}{120 \times 10^{-6} \left(\frac{W}{L}\right)_n 2.2} \left[\ln \left(\frac{3.9}{0.5} \right) - \ln \left(\frac{2.4}{2} \right) \right]$$

$$\left(\frac{W}{L}\right)_n = 6.1$$

$$V_{th} = \frac{V_{TOn} + \sqrt{\frac{1}{K_R}} \left(V_{DD} + V_{TOp} \right)}{1 + \sqrt{\frac{1}{K_R}}} = 1.5 \qquad K_R = 0.51$$

$$K_R = \frac{\mu_n C_{ox} \left(\frac{W}{L}\right)_n}{\mu_p C_{ox} \left(\frac{W}{L}\right)_p} = 0.51 \qquad \left(\frac{W}{L}\right)_p = 31$$

CMOS Ring Oscillator



→ Consider cascaded connection of three identical CMOS inverter

→ Here o/p node of 3rd inverter acts as a input node of first inverter

→ Here this configuration forms voltage feed back loop.

→ A closed loop cascaded connection of any odd no of inverter display astable behaviour.

→ ∴ circuit is called as ring Oscillator

→ "T" Oscillating period in terms of avg propagation delay is given by

$$T = \tau_{PHL1} + \tau_{PLH1} + \tau_{PHL2} + \tau_{PHH_2} + \tau_{PHL3} + \tau_{PLH3}$$

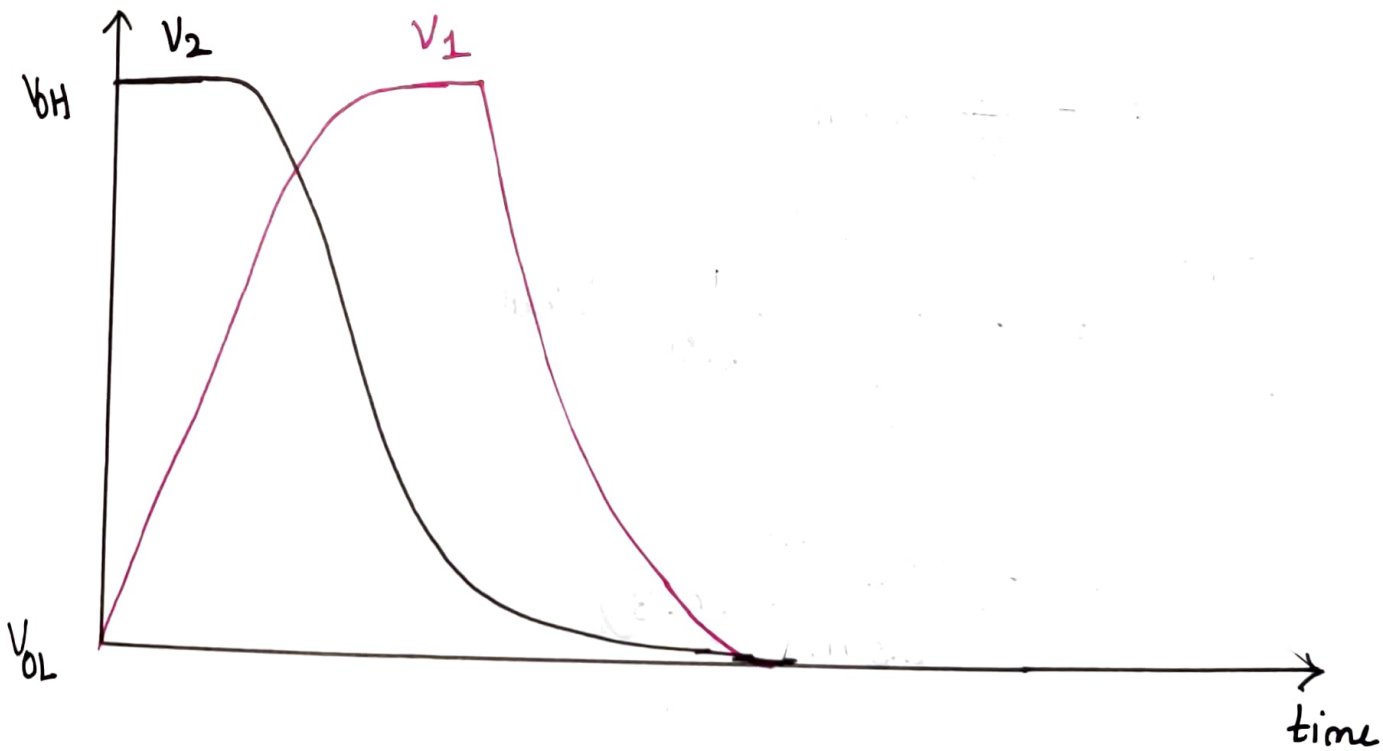
$$= 2\tau_p + 2\tau_p + 2\tau_p$$

$$= 6\tau_p$$

$$= \underline{3.2\tau_p}$$

$$\rightarrow f = \frac{1}{T} = \frac{1}{2 \times n \times \tau_p}$$

n = no of Inverter stages.



Problems 1.

1. consider a CMOS inverter with following spec

$V_{DD} = 3.3$

$V_{gs} = 3.3V$

$I_{sat} = 2mA$ If $V_{DS} > 2.5\,V$

I/p is a step input

calculate τ_{PHL}

$C_L = 300fF.$

$$dt = -\frac{C}{I_D} dV_{out}$$

$$\int_0^{t_{sat}} dt = -C \int_{3.3}^{2.5} \frac{1}{2.0} dV_{out}$$

$$= \frac{-300 \times 10^{-15}}{2.0m} (-0.8)$$

$$= 120\,ps$$

$$\int_{t_{sat}}^{t_{50}} dt = -C \int_{2.5}^{1.65} \frac{1}{I_{Linear}} dV_{out}$$

$$= -C \int_{2.5}^{1.65} \frac{1}{\frac{K_n}{2}\left[2(V_{GS}-V_T)V_{ds} - V_{ds}^2\right]} dV_{out}$$

$$= -300\times10^{-15} \int_{2.5}^{1.65} \frac{1}{\frac{K_n}{2}\left[2(3.3-0.8)V_0 - V_0^2\right]} dV_{out}$$

$$I_{sat} = \frac{K_n}{2}(V_{GS}-V_{Tn})^2$$

$$2\times10^{-3}\times2 = K_n\left[3.3-0.8\right]^2$$

$$K_n = \frac{4\times10^{-3}}{2.5^2}$$

$$= 0.64\times10^{-3}$$

$$= -300\times10^{-15} \int_{2.5}^{1.65} \frac{1}{\frac{0.64\times10^{-3}}{2}\left[5V_0 - V_0^2\right]} dV_{out}$$

$$= \frac{-300\times10^{-15}\times2}{0.64\times10^{-3}} \ln\left[\frac{V_0}{5 - V_0}\right]_{2.5}^{1.65}$$

$$= \frac{-600\times10^{-15}}{0.64\times10^{-3}} \ln\left[\frac{1.65}{5-1.65}\right] - \ln\left[\frac{2.5}{5-2.5}\right]$$

$$= 133\,ps$$

$$t_{delay} = 120 + 133 = \underline{253\ ps}$$

2) $V_{DD} = 5V$

$\tau_{fall} = ?$

$V_{out} = V_{90} = 4.5V$

$V_{out} = V_{10} = 0.5V$

$C_L = 1PF$

$\mu_n C_{ox} = 20 \frac{\mu A}{V^2}$

$\left(\frac{W}{L}\right)_n = 10$

$V_{Tn} = 1$

$$\tau = \frac{C \Delta V}{I_{avg}}$$

$$I_{avg} = \frac{1}{2}\left[I_1 + I_2 \right]$$

90%

10%

Sat

linear

Falling delay

$V_{in} = 5V$

$V_{out} = (Sat) = 4.5$

V_{out} (Linear) $= 0.5$

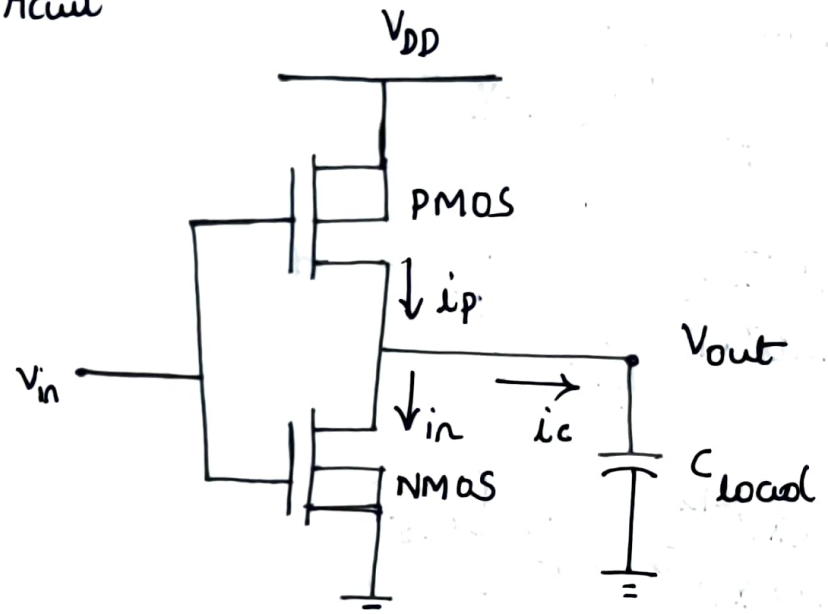
$$\frac{1}{2}\left[\frac{K_n}{2}\left[V_{in} - V_{Tn} \right]^2 + \frac{K_n}{2}\left[2(V_{in} - V_{Tn}) V_{out} - V_{out}^2 \right] \right]$$

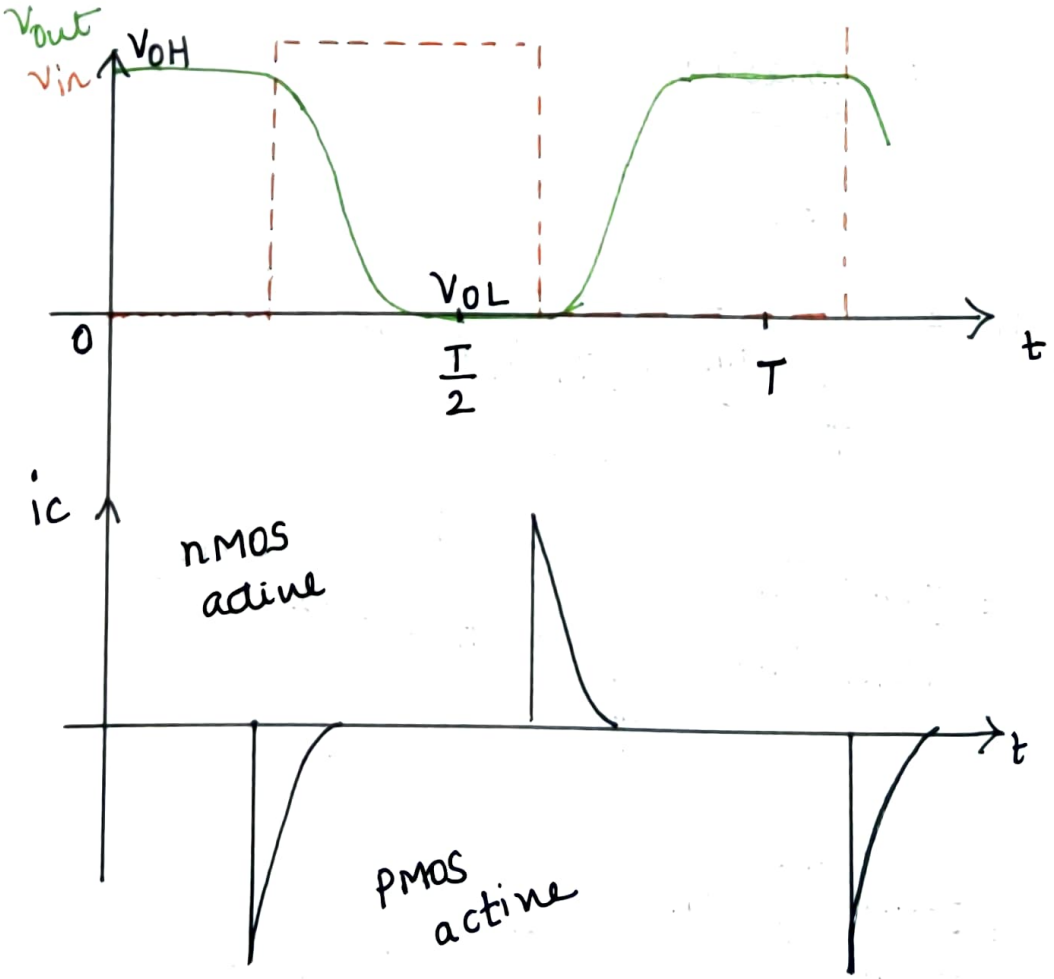
$$= \frac{1}{2}\left[\frac{1}{2} 20 \times 10^{-6} \times 10 \left[5 - 1 \right]^2 + \frac{1}{2} 20 \times 10^{-6} \times 10 \left[2(5-1)0.5 - 0.5^2 \right] \right]$$

$$= 0.9875\ mA$$

Switching power dissipation of CMOS Inverter

Circuit





→ W.K.T. Static power dissipation of CMOS inverter is negligable

→ When i/p switches from logic 0 to logic 1 or logic 1 to logic 0 CMOS inverter inevitably dissipate power

→ Typical i/p and o/p waveforms (vtg & current) shown in figure.

→ When i/p switches from low to high PMOS off
NMOS on

→ In this phase C_{load} discharges through NMOS.

→ Thus i_c = instintaneous drain current of nMOS

→ When i/p switches from high to LOW PMOS on
NMOS off

→ In this phase C_{load} charges towards V_{DD}

i_c = instintaneous drain current of PMOS.

→ Avg power dissipation of CMOS inverter is given by

$$P_{avg} = \frac{1}{T}\int_0^T v(t)\, i(t)\, dt$$

$$= \frac{1}{T}\int_0^{T/2} V_c(t)\, i_c(t)\, dt + \int_{\frac{T}{2}}^{T} v_c(t) i_c(t)\, dt$$

$0 \to \frac{T}{2}$ $\quad V_c(t) = V_{out}$

NMOS on $\quad i_c(t) = -i_n(t)$

$$= -C_{load}\frac{dV_0}{dt}$$

$\frac{T}{2} \to T$ $\quad V_c(t) = V_{DD} - V_0$

PMOS on $\quad i_c(t) = C_{load}\frac{dV_0}{dt}$

$$= \frac{1}{T}\int_0^{T/2} -C_{load} V_0 \frac{dV_0}{dt}\, dt + \int_{\frac{T}{2}}^{T} (V_{DD} - V_0)\, C_{load}\frac{dV_0}{dt}\, dt$$

$$= \frac{1}{T}\left[-\frac{C_{load}}{2} \int_0^{T/2} 2V_0 \frac{dV_0}{dt}\, dt + \int_{\frac{T}{2}}^{T} V_{DD} C_{load} \frac{dV_0}{dt}\, dt \right.$$

$$\left. + \int_{\frac{T}{2}}^{T} -\frac{C_{load}}{2} 2V_0 \frac{dV_0}{dt}\, dt \right]$$

$$= \frac{1}{T}\left[-\frac{C_{load}}{2} \int_0^{T/2} \frac{dV_0^2}{dt}\, dt + \int_{\frac{T}{2}}^{T} V_{DD} C_{load} \frac{dV_0}{dt}\, dt \right.$$

$$\left. - \frac{C_{load}}{2} \int_{\frac{T}{2}}^{T} \frac{dV_0^2}{dt^2}\, dt \right]$$

$$= \frac{1}{T}\left[\frac{-C_{load}}{2} V_0^2 \Big|_0^{T/2} + C_{load} V_{DD} V_0 \Big|_{\frac{T}{2}}^{T} - \frac{C_{load}}{2} V_0^2 \Big|_{\frac{T}{2}}^{T} \right]$$

$$= \frac{1}{T}\left[\frac{C_{load} V_{DD}^2}{2} + \left(C_{load} V_{DD}^2 - 0 \right) - \left(\frac{C_{load} V_{DD}^2}{2} - 0 \right) \right]$$

$$P = \frac{1}{T} C_{load} V_{DD}^2$$

$$\boxed{P = C_{load} V_{DD}^2 f}$$

→ Average power dissipation of CMOS inverter is Proportional to Switching frequency.

→ ∴ LOW POWER advantage of CMOS circuit is less Prominent in high speed circuits

→ P_{avg} is independent of transistor sizing.

Power delay product

→ Power delay product PDP is a fundamental param which is using for measuring quality and performanc of CMOS process.

→ PDP can be interpreted as Average energy required for gate to switch its o/p vtg from high to low o low to high

→ In CMOS energy dissipated

i) by PMOS n/w while o/p C_{load} is charging from $0 \rightarrow V_{DD}$

ii) by NMOS n/w while C_{load} is discharging from $V_{DD} \rightarrow 0$

$$PDP = \text{Power} \times \text{Delay}$$

$$= \alpha V^2 f \times T$$

$$\underline{\underline{CV^2}}$$

→ Since PDP is proportional to C_{load} & V_{DD}, both these parameters should be minimized to achieve better performance.

→ PDP can also be written as

$$PDP = 2\tau_p \cdot P_{avg}$$

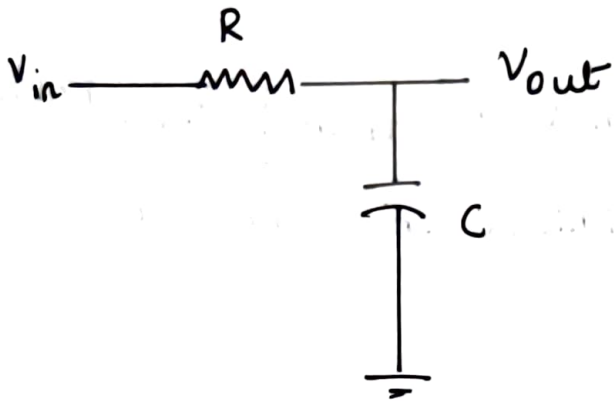
$$= \cancel{2}\left[\frac{\tau_{PHL} + \tau_{PLH}}{\cancel{2}}\right] C_{load} V_{DD}^2 f$$

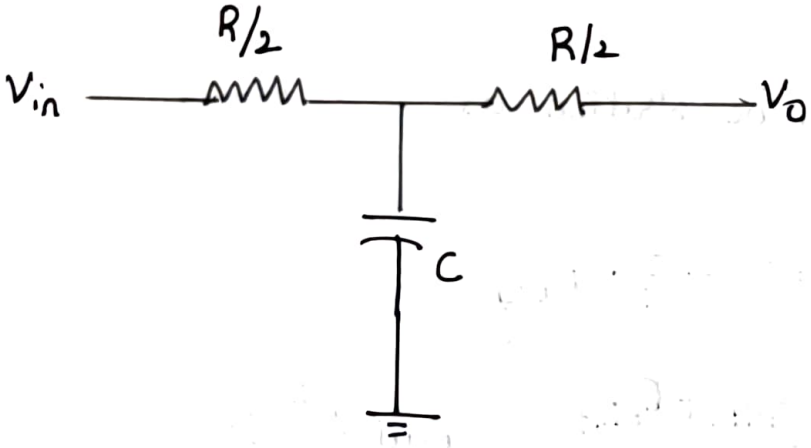
$$= (\tau_{PHL} + \tau_{PLH}) C_{load} V_{DD}^2 \frac{1}{\tau_{PHL} + \tau_{PLH}}$$

$$\underline{PDP = C_{load} V_{DD}^2}$$

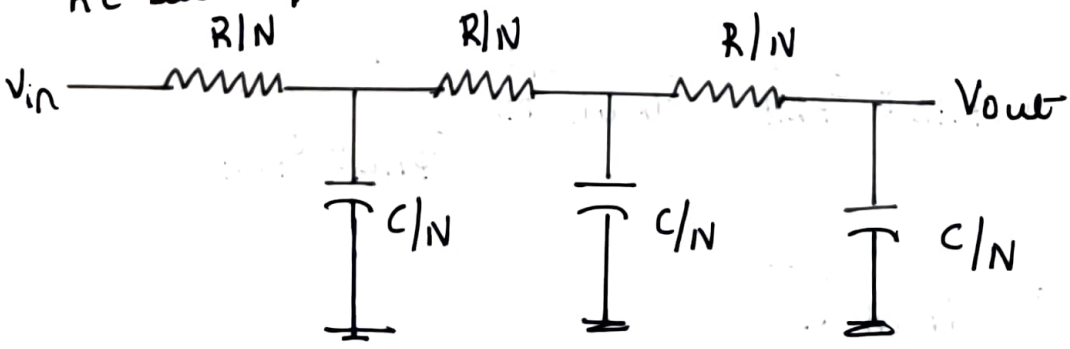
calculation of interconnection delay.

RC Delay models.





RC Ladder



→ Interconnect line could be modeled as lumped RC n/w if time of flight across the interconnection line is significantly shorter than signal rise/fall time

$$V_{out} = V_{DD}\left(1 - \exp\left(-\frac{t}{RC}\right)\right)$$

$$t = \tau_{PLH} \qquad V_{out} = V_{50\%} = \frac{V_{OH} - V_{OL}}{2} = \frac{V_{DD}}{2}$$

$$\frac{V_{DD}}{2} = V_{DD}\left[1 - e^{-\frac{\tau_{PLH}}{RC}}\right]$$

$$e^{-\frac{\tau_{PLH}}{RC}} = 0.5$$

$$-\frac{\tau_{PLH}}{RC} = -0.69$$

$$\tau_{PLH} \simeq 0.69\,RC$$

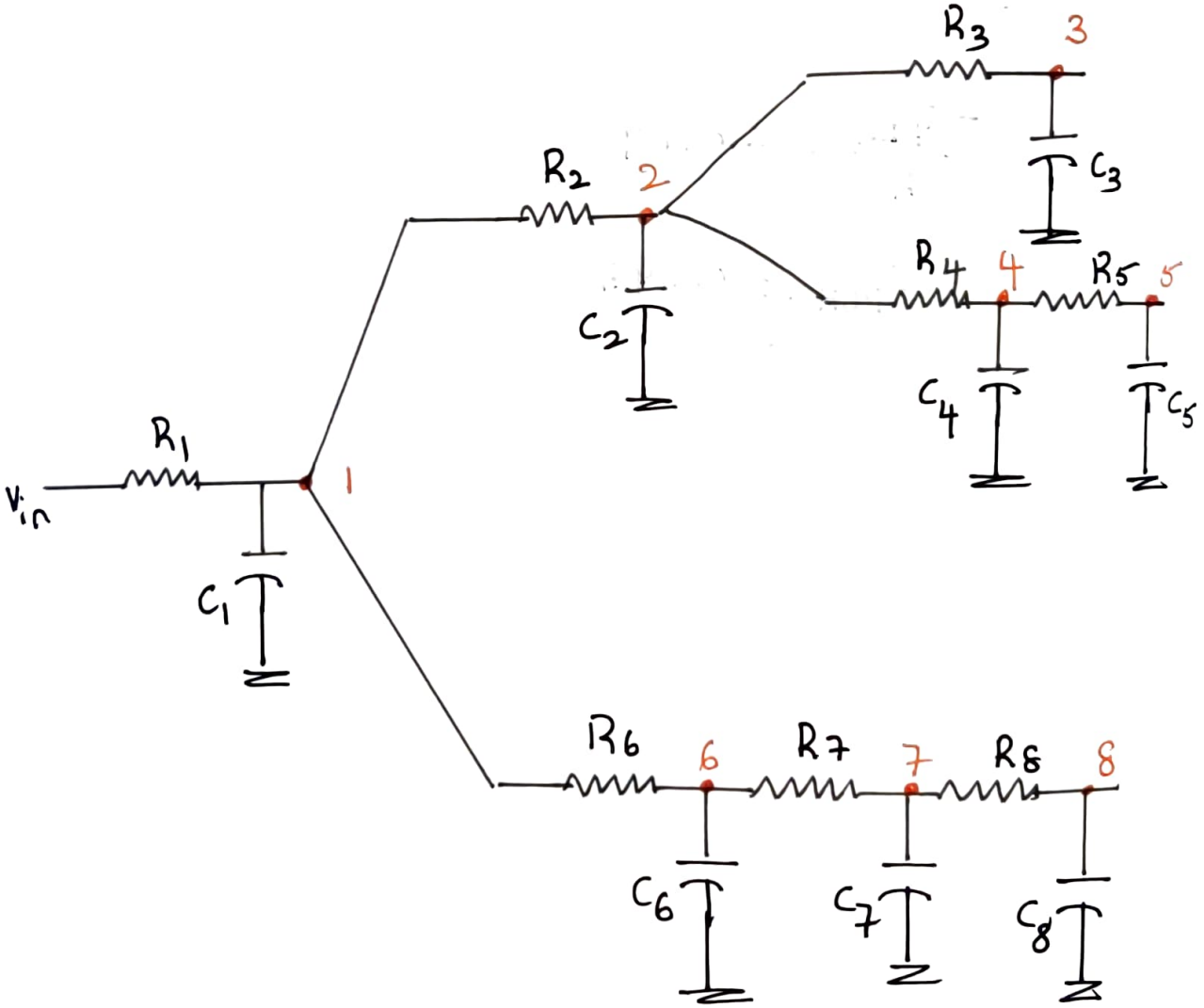
Elmore delay :-

→ Consider RC network

i There are no resistor loops in a n/w.

ii all cap are connected b/w node & ground.

iii There is only one i/p node in a circuit.



→ Let P_i is the unique path from i/p node to node i $i = 1, 2, 3 \ldots N$

→ Let $P_{ij} = P_i \cap P_j$

= common path

$$\tau_{Di} = \sum_{j=1}^{N} C_j \sum_{\text{for all } k \in P_{ij}} R_k$$

N = Total no of nodes

i = node where delay is calculated

$$\therefore \tau_{D7} = C_1R_1 + C_2R_1 + C_3R_1 + C_4R_1 + C_5R_1 + C_6(R_1+R_6) + C_7(R_1+R_6+R_7) + C_8(R_1+R_6+R_7)$$

=

@ node 5

$$\tau_{D5} = C_1R_1 + C_2(R_1+R_2) + C_3(R_1+R_2) + C_4(R_1+R_2+R_4) + C_5(R_1+R_2+R_4+R_5) + C_6R_1 + C_7R_1 + C_8R_1$$

=

④ $V_{Ton} = 0.8\ V$

$V_{Top} = -1\ V$

$\mu_n C_{ox} = 50 \frac{\mu A}{V^2}$

$\mu_p C_{ox} = 20 \frac{\mu A}{V^2}$

$V_{DD} = 5\ V$

$L_n = L_p = 1\mu m$

$C_{out} = 2\ pF$

$V_{th} = 2.2\ V$

$\tau_{rise} = 5\ ns$

$V_{OH} = V_{DD} = 5\ V$

$V_{OL} = 0$

$\tau_{rise} =$