DIGITAL VLSI DESIGN

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PES UNIVERSITY ONLINE

MOS INVERTERS: SWITCHING CHARACTERISTICS AND INTERCONNECT EFFECTS

Fabrication of MOSFETs & Circuit Design Process

Unit 3: Switching Characteristics and Interconnect Effects				
25	R1: Chap 6 (6.1 -6.7)	Introduction, Delay-Time Definitions (6.1,6.2)	19%	60%
26 – 28		Calculation of Delay Times (6.3)		
29 – 31		Calculation of Delay Times (6.4)		
31 -32		Estimation of Interconnect Parasitic (6.5)		
32 -33		Calculation of Interconnect Delay (6.6)		
34		Switching Power Dissipation of CMOS Inverters (6.7)		

Reference Books:

R1: CMOS Digital Integrated Circuits Analysis And Design, **Sung-Mo (Steve) Kang**

CMOS Switching Characteristics

we studied the

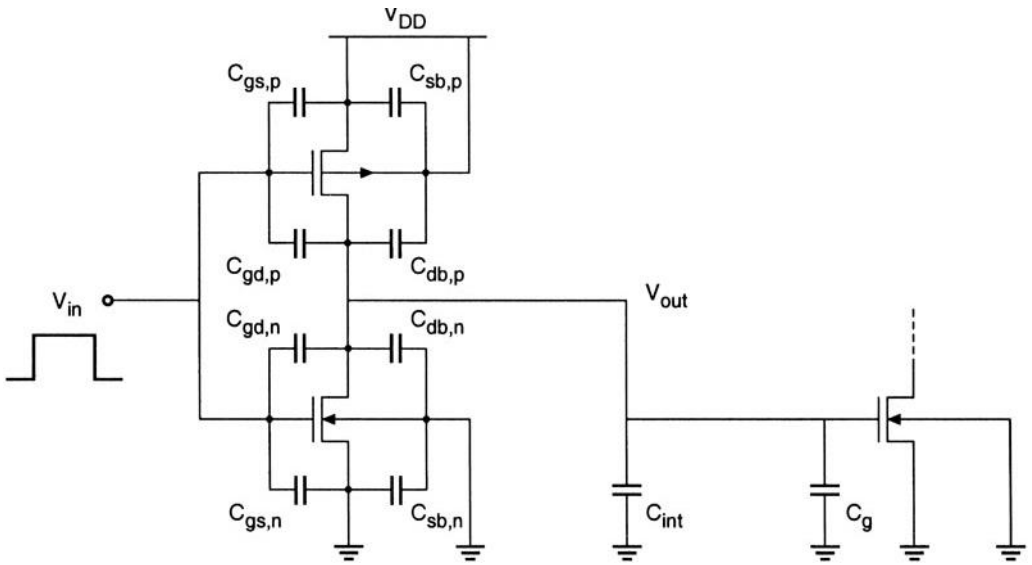
- DC (or Static) characteristics of the CMOS inverter
  - how to calculate: V_{OH}, V_{OL}, V_{IL}, V_{IH}, V_{th}, NM_L, NM_H,
  - we learned that we can modify some of these parameters using the W/L ratios of the inverter

- specifically, we say that the V_{th} is solely dependent on W/L and is usually the most important and most commonly controlled parameter

- Now we look into the Switching (or AC or Dynamic) behavior of the inverter
  - the switching characteristics give us how *fast* the circuit will run
  - when designing, we must meet both DC and AC specs

CMOS Switching Characteristics

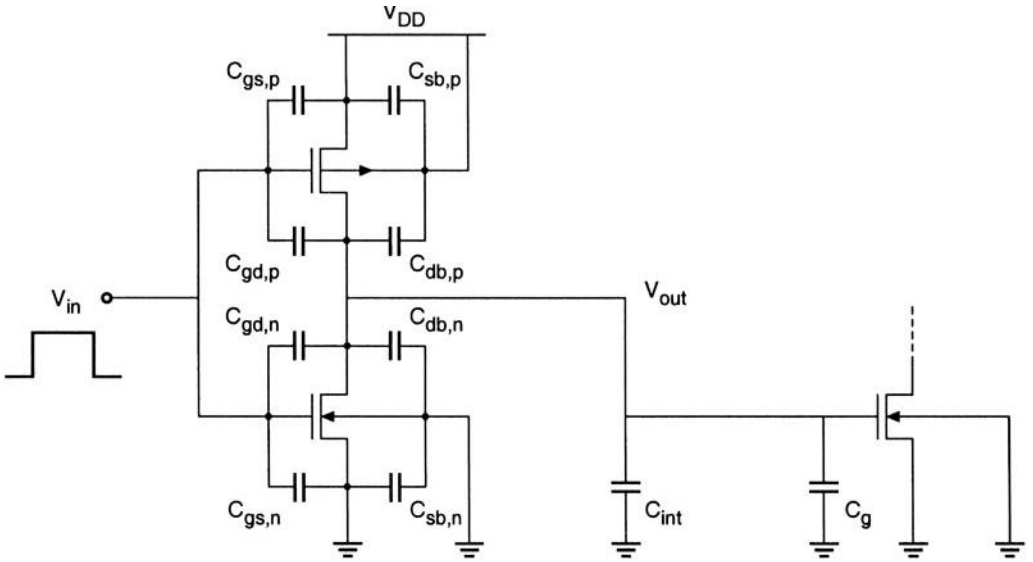
- In an AC analysis, we need to consider the capacitance in the circuit
- we consider an inverter that is driving another CMOS device or multiple CMOS devices in parallel



CMOS Switching Characteristics

there are 4 main groups of capacitance in the circuit

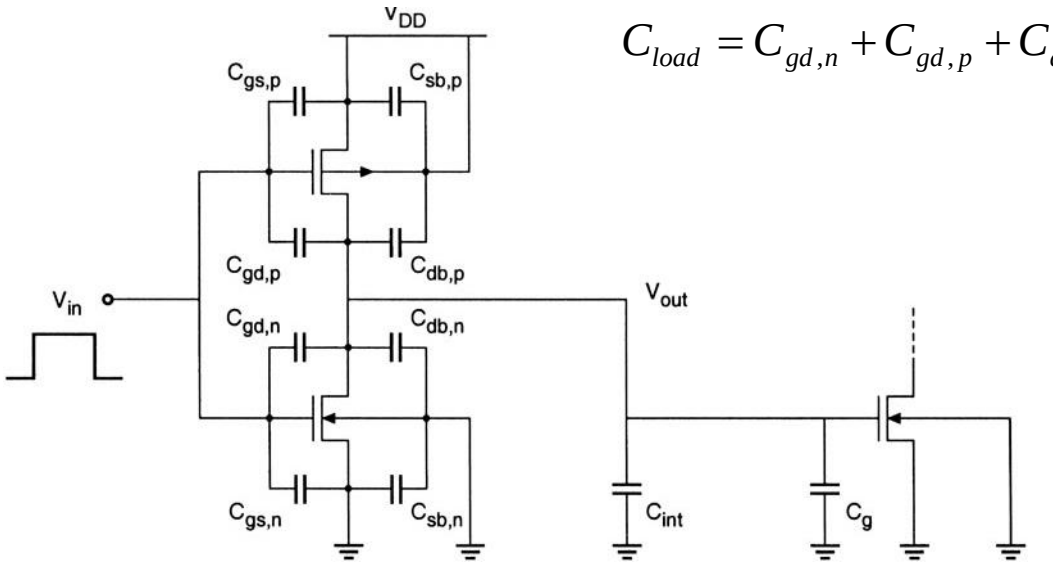
1) Driver's Oxide Capacitance
2) Driver's Junction Capacitance
3) Interconnect Capacitance
4) Receiver Oxide Capacitance



CMOS Switching Characteristics

- We know that all of these capacitances vary as the dimensions of the inverter are altered and for various interconnect configurations

- In order to get a feel for how the capacitance effects performance, we assume that we can *lump* all of the capacitances into a fixed load capacitance (C_{load})



$$C_{load} = C_{gd,n} + C_{gd,p} + C_{db,n} + C_{db,p} + C_{\text{int}} + C_g$$

CMOS Switching Characteristics

- In this expression some of the capacitances are eliminate :

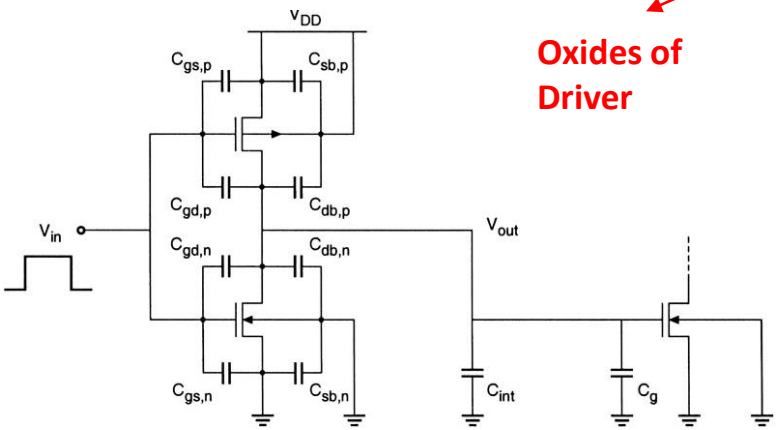
  $C_{sb,n}$, $C_{sb,p}$: There is no voltage change from $V_{sb,n}$ or $V_{sb,p}$ so there is no net capacitance

  $C_{gs,n}$, $C_{gs,p}$: Since these are connected between V_{in} and V_{DD}/$V_{SS,}$ the *input* drives these capacitances. It is not part of the capacitance that the device *output* drives.

- The expression does include the interconnect and gate capacitance of the circuits that this inverter is driving

$$C_{load} = C_{gd,n} + C_{gd,p} + C_{db,n} + C_{db,p} + C_{\text{int}} + C_g$$

Oxides of Driver | **Junctions of Driver** | **Interconnect** | **Oxide of Receiver**

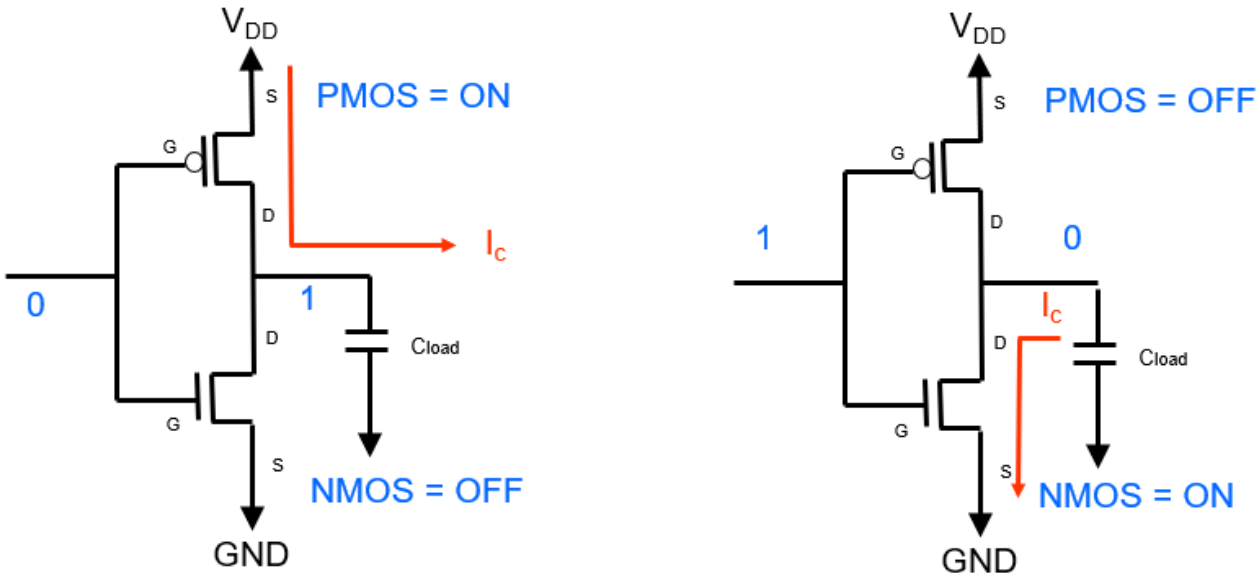


CMOS Switching Characteristics

- **CMOS Switching Characteristics**

  - the speed of the device describes how fast we can charge or discharge the load capacitor

$$i_C = C\frac{dV}{dt}$$



CMOS Switching Characteristics

- Delay Time Definition

τ_{PHL} ---- determines the input to output signal delay during the high to low transitions of the output

τ_{PLH} ---- determines the input to output signal delay during the Low to high transitions of the output

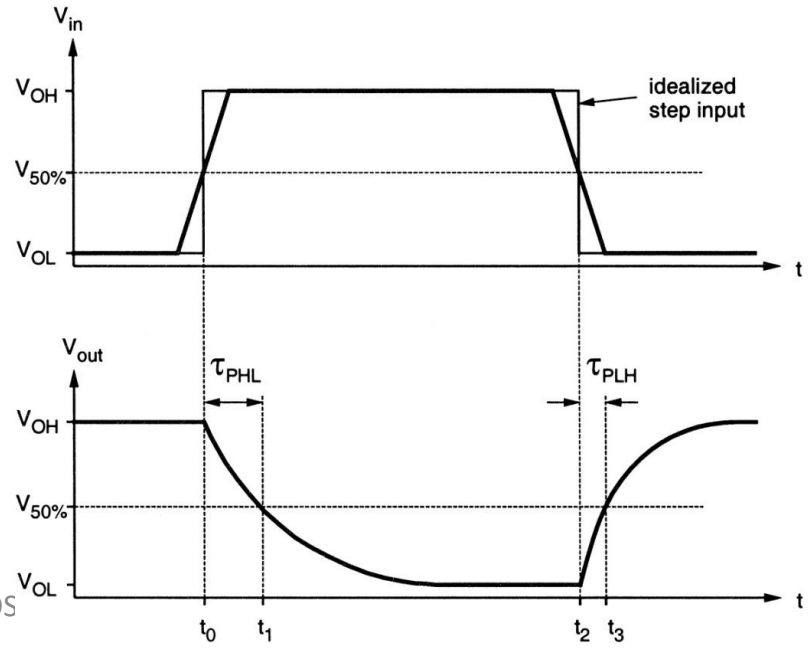
CMOS Switching Characteristics

Delay Time Definition

τ_{PHL} is the time delay between the $V_{50\%}$ transition of the rising input voltage and the $V_{50\%}$ transition of the falling output voltage.

τ_{PLH} is defined as the time delay between the $V_{50\%}$ transition of the falling input voltage and the $V_{50\%}$ transition of the rising output voltage

To simply the analysis and the derivation of delay expressions, the input voltage waveforms is usually assumed to be an ideal step pulse with zero rise and fall time.



CMOS Switching Characteristics

• Delay Time Definition

Under this assumption

- τPHL becomes the time required for the output voltage to fall from VOH to the V50% level and
- τPLH becomes the time required for the output voltage to rise from VOL to the V50% level,

- $V_{50\%} = V_{OL} + \frac{1}{2}\cdot(V_{OH} - V_{OL}) = \frac{1}{2}\cdot(V_{OH} + V_{OL})$

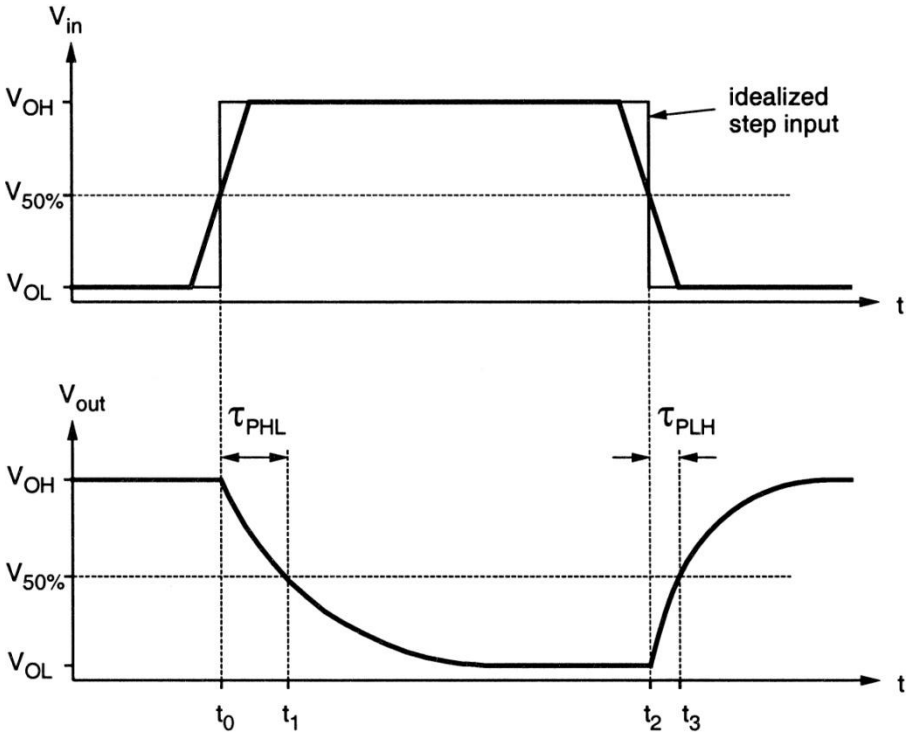
$$\tau_{PHL} = t_1 - t_0$$

$$\tau_{PLH} = t_3 - t_2$$

- Note that in CMOS:

$V_{OH}=V_{DD}$
V_{OL}= gnd

So $V_{50\%}=V_{DD}/2$



CMOS Switching Characteristics

- The average propagation delay τp of the inverter characterizes the average time required for the input signal to propagate through the inverter.

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2}$$

CMOS Switching Characteristics

fig6.4 refer, for the definition of output rise and fall times.

The rise time τ rise is defined here as

the time required for the output voltage to rise from the V10% level to V90% level.

The fall time τ fall is defined here as

the time required for the output voltage to drop from the V90% level to V10% level.

The voltage levels V10% and V90% are defined as

$$V_{10\%} = V_{OL} + 0.1 \cdot (V_{OH} - V_{OL})$$
$$V_{90\%} = V_{OL} + 0.9 \cdot (V_{OH} - V_{OL})$$

Thus, the output rise and fall times are found from Fig. 6.4 as follows

$$\tau_{fall} = t_B - t_A$$
$$\tau_{rise} = t_D - t_C$$

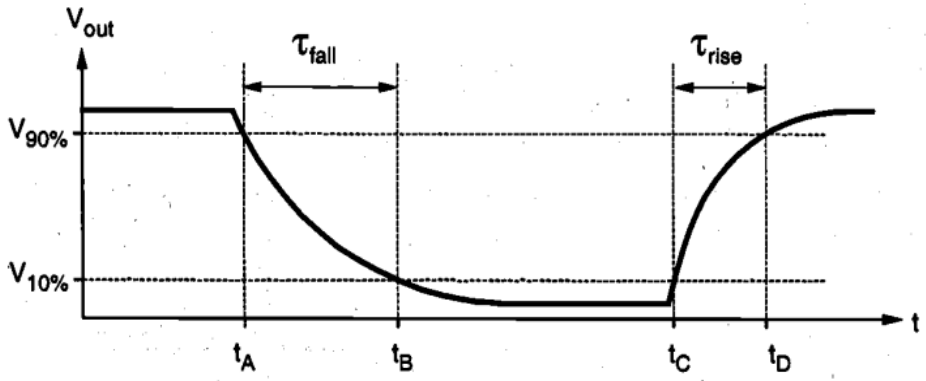


Figure 6.4. Output voltage rise and fall times.

CMOS Switching Characteristics

Calculation of Delay Times

- The simplest approach for calculating the propagation delay times τPHL and τPLH is based on estimating the average capacitance current during charge down and charge up respectively.
- If the capacitance current during an output transition is approximated by a constant average current I_{avg}, the delay times are found as

$$\tau_{PHL} = \frac{C_{load} \cdot \Delta V_{HL}}{I_{avg\,HL}} = \frac{C_{load}\,(V_{OH} - V_{50\%})}{I_{avg\,HL}}$$

$$I_{avg\,HL} = \frac{1}{2}\left[I_{C}\,(V_{in} = V_{OH},\ V_{out} = V_{OH}) + I_{C}(V_{in} = V_{OH},\ V_{out} = V_{50\%}) \right]$$

(Sat) (linear)

CMOS Switching Characteristics

$$t_{pLH} = \frac{C_{load}\,\Delta V_{LH}}{I_{avgLH}} = \frac{C_{load}\,(V_{OL} - V_{50\%})}{I_{avg\,LH}}$$

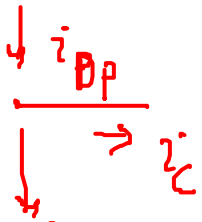
$$I_{avg_{LH}} = \frac{1}{2}\left[i_c(V_{in} = V_{OL},\ V_{Out} = V_{OL}) + i_c\,(V_{in} = V_{OL},\ V_{out} = V_{50\%}) \right.$$

CMOS Switching Characteristics

Calculation of Delay Times

- While the average current method is relatively simple and requires minimal calculation , it neglects the variations of the capacitance current between the beginning and end points of the transition.
- Average current method will not provide a very accurate estimate of the delay times.
- The delay times can be found more accurately solved by using state equation of the output node in the time domain.
- The differential equation associated with the output node is given below

$$C_{load}\frac{dV_{out}}{dt} = i_C = I_{Dp} - I_{Dn}$$



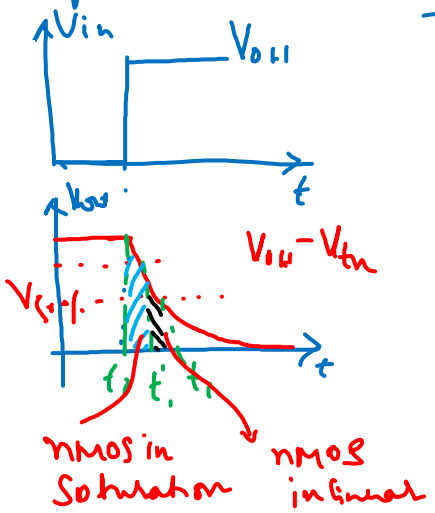
Consider V_{in} changes from low-to-high

$i_{Dp} = 0, \Rightarrow$ $C_{load}\frac{dV_{out}}{dt} = -I_{Dn}$

CMOS Switching Characteristics

Calculation of Delay Times

The input and output voltage waveforms during the hi to low transition is illustrated in fig below



→ When nMOS starts conducting, initially it will be in saturation region

→ When Vout falls below VOH − Vtn, nMOS starts conducting in linear region

→ First consider nMOS in saturation

$$I_{Dn} = \frac{k_n}{2}(V_{OH} - V_{tn})^2$$

$$C_{load}\frac{dV_{out}}{dt} = -I_{Dn}$$

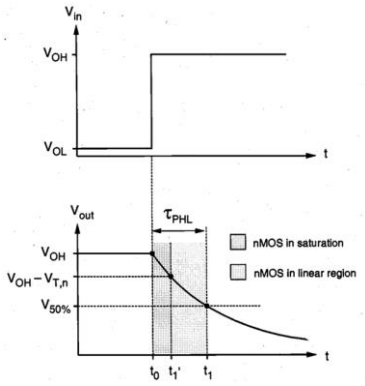
$$\int_{t_0}^{t_1} dt = -C_{load}\int_{V_{OH}}^{V_{OH}-V_{tn}} \left(\frac{1}{I_{Dn}}\right) dt$$

$$t_1' - t_0 = \frac{2C_{load}V_{tn}}{k_n(V_{OH}-V_{tn})}$$

At $t = t_1'$, the o/p voltage will be $V_{OH} - V_{tn}$ & transistor will be at the saturation–linear boundary

→ Now nMOS is in linear region with

$$I_{Dn} = \frac{k_n}{2}\left[2(V_{OH}-V_{tn})V_{out} - V_{out}^2\right]$$



CMOS Switching Characteristics

Calculation of Delay Times

$$\int_{t_1}^{t_1'} dt = -C_{load} \int_{V_{OH}-V_{tn}}^{V_{50\%}} \left(\frac{1}{I_{Dn}}\right) dV_{out}$$

$$= \frac{-2C_{load}}{k_n} \int_{V_{OH}-V_{tn}}^{V_{50\%}} \frac{dV_{out}}{2(V_{OH}-V_{tn})V_{out} - V_{out}^2}$$

$$t_1' - t_1 = \frac{2C_{load}}{k_n} \cdot \frac{1}{2(V_{OH}-V_{tn})} \ln\left(\frac{V_{out}}{2(V_{OH}-V_{tn}) - V_{out}}\right)\Bigg|_{V_{OH}-V_{tn}}^{V_{50\%}}$$

$$= \frac{C_{load}}{k_n 2(V_{OH}-V_{tn})} \ln\left(\frac{2(V_{OH}-V_{tn}) - V_{50\%}}{V_{50\%}}\right)$$

$$\tau_{pHL} = \frac{C_{load}}{k_n 2(V_{OH}-V_{tn})} \left[\frac{2V_{tn}}{(V_{OH}-V_{tn})} + \ln\left(\frac{2(V_{OH}-V_{tn}) - V_{50\%}}{V_{50\%}}\right)\right]$$

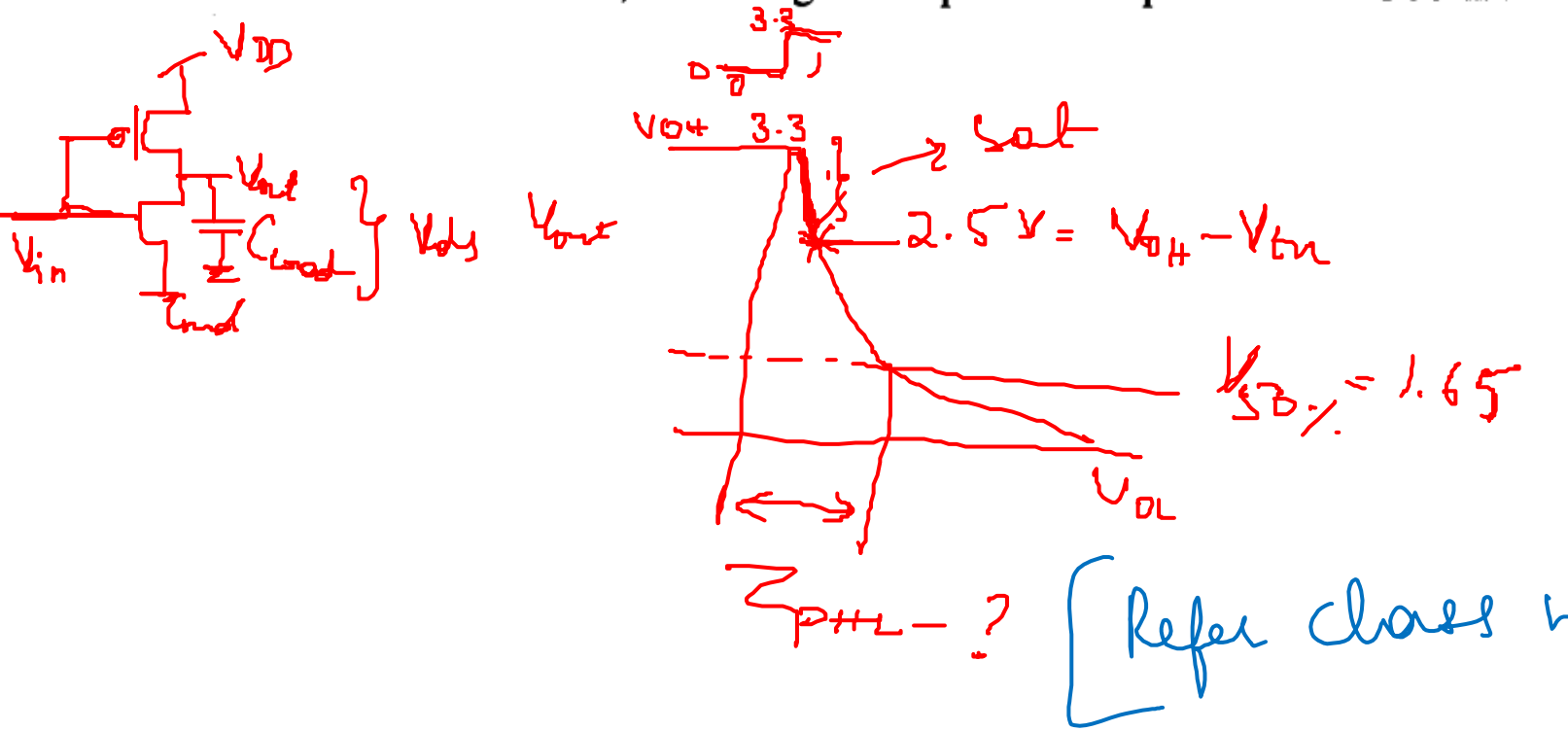
Sub $V_{OH} = V_{DD}$, $V_{OL} = 0$

$$\tau_{pHL} = \frac{C_{load}}{k_n(V_{DD}-V_{tn})} \left[\frac{2V_{tn}}{V_{DD}-V_{tn}} + \ln\left(4\left(\frac{V_{DD}-V_{tn}}{V_{OH}+V_{OL}}\right) - 1\right)\right]$$

CMOS Switching Characteristics

Example 6.1.

Consider the CMOS inverter circuit shown in Fig. 6.2, with V_{DD} = 3.3 V. The *I-V* characteristics of the nMOS transistor are specified as follows: when V_{GS} = 3.3 V, the drain current reaches its saturation level I_{sat} = 2 mA for $V_{DS} \geq 2.5$ V. Assume that the input signal applied to the gate is a step pulse that switches instantaneously from 0 V to 3.3 V. Using the data above, calculate the delay time necessary for the output to fall from its initial value of 3.3 V to 1.65 V, assuming an output load capacitance of 300 fF.



CMOS Switching Characteristics

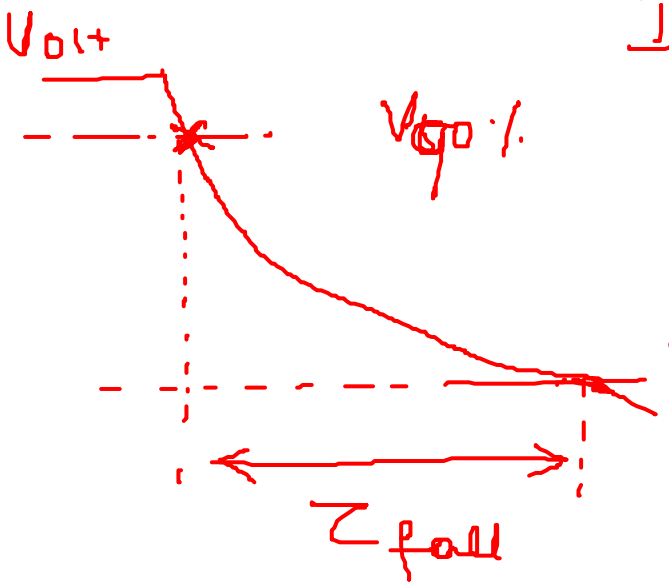
Example 6.2.

For the CMOS inverter shown in Fig. 6.2 with a power supply voltage of $V_{DD} = 5$ V, determine the fall time τ_{fall}, which is defined as the time elapsed between the time point at which $V_{out} = V_{90\%} = 4.5$ V and the time point at which $V_{out} = V_{10\%} = 0.5$ V. Use both the average-current method and the differential equation method for calculating τ_{fall}. The output load capacitance is 1 pF. The nMOS transistor parameters are given as

$\mu_n C_{ox} = 20\ \mu A/V^2$
$(W/L)_n = 10$
$V_{T,n} = 1.0$ V

[Refer Class work]

Average current method



$$I_{avg} = \frac{1}{2}\left[I_C(V_{in}=5V, V_{out}=V_{90\%}) + I_C(V_{in}=5V, V_{out}=V_{10\%}) \right]$$

$$= \frac{1}{2}\left[\frac{1}{2}k_n(V_{in}-V_{tn})^2 + \frac{1}{2}k_n\left[2(V_{in}-V_{tn})V_{out} - V_{out}^2\right] \right]$$

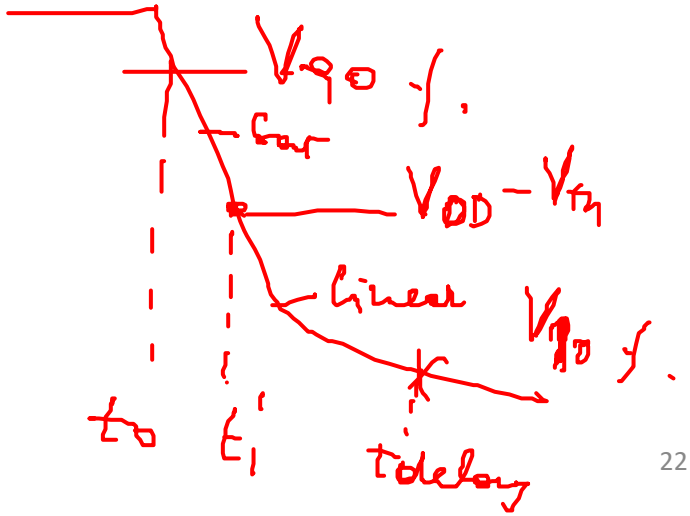
$\rightarrow \approx 0.98$ mA

CMOS Switching Characteristics

$$t_{fall} = \frac{C_{load}\left(V_{90\%} - V_{10\%}\right)}{I_{avg}}$$

$$= \frac{1 \times 10^{-12}\left(4.5 - 0.5\right)}{0.98m}$$

$$= 4.05ns$$



CMOS Switching Characteristics

- In a CMOS inverter, the charge-up event of the output load capacitance for falling input transition is completely analogous to the charge-down event for rising input.
- When the input voltage switches from high (VOH) to low (VOL)' the nMOS transistor is cut off, and the load capacitance is being charged up through the pMOS transistor.
- Following a very similar derivation procedure, the propagation delay time τPLH can be found as

$$\tau_{PLH} = \frac{C_{load}}{k_p\left(V_{OH} - V_{OL} - |V_{T,p}|\right)}\left[\frac{2|V_{T,p}|}{V_{OH} - V_{OL} - |V_{T,p}|} + \ln\left(\frac{2\left(V_{OH} - V_{OL} - |V_{T,p}|\right)}{V_{OH} - V_{50\%}} - 1\right)\right]$$

For $V_{OH} = V_{DD}$ and $V_{OL} = 0$, (6.23a) becomes

$$\tau_{PLH} = \frac{C_{load}}{k_p\left(V_{DD} - |V_{T,p}|\right)}\left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln\left(\frac{4\left(V_{DD} - |V_{T,p}|\right)}{V_{DD}} - 1\right)\right]$$

$$\tau_{PHL} = \frac{C_{load}}{k_n\left(V_{DD} - V_{T,n}\right)}\left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln\left(\frac{4\left(V_{DD} - V_{T,n}\right)}{V_{DD}} - 1\right)\right]$$

Comparing the delay expression PHL and PLH, we can see that the sufficient conditions for balanced propagation delays, i.e., for τPHL = τ PLH in a CMOS inverter are:

$$V_{T,n} = |V_{T,p}| \quad \text{and}$$

$$k_n = k_p \quad (\text{or } W_p/W_n = \mu_p/\mu_n)$$

CMOS Switching Characteristics

- All of the delay time derivations in this section were made under the simplifying assumption that the input signal waveform is a step pulse with zero rise and fall times.
- Now, consider the case where the input voltage waveform is not an ideal pulse waveform, has finite rise and fall times τ_r and τ_f .
- The exact calculation of the output voltage delay times is more complicated under this more realistic assumption.
- To simplify the estimation of the actual propagation delay times calculated under the step-input assumption, using the following empirical expression:

$$\tau_{PHL}(actual) = \sqrt{\tau_{PHL}^2(step\ input) + \left(\frac{\tau_r}{2}\right)^2}$$

$$\tau_{PLH}(actual) = \sqrt{\tau_{PLH}^2(step\ input) + \left(\frac{\tau_f}{2}\right)^2}$$

Inverter Design with delay constraints

- Timing specifications is one of the most fundamental issues in digital circuits design which ultimately determine the overall performance of complex circuits.
- The delay constraints should be considered together with other design constraints such as noise margin, logic switching threshold, silicon area and power dissipation.
- Thus, the design process usually involves the balancing of mostly conflicting requirements for optimum overall performance.
- The goal is to determine the channel dimensions (Wn, Wp) of nMOS and pMOS transistor which satisfy certain timing requirements.
- The load capacitance C_{load} consists of
  - Intrinsic components (parasitic drain capacitance which depends on transistor dimension) and
  - Extrinsic components (interconnect / wiring capacitance and fanout capacitances which are independent of transistor dimensions of the inverter under consideration

Inverter Design with delay constraints

- If C_{load} mainly consists of extrinsic components and if this overall load capacitance can be estimated accurately and independently of the transistor dimensions, then the problems of inverter design can be reduced to a straight forward as in case of previous calculation.
- (W/L) of nMOS to satisfy a given target value of high-to-low propagation delay can be found as

$$\tau_{PHL} = \frac{C_{load}}{k_n\left(V_{DD} - V_{T,n}\right)}\left[\frac{2\,V_{T,n}}{V_{DD} - V_{T,n}} + \ln\left(\frac{4\left(V_{DD} - V_{T,n}\right)}{V_{DD}} - 1\right)\right]$$

$$\left(\frac{W_n}{L_n}\right) = \frac{C_{load}}{\tau^*_{PHL}\,\mu_n\,C_{ox}\left(V_{DD} - V_{T,n}\right)}\left[\frac{2\,V_{T,n}}{V_{DD} - V_{T,n}} + \ln\left(\frac{4\left(V_{DD} - V_{T,n}\right)}{V_{DD}} - 1\right)\right]$$

Inverter Design with delay constraints

- (W/L) of pMOS to satisfy a given target value of Low to high propagation delay can be found as

$$\tau_{PLH} = \frac{C_{load}}{k_p\left(V_{DD} - |V_{T,p}|\right)}\left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln\left(\frac{4\left(V_{DD} - |V_{T,p}|\right)}{V_{DD}} - 1\right)\right]$$

$$\left(\frac{W_p}{L_p}\right) = \frac{C_{load}}{\tau^*_{PLH}\,\mu_p\,C_{ox}\left(V_{DD} - |V_{T,p}|\right)}\left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln\left(\frac{4\left(V_{DD} - |V_{T,p}|\right)}{V_{DD}} - 1\right)\right]$$

Inverter Design with delay constraints

A company in Urbana, IL called Prairie Technology has access to a CMOS fabrication process with the device parameters listed below.

$\mu_n C_{ox} = 120\ \mu A/V^2$
$\mu_p C_{ox} = 60\ \mu A/V^2$
$L = 0.6\ \mu m$ for both nMOS and pMOS devices
$V_{T0,n} = 0.8\ V$
$V_{T0,p} = -1.0\ V$
$W_{min} = 1.2\ \mu m$

Design a CMOS inverter by determining the channel widths W_n and W_p of the nMOS and pMOS transistors, to meet the following performance specifications.

- $V_{th} = 1.5$ V for $V_{DD} = 3$ V,
- Propagation delay times $\tau^*_{PHL} \leq 0.2$ ns and $\tau^*_{PLH} \leq 0.15$ ns,
- A falling delay of 0.35 ns for an output transition from 2 V to 0.5 V, assuming a combined output load capacitance of 300fF and ideal step input.

Refer class work

CMOS Ring Oscillator Circuit

- Consider the cascade connection of three identical CMOS inverters, as shown in Fig. 6.9, where the output node of the third inverter is connected to the input node of the first inverter.

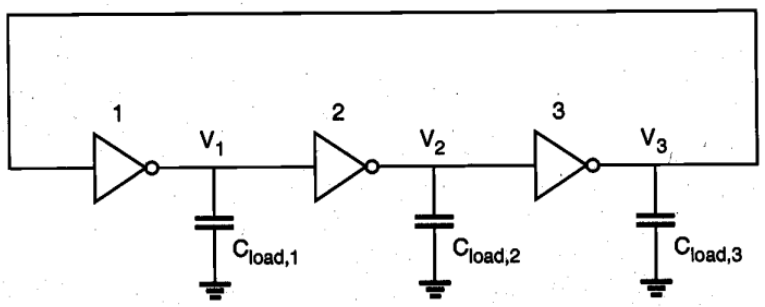


Figure 6.9. Three-stage ring oscillator circuit consisting of identical inverters.

this example will provide us with a simple demonstration of astable behavior in digital circuits

- The three inverters form a voltage feedback loop
- It can be found by simple inspection that this circuit does not have a stable operating point.
- The only DC operating point, at which the input and output voltages of all inverters are equal to the logic threshold Vth, is inherently unstable in the sense that any disturbance in node voltages would make the circuit drift away from the DC operating point.

CMOS Ring Oscillator Circuit

- In fact, a closed loop cascade connection of any odd number of inverters will display astable behavior.
- i.e., such a circuit will oscillate once any of the inverter input or output voltages deviate from the unstable operating point, Vth.
- Therefore, the circuit is called a ring oscillator.

CMOS Ring Oscillator Circuit

$T = \tau_{pHL_1} + \tau_{pLH_1} + \tau_{pHL_2} + \tau_{pLH_2} + \tau_{pHL_3} + \tau_{pLH_3}$

The propagation delay of inverter is given by

$$\tau_p = \frac{\tau_{pHL} + \tau_{pLH}}{2} \Rightarrow 2\tau_p = \tau_{pHL} + \tau_{pLH}$$

$T = 2\tau_p + 2\tau_p + 2\tau_p$ [Since all inverters are identical so τ_p is same for all]

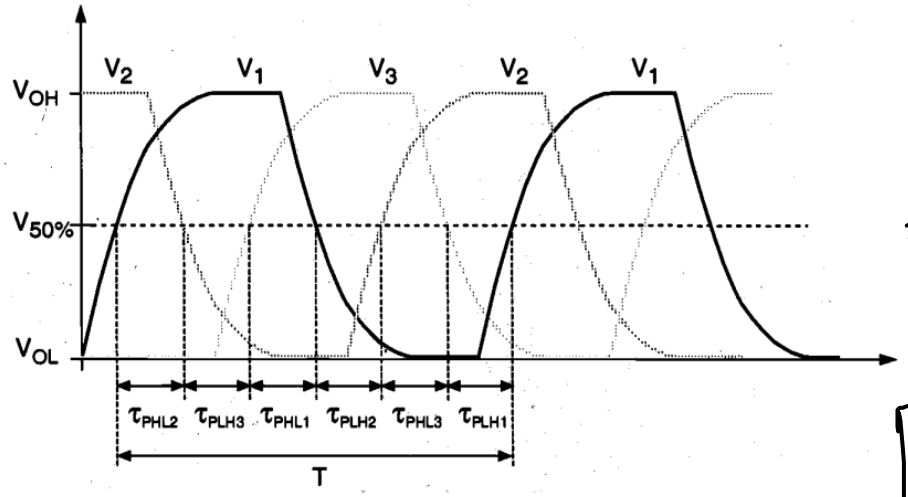


Figure 6.10. Typical voltage waveforms of the three inverters shown in Fig. 6.9.

$T = 2\ 3\tau_p$

$T = 2.n\tau_p$

where n = no of inverters

$$f = \frac{1}{T} = \frac{1}{2n\tau_p}$$

Estimation of interconnect parasitics

- The conventional delay estimation approaches seek to classify three main components of the output load; all of which are assumed to be purely capacitive as
    1. Internal parasitic capacitance
    2. Interconnect (line) capacitances
    3. Input capacitance of the fan-out gates

- The load capacitance imposed by the interconnection lines present serious problems, especially in submicron circuits.

Estimation of interconnect parasitics

- Fig shows a simple situation when an inverter is driving three other inverters, linked by interconnection line of different length and geometry
- Each interconnection line ---Lumped capacitance
- Then the total load seen by the primary inverter is simply the sum of all capacitive components
- Has a non-negligible resistance in addition to its capacitance making the interconnect a true transmission line.

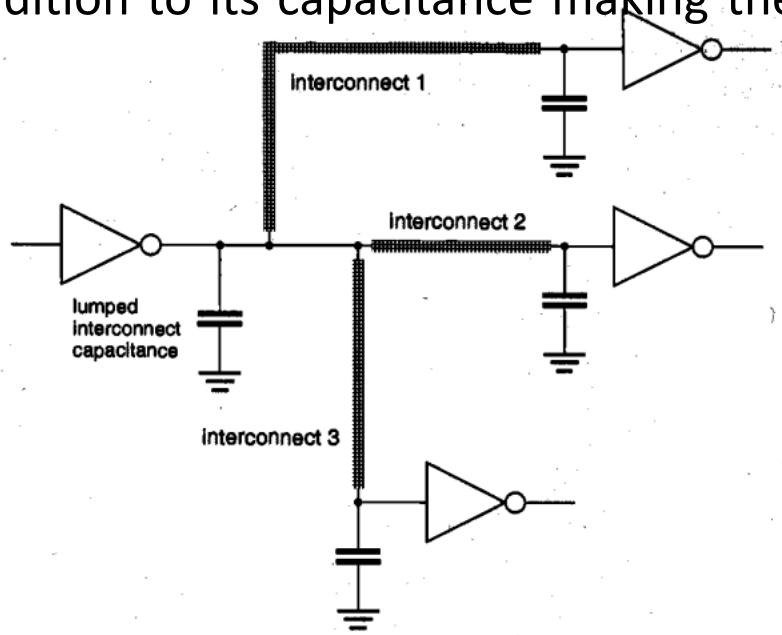


Figure 6.11. An inverter driving three other inverters over interconnection lines.

Estimation of interconnect parasitics

Interconnect Modeling

- we choose the appropriate model based on the rise/fall time of the driver relative to the *prop delay* of the interconnect

- the *prop delay* (t_{prop}) is the time it takes for the wave to travel down the length of the interconnect:

- the velocity of a wave in a dielectric is given by:

$$v = \frac{c}{\varepsilon_r}$$

- the *prop delay* can then be given by:

$$t_{prop} = \frac{length}{v}$$

Estimation of interconnect parasitics

- In realistic conditions, the interconnection line is in very close proximity to a number of other lines, either on the same level or different level
- The capacitive / inductive coupling and the signal interference between neighboring lines should be taken into account for an accurate estimation of delays.
- If the time of flight across the interconnection line (as determined by the speed of light) is much shorter than the rise /fall time then the wire can be modeled as a lumped or capacitive load or distributed RC network.
- Else i.e., time of flight across the interconnect line is longer then the rise or fall time -→ inductance also becomes importance and the interconnection line must be modeled as transmission lines.
- Thumb rule

$$\tau_{rise}\left(\tau_{fall}\right) < 2.5 \times \left(\frac{l}{v}\right) \Rightarrow \{\text{transmission} - \text{line modeling}\}$$

$$2.5 \times \left(\frac{l}{v}\right) < \tau_{rise}\left(\tau_{fall}\right) < 5 \times \left(\frac{l}{v}\right) \Rightarrow \begin{Bmatrix}\text{either transmission} - \text{line} \\ \text{or lumped modeling}\end{Bmatrix}$$

$$\tau_{rise}\left(\tau_{fall}\right) > 5 \times \left(\frac{l}{v}\right) \Rightarrow \{\text{lumped modeling}\}$$

Estimation of interconnect parasitics

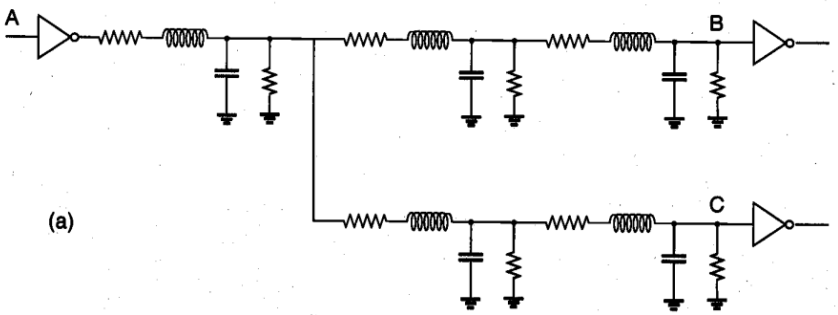
- Thumb rule

$$\tau_{rise}\left(\tau_{fall}\right) < 2.5 \times \left(\frac{l}{v}\right) \quad \Rightarrow \quad \{\text{transmission} - \text{line modeling}\}$$

$$2.5 \times \left(\frac{l}{v}\right) < \tau_{rise}\left(\tau_{fall}\right) < 5 \times \left(\frac{l}{v}\right) \quad \Rightarrow \quad \begin{Bmatrix}\text{either transmission} - \text{line} \\ \text{or lumped modeling}\end{Bmatrix}$$

$$\tau_{rise}\left(\tau_{fall}\right) > 5 \times \left(\frac{l}{v}\right) \quad \Rightarrow \quad \{\text{lumped modeling}\}$$

Estimation of interconnect parasitics



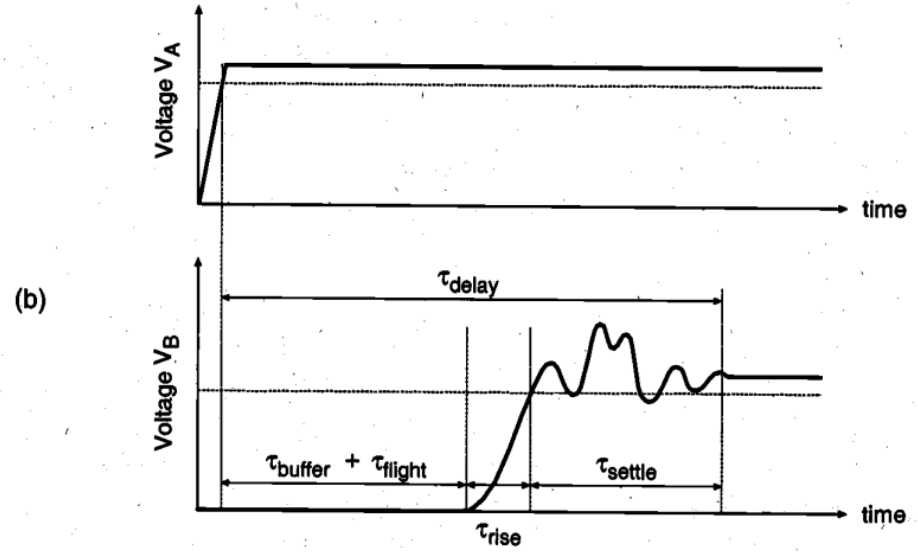


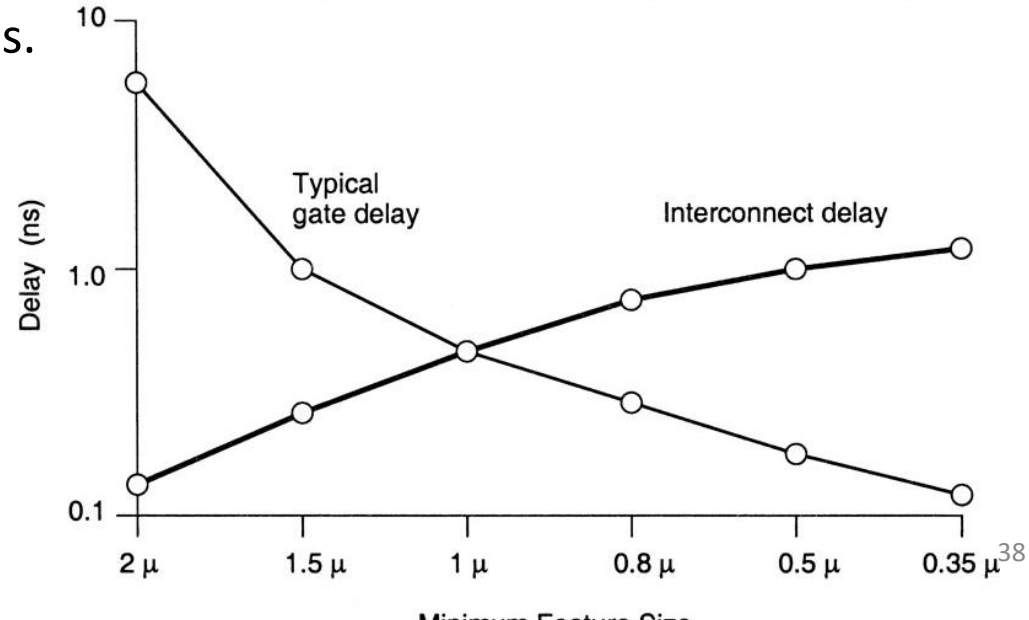
Figure 6.12. (a) An RLCG interconnection tree. (b) Typical signal waveforms at the nodes A and B, showing the signal delay and the various delay components.

Estimation of interconnect parasitics

- Fig shows typical intrinsic gate delay and interconnect delay are plotted qualitatively for different technologies
- Submicron technologies --→ the interconnect delay starts to dominate the gate delay.
- to deal with the implications and to optimize a system for speed, chip designer must have reliable and efficient means for

i. estimating the interconnect parasitic in a large chip and

ii. Simulating the transient effects.



Estimation of interconnect parasitics

- Fig 6,14 shows the typical statistical distribution of wire lengths on a chip, normalized for the chip diagonal length.
- The distribution plot clearly exhibits two distinct peaks, one for the relatively shorter intra-module connections,
- And the other for the longer inter-module connections.
- Small number of interconnections may be long
- Typically used for global signal bus connection and for clk distribution
- Long interconnections are usually the most problematic ones.

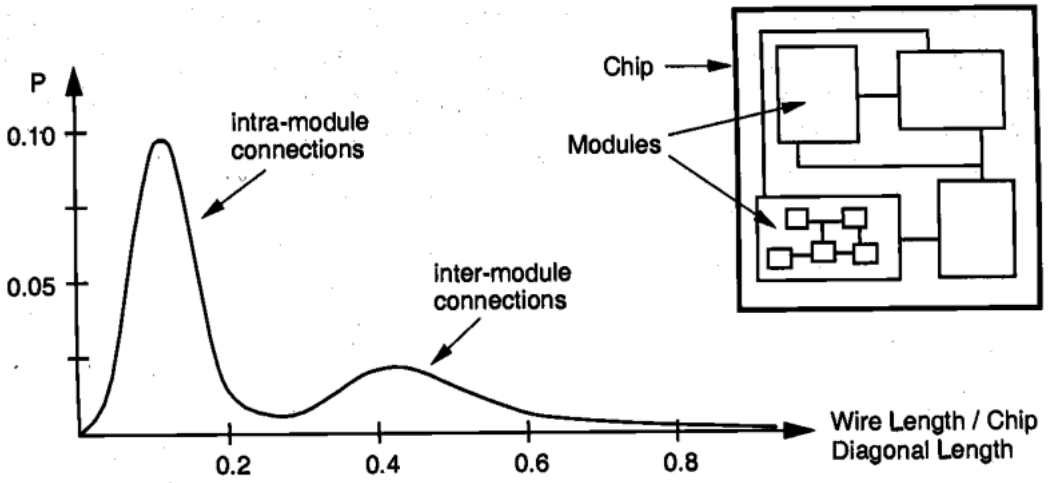
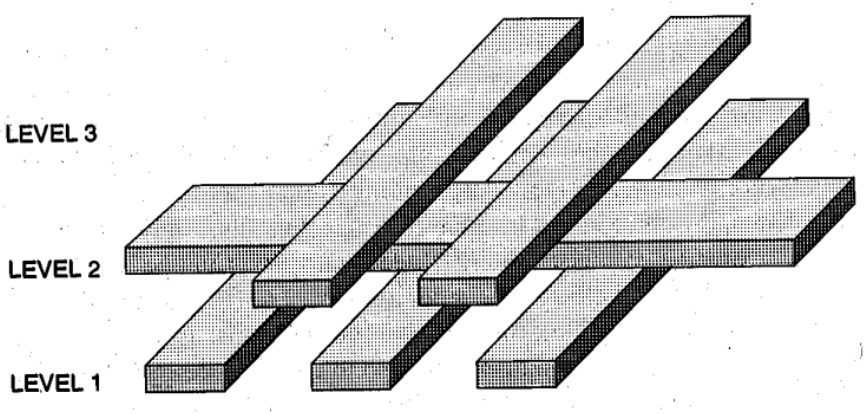


Figure 6.14. Statistical distribution of interconnection length on a typical chip.

Interconnect Capacitance Estimation

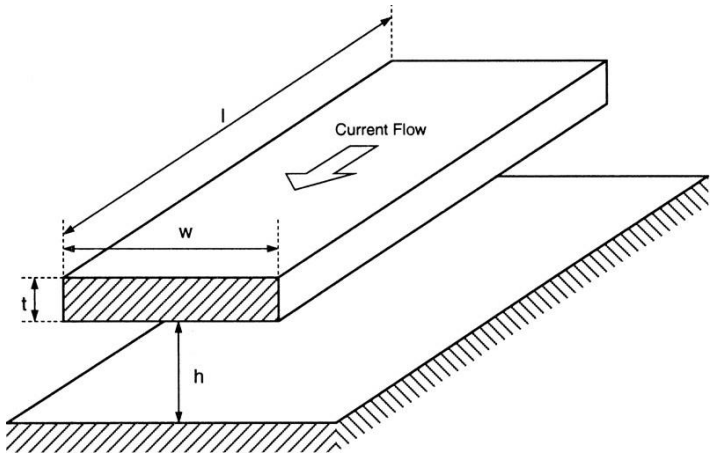
- In VLSI, the parasitic interconnect capacitances are most difficult parameters to estimate accurately.
- Each interconnection wire - 3 D structure with significant variations of
  - ✓ Shape
  - ✓ Thickness
  - ✓ Vertical distance from the ground plane (substrate),
  - ✓ Also each interconnect lines is surrounded by an number of other lines, either on the same level or on different levels, running in close proximity of each other.

The accurate estimation of parasitic cap. Of these wires w.r.t substate, as well as w.r.t each other is a complicated task.



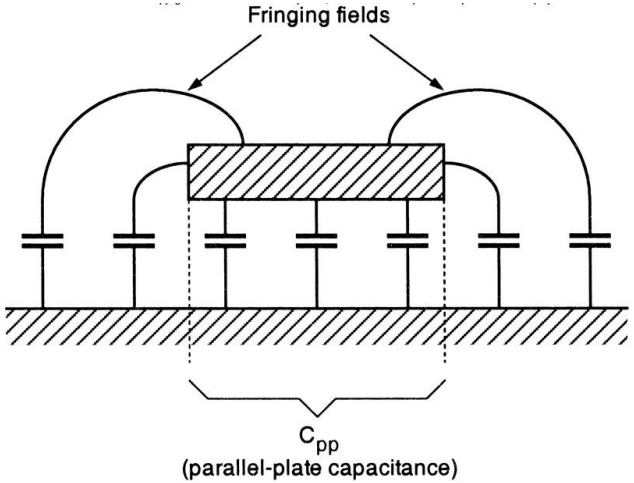
Interconnect Capacitance Estimation

- Wire segment has a length of (l) in the current direction, A width a width of (w) and a thickness of (t).
- the interconnect segment runs parallel to the chip surface and is separated from the ground plane by a dielectric (oxide) layer of height (h).



$$C = \frac{\varepsilon \cdot A}{t}$$

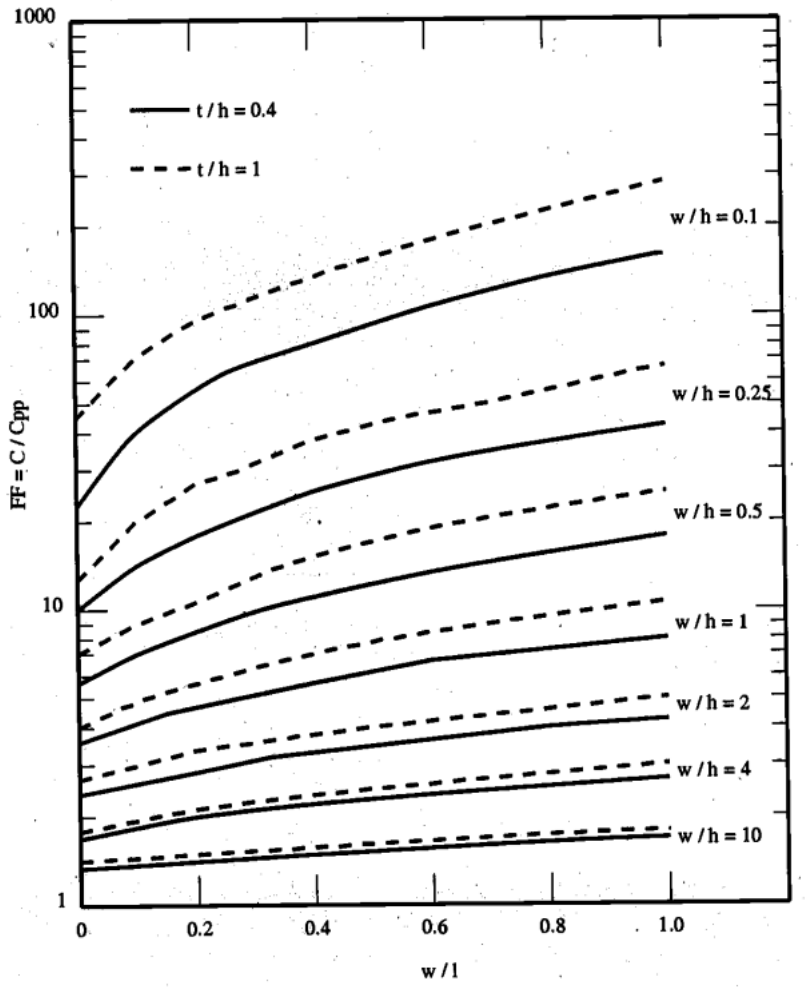
In interconnect lines where the wire thickness (t) is comparable in magnitude to the ground-plane distance (h),fringing electric fields significantly increase the total parasitic capacitance



Some of the capacitance is resulted from the **fringe effect of the structure**. The electric lines of the forces come out of the side of the trace and propagates down to the ground layer.

Interconnect Capacitance Estimation

- Figure 6.18 shows the variation of the fringing-field factor FF = Ctotal / Cpp, as a function of (t/h), (w/h) and (w/l).
- It can be seen that the influence of fringing fields increases with the decreasing (w/h) ratio, and
- that the fringing-field capacitance can be as much as 10-20 times larger than the parallel-plate capacitance.



Interconnect Capacitance Estimation

- In the submicron fabrication technologies allow the width of the metal lines to be decreased rather significantly, but the thickness of the line must be preserved in order to ensure structural integrity.
- This situation, which involves narrow metal lines with a considerable vertical thickness, makes these interconnection lines especially vulnerable to fringing field effects
- A set of simple formulas developed by Yuan and Trick in the early 1980's can be used to estimate the capacitance of the interconnect structures in which fringing fields complicate the parasitic capacitance calculation.
- The following two cases are considered for two different ranges of width line width (w).

$$C=\varepsilon\left[\frac{\left(w-\frac{t}{2}\right)}{h}+\frac{2\pi}{\ln\left(1+\frac{2h}{t}+\sqrt{\frac{2h}{t}\left(\frac{2h}{t}+2\right)}\right)}\right] \quad for \quad w\geq\frac{t}{2} \qquad (6.53)$$

$$C=\varepsilon\left[\frac{w}{h}+\frac{\pi\left(1-0.0543\cdot\frac{t}{2h}\right)}{\ln\left(1+\frac{2h}{t}+\sqrt{\frac{2h}{t}\left(\frac{2h}{t}+2\right)}\right)}+1.47\right] \quad for \quad w<\frac{t}{2} \qquad (6.54)$$

These formulas permit the accurate approximation of the parasitic capacitance values to within 10% error, even for very small values of (t/h).

Interconnect Capacitance Estimation

- the capacitive coupling between neighboring lines is increased when the thickness of the wire is comparable to its width.
- This coupling between the interconnect lines is mainly responsible for signal crosstalk, where transitions in one line can cause noise in the other lines.

  - *Cross-talk* refers to the noise that is generated on a line due to capacitive coupling from neighboring lines that are switching.

  - as geometries get smaller, lines are closer together so capacitance goes up.

  - we can reduce cross-talk by separating the traces or inserting ground lines between the signals, but this takes area.

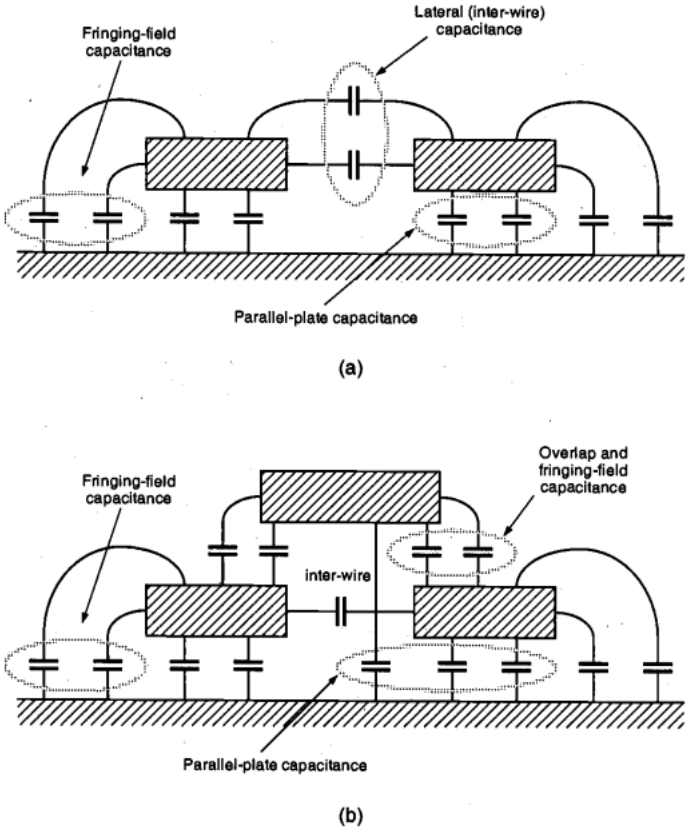


Figure 6.20. Capacitive coupling components, (a) between two parallel lines running on the same level, and (b) between three parallel lines running on two different levels.

Interconnect Capacitance Estimation

- Interconnect Capacitance

- interconnect modeling becomes a complex problem due to the 3D geometries present on-chip

- we typically take a *guess* at the capacitance of the interconnect for initial simulations.

- once we start physically laying out our design, we can use the CAD tool to *extract* the actual capacitance and back annotate it into our simulation.

- we then run a new simulation with accurate capacitance models to verify timing is still met post-layout.

Interconnect Capacitance Estimation

- The cross-section view of a double-metal CMOS structure, where the individual parasitic capacitances between the layers are also indicated.

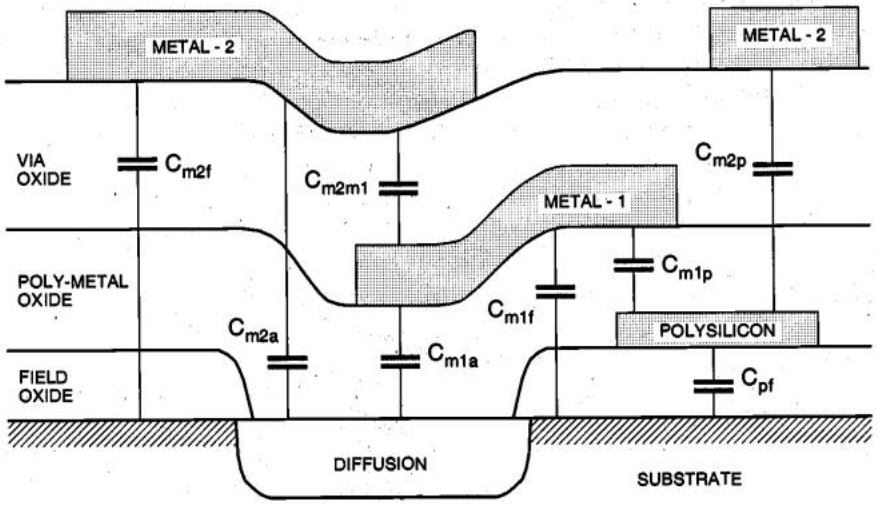


Figure 6.22. Cross-sectional view of a double-metal CMOS structure, showing capacitances between various layers.

Interconnect Capacitance Estimation

- The vertical thickness values of the different layers in a typical 0.8-micron CMOS technology are given in Table 6.1

Field oxide thickness	0.52	µm	
Gate oxide thickness	16.0	nm	(= 0.016 µm)
Polysilicon thickness	0.35	µm	(minimum width 0.8 µm)
Poly - metal oxide thickness	0.65	µm	
Metal - 1 thickness	0.60	µm	(minimum width 1.4 µm)
Via oxide thickness	1.00	µm	
Metal - 2 thickness	1.00	µm	(minimum width 1.4 µm)
n + junction depth	0.40	µm	
p + junction depth	0.40	µm	
n - well junction depth	3.50	µm	

Table 6.1. Thickness values of different layers in a typical 0.8 micron CMOS process.

Interconnect Capacitance Estimation

- Table 6.2 contains the capacitance values between the various layers shown in Fig. 6.22, for the same 0.8-micron CMOS process. The perimeter values are to be used to calculate the fringing field capacitances

Poly over field oxide	C_{pf}	Area	0.066	fF / μm^2
		Perimeter	0.046	fF / μm
Metal - 1 over field oxide	C_{m1f}	Area	0.030	fF / μm^2
		Perimeter	0.044	fF / μm
Metal - 2 over field oxide	C_{m2f}	Area	0.016	fF / μm^2
		Perimeter	0.042	fF / μm
Metal - 1 over Poly	C_{m1p}	Area	0.053	fF / μm^2
		Perimeter	0.051	fF / μm
Metal - 2 over Poly	C_{m2p}	Area	0.021	fF / μm^2
		Perimeter	0.045	fF / μm
Metal - 2 over Metal - 1	C_{m2m1}	Area	0.035	fF / μm^2
		Perimeter	0.051	fF / μm

Table 6.2. Parasitic capacitance values between various layers, for a typical double-metal 0.8 micron CMOS technology.

Interconnect Capacitance Estimation

- - interconnect modeling becomes a complex problem due to the 3D geometries present on-chip

  - we typically take a *guess* at the capacitance of the interconnect for initial simulations.

  - once we start physically laying out our design, we can use the CAD tool to *extract* the actual
    capacitance and back annotate it into our simulation.

  - we then run a new simulation with accurate capacitance models to verify timing is still met post-layout.

Interconnect Resistance

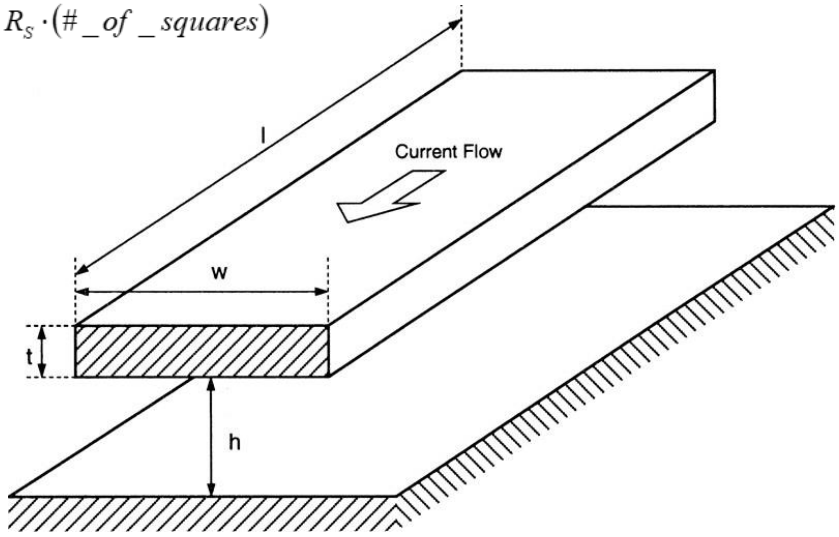
- Interconnect Resistance

  - The resistance of a line depends on the type of material used (e.g., polysilicon, aluminum, or gold), the dimensions of the line and finally, the number and locations of the contacts on that line. Consider again the interconnection line shown in

The total resistance in the indicated current direction can be found as

$$R_{wire} = \rho \cdot \frac{l}{w \cdot t} = R_{sheet}\left(\frac{l}{w}\right)$$

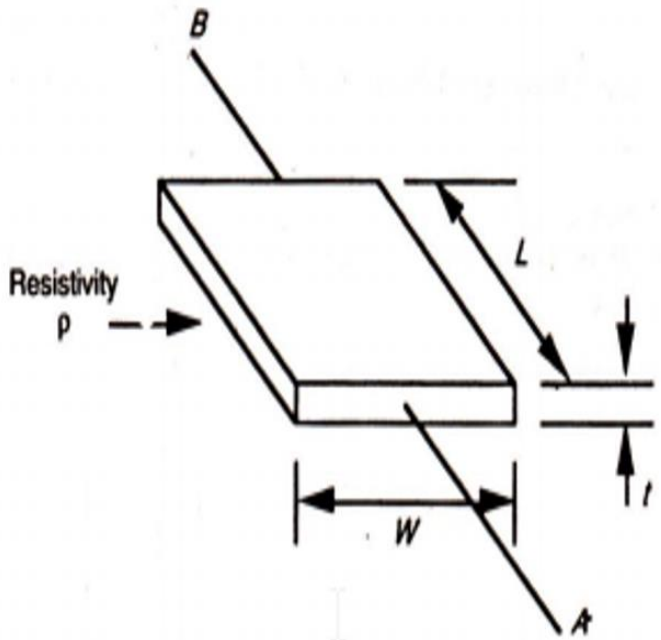
$$R = \frac{\rho \cdot l}{A} = R_S \cdot (\#\_of\_squares)$$



- where (p) represents the characteristic resistivity of the interconnect material, and R_{sheet} represents the sheet resistivity of the line, in (Ω/square)

$$R_{sheet} = \frac{\rho}{t}$$

Interconnect Resistance



the resistance R_{AB} between two opposite faces.

$$R_{AB} = \frac{\rho L}{A} \text{ ohm}$$

where

A = cross-section area

$$R_{AB} = \frac{\rho L}{tW} \text{ ohm}$$

Now, consider the case in which $L = W$, that is, a square of resistive material, then $R_{AB} = \frac{\rho}{t} = R_s$

where

R_s = ohm per square or sheet resistance

Thus

$$R_s = \frac{\rho}{t} \text{ ohm per square}$$

Rs is completely independent of the area of the square :

Ex: 1 μm per side square slab of material has exactly the same resistance as a 1 cm per side square slab of the same material if the thickness is the same.

Calculation of Interconnect Delay

RC Delay Model

- The simplest model which can be used to represent the resistive and capacitive parasitics of the interconnect line consists of one lumped resistance and one lumped capacitance (Fig. 6.23(a)).
- Assuming that the capacitance is discharged initially, and assuming that the input signal is a rising step pulse at time t = 0, the output voltage waveform of this simple RC circuit is found as

$$V_{out}(t) = V_{DD}\left(1 - e^{-\frac{t}{RC}}\right)$$

The rising output voltage reaches the 50%-point at $t = \tau_{PLH}$, thus, we have

$$V_{50\%} = V_{DD}\left(1 - e^{-\frac{\tau_{PLH}}{RC}}\right)$$

and the propagation delay for the simple lumped RC network is found as

$$\tau_{PLH} \approx 0.69\,RC$$

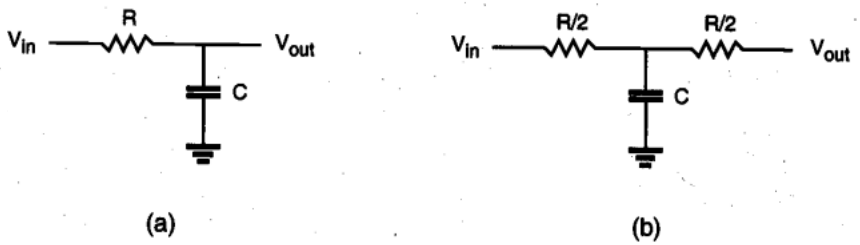


Figure 6.23. (a) Simple lumped RC model of an interconnect line, where R and C represent the total line resistance and capacitance, respectively. (b) The T-model of the same line.

Calculation of Interconnect Delay

RC Delay Model

- The transient behavior of an interconnect line can be more accurately represented using the RC ladder network, shown in Fig. 6.24.
- Each RC-segment consists of a series resistance (R/N), and a capacitance (C/N) connected between the node and the ground.
- It can be expected that the accuracy of this model increases with increasing N, where the transient behavior approaches that of a distributed RC line for very large values of N. Y
- The delay analysis of such RC networks of higher complexity requires either full-scale SPICE simulation, or other delay calculation methods such as the Elmore delay formula.

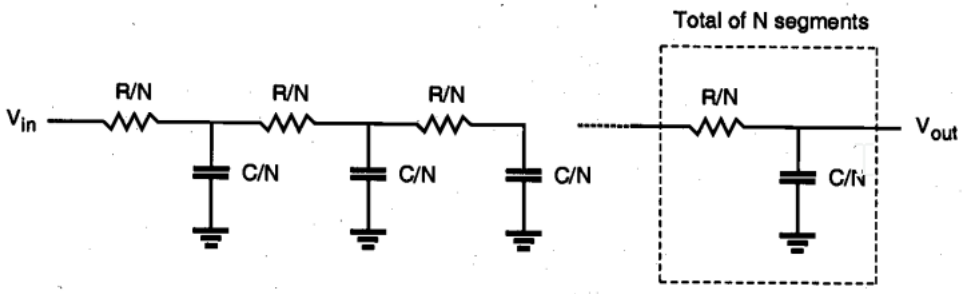


Figure 6.24. Distributed RC ladder network model consisting of N equal segments.

Calculation of Interconnect Delay

The Elmore Delay

Consider a general RC tree network, as shown in Fig. 6.25. Note that

(i) there are no resistor loops in this circuit,

(ii) all of the capacitors in an RC tree are connected between a node and the ground, and

(iii) there is one input node in the circuit. Also notice that there is a unique resistive path, from the input node to any c

Inspecting the general topology of this RC tree network, we can make the following path definitions:

1. Let Pi denote the unique path from the input node to node i, i = 1, 2, 3, ..., N.
2. Let Pij = Pi ∩ Pj denote the portion of the path between the input and the node i, which is common to the path between the input and node j

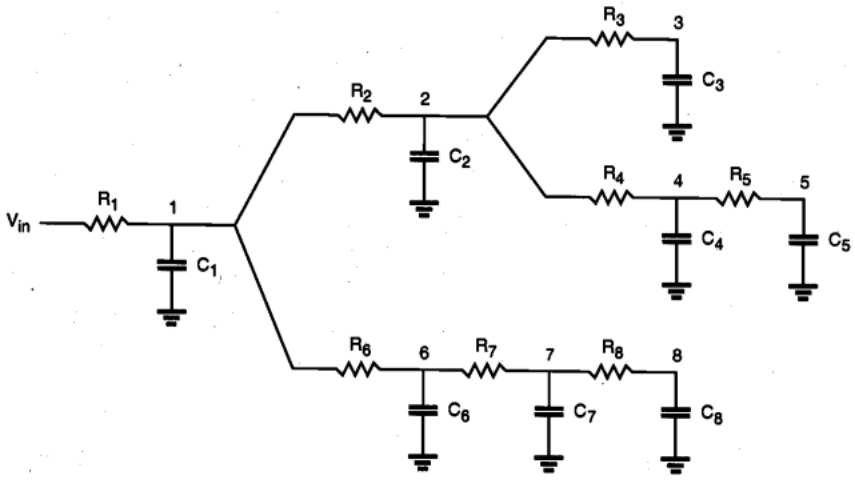


Figure 6.25. A general RC tree network consisting of several branches.

Calculation of Interconnect Delay

The Elmore Delay

Assuming that the input signal is a step pulse at time t = 0, the Elmore delay at node i of this RC tree is given by the following expression

$$\tau_{Di} = \sum_{j=1}^{N} C_j \sum_{\substack{\text{for all} \\ k \in P_{ij}}} R_k$$

Although this delay is an approximation for the actual signal propagation delay from the input node to node i, it provides a fairly simple and accurate means of predicting the behavior of the RC line

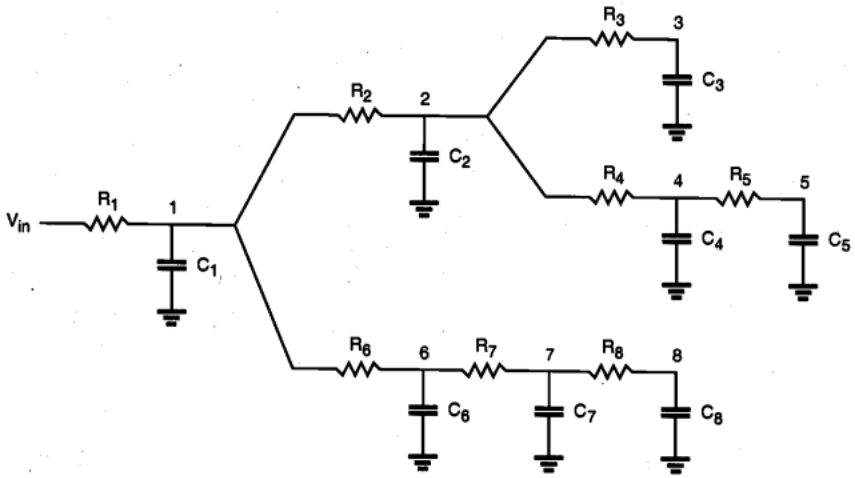


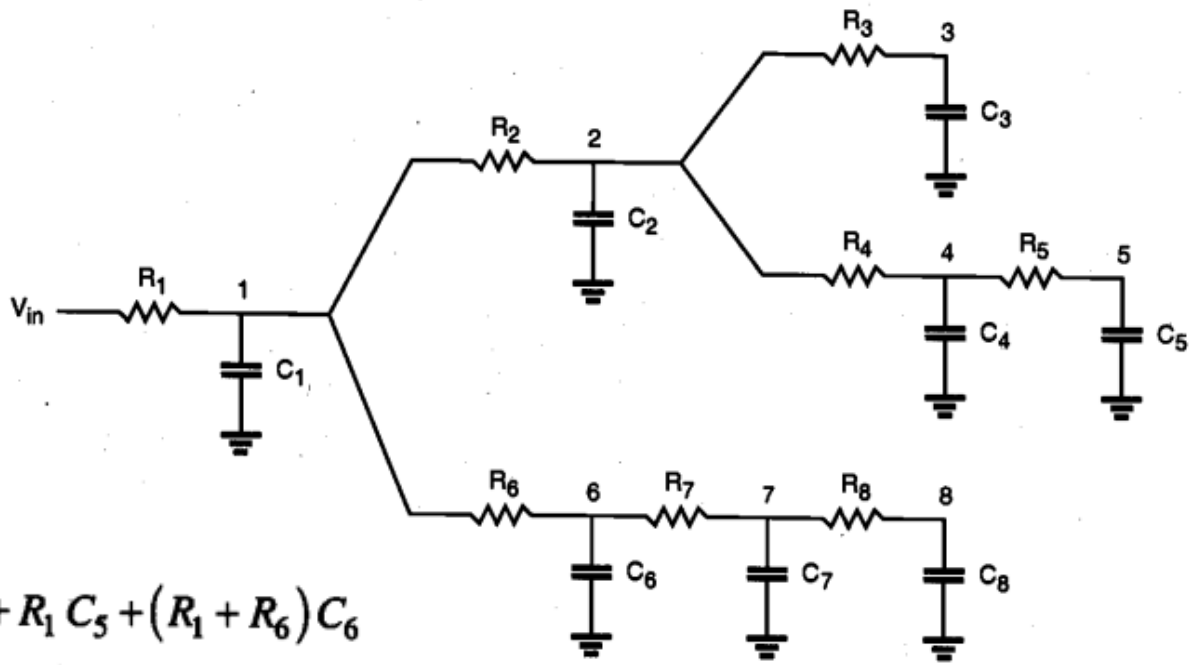
Figure 6.25. A general RC tree network consisting of several branches.

Calculation of Interconnect Delay

The Elmore Delay

the Elmore delay at node 7 can be found according to equation as

$$\tau_{Di} = \sum_{j=1}^{N} C_j \sum_{\substack{for\ all \\ k \in P_{ij}}} R_k$$



$$\tau_{D7} = R_1 C_1 + R_1 C_2 + R_1 C_3 + R_1 C_4 + R_1 C_5 + (R_1 + R_6) C_6 + (R_1 + R_6 + R_7) C_7 + (R_1 + R_6 + R_7) C_8$$

Figure 6.25. A general RC tree network consisting of several branches.

Calculation of Interconnect Delay

The Elmore Delay

- now the simple RC ladder network shown in Fig.
- Here, the entire network consists of one single branch, and the Elmore delay from the input to the output (node N) is found as

$$\tau_{DN} = \sum_{j=1}^{N} C_j \sum_{k=1}^{j} R_k$$

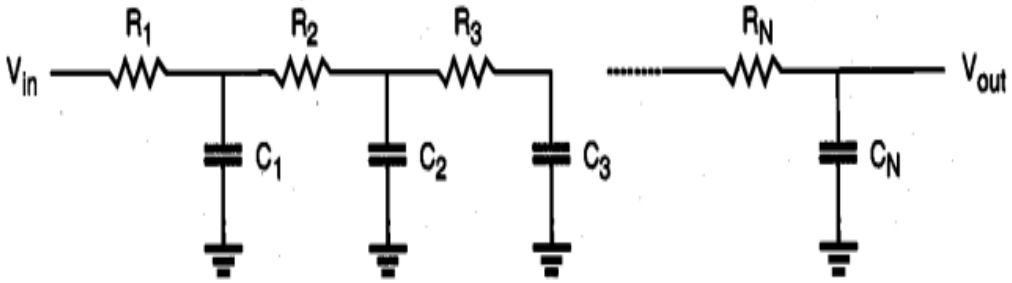


Figure 6.26. Simple RC ladder network consisting of one branch.

If we further assume a uniform RC ladder network, consisting of identical elements (R/N) and (C/N) as shown in Fig. 6.24, then the Elmore delay from the input to the output node becomes

Calculation of Interconnect Delay

The Elmore Delay

If we further assume a uniform RC ladder network, consisting of identical elements (R/N) and (C/N) as shown in Fig. 6.24, then the Elmore delay from the input to the output n

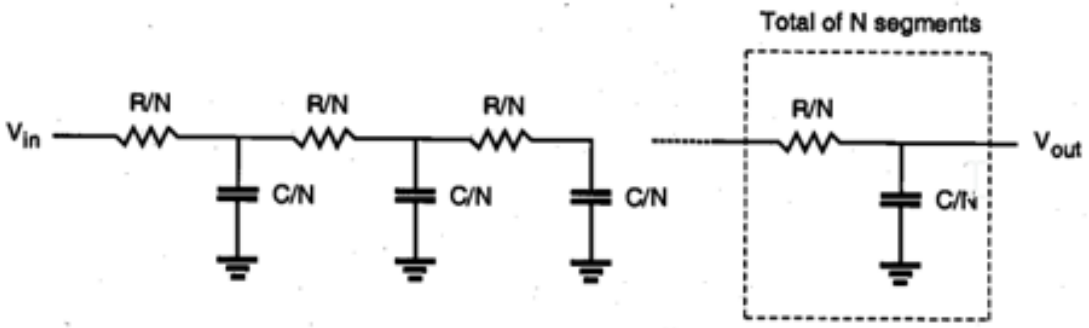


Figure 6.24. Distributed RC ladder network model consisting of N equal segments.

$$\tau_{DN} = \sum_{j=1}^{N} \left(\frac{C}{N}\right) \sum_{k=1}^{j} \left(\frac{R}{N}\right)$$

$$= \left(\frac{C}{N}\right)\left(\frac{R}{N}\right)\left(\frac{N(N+1)}{2}\right) = RC\left(\frac{N+1}{2N}\right)$$

For very large N (distributed RC line behavior), this delay expression reduces t0

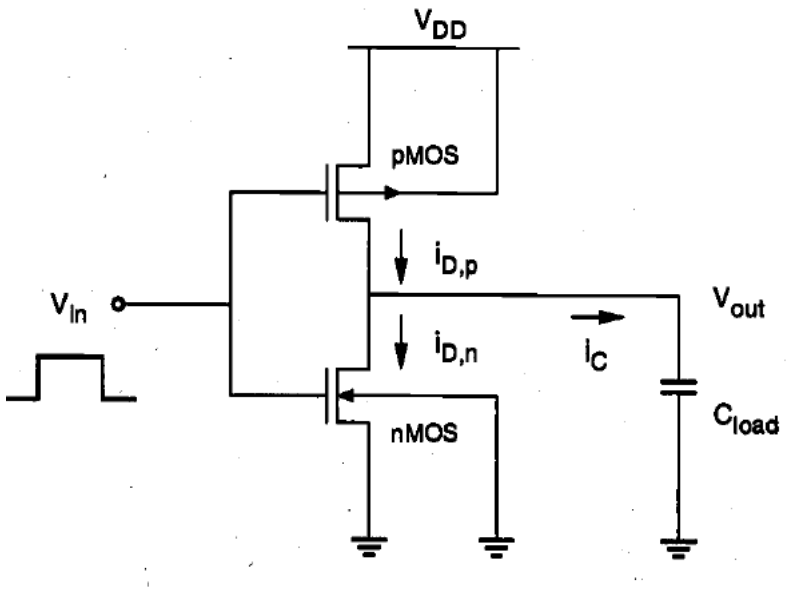
$$\tau_{DN} = \frac{RC}{2} \qquad for\ N \to \infty$$

Calculation of Interconnect Delay

Refer text book example problem 6.5

Switching power Dissipation

- Consider the simple CMOS inverter circuit shown in fig
- assume that the input voltage is an ideal step waveform with negligible rise and fall times. Typical



Switching power Dissipation

- input and output voltage waveforms and the expected load capacitor current waveform are shown in Fig.

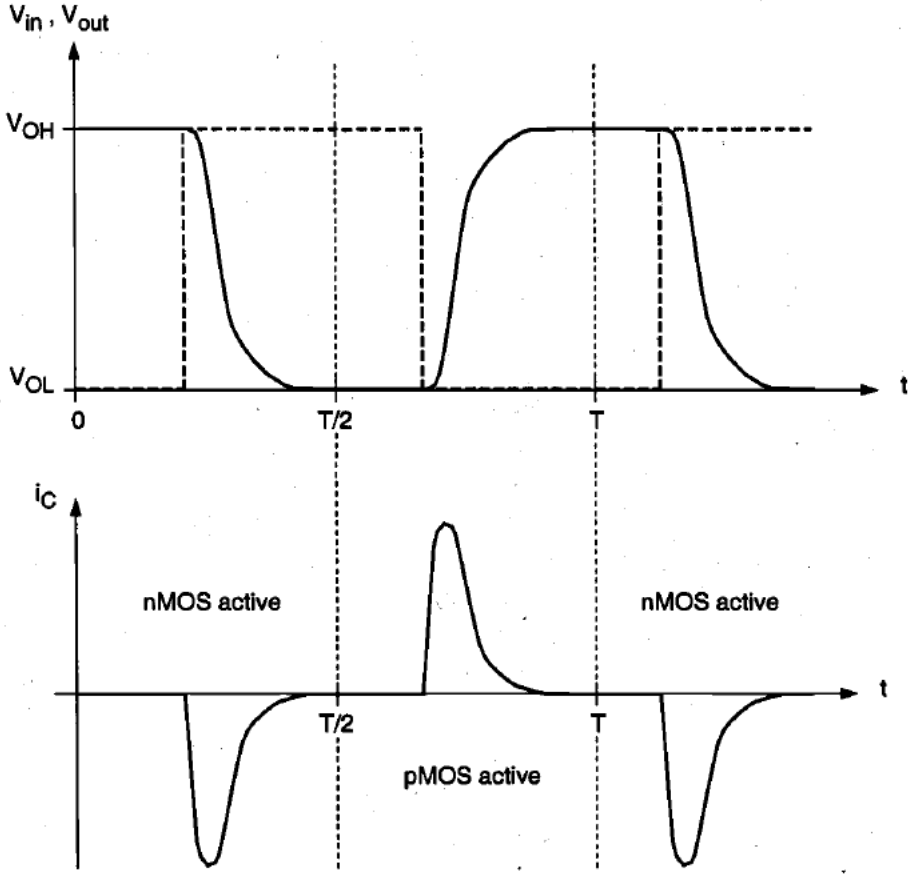


Figure 6.28. Typical input and output voltage waveforms and the capacitor current waveform during switching of the CMOS inverter.

Switching power Dissipation

When input voltage switches from low to high	When input voltage switches from high to low
• PMOS is off • nMOS starts conducting • Output load capacitance is being discharged through the nMOS transistor • Capacitor current is equal to instantaneous drain current of nMOS	• nMOS is off • PMOS start conducting • Output load capacitance is being charged up through PMOS • Capacitor current equal to the drain current of PMOS

- Assuming periodic input and output waveforms, the average power dissipated by any device over one period can be found as

$$P_{avg} = \frac{1}{T}\int_0^T v(t)\cdot i(t)\,dt$$

Switching power Dissipation

- Assuming periodic input and output waveforms, the average power dissipated by any device over one period can be found as
- the average power dissipation of the CMOS inverter can be calculated as the power required to charge up and charge down the output load capacitance.

$$P_{avg} = \frac{1}{T}\left[\int_0^{T/2} V_{out}\left(-C_{load}\frac{dV_{out}}{dt}\right)dt + \int_{T/2}^{T}(V_{DD}-V_{out})\left(C_{load}\frac{dV_{out}}{dt}\right)dt\right]$$

$$P_{avg} = \frac{1}{T}\left[\left(-C_{load}\frac{V_{out}^2}{2}\right)\Bigg|_0^{T/2} + \left(V_{DD}\cdot V_{out}\cdot C_{load} - \frac{1}{2}C_{load}V_{out}^2\right)\Bigg|_{T/2}^{T}\right]$$

$$P_{avg} = \frac{1}{T}C_{load}V_{DD}^2$$

Switching power Dissipation

$$P_{avg} = \frac{1}{T} C_{load} V_{DD}^2$$

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- The average power dissipation of the CMOS inverter is proportional to the switching frequency *f*
- Therefore, the low-power advantage of CMOS circuitsbecomes less prominent in
- high-speed operation, where the switching frequency is high.

Switching power Dissipation

- The switching power expression derived for the CMOS inverter also applies to all general CMOS, as shown in fig

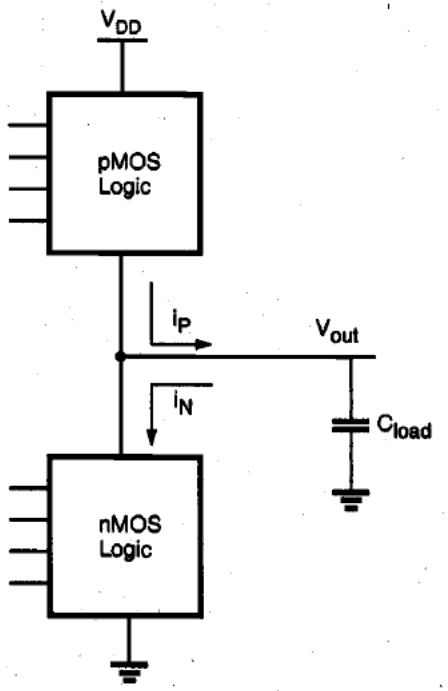

Figure 6.29. Generalized CMOS logic circuit.

THANK YOU

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