DIGITAL VLSI DESIGN

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Electronics and Communication Engineering

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Unit 2: Fabrication of MOSFETs & Circuit Design Process

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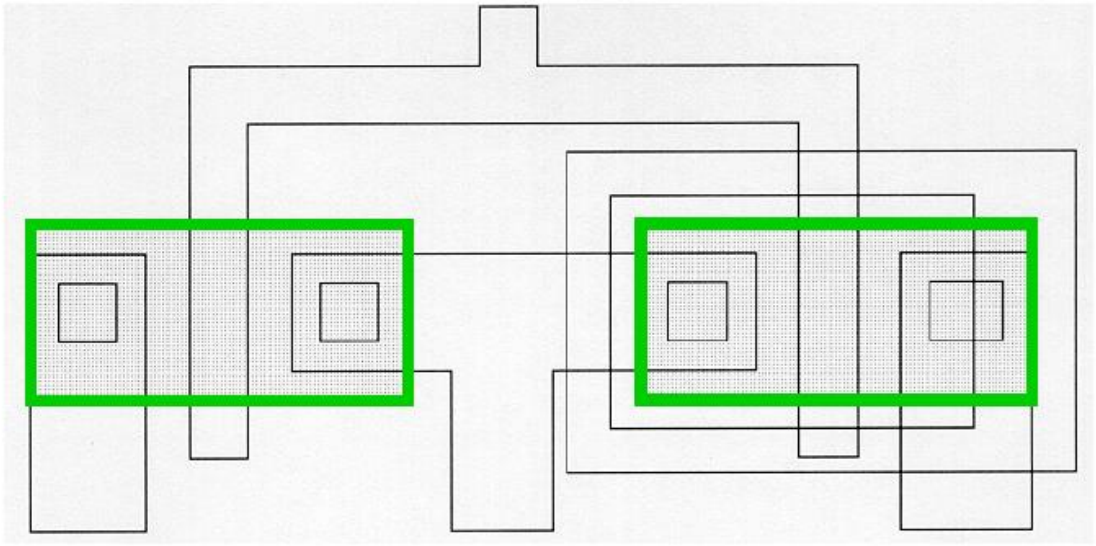
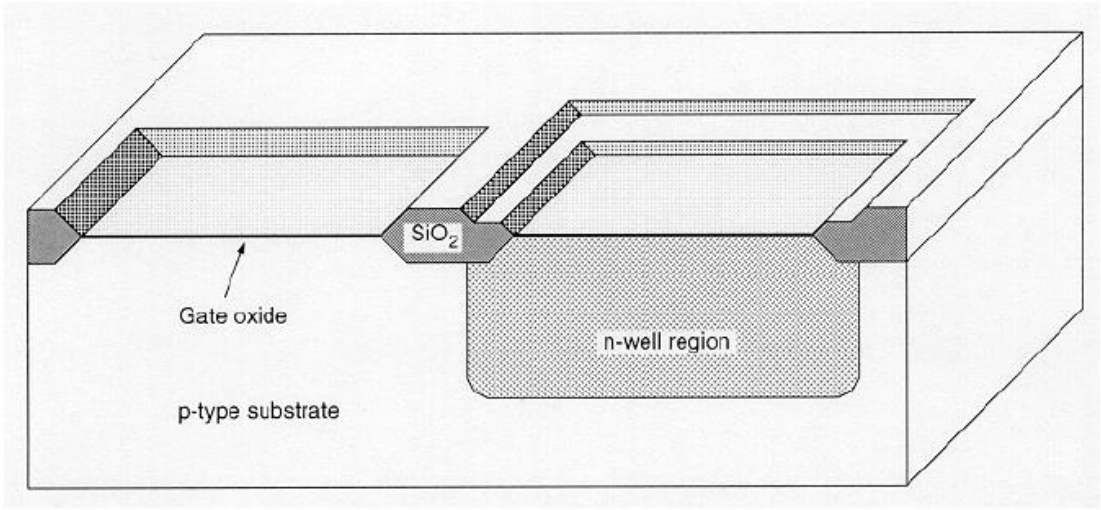
CMOS Process

active

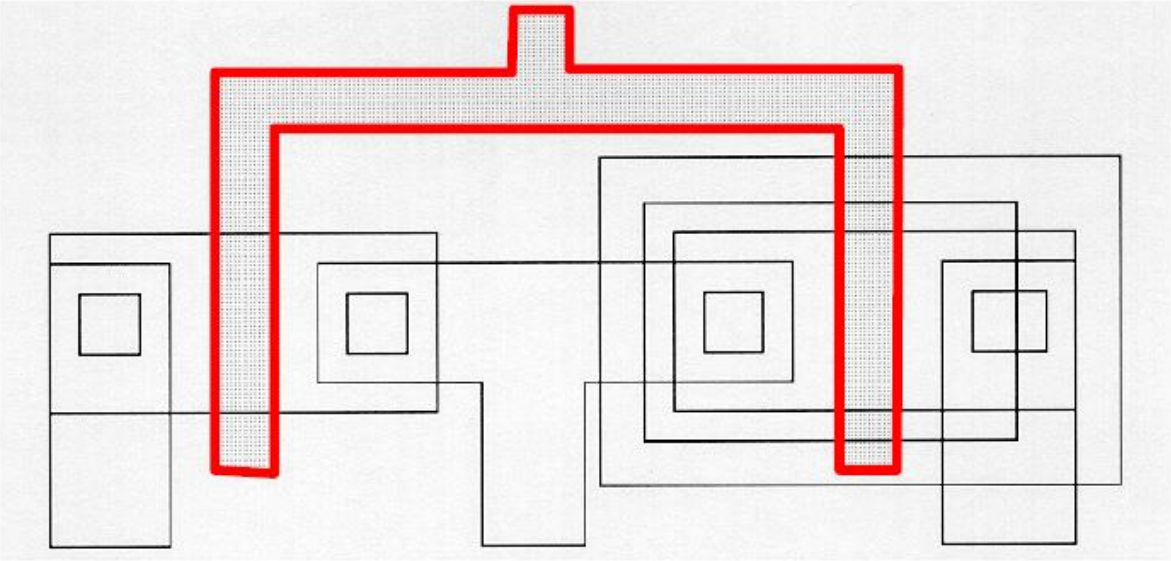


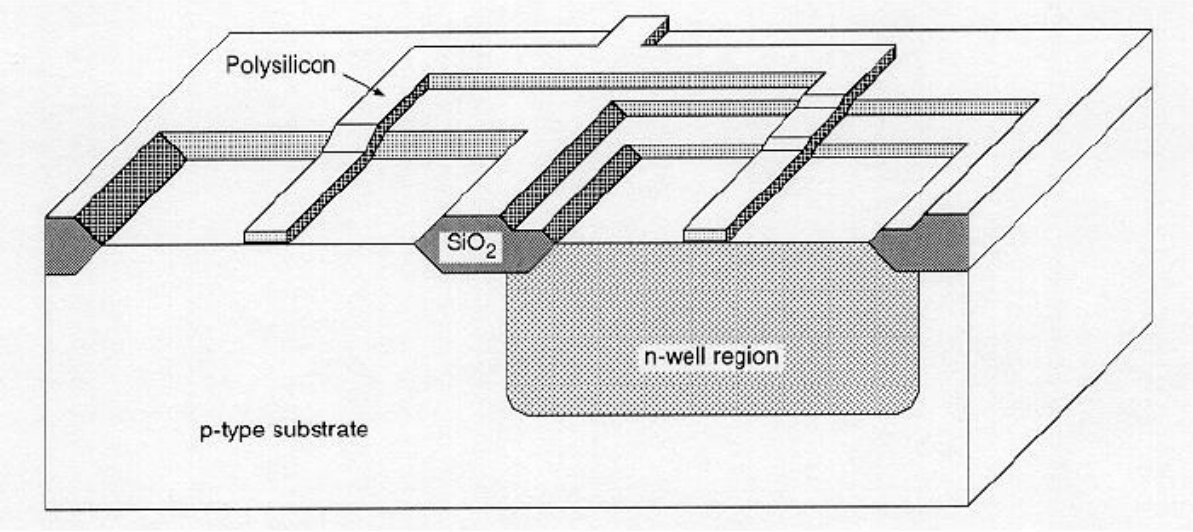


P-type substrate

- n-well region for PMOS
- thin gate oxide is grown on top of the active regions
- thick field oxide is grown in the areas surrounding the transistor active regions
- gate oxide thickness and quality affect the operational characteristics of the MOS transistor and reliability.

CMOS Process

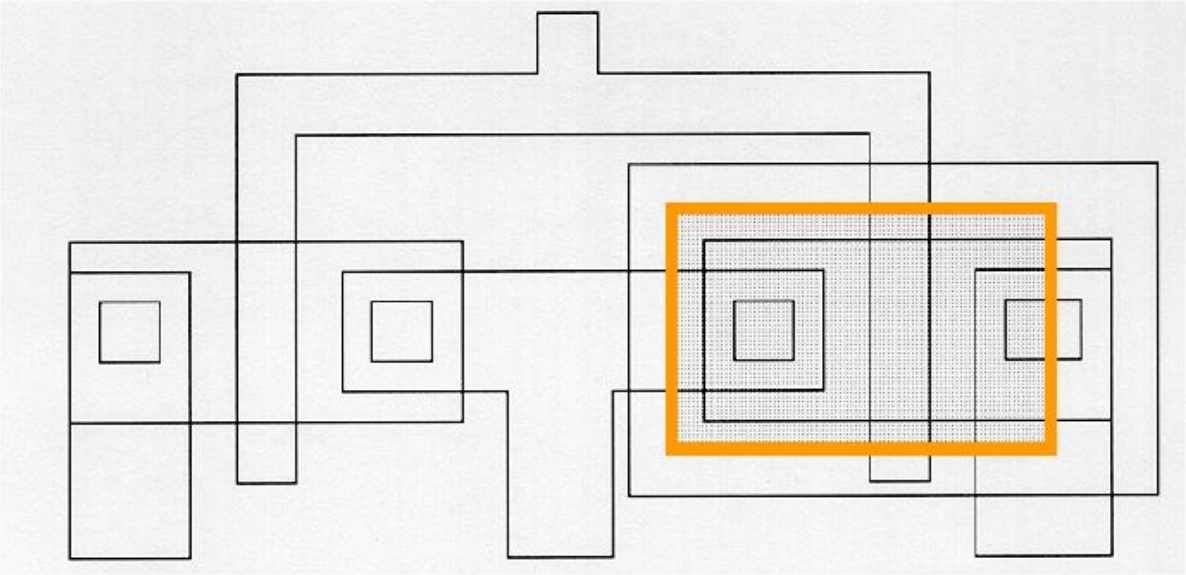


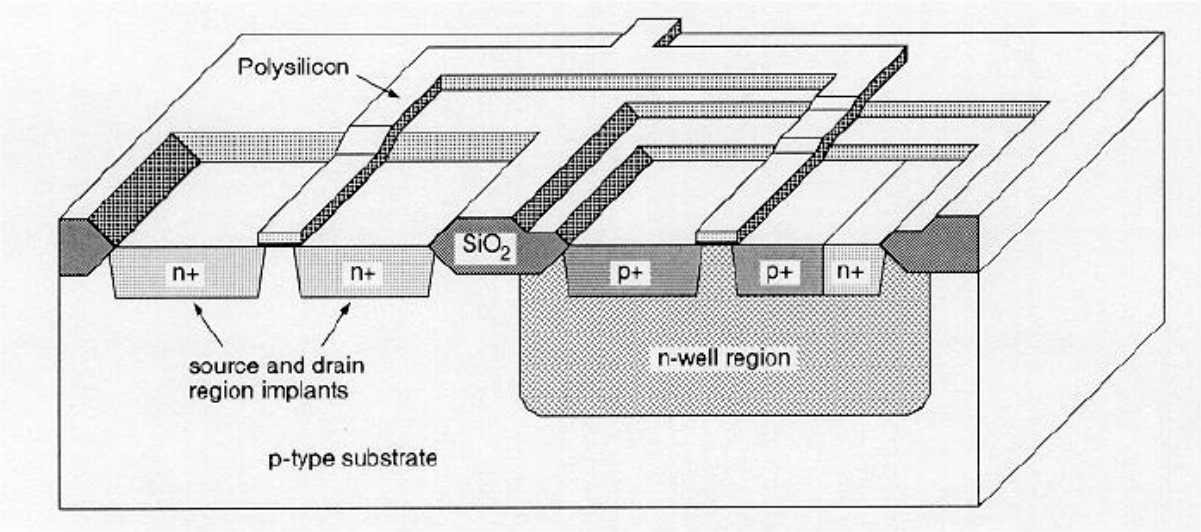


Poly

- The polysilicon layer is deposited using chemical vapor deposition (CVD) and patterned by dry (plasma) etching.
- The created polysilicon lines will function as the gate electrodes of the nMOS and the pMOS transistors and their interconnects.
- Also, the polysilicon gates act as self-aligned masks for the source and drain implantations that follow this step.

CMOS Process

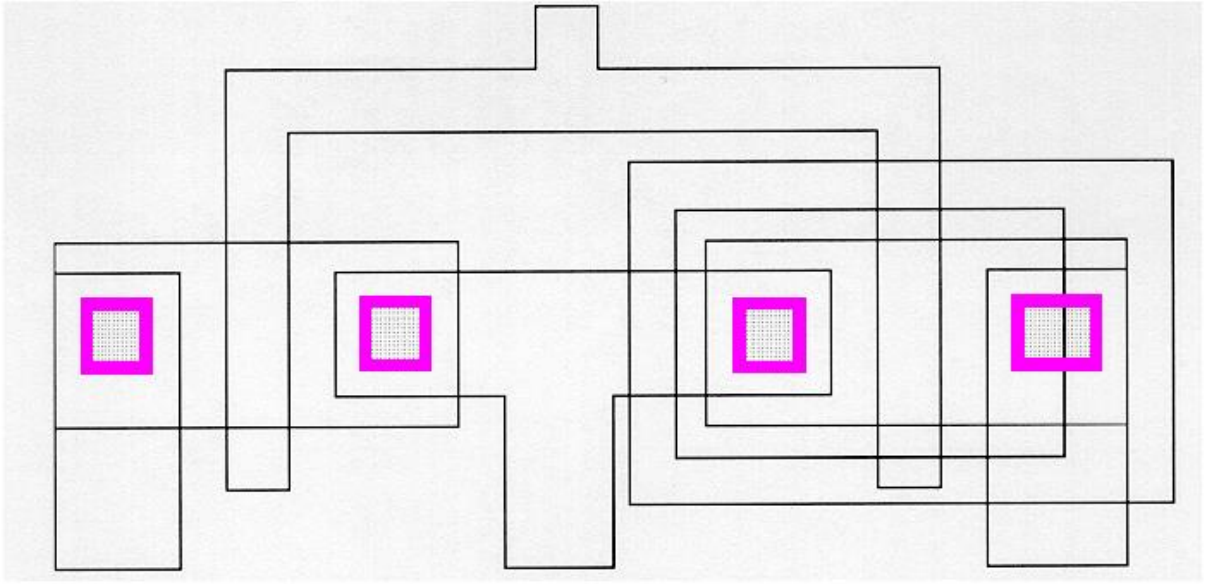


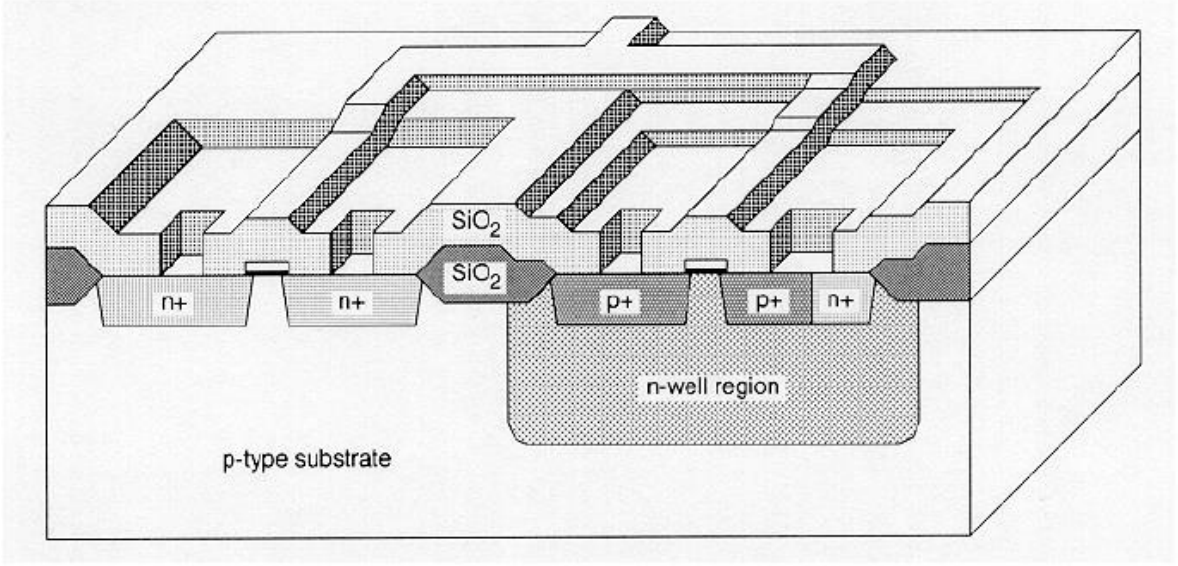


Implant

- Using a set of two masks, the n+ and p+ regions are implanted into the substrate and into the n-well, respectively.
- Also, the ohmic contacts to the substrate and to the n-well are implanted in this process step.

CMOS Process



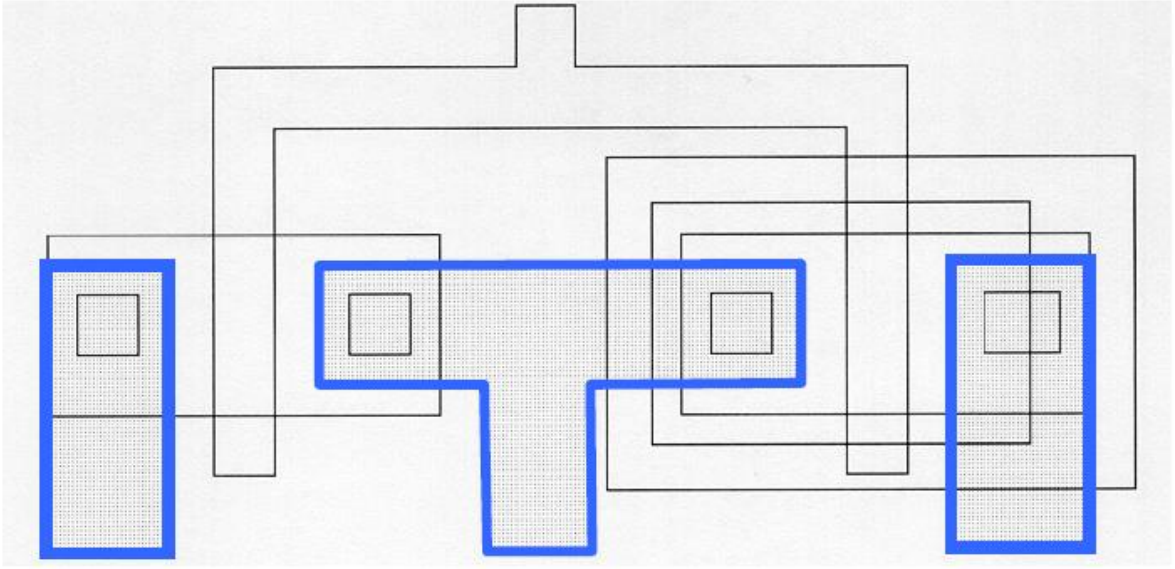


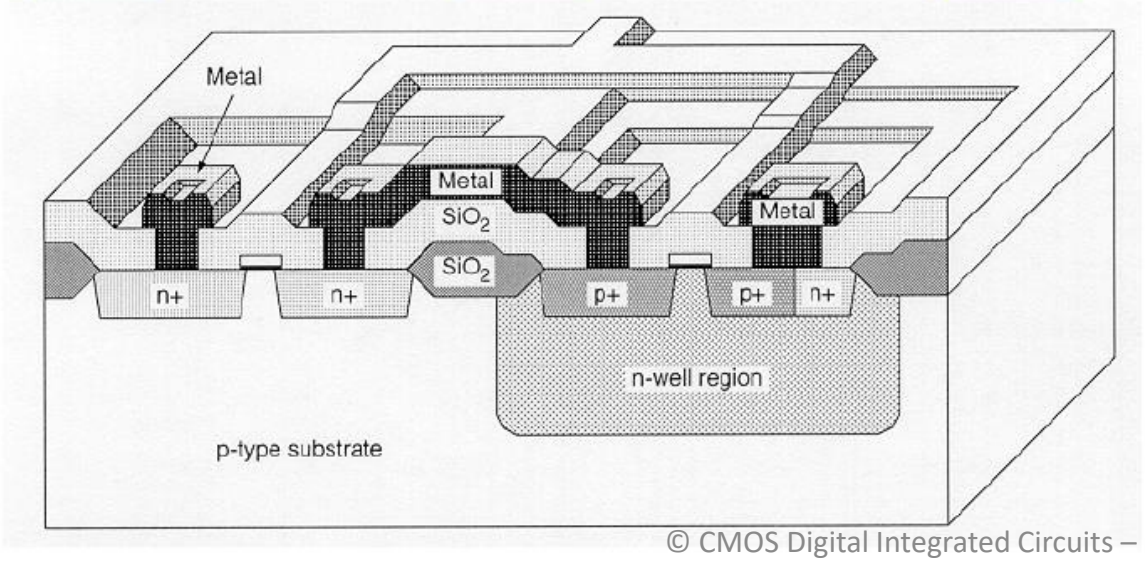
Contacts

- An insulating silicon dioxide layer is deposited over the entire wafer using CVD.
- Then, the contacts are defined and etched away to expose the silicon or polysilicon contact windows.
- These contact windows are necessary to complete the circuit interconnections using the metal layer, which is patterned in the next step.

CMOS Process

metal





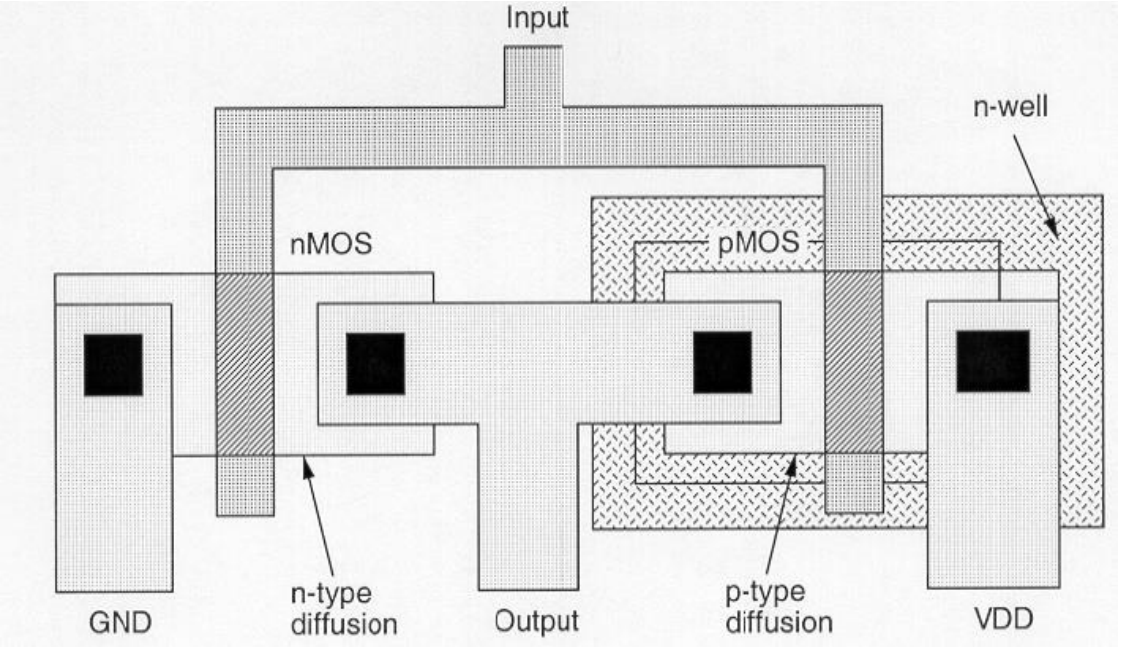
Metal

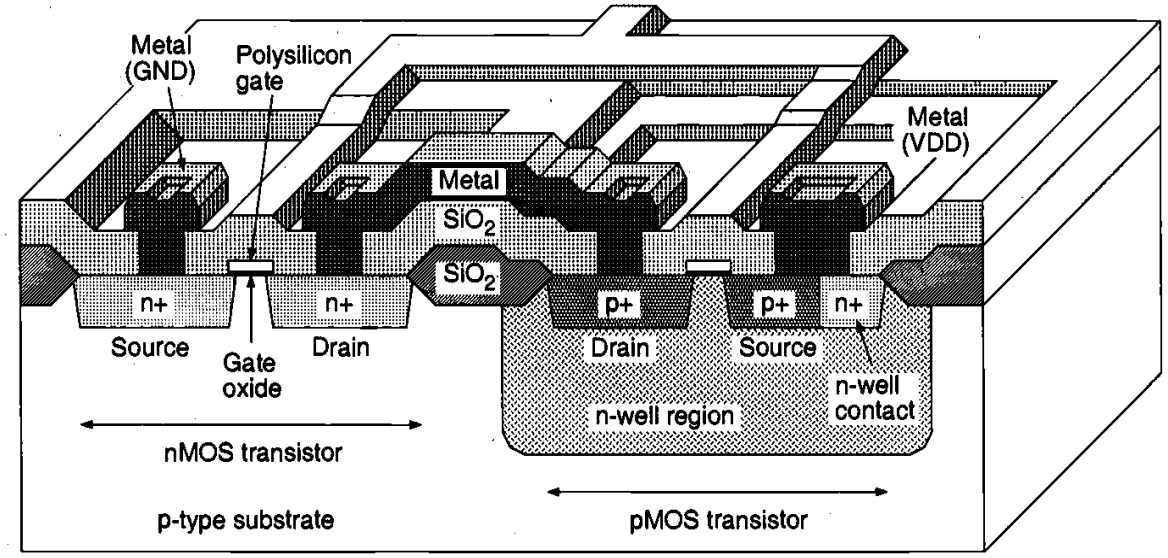
- Metal (aluminum) is deposited over the entire chip surface using metal evaporation, and the metal lines are patterned through etching.
- Since the wafer surface is non-planar, the quality and the integrity of the metal lines created in this step are very critical and are ultimately essential for circuit reliability.

Composite Mask Layout

- The composite layout and the resulting cross-sectional view of the chip, showing one nMOS and one pMOS transistor (in the n-well), and the polysilicon and metal interconnections.

- The final step is to deposit the passivation layer (for protection) over the chip, except over wire-bonding pad areas.





n-well Process

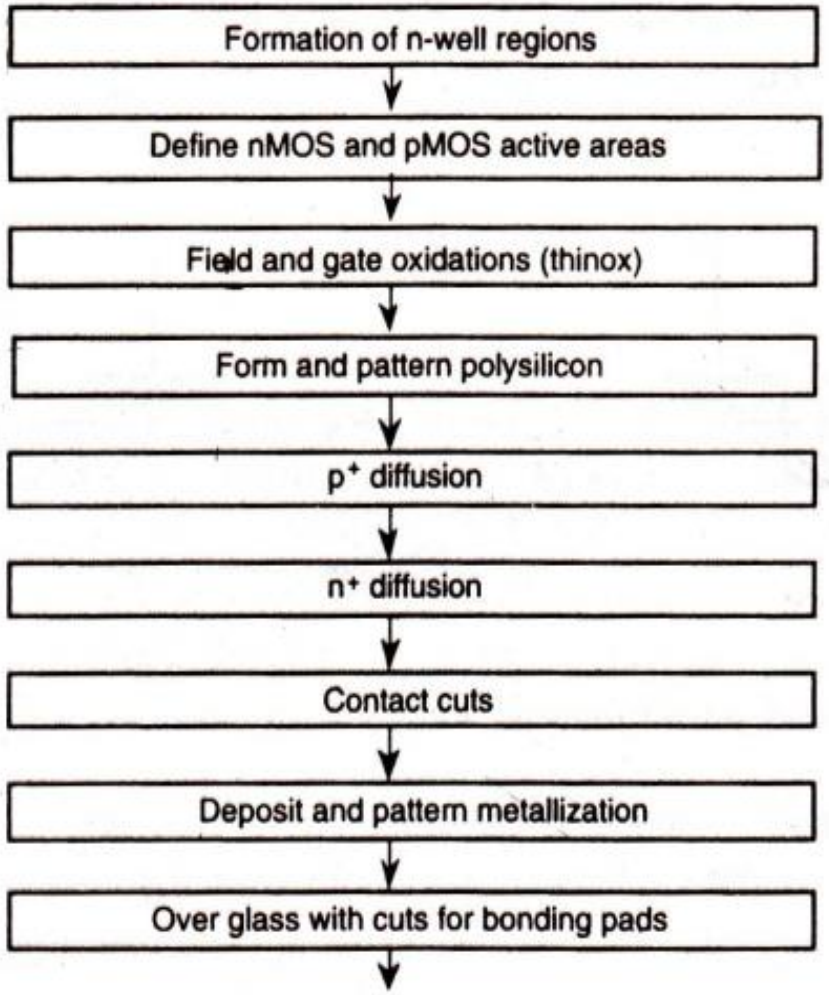


FIGURE 1.11 Main steps in a typical n-well process.

Advantage of n-well process is that it can be fabricated on the same line as conventional nmos. So, this process is often retrofitted to existing nmos processes.

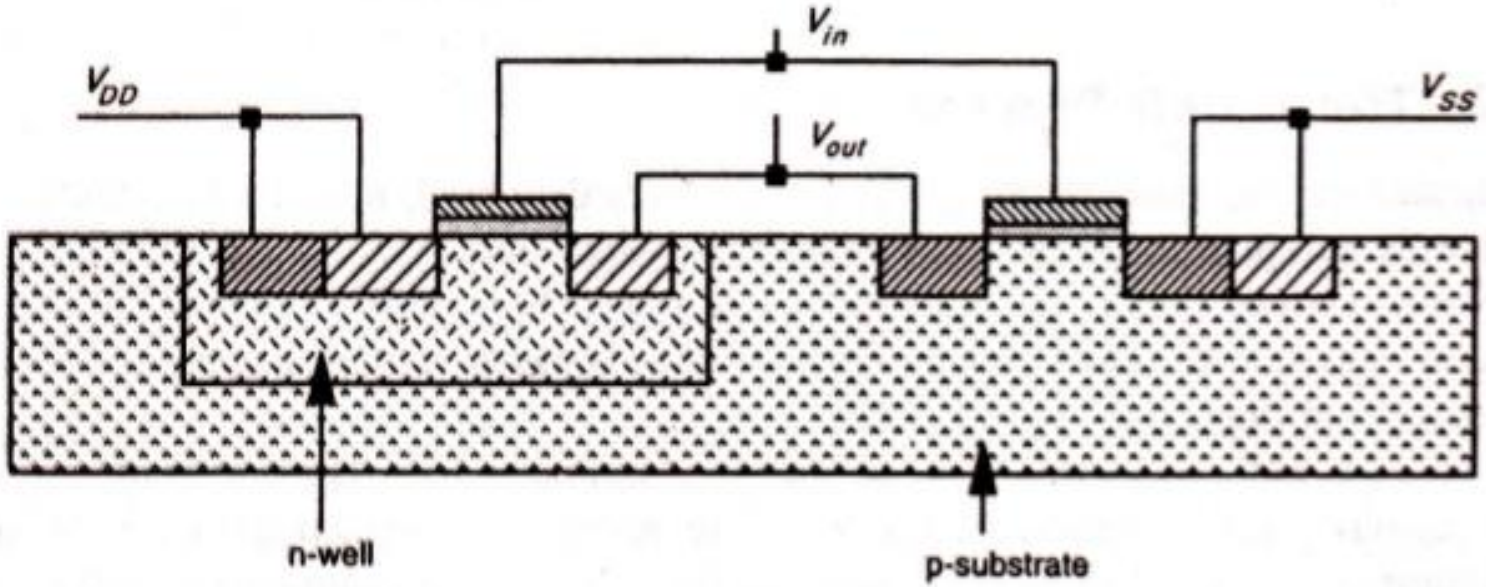


FIGURE 1.12 Cross-sectional view of n-well CMOS inverter.

N-well CMOS circuits are superior to p-well because of the lower substrate bias effects on transistor threshold voltage and inherently lower parasitic capacitances associated with source and drain regions

The Twin-Tub Process

- This technology provides the basis for separate optimization of p- and n-devices in terms of threshold voltage, body effect.
- Starting material is either n+ or p+ substrate with a lightly doped epitaxial layer or epi layer.
- This layer is used as protection against latch-up.
- The aim of epitaxy (=> arranged upon) is to grow high purity silicon layers of controlled thickness with accurately calculated doping concentrations distributed homogenously throughout the layer.
- Electrical properties of this layer is determined by the dopant and its concentration in the silicon.
- N-well and p-well are formed on this layer; which forms the actual substrate.

Process Steps

- Similar to p-well process except for the tub formation where both n-well and p-wells are utilized:
  - Tub formation
  - Thin oxide etching
  - Source and drain implantations
  - Contact cut definitions
  - metallization

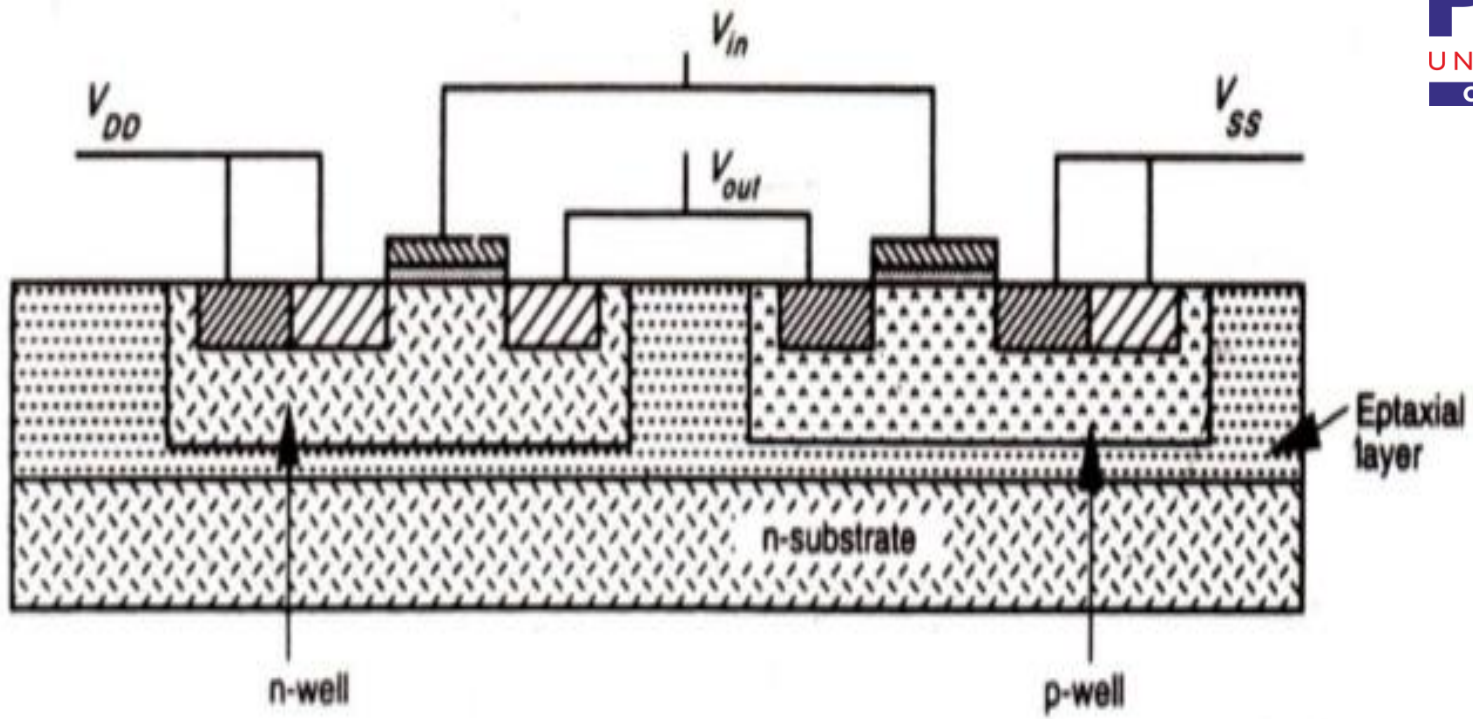


FIGURE 1.14 Twin-tub structure.

THANK YOU

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