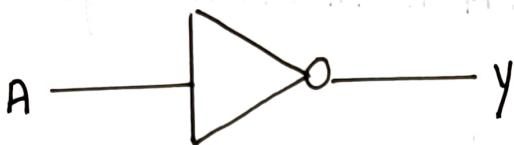


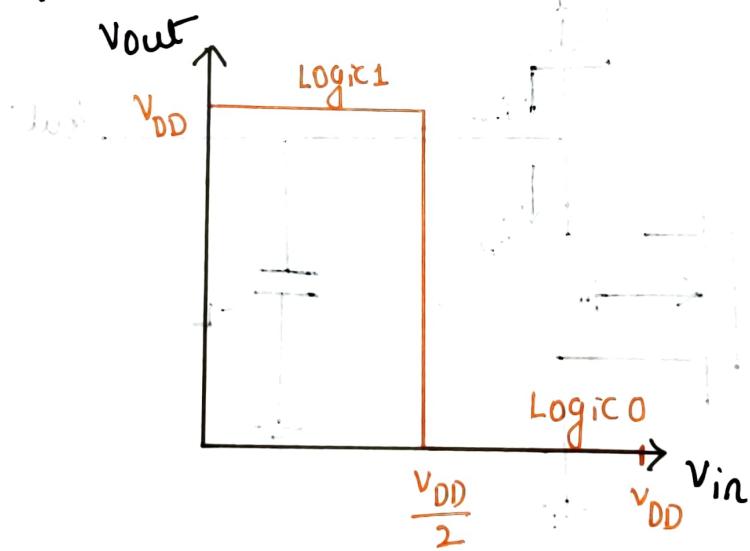
Introduction to inverters

- The logic symbol and truth table of inverter are shown in figure.



A	y
0	1
1	0

- Voltage transfer char



Logic 1 = "Vdd"

Logic 0 = "Gnd"

- VTC of ideal inverter is as shown in figure.

- V_{th} is called inverter threshold voltage

$$\text{ideally } V_{th} = \frac{V_{DD}}{2}$$

- If input voltage in between of V_{th}

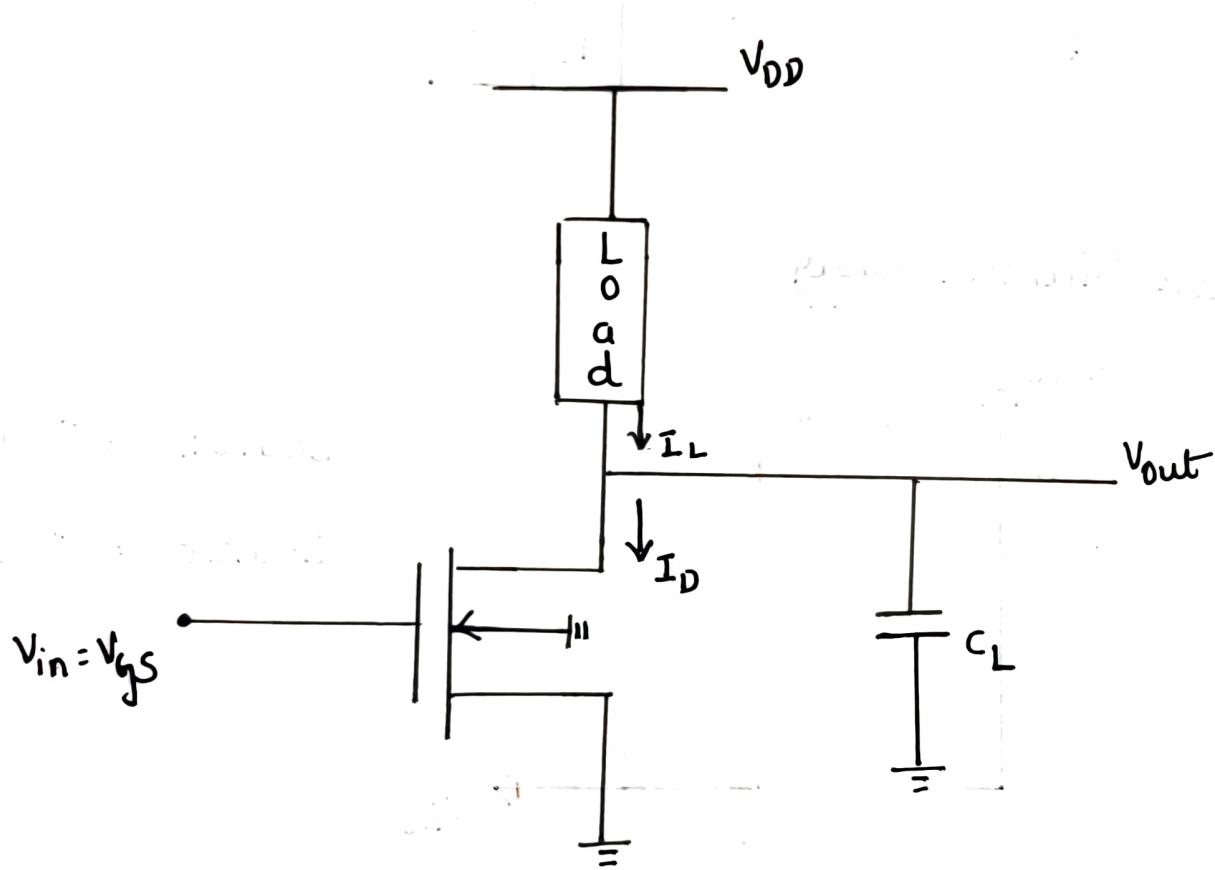
$$V_{out} = V_{DD}$$

→ If V_{in} is between V_{th} & V_{DD}

$$V_{out} = 0$$

→ O/p switches from V_{DD} to 0 when $V_{in} = V_{th} = \frac{V_{DD}}{2}$

→ The generic st of nMOS inverter is shown in fig.



→ For this circuit

$$\left. \begin{array}{l} V_{in} = V_{gs} \\ \text{and} \\ V_{out} = V_{DS} \end{array} \right\} \text{Bulk is connected to ground.}$$

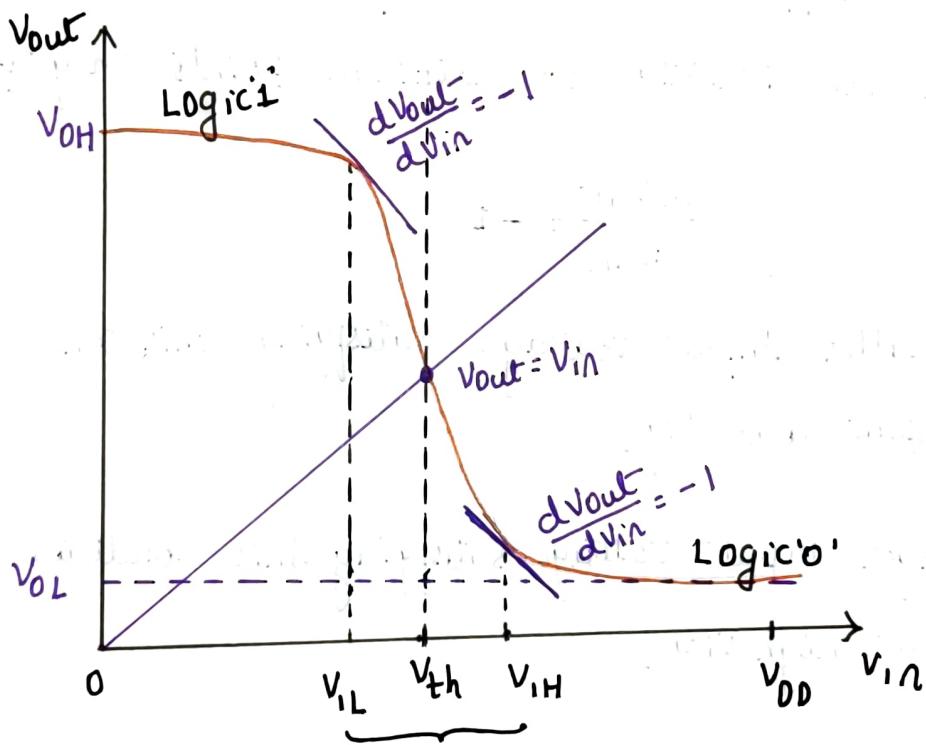
$$\therefore V_{SB} = 0 = V_S - V_B$$

$$0 - 0 = 0$$

→ In generalized representation, load device is a two terminal

circuit element with terminal current I_L and terminal voltage V_L

- One terminal of load device is connected to drain terminal of nMOS while other terminal connected to V_{DD} .
- Out terminal of inverter is connected to i/p of other inverter therefore impedance seen is capacitance.
- VTC of realistic MOS inverter is shown in figure.



transition from
Logic 1 to Logic 0.

- VTC voltage transfer char is a graph which is a variation of V_{out} as a function of V_{in} .
- There are several significant difference between ideal and practical inverter VTC

- When 1/p vtg is very low nMOS acts as open switch $\therefore I_L = 0 ; V_L = 0$
 - $\therefore V_{out} = V_{OH}$
 - As V_{in} vtg increases driver transistor starts conducting and 0/p vtg eventually starts to decrease
 - This drop doesn't happen abruptly as in case of ideal inverter. it happens with finite slope
 - Here we can identify two critical points on graph
- $$\frac{dV_{out}}{dV_{in}} = -1$$
- The smaller input voltage satisfying this condition is called V_{IL} input low vtg.
 - The larger input voltage satisfying this condition is called V_{IH} input high vtg.
 - Both these play significant role in noise margin determination
 - When 1/p vtg is further increased and 0/p vtg further drops and reaches V_{OL} when $V_{in} = V_{OH}$.
 - When $V_{in} = V_{th}$

$$V_{out} = V_{in}$$

→ Thus we have ⑤ critical V_{TG}.

V_{OH} : Maximum O/p V_{TG} when Output level is logic 1

V_{OL} : Minimum O/p V_{TG} when output level is logic 0

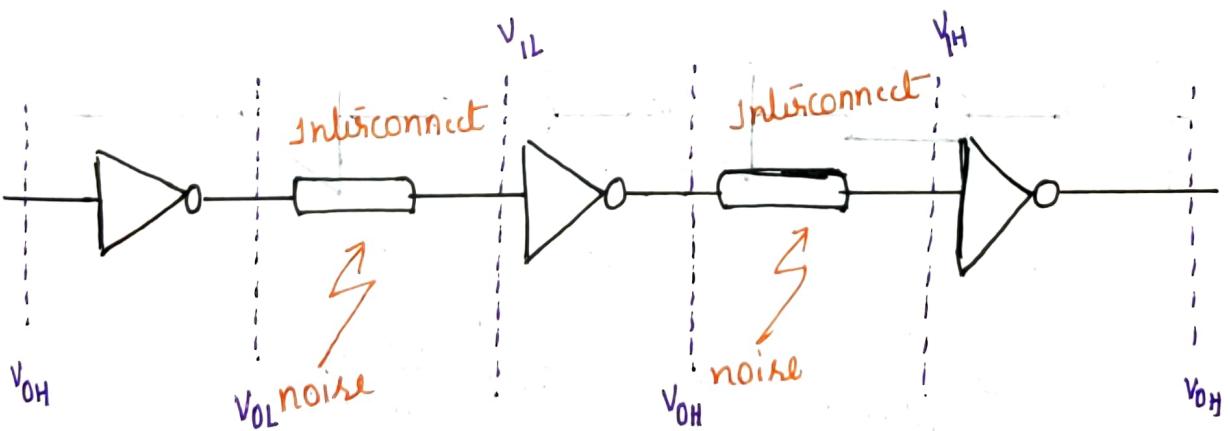
V_{IL} : Maximum S/p V_{TG} which can be interpreted as logic 0

V_{IH} : Minimum S/p V_{TG} which can be interpreted as logic 1

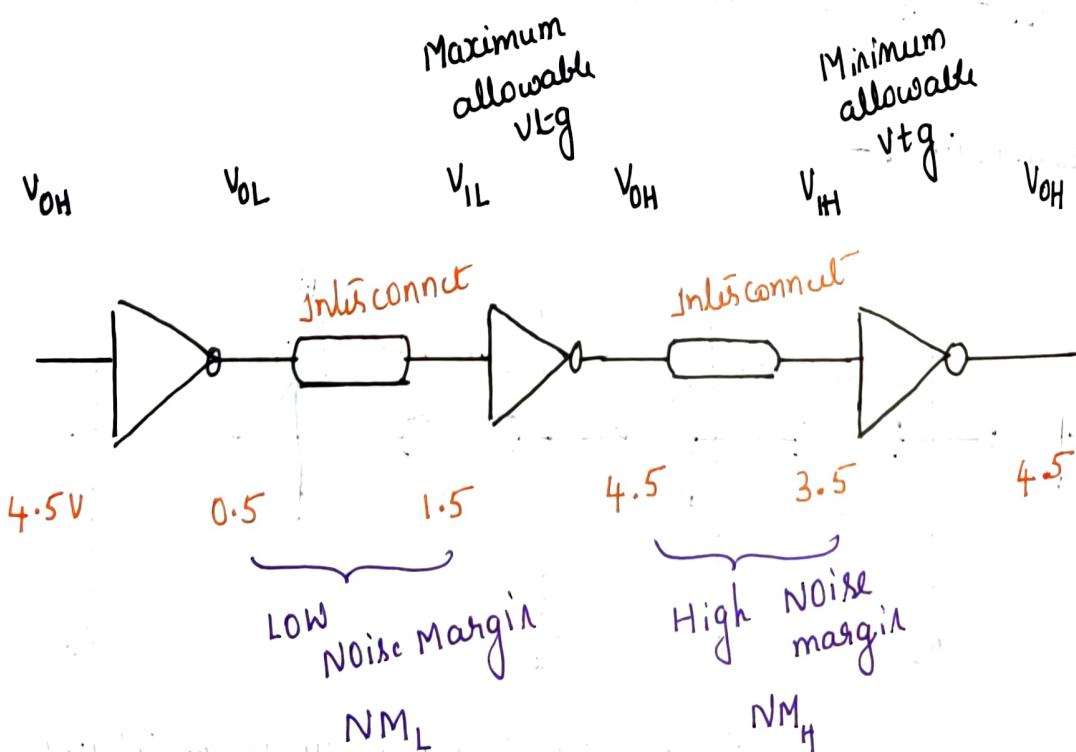
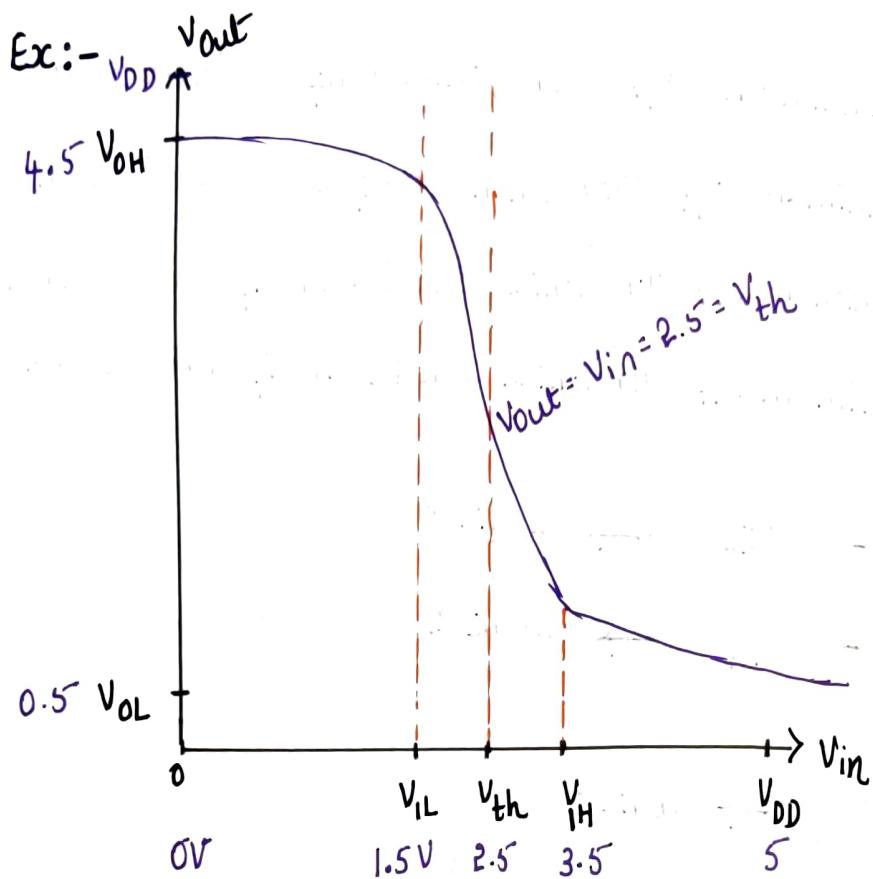
* $0V - V_{IL} \rightarrow \text{Logic 0}$ }
 $V_{DD} - V_{IH} \rightarrow \text{Logic 1}$ } S/p

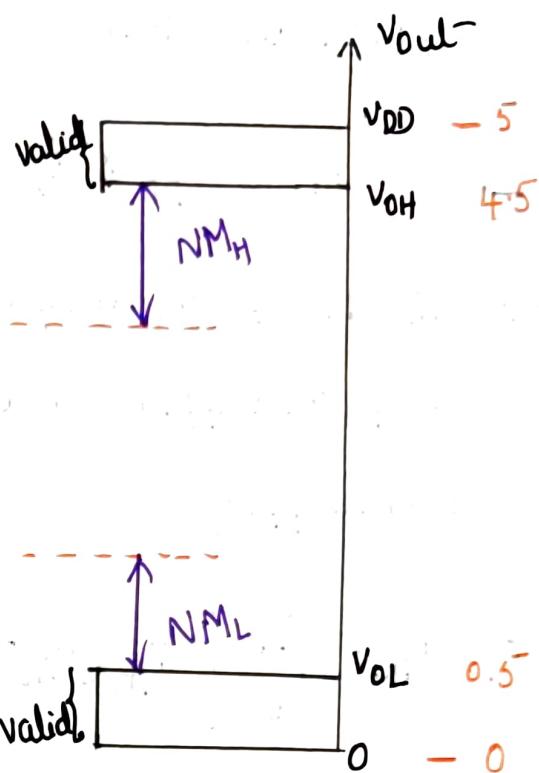
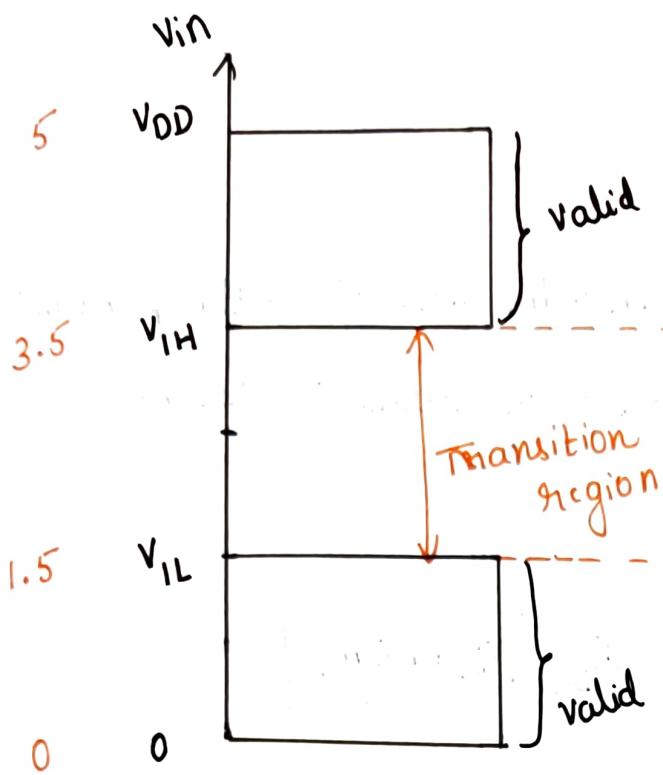
$0 - V_{OL} \rightarrow \text{logic 0}$ } O/p
 $V_{DD} - V_{OH} \rightarrow \text{logic 1}$

Noise margin :-



Propagation of digital signal under the influence of noise.





$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

→ In general

$$V_{out} = f(V_{in})$$

→ With noise

$$V'_{out} = f(V_{in} + \Delta V_{noise})$$

→ Using Taylor expansion

$$V'_{out} = f(V_{in}) + \frac{dV_{out}}{dV_{in}} \Delta V_{noise} + \text{higher order terms}$$

(neglected)

Perturbed O/p = nominal O/p + gain x External Perturbation.

power and area

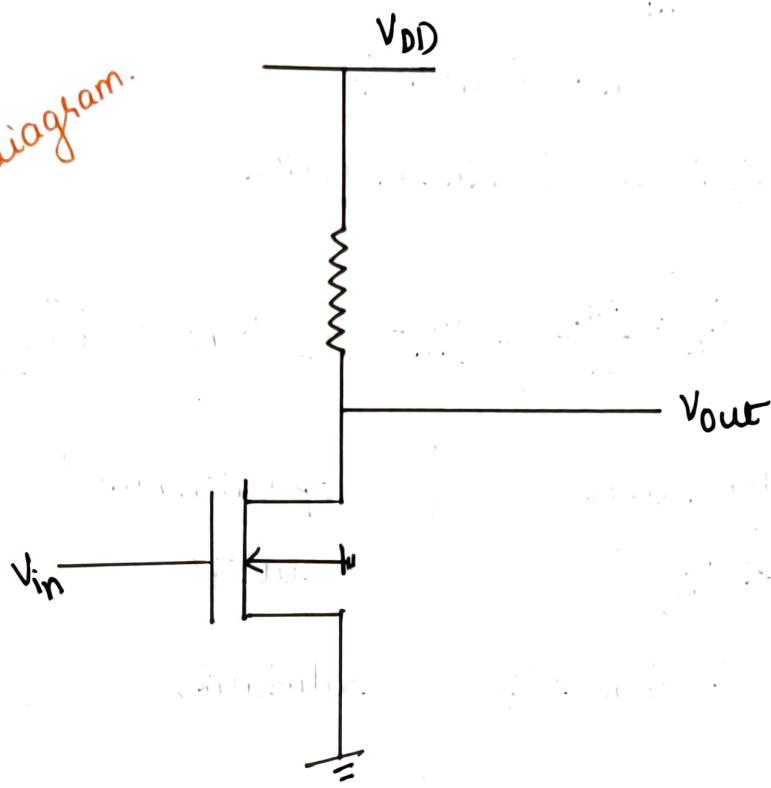
$$\rightarrow P_{DC} = V_{DD} \times I_{DC}$$

\rightarrow The D.C. power dissipation of inverter circuit is the product of power supply voltage and amount of current drawn from supply.

$$\rightarrow P_{DC} = \frac{V_{DD}}{2} \left[I_{DC} (v_{in} = \text{Low}) + I_{DC} (v_{in} = \text{High}) \right]$$

Resistive Load Inverter

Circuit diagram.



- The basic alt of resistive load inverter is shown in figure.
- The load is a simple resistor and driver is nMOS enhancement mode MOSFET.
- For s/p v_{tg} smaller than V_{TO} transistor is cutoff and does not conduct any drain current since $V_{RD} = 0$ $V_{out} = V_{DD}$
- When $V_{in} > V_{TO}$, MOSFET switched in saturation
- $$\therefore I_R = \frac{k_n}{2} [V_{in} - V_{TO}]^2 \dots \dots \dots \textcircled{1}$$
- With increasing s/p v_{tg} drain current also increases and o/p v_{tg} V_{out} starts to drop.

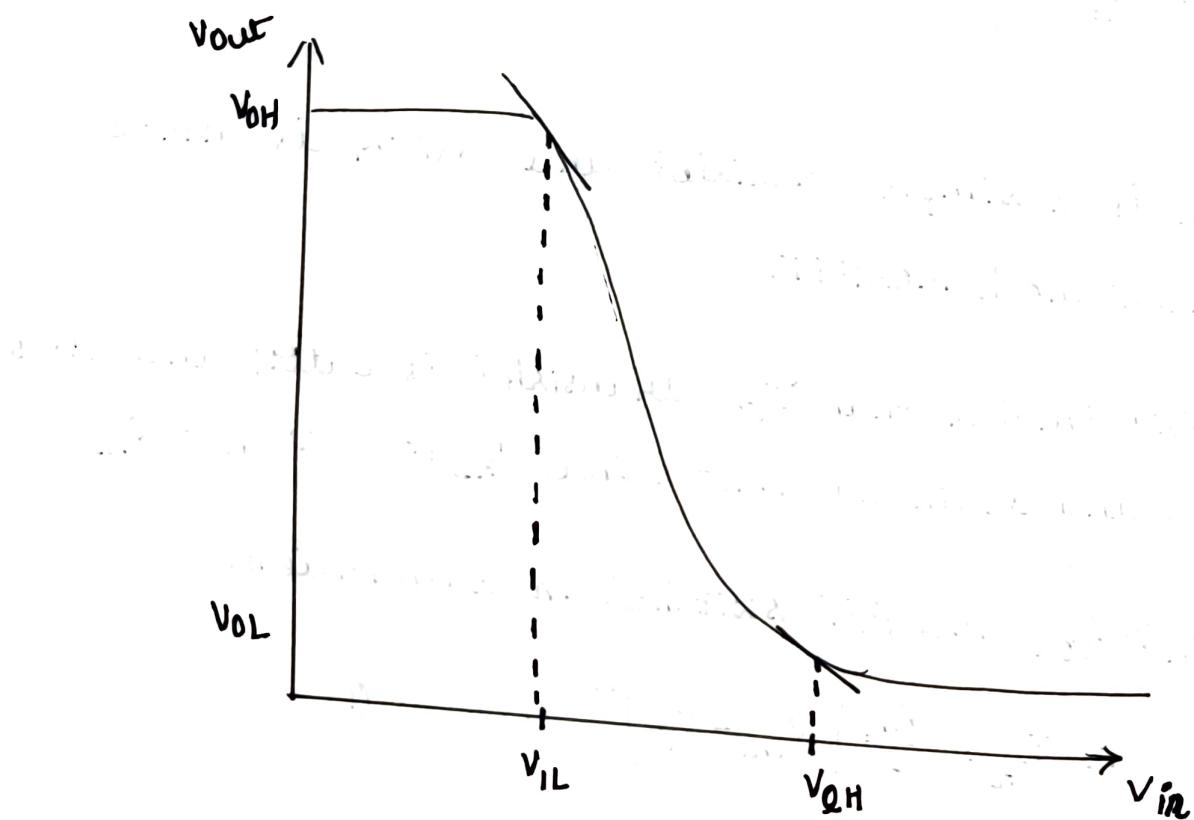
→ When $V_{in} > V_{IH}$

OR $V_{in} > V_{out} + V_{TO}$

→ driver MOSFET enters linear region

$$I_R = \frac{K_n}{2} \left[2(V_{in} - V_{TO}) V_{out} - V_{out}^2 \right]$$

IP Vtg range	Operating mode
$V_{in} < V_{TO}$	Cut off
$V_{TO} < V_{in} < V_{out} + V_{TO}$	Saturation
$V_{in} > V_{out} + V_{TO}$	Linear.



I $V_{OH} :-$

apply K.V.L. to loop

$$V_{out} = V_{DD} - I_D R_D$$

\rightarrow In cutoff $I_D \approx 0$

$$V_{out} = V_{OH} = V_{DD}$$

II $V_{OL} :-$

\rightarrow To attain $V_{OL} = V_{out}$

$$V_{in} = V_{OH} = V_{DD}$$

\rightarrow MOSFET Operates in Linear region

$$I_R = \frac{K_n}{2} \left[(V_{GS} - V_{TO}) 2V_{DS} - V_{DS}^2 \right]$$

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{K_n}{2} \left[(V_{DD} - V_{TO}) V_{OL} - V_{OL}^2 \right]$$

$$2 \frac{V_{DD}}{R_L} - 2 \frac{V_{OL}}{R_L} = K_n 2(V_{DD} - V_{TO}) V_{OL} - K_n V_{OL}^2$$

$$\frac{K_n R_L}{2} V_{OL}^2 - \frac{K_n R_L}{2} \left[(V_{DD} - V_{TO}) \right] V_{OL} - V_{OL} + V_{DD} = 0$$

$$\frac{K_n R_L}{2} V_{OL}^2 - \frac{K_n R_L}{2} \left[2(V_{DD} - V_{TO}) + \frac{2}{K_n R_L} \right] V_{OL} + \frac{2}{K_n R_L} V_{DD} = 0$$

$$V_{OL}^2 - 2 \left[V_{DD} - V_{TO} + \frac{1}{K_n R_L} \right] V_{OL} + \frac{2}{K_n R_L} V_{DD} = 0$$

$$V_{OL} = \frac{+2 \left[V_{DD} - V_{TO} + \frac{1}{K_n R_L} \right] + \sqrt{4 \left(V_{DD} - V_{TO} + \frac{1}{K_n R_L} \right)^2 - 4 \left(\frac{2}{K_n R_L} V_{DD} \right)}}{2}$$

$$\therefore V_{OL} = \left(V_{DD} - V_{TO} + \frac{1}{K_n R_L} \right) \pm \sqrt{\left(V_{DD} - V_{TO} + \frac{1}{K_n R_L} \right)^2 - \frac{2 V_{DD}}{K_n R_L}}$$

III V_{IL}

$\rightarrow V_{IL}$ is the smaller of two s/p vgs at which slope = -1

$$\frac{dV_o}{dV_i} = -1$$

$V_{in} = V_{IL}$ @ this point MOS in satⁿ

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{K_n}{2} \left[V_{IL} - V_{TO} \right]^2$$

differentiating this eqⁿ w.r.t. v_{in}

$$-\frac{1}{R_L} \frac{dV_{out}}{dv_{in}} = K_n \left[v_{IL} - V_{TO} \right]$$

$$-\frac{1}{R_L} (-1) = K_n (v_{in} - V_{TO})$$

$$V_{IL} = V_{TO} + \frac{1}{K_n R_L}$$

$$\begin{aligned} \frac{V_{out}}{[v_{in} = v_{IL}]} &= V_{DD} - I_0 R_L \\ &= V_{DD} - \frac{K_n}{2} \left[v_{IL} - V_{TO} \right]^2 R_L \\ &= V_{DD} - \frac{K_n}{2} \left[\cancel{V_{TO}} + \frac{1}{K_n R_L} - \cancel{V_{TO}} \right]^2 R_L \\ &= V_{DD} - \frac{1}{2 K_n R_L} \end{aligned}$$

IV v_{IH} :

$$v_{in} = v_{IH} \quad (\text{Linear})$$

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{K_n}{2} \left[2(v_{in} - V_{TO}) V_{out} - \frac{V_{out}^2}{2} \right]$$

diff above eqⁿ w.r.t. V_{in} .

$$-\frac{1}{R_L} \frac{dV_0}{dV_{in}} = \frac{K_n}{2} \left[2(V_{in} - V_{T0}) \frac{dV_0}{dV_{in}} + 2V_{out} - 2V_{out} \frac{dV_0}{dV_{in}} \right]$$

$$\frac{dV_0}{dV_{in}} = -1$$

$$\frac{1}{R_L} = \frac{K_n}{2} \left[2[V_{IH} - V_{T0}](-1) + 2V_{out} + 2V_{out} \right]$$

$$\frac{1}{R_L} = \frac{K_n}{2} \left[(V_{IH} - V_{T0})(-1) + 2V_{out} \right]$$

$$V_{IH} = 2V_{out} + V_{T0} - \frac{1}{K_n R_L}$$

$$\frac{V_{out}}{V_{in} = V_{IH}} = \frac{V_{DD}}{V_{DD} - I_D R_L}$$

$$= V_{DD} - \frac{K_n R_L}{2} \left[(V_{IH} - V_{T0}) 2V_{out} - V_{out}^2 \right]$$

$$\frac{V_{DD} - V_{out}}{R_L} = V_{DD} - \frac{K_n R_L}{2} \left[(2V_{out} + V_{T0} - \frac{1}{K_n R_L} - V_{T0}) 2V_{out} - V_{out}^2 \right]$$

=

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{K_n}{2} \left[2(V_{IH} - V_{TO})V_{out} - \frac{V_{out}^2}{2} \right]$$

$$V_{DD} - V_{out} = \frac{K_n R_L}{2} \left[2 \left(2V_{out} + V_{TO} - \frac{1}{K_n R_L} - V_{TO} \right) V_{out} - \frac{V_{out}^2}{2} \right]$$

$$V_{DD} - V_{out} = \frac{K_n R_L}{2} \left[2V_{out}^2 - \frac{1}{K_n R_L} V_{out} - \frac{V_{out}^2}{2} \right]$$

$$V_{DD} - V_{out} = K_n R_L \left[\frac{3}{2} V_{out}^2 - \frac{1}{K_n R_L} V_{out} \right]$$

$$V_{out}^2 \left(\frac{3}{2} K_n R_L \right) - V_{out} - V_{DD} = 0$$

$$V_{out} = \frac{-D \pm \sqrt{D - 4 \left(\frac{3}{2} K_n R_L \right) (-1)V_{DD}}}{\frac{3}{2} K_n R_L}$$

$$= \frac{-D \pm \sqrt{D + 6 K_n R_L V_{DD}}}{\frac{3}{2} K_n R_L}$$

$$\sqrt{\frac{2 \cdot 6 K_n R_L V_{DD}}{3 K_n^2 R_L^2}}$$

$$= \sqrt{\frac{2 V_{DD}}{3 K_n R_L}}$$

$$= \frac{2}{3} \cdot \frac{1}{K_n R_L} + \sqrt{\frac{4}{9} \cdot \frac{1}{(K_n R_L)^2} + \frac{4}{9} \cdot \frac{1}{(K_n R_L)^2} \cdot \frac{6 K_n R_L V_{DD}}{3}}$$

$$V_{out} = \sqrt{\frac{2}{3} \cdot \frac{V_{DD}}{K_n R_L}}$$

→ V_{th} is calculated by substituting

$$V_{in} = V_{out} = V_{th}$$

→ at this point transistor in saturation

$$\therefore \frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \left[V_{in} - V_{TO} \right]^2$$

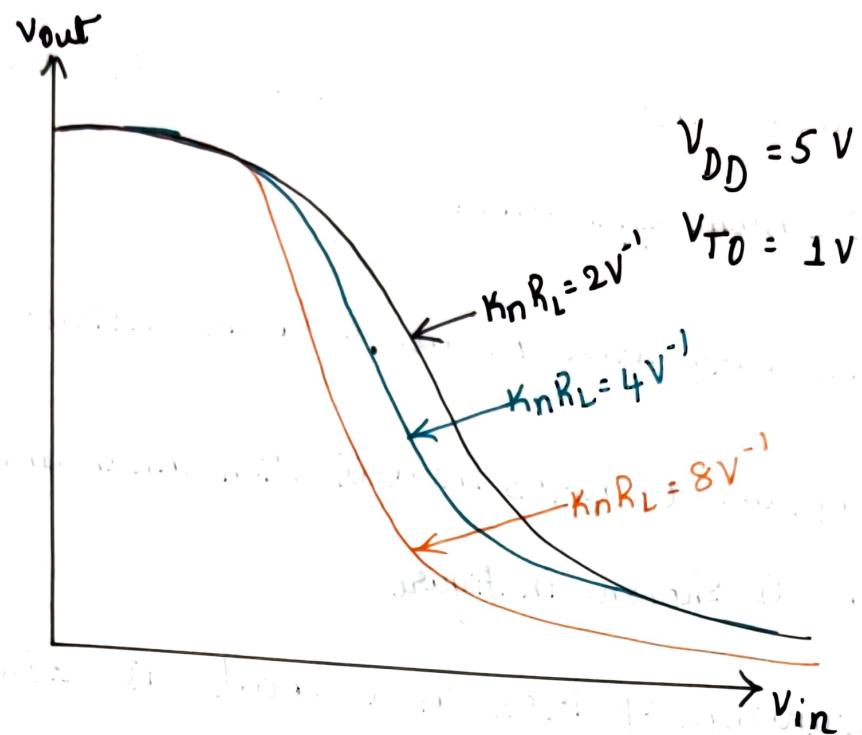
$$\frac{V_{DD} - V_{th}}{R_L} = \frac{k_n}{2} \left[V_{th} - V_{TO} \right]^2$$

$$V_{DD} - V_{th} = \frac{k_n R_L}{2} \left[V_{th}^2 + V_{TO}^2 - 2 V_{th} V_{TO} \right]$$

$$\frac{k_n R_L}{2} V_{th}^2 - (k_n R_L V_{TO} + 1) V_{th} + (V_{TO}^2 - V_{DD}) = 0$$

Solving this second Order equation solution to this
second Order equation is found.

→ The term $k_n R_L$ plays important role in the shape of VTC.



→ Larger the value of $k_n R_L$ V_{OL} becomes smaller and shape of VTC approaches the ideal inverter

Power consumption and chip area

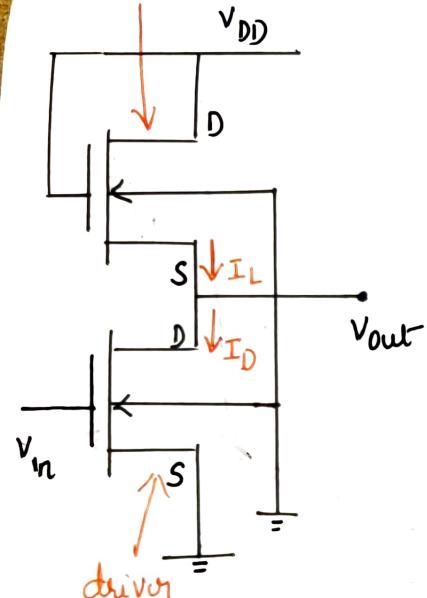
$$P_{DC} = \frac{V_{DD}}{2} \left[I_{DC} [V_{in} = \text{low}] + I_{DC} [V_{in} = \text{high}] \right]$$

$$= \frac{V_{DD}}{2} \left[\frac{V_{DD} - V_{out}}{R_L} \right]$$

Inverter with n-type MOSFET load.

- Resistive load inverter is not a suitable candidate for VLSI system applications.
- It consumes large area because of load resistor
- Circuit diagram of nMOS inverter with enhancement nMOS load is shown in figure.
- Main advantage of MOS as a load is reduced Silicon area.
- Inverter circuit with active load is better in overall performance compared to passive load inverter
- Circuit diagram of nMOS inverter with saturated load nMOS is shown in figure 1.
- Circuit of nMOS inverter with nMOS linear load is shown in figure 2.
- Depending on voltage applied to gate terminal load is either operated in linear or saturation region

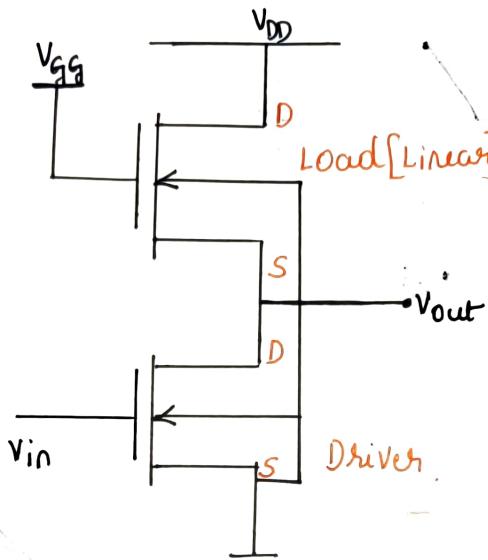
Load [Saturation]



V_{DD}

V_{GG}

Load [Linear]



→ Saturated enhancement load inverter

requires single power supply.

→ Simple fabrication process.

→ V_{OH} limited to $V_{DD} - V_{Tload}$.

→ Linear enhancement load inverter

requires two power supply.

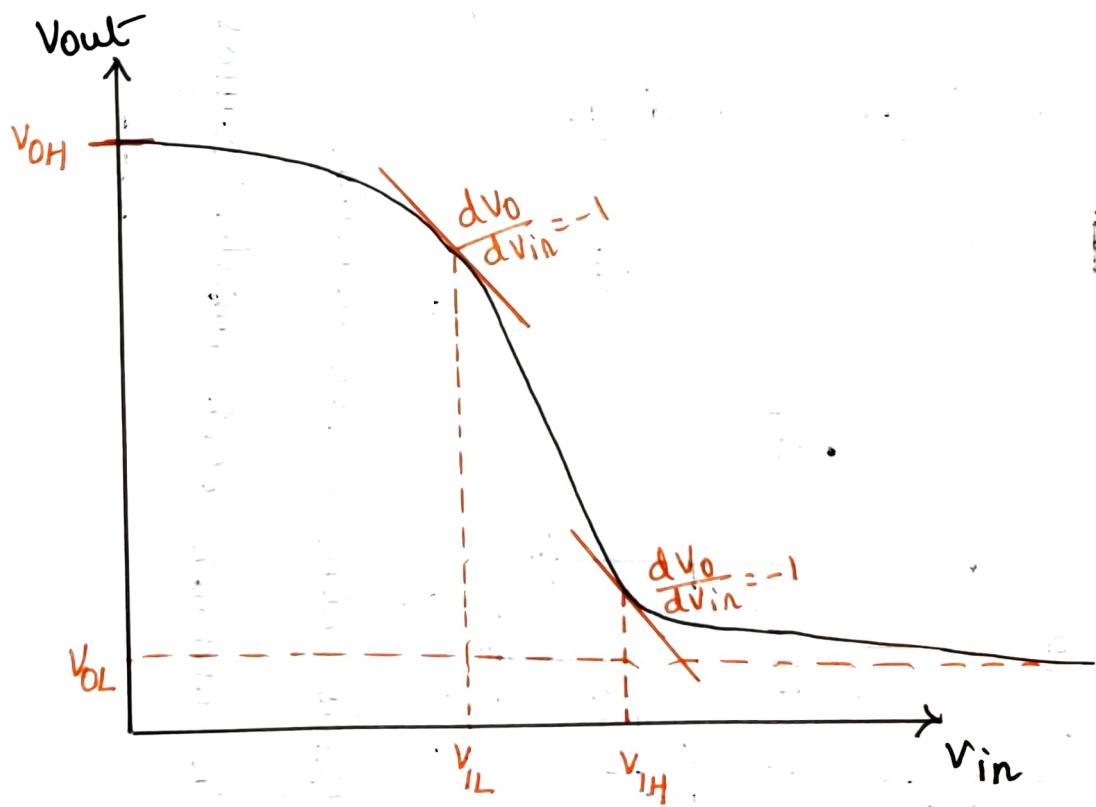
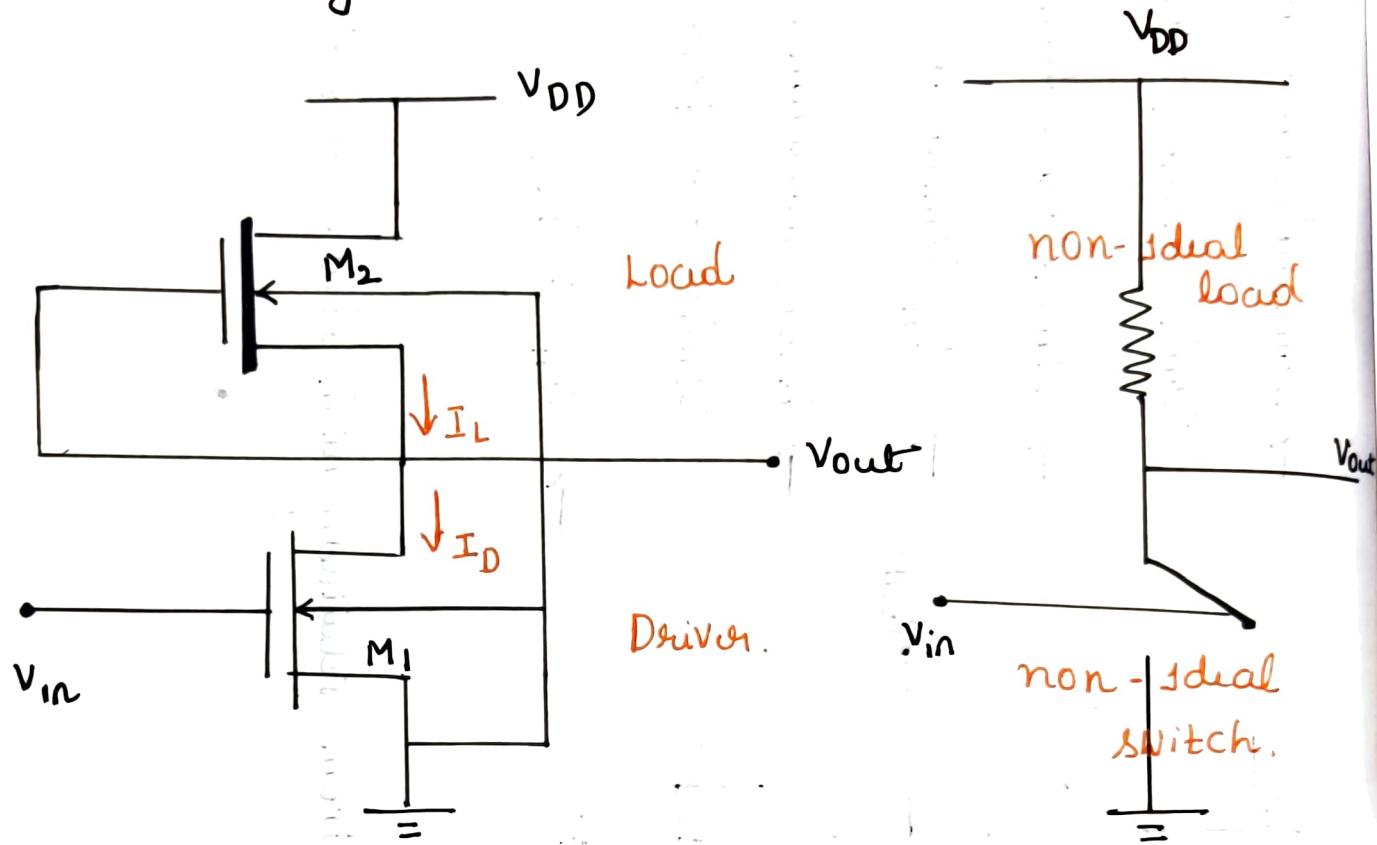
→ $V_{OH} \approx V_{DD}$.

→ yields high noise margin.

→ In addition both inverters suffer from relatively high stand-by power dissipation.

Depletion load nMOS inverter

Circuit diagram :-



V_{in}	V_{out}	Driver	Load
V_{OL}	V_{OH}	cutoff	Linear
V_{IL}	$\approx V_{OH}$	Saturation	Linear
V_{OH}	V_{OL}	Linear	Saturation
V_{IH}	\approx small	Linear	Saturation

→ Circuit diagram of depletion load MOS inverter is shown in figure.

→ here driver is a enhancement mode nMOS with $V_{T_{driver}} > 0$

→ Load is a depletion mode nMOS $V_{T_{load}} < 0$.

→ for load gate and source terminals are shorted

$$\therefore V_{GS} = 0. \text{ [always]}$$

$$\rightarrow V_{GS} = 0$$

$$\therefore V_{GS} > V_{T_{load}}$$

∴ load is always
have conducting
channel

$$V_{T_{load}} < 0$$

→ body terminal of both load and driver are connected
and since they are fabricated on same substrate.

→ ∵ of this condition always load MOSFET suffers from body effect.

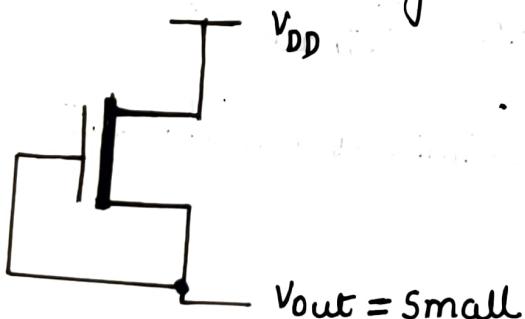
$$\therefore V_{Tload} = V_{TOload} + r \left[\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right]$$

$$V_{SB} = V_{out}$$

$$V_{Tload} = V_{TOload} + r \left[\sqrt{2\phi_F + V_{out}} - \sqrt{2\phi_F} \right]$$

→ Operating condition of load MOS is always depends on V_{out}

(i) When V_{out} is very small



$$V_{DS} = V_{DD}$$

$$V_g = V_{out} = \text{Small}$$

Condition:

$$V_{DS} > V_{GS} - V_{THload}$$

$$V_{DD} > V_{out} - V_{thload}$$

$$V_{out} < V_{DD} + V_{Tlocal}$$

∴ MOS operates in saturation

$$\therefore I_L = \frac{Kn}{2} \left[V_{GS} - V_{TH} \right]^2$$

$$= \frac{Kn}{2} \left[0 - V_{TLoad} \right]^2$$

$$I_L = \frac{Kn}{2} \left[|V_{TLoad}| \right]^2$$

ii) When V_{out} is very large

$$V_{DS} = V_{DD} - V_{out}$$

$$V_{DS} \approx \text{small}$$

$$\therefore V_{DS} < V_{GS} - V_{TH}$$

$$V_g \approx \text{Large } V_{out}$$

$$\therefore I_L = \frac{Kn}{2} \left[2(V_{GS} - V_{TH}) V_{DS} - V_{DS}^2 \right]$$

$$I_L = \frac{Kn}{2} \left[2(0 - V_{TLoad})(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2 \right]$$

I

V_{OH}

When $V_{in} < V_{T_{driver}}$

$M_1 - \text{Off}$

$M_2 - \text{Linear.}$

$$\therefore I_D = 0 = I_L$$

$$\boxed{\therefore V_{out} = V_{DD} = V_{OH}}$$

II

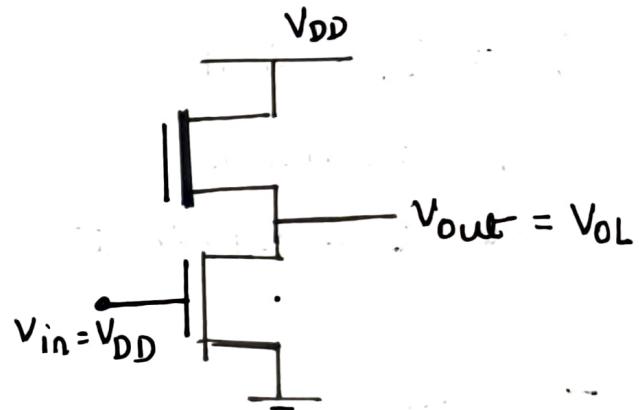
V_{OL}

$$V_{out} = V_{OL}$$

$$V_{in} = V_{DD}$$

$M_1 - \text{Linear.}$

$M_2 - \text{Saturation.}$



$$\therefore I_D = \frac{k_n}{2} \left[(V_{GS} - V_{Th}) V_{DS}^2 - V_{DS}^2 \right]$$

$$= \frac{k_n}{2} \left[(V_{DD} - V_{T_{driver}}) V_{OL} - V_{OL}^2 \right] \quad \text{--- (1)}$$

$$I_L = \frac{k_n l_{load}}{2} \left[|V_{T_{load}}|^2 \right]$$

$$I_D = I_L$$

$$\frac{k_{ndriver}}{2} \left[2(v_{DD} - v_{T_{driver}})v_{OL} - v_{OL}^2 \right] = \frac{k_{Tload}}{2} \left[|v_{T_{load}}|^2 \right]$$

$$v_{OL}^2 - 2(v_{DD} - v_{T_{driver}})v_{OL} + \frac{k_{nlocal}}{k_{ndriver}} |v_{T_{load}}|^2 = 0$$

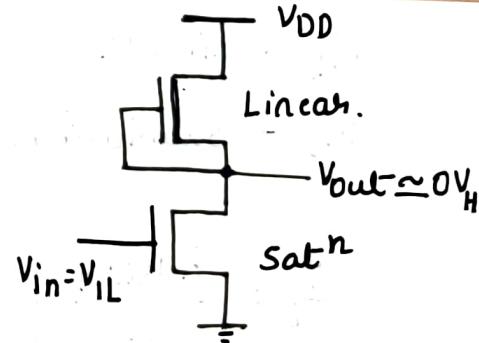
$$v_{OL} = \frac{+2(v_{DD} - v_{T_{driver}}) \pm \sqrt{4(v_{DD} - v_{T_{driver}})^2 - 4\left(\frac{k_{nlocal}}{k_{ndriver}} |v_{T_{load}}|^2\right)}}{2}$$

$$v_{OL} = (v_{DD} - v_{T_{driver}}) \pm \sqrt{(v_{DD} - v_{T_{driver}})^2 - \frac{k_{Tload}}{k_{ndriver}} |v_{T_{load}}|^2}$$

III

$$v_{IL}$$

$$I_D = \frac{k_{ndriver}}{2} \left[v_{IL} - v_{T_{driver}} \right]^2$$



$$I_L = \frac{k_{Tload}}{2} \left[2(0 - v_{T_{load}})(v_{DD} - v_{out}) - (v_{DD} - v_{out})^2 \right]$$

$$\frac{k_{ndriver}}{2} (v_{IL} - v_{T_{driver}})^2 = \frac{k_{Tload}}{2} \left[2|v_{T_{load}}|(v_{DD} - v_{out}) - (v_{DD} - v_{out})^2 \right]$$

diff. this eq^n w.r.t. v_{in}

$$\frac{k_{ndriver}}{2} 2(v_{IL} - v_{T_{driver}}) = \frac{k_{Tload}}{2} \left[2|v_{T_{load}}| - \frac{dv_0}{dv_{in}} + 2(v_{DD} - v_{out}) \frac{dv}{dv_{in}} \right]$$

$$-2(v_{DD} - v_{out}) \left(-\frac{dv_0}{dV_{in}} \right)$$

$$\frac{dv_0}{dv_i} = -1$$

$$k_{driver} (v_{IL} - v_{T_{driver}}) = \frac{k_{load}}{2} \left[2|v_{T_{load}}| - 2(v_{DD} - v_{out}) \right]$$

$$v_{IL} = v_{T_{driver}} + \frac{k_{load}}{k_{driver}} \left[v_{out} - v_{DD} + v_{T_{load}} \right]$$

v_{IH}

$$v_{in} = v_{IH}$$

$$v_{out} \approx v_{OL}$$

M₁ - Linear

M₂ - Saturation

$$I_D = \frac{k_{driver}}{2} \left[2(v_{IH} - v_{T_{driver}}) v_{out} - v_{out}^2 \right]$$

$$I_L = \frac{k_{load}}{2} \left[0 - v_{T_{load}} \right]^2$$

$$\frac{k_{driver}}{2} \left[2(v_{IH} - v_{T_{driver}}) v_{out} - v_{out}^2 \right] = \frac{k_{load}}{2} \left[|v_{T_{load}}|^2 \right]$$

$$\text{diff } c g^n \text{ w.r.t. } V_{in} \quad \frac{dv_0}{dv_i} = -1$$

$$\frac{K_{\text{driver}}}{2} \left[2(V_{IH} - V_{T\text{driver}}) \frac{dV_0}{dV_i} + 2V_{out} - 2V_{out} \frac{dV_0}{dV_i} \right]$$

$$= \frac{K_{\text{load}}}{2} \left[2|V_{T\text{load}}| \frac{dV_{T\text{load}}}{dV_0} \cdot \frac{dV_0}{dV_i} \right]$$

$$K_{\text{driver}} \left[(V_{IH} - V_{T\text{driver}}) + 2V_{out} \right] = K_{\text{load}} \left[|V_{T\text{load}}| \frac{dV_{T\text{load}}}{dV_0} \right]$$

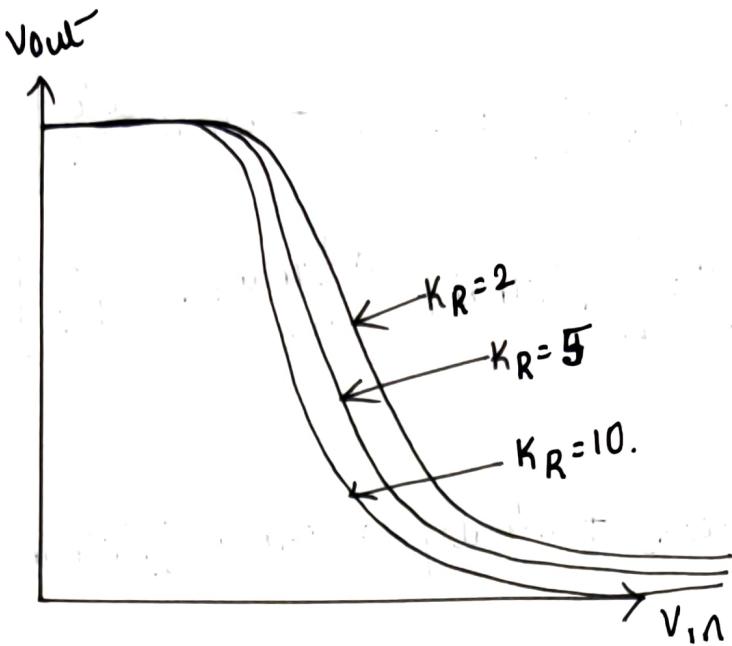
$$V_{IH} = V_{T\text{driver}} + 2V_{out} + \frac{K_{\text{load}}}{K_{\text{driver}}} |V_{T\text{load}}| \frac{dV_{T\text{load}}}{dV_{out}}$$

$$\frac{dV_{T\text{load}}}{dV_{out}} = \frac{V}{2\sqrt{2Q_F + V_{out}}}$$

$$K_R = \frac{K_{\text{driver}}}{K_{\text{load}}}$$

One imp observation that unlike enhancement mode MOSFET a sharp VTC transition and large N.M. can be obtained with relatively small driver to load ratios.

→ Thus relatively small area is occupied by depletion load MOSFET compared to enhancement f resistive load inverter



Design Of depletion load inverter

- i. Power supply V_{DD}
 - ii. $V_{T_{load}}$ $V_{T_{driver}}$
 - iii. $(\frac{W}{L})$ of load & driver
- External constraints
dictated by
others.

$\therefore K_R$ is the Only the design parameter

$$K_R = \frac{K_{driver}}{K_{load}}$$

$$K_R = \frac{K_{driver} \cdot \left(\frac{W}{L}\right)_{driver}}{K_{load} \cdot \left(\frac{W}{L}\right)_{load}}$$

→ For same
Process

$$K_R = \frac{\left(\frac{W}{L}\right)_{driver}}{\left(\frac{W}{L}\right)_{load}}$$

POWER AND AREA CONSIDERATIONS:-

$$P = \frac{V_{DD}}{2} \left[\frac{k_{load}}{2} \left[-|V_{Tload}| \right]^2 \right]$$

OR

$$P = \frac{V_{DD}}{2} \left[\frac{k_{driver}}{2} \left[2(V_{DD} - V_{Tdriver}) V_{OL} - V_{OL}^2 \right] \right]$$

$$1. NM_L = V_{IL} - V_{OL}$$

$$2. NM_H = V_{OH} - V_{IH}$$

$$3. V_{OH} = V_{DD} \quad \text{Resistive load Inverter}$$

$$4. V_{OL} = V_{DD} - V_{TO} + \frac{1}{K_n R_L} - \sqrt{\left(V_{DD} - V_{TO} + \frac{1}{K_n R_L}\right)^2 - \frac{2V_{DD}}{K_n R_L}}$$

$$5. V_{IL} = V_{TO} + \frac{1}{K_n R_L} \quad : V_{out} = V_{DD} - \frac{1}{2K_n R_L}$$

$$6. V_{IH} = V_{TO} + 2V_{out} - \frac{1}{K_n R_L} \quad V_{out} = \sqrt{\frac{2}{3} \frac{V_{DD}}{K_n R_L}}$$

$$V_{IH} = V_{TO} + \sqrt{\frac{8}{3} \frac{V_{DD}}{K_n R_L}} - \frac{1}{K_n R_L}$$

$$7. P_{dc} = \frac{V_{DD}}{2} \cdot \frac{V_{DD} - V_{OL}}{R_L}$$

$$8. V_{OH} = V_{DD} \quad \text{depletion nmos load Inverter}$$

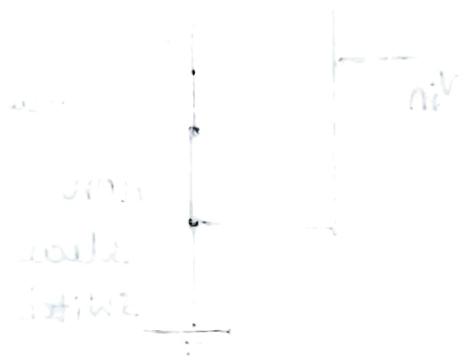
$$9. V_{OL} = V_{DD} - V_{TO} - \sqrt{(V_{OH} - V_{TO})^2 - \frac{K_{load}}{K_{driver}} |V_{Tload}|^2}$$

$$10. V_{IL} = V_{TO} + \frac{K_{load}}{K_{driver}} \left[V_{out} - V_{DD} + |V_{Tload}| \right]$$

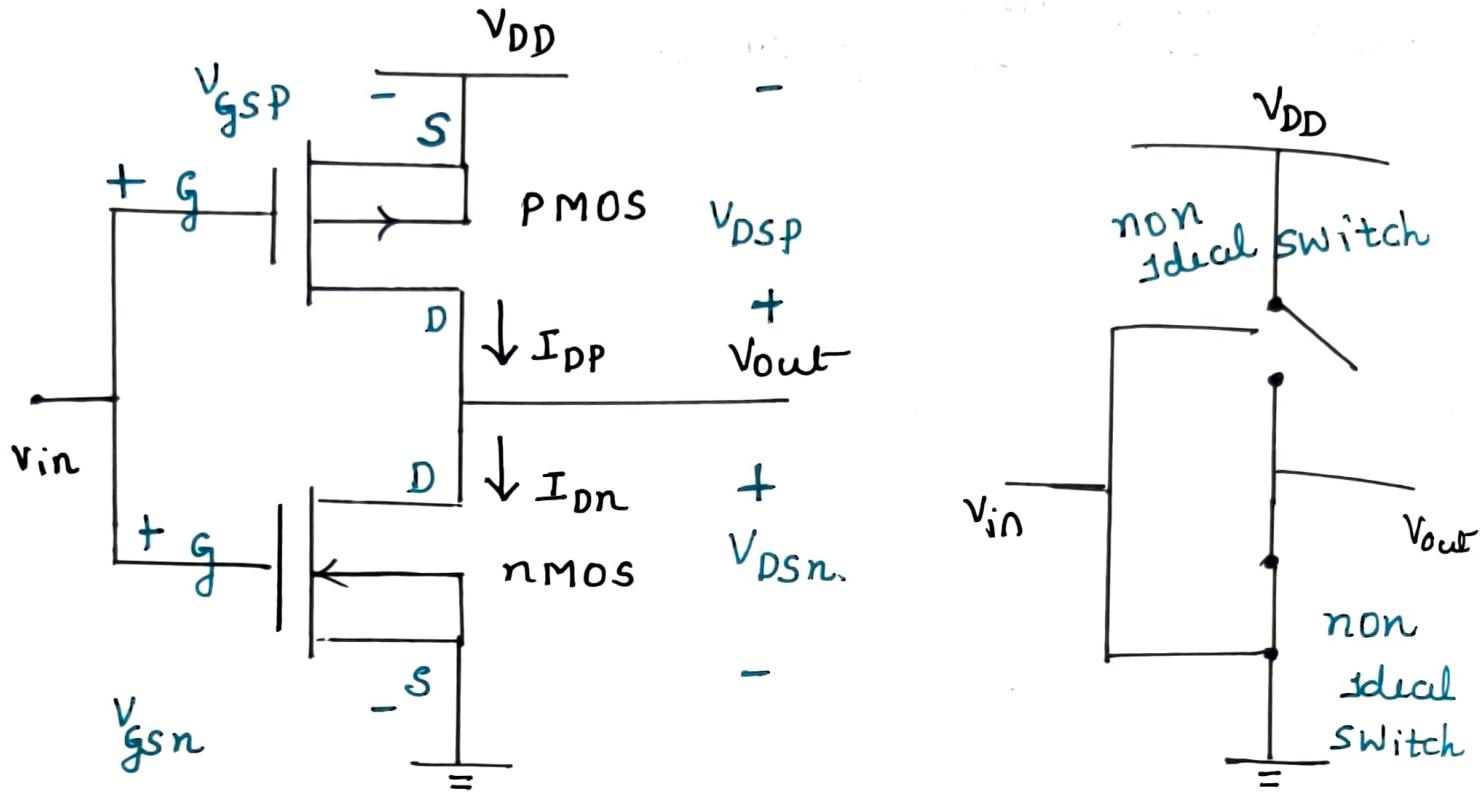
$$11. V_{IH} = V_{TO} + 2V_{out} + \frac{K_{load}}{K_{driver}} \left[|V_{Tload}| \right] \frac{dV_{Tload}}{dV_{out}}$$

$$12. \quad K_R = \frac{(w/L)_{\text{drive}}}{(w/L)_{\text{load}}}$$

$$13. \quad P_{dc} = \frac{V_{DD}}{2} \cdot \frac{K_{\text{local}}}{2} \left[|v_{T\text{load}}| \right]^2$$



CMOS Inverter :-



→ The circuit diagram of CMOS inverter is shown in figure.

→ It consists of enhancement mode nMOS & enhancement mode PMOS operating in complementary mode

→ ∴ it is called complementary MOS or CMOS

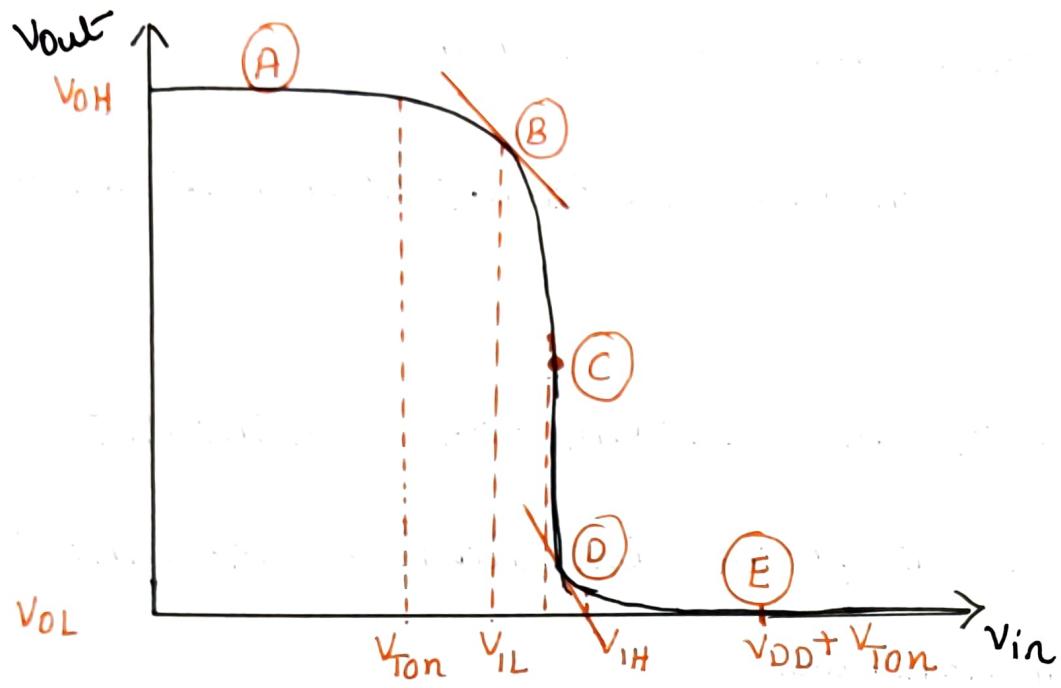
→ When I/P is logic 1 nMOS block drives O/P to logic low (pulls down) and PMOS acts as load.

- When S/p is logic 0 pMOS drives D/p to logic high (Pulls up) while nMOS acts as load
- consequently both MOS contributes equally to circuit operation.
- advantage of CMOS inverter over other inverter
 - (i) Steady state power dissipation of CMOS inverter is virtually negligible
 - (ii) VTC exhibits full voltage swing between OV to V_{DD} . VTC transition is usually sharp.

→ fabrication process of CMOS process is usually more complex than standard nMOS process.

Circuit Operation

- S/p v_{tg} is connected to gate of both nMOS & PMOS thus MOSFET's are directly fed from S/p.
- The substrate of nMOS is connected to ground & PMOS bulk is connected to V_{DD} in order to maintain MOSFET free from body effect.



Region	V_{in}	V_{out}	nMOS	PMOS
(A)	$< V_{Ton}$	V_{OH}	cutoff	linear
(B)	V_{IL}	$\approx V_{OH}$	Saturation	linear
(C)	V_{th}	V_{th}	Saturation	Saturation
(D)	V_{IH}	$\approx V_{OL}$	linear	sat ⁿ
(E)	$> V_{DD} + V_{Ton}$	V_{OL}	linear	cutoff

$$\rightarrow V_{GSn} = V_{in}$$

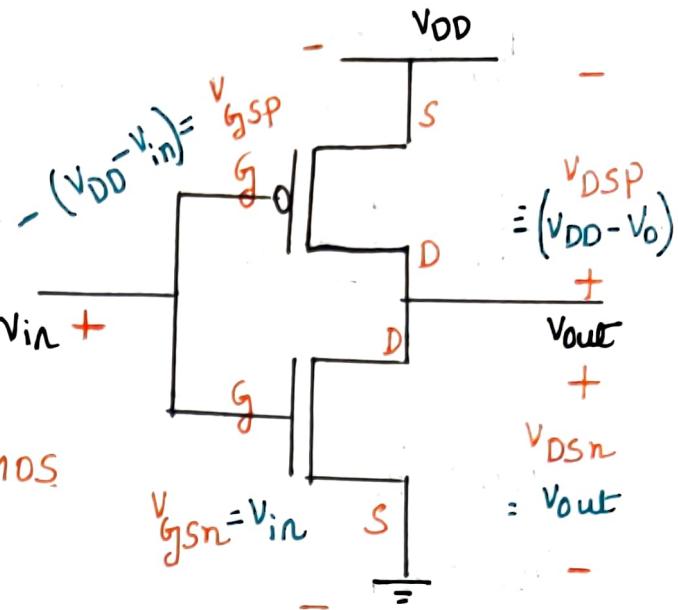
$$V_{DSn} = V_{out}$$

} nMOS

$$\rightarrow V_{GSp} = -(V_{DD} - V_{in})$$

$$V_{DSP} = -(V_{DD} - V_{out})$$

} pMOS



Region A :-

$$V_{in} < V_{Ton}$$

$$V_{out} = V_{DD} = V_{OH}$$

$$nMOS = \text{off}$$

$$pMOS = \text{on [Linear]}$$

$$I_{Dn} = 0$$

$$I_{Dp} = 0$$

$$V_{DSP} = 0$$

$$V_{DSn} = V_{OH} = V_{out}$$

Region (B) :-

$$V_{in} = V_{IL}$$

nMOS Saturation

pMOS Linear.

$$I_{Dn} = \frac{k_n}{2} \left[v_{gsn} - v_{thn} \right]^2 \dots \dots 1$$

$$I_{DP} = \frac{k_p}{2} \left[2(v_{gsp} - v_{dhp})v_{dsp} - v_{dsp}^2 \right] \dots \dots 2$$

$$v_{gsn} = v_{IL}$$

$$v_{dsn} = v_{out}$$

$$v_{gsp} = v_{in} - v_{DD}$$

$$v_{dsp} = v_{out} - v_{DD}$$

$$I_{Dn} = \frac{k_n}{2} \left[v_{IL} - v_{thn} \right]^2 \dots \dots 1$$

$$I_{DP} = \frac{k_p}{2} \left[2(v_{in} - v_{DD} - v_{dhp})(v_{out} - v_{DD}) - (v_{out} - v_{DD})^2 \right]$$

$$I_{Dn} = I_{DP}$$

$$\frac{k_n}{2} \left[v_{IL} - v_{dhn} \right]^2 = \frac{k_p}{2} \left[2(v_{IL} - v_{DD} - v_{dhp})(v_{out} - v_{DD}) - (v_{out} - v_{DD})^2 \right]$$

differentiating eqn w.r.t. v_{in}

$$\frac{dv_o}{dv_i} = -1$$

$$\frac{K_n}{K_p} \alpha \left[V_{IL} - V_{thn} \right] = \left[2(V_{IL} - V_{DD} - V_{thp}) \left(+ \frac{dV_o}{dV_i} \right) + \alpha (V_{out} - V_{DD}) \right. \\ \left. - \alpha (V_{out} - V_{DD}) \frac{dV_o}{dV_i} \right]$$

$$\frac{K_n}{K_p} = K_R$$

$$K_R \not\propto \left[V_{IL} - V_{thn} \right] = \left[\not\propto (V_{DD} + V_{thp} - V_{IL}) + \not\propto (V_{out} - V_{DD}) \right]$$

$$K_R V_{IL} + V_{IL} = K_R V_{thn} + \alpha V_{out} - V_{DD} + V_{thp}$$

$$\boxed{V_{IL} = \frac{\alpha V_{out} - V_{DD} + K_R V_{thn} + V_{thp}}{1 + K_R}}$$

Region C

$$V_{in} = V_{th}$$

$$V_{out} = V_{th}$$

nMOS - Saturation

pMOS - Saturation

$$I_{Dn} = \frac{K_n}{2} \left[V_{gsn} - V_{thn} \right]^2 \dots \dots 1$$

$$I_{dp} = \frac{K_p}{2} \left[V_{gsp} - V_{thp} \right]^2 \dots \dots 2$$

$$V_{gsn} = V_{th}$$

$$V_{gsp} = V_{th} - V_{DD}$$

$$I_{Dn} = \frac{k_n}{2} \left[V_{in} - V_{thn} \right]^2$$

$$I_{DP} = \frac{k_p}{2} \left[V_{in} - V_{DD} - V_{thp} \right]^2$$

$$I_{Dn} = I_{DP}$$

$$\frac{k_n}{2} \left[V_{in} - V_{thn} \right]^2 = \frac{k_p}{2} \left[V_{in} - V_{DD} - V_{thp} \right]^2$$

$$V_{in} - V_{thn} = \pm \sqrt{\frac{k_p}{k_n}} \left[V_{in} - V_{DD} - V_{thp} \right]$$

$$V_{in} + V_{in} \sqrt{\frac{1}{K_R}} = \sqrt{\frac{1}{K_R}} V_{DD} + \sqrt{\frac{1}{K_R}} V_{thp} + V_{thn}$$

$$V_{in} = V_{th} = \frac{\sqrt{\frac{1}{K_R}} (V_{DD} + V_{thp}) + V_{thn}}{1 + \sqrt{\frac{1}{K_R}}}$$

Region D

$$V_{in} = V_{IH}$$

nMOS \rightarrow Linear

pMOS \rightarrow Saturation

$$I_{Dn} = \frac{K_n}{2} \left[(V_{gs} - V_{thn}) \alpha V_{ds} - V_{ds}^2 \right] \dots \dots \textcircled{1}$$

$$I_{DP} = \frac{K_p}{2} \left[V_{gs} - V_{dhp} \right]^2 \dots \dots \textcircled{2}$$

$$V_{gsn} = V_{IH}$$

$$V_{ds} = V_{out}$$

$$V_{gsp} = V_{IH} - V_{DD}$$

$$I_{Dn} = \frac{K_n}{2} \left[(V_{IH} - V_{thn}) \alpha V_{out} - V_{out}^2 \right]$$

$$I_{DP} = \frac{K_p}{2} \left[V_{IH} - V_{DD} - V_{dhp} \right]^2$$

$$I_{Dn} = I_{DP}$$

$$\frac{K_n}{2} \left[\alpha (V_{IH} - V_{dhn}) V_{out} - V_{out}^2 \right] = \frac{K_p}{2} \left[V_{IH} - V_{DD} - V_{dhp} \right]^2$$

differentiating eqn w.r.t. V_{in} $\frac{dV_0}{dV_i} = -1$

$$\frac{K_n}{2} \left[\alpha (V_{IH} - V_{dhn}) \frac{dV_0}{dV_i} + \alpha V_{out} - 2V_{out} \frac{dV_0}{dV_i} \right] = \frac{K_p}{2} \alpha \left[V_{IH} - V_{DD} - V_{dhp} \right]$$

$$\frac{K_n}{K_p} \left[-(V_{IH} - V_{thn}) + 2V_{out} \right] = \left[V_{IH} - V_{DD} - V_{thp} \right]$$

$$(2V_{out} + V_{thn})K_R + V_{DD} + V_{thp} = V_{IH}(1 + K_R)$$

$$V_{IH} = \frac{K_R(2V_{out} + V_{thn}) + V_{DD} + V_{thp}}{1 + K_R}$$

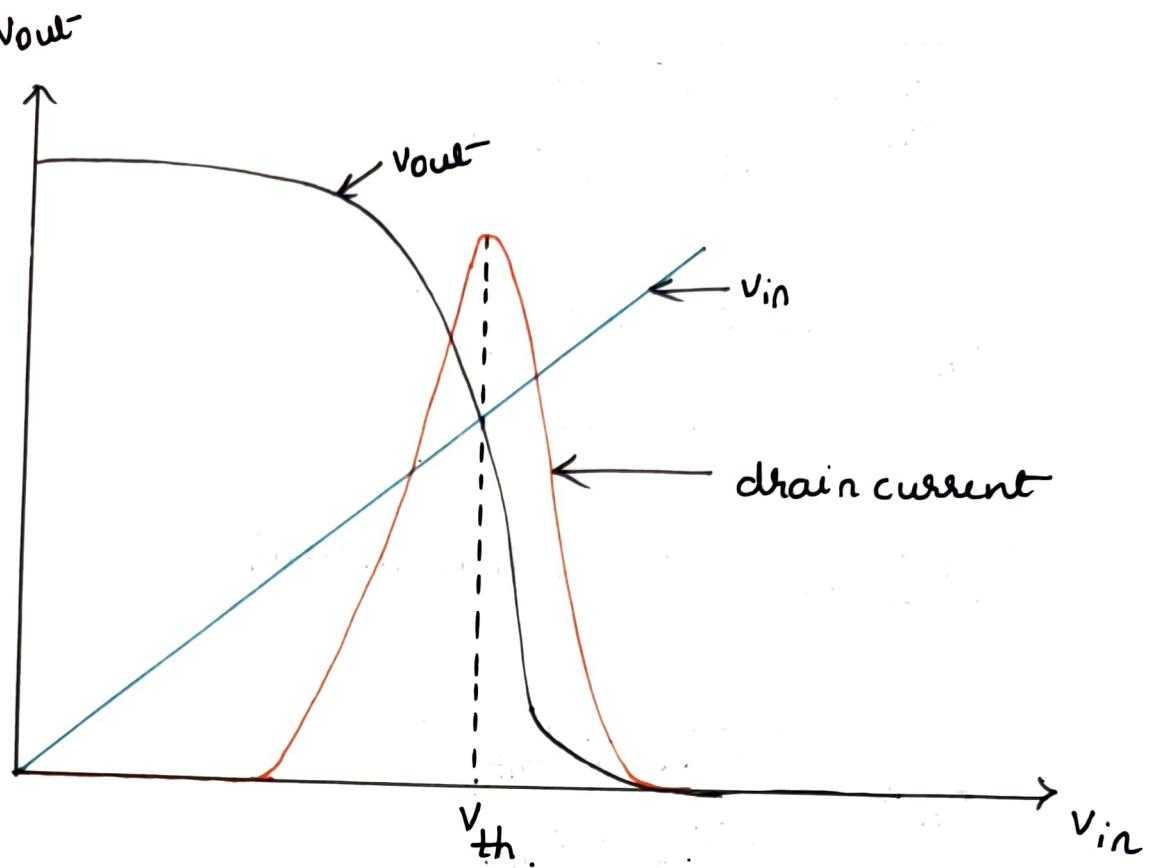
Region E

$$I_{gsn} > V_{out} + V_{thn}$$

nMOS - Linear

PMOS - cut off

$$V_{out} = V_{OL} = 0$$



Design of CMOS inverter

- Inverter threshold is therefore identified as one of the most important parameter that char steady state I/p - O/p behaviour of CMOS inverter
- V_{DD} swing of CMOS inverter is 0 - V_{DD}.
- noise margin is wide.

W.K.T.

$$V_{th} = \frac{\sqrt{\frac{1}{K_R}} (V_{DD} + V_{hp}) + V_{dn}}{1 + \sqrt{\frac{1}{K_R}}}$$

$$\sqrt{\frac{1}{K_R}} = \frac{V_{th} - V_{thn}}{V_{DD} + V_{thp} - V_{th}}$$

$$K_R = \left(\frac{V_{DD} + V_{thp} - V_{th}}{V_{th} - V_{thn}} \right)^2$$

$$V_{th} = \frac{1}{2} V_{DD} \quad \left[\text{for ideal inverter} \right]$$

$$K_R = \left(\frac{0.5 V_{DD} + V_{thp}}{0.5 V_{DD} - V_{thn}} \right)^2$$

For Symmetrical Inverters

$$V_{thn} = |V_{thp}|$$

$$\therefore K_R = 1$$

$$\frac{K_n}{K_p} = 1 \quad K_n = K_p$$

$$\frac{\mu_n C_{ox} \left(\frac{W}{L}\right)_n}{\mu_p C_{ox} \left(\frac{W}{L}\right)_p} = 1$$

$$2.5 \left(\frac{W}{L}\right)_n = \left(\frac{W}{L}\right)_p$$

→ For Symmetric Invertor

$$V_{IL} = \frac{1}{8} (3V_{DD} + 2V_{thn})$$

$$V_{IH} = \frac{1}{8} (5V_{DD} - 2V_{thn})$$

$$V_{OH} = V_{DD}$$

$$V_{OL} = 0$$

$$V_{IL} + V_{IH} = V_{DD} \quad \left[\text{for Symmetric Inv} \right]$$

$$NM_L = V_{IL} - V_{OL} = V_{IL}$$

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{IH}$$

Problems:-

- I. Consider CMOS inverter circuit with the following parameters

$$V_{DD} = 3.3 \text{ V}$$

$$V_{TO,n} = 0.6 \text{ V}$$

$$V_{TO,p} = -0.7 \text{ V}$$

$$K_n = 200 \frac{\mu\text{A}}{\text{V}^2}$$

$$K_p = 80 \frac{\mu\text{A}}{\text{V}^2}$$

Calculate noise margin of the circuit

$$K_n = \frac{K_n}{K_p} = 2.5 \neq 1 \quad \left. \begin{array}{l} \\ \\ \end{array} \right\} \therefore \text{it is not a symmetric inv}$$
$$V_{TO,n} \neq V_{TO,p}$$

i) $V_{OH} = V_{DD} = 3.3 \text{ V}$

ii) $V_{OL} = 0 \text{ V}$

iii) V_{IL}

W.K.T

$$V_{IL} = \frac{2V_{out} + V_{TO,p} - V_{DD} + K_R V_{TO,n}}{1 + K_R}$$

$$= \frac{2V_{out} - 0.7 - 3.3 + 2.5(0.6)}{3.5}$$

$$V_{IL} = 0.57V_{out} - 0.714$$

@ Region B

$$K_R \underbrace{\left[V_{GS} - V_{TO_n} \right]^2}_{\text{Sat } n} = 2 \underbrace{\left[(V_{GS} - V_{TOP}) V_{DS} - V_{DS}^2 \right]}_{\text{Linear } P}$$

$$2.5 \left[0.57V_{out} - 0.714 - 0.6 \right]^2 = 2 \left[(0.57V_{out} - 0.714 + 0.7)^{-3.3} \right. \\ \left. (V_{out} - 3.3) - (V_{out} - 3.3)^2 \right]$$

$$2.5 \left[0.57V_{out} - 1.314 \right]^2 = 2 \left[(0.57V_{out} - 3.314)(V_{out} - 3.3) \right. \\ \left. - (V_{out} - 3.3)^2 \right]$$

$$2.5 \left[0.3249V_{out}^2 + 1.726 - 1.49V_{out} \right]$$

$$= 2 \left[0.57V_{out}^2 - 1.881V_{out} - 3.314V_{out} + 10.936^2 \right. \\ \left. - V_{out}^2 - 10.89 + 6.6V_{out} \right]$$

$$0.81255V_{out}^2 + 4.315 - 3.725V_{out} = 0.14V_{out}^2 + 2.87V_{out} + 10.9876 - 3.79V_{out}$$

$$0.67 V_{out}^2 + 0.06 V_{out} - 6.66 = 0$$

$$\underline{\underline{V_{out}}} = 3.1 \text{ V}$$

$$\begin{aligned}\therefore V_{IL} &= 0.57 V_{out} - 0.714 \\ &= \underline{\underline{1.053 \text{ V}}}\end{aligned}$$

W.K.T.

$$V_{IH} = \frac{V_{DD} + V_{TO,p} + K_R (2V_{out} + V_{Ton})}{1 + K_R}$$

$$= \frac{3.3 - 0.7 + 2.5 (2V_{out} + 0.6)}{3.5}$$

$$= \underline{\underline{1.17 + 1.42 V_{out}}}$$

$$\frac{K_n}{2} \left[2(V_{gsn} - V_{dhn}) V_{dsn} - V_{dsn}^2 \right] = \frac{K_p}{2} \left[V_{gsp} - V_{hp} \right]^2$$

$$V_{gsn} = V_{IH} = 1.17 + 1.42 V_{out}$$

$$V_{dsn} = V_{out}$$

$$\begin{aligned}V_{gsp} &= V_{IH} - V_{DD} = 1.17 + 1.42 V_{out} - 3.3 \\ &= -2.13 + 1.42 V_{out}\end{aligned}$$

$$2.5 \left[2 \left(1.17 + 1.42 V_{\text{out}}^{-0.6} \right) V_{\text{out}} - V_{\text{out}}^2 \right] = \left[1.42 V_{\text{out}} - 2.13 + 0.7 \right]^2$$

$$2.5 \left[\frac{1.14 V_{\text{out}}}{2.34 V_{\text{out}}} + 2.84 V_{\text{out}}^2 - V_{\text{out}}^2 \right] = \left[2.0164 V_{\text{out}}^2 + 2.0449 - 4.0612 V_{\text{out}} \right]$$

$$4.6 V_{\text{out}}^2 + 2.85 V_{\text{out}} = 2.0164 V_{\text{out}}^2 - 4.0612 V_{\text{out}} + 2.0449$$

$$2.58 V_{\text{out}}^2 + \frac{6.91}{9.972} V_{\text{out}} - 2.044 = 0$$

$$\underline{\underline{V_{\text{out}} = 0.268}}$$

$$\therefore V_{IH} = 1.42 (0.268) + 1.17$$

$$= \underline{\underline{1.55 \text{ V}}}$$

$$\begin{aligned} \therefore NM_L &= 1.08 \text{ V} \\ NM_H &= 1.75 \text{ V} \end{aligned} \quad \left. \right\}$$

2. Design CMOS Inverter

$$V_{TOn} = 0.6 \text{ V}$$

$$V_{Top} = -0.7 \text{ V}$$

$$\mu_{nCox} = 60 \text{ mA/V}^2$$

$$\mu_{pCox} = 25 \text{ mA/V}^2$$

$$\left(\frac{W}{L}\right)_n = 8$$

$$\left(\frac{W}{L}\right)_p = 12$$

$$V_{DD} = 3.3 \text{ V}$$

$$V_{DD} = 5V$$

$$k_n' = 30 \mu A/V^2$$

$$V_{T_0} = 1V$$

$$V_{OL} = 0.2V$$

Determine $(\frac{W}{L})$ of driver in a resistive load
inverter

$$R_L = ?$$

$$V_{OH} = V_{DD} \rightarrow \text{cut-off}$$

$$V_{OL} = 0.2 \rightarrow \text{Linear} \rightarrow V_{in} = V_{DD}$$

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n'}{2} \left(\frac{W}{L} \right) \left[2(v_{gs} - v_{thn}) v_{ds} - v_{ds}^2 \right]$$

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{k_n'}{2} \left(\frac{W}{L} \right) \left[2 [v_{DD} - v_{thn}] v_{OL} - v_{OL}^2 \right]$$

$$\frac{5 - 0.2}{R_L} = \frac{30 \times 10^{-6}}{2} \left(\frac{W}{L} \right) \left[2 [5 - 1] 0.2 - 0.2^2 \right]$$

$$\frac{W}{L} \cdot R_L = 2.05 \times 10^5 \Omega$$

$\frac{W}{L}$	R_L	P_{dc} $\frac{V_{DD}}{2} \cdot \frac{V_{DD} - V_{OL}}{R_L}$
1	205.0	58.5
2	102.5	117.1

4) Consider a resistive load inverter

$$V_{DD} = 5V$$

$$K_n^{-1} = 20 \frac{mA}{V^2}$$

calculate critical v_{tg} on VTC if

$$V_{TO} = 0.8V$$

find

$$R_L = 200k\Omega$$

Noise margin.

$$\left(\frac{W}{L}\right) = 2$$

$$i. \quad V_{OH} = V_{DD} = 5V$$

$$ii. \quad V_{OL} = V_{DD} - V_{TO} + \frac{1}{K_n R_L} - \sqrt{\left(V_{DD} - V_{TO} + \frac{1}{K_n R_L}\right)^2 - \frac{2V_{DD}}{K_n R_L}}$$

$$= 5 - 0.8 + \frac{1}{20 \times 10^6 \times 2 \times 200 \times 10^3} - \sqrt{(5 - 0.8 + 0.125)^2 - \frac{10}{8}}$$

$$5 - 0.8 + 0.125$$

$$- 4.177$$

$$= 0.148V$$

$$V_{IL} = V_{TO} + \frac{1}{K_n R_L} = 0.8 + \frac{1}{8} = 0.925V$$

$$V_{IH} = V_{TO} + \sqrt{\frac{8}{3} \frac{V_{DD}}{K_n R_L}} - \frac{1}{K_n R_L}$$

$$= 0.8 + \sqrt{\frac{8 \times 5}{3 \times 8}} - \frac{1}{8}$$

$$= 1.965V$$

$$NM_L = 0.925 - 0.15 = 0.78V$$

$$NM_H = 5 - 1.97 = 3.03V$$

5) Design a resistive load inverter with $R = 1k\Omega$

$$V_{OL} = 0.6V$$

$$V_{DD} = 5V$$

$$V_{TO} = 1V$$

$$K_n' = 22 \frac{mA}{V^2}$$

Determine $\frac{W}{L}$ & N.M

→ To calculate $\frac{W}{L}$

When $V_{out} = \text{Logic 1}$

cutoff

$V_{out} = \text{Logic 0}$

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{K_n'}{2} \frac{W}{L} \left[2(V_{DD} - V_{TO}) V_{OL} - V_{OL}^2 \right]$$

$$\frac{5 - 0.6}{1000} = \frac{22 \times 10^{-6}}{2} \frac{W}{L} \left[2(5 - 1)0.6 - 0.6^2 \right]$$

$$4.4 \times 10^{-3} = 11 \times 10^{-6} \frac{W}{L} \left[4.8 - 0.36 \right]$$

$$\frac{W}{L} = \underline{\underline{90.09}}$$

$$V_{OH} = 5$$

$$V_{DL} = 0.6$$

$$V_{IL} = 1 + \frac{1}{22 \times 10^{-6} \times 90.09 \times 1 \times 10^3}$$

$$\underline{\underline{V_{IL} = 1.5}}$$

$$V_{IH} = 1 + \sqrt{\frac{8}{3} \times \frac{5}{\frac{0.5045}{1.98}}} - \cancel{\frac{1}{0.5045}} 1.98$$

$$= \underline{\underline{3.09V}}$$

6. calculate critical voltages f N.M. of the following
inverter

$$V_{DD} = 5$$

$$V_{T_{drive}} = 1$$

$$V_{T_{load}} = -3$$

$$\left(\frac{W}{L}\right)_d = 2$$

$$\left(\frac{W}{L}\right)_L = \frac{1}{3}$$

$$k'_{ndri} = k'_{nload} = 25 \frac{\mu A}{V^2}$$

$$V = 0.4$$

$$\phi_F = -0.3 \text{ V}$$

i) $V_{OH} = 5$

ii) $V_{OL} = V_{OH} - V_{TO} - \sqrt{(V_{OH} - V_{TO})^2 - \frac{k_L}{k_d} |V_{T_{load}}|^2}$

$$= 5 - 1 - \sqrt{(5 - 1)^2 - \frac{1}{6} |3^2|}$$

$$= 0.192 \text{ V}$$

$$V_{T\text{load}} = V_{T0\text{ load}} + V \left(\sqrt{2\phi_F + V_{OL}} - \sqrt{2\phi_F} \right)$$

$$= -3 + 0.4 \left(\sqrt{0.6 + 0.2} - \sqrt{0.6} \right)$$

$$= \underline{\underline{-2.95V}}$$

$$\therefore \underline{\underline{V_{OL} = 0.186V}}$$

$$111) \quad V_{IL} = V_{T0} + \frac{K_{load}}{K_{driver}} \cdot \left[V_{out} - V_{DD} + |V_{T\text{load}}| \right]$$

$$= 1 + \frac{1}{6} \left[V_{out} - 5 + \frac{236}{3} \right]$$

$$= 1 + 0.166 V_{out} - 0.33$$

$$V_{in} = V_{IL}$$

$$= 1.66 V_{out} + 0.566$$

$$V_{out} = V_{DD} = 5$$

$$V_{T\text{load}} = -3 + 0.4 \left[\sqrt{0.6 + 5} - \sqrt{0.6} \right] \Rightarrow$$

$$= \underline{\underline{-2.36V}}$$

$$\frac{K_{driver}}{2} (V_{IL} - V_{TO})^2 = \frac{K_{load}}{2} \left[2 | V_{Tload} | (V_{DD} - 6V_{IL} + 3.35) - (V_{DD} - 6V_{IL} + 3.35)^2 \right]$$

$$V_{IL} = \frac{0.98V}{1.36V} \rightarrow V_{IL} > V_{T_{driver}}$$

iV) V_{IH} $V_{in} = \text{high}$
 $V_{out} = \text{low}$

$$V_{Tload} = -2.95$$

$$V_{IH} = V_{TO} + 2V_{out} + \frac{K_{load}}{K_{driver}} \left[-V_{Tload}(V_{out}) \right] \frac{dV_{Tload}}{dV_{out}}$$

$$\frac{dV_{Tload}}{dV_{out}} = \frac{\sqrt{}}{2\sqrt{2}\phi_F + V_{out}} = 0.22$$

$$= 1 + 2V_{out} + \frac{1}{6} [-2.95 \cdot 0.22]$$

$$= 2V_{out} + 1.1$$

$$V_{out} = 0.5V_{IH} - 0.55$$

$$2(2(v_{IH} - 1)(0.5v_{IH} - 0.55) - (0.5v_{IH} - 0.55)^2] \\ = \frac{1}{3} 2.95^2$$

$$v_{IH} = -0.35 \\ \textcircled{2.43} \text{ valid}$$

$$NM_L = \cancel{2.57} 1.17V$$

$$\underline{\underline{NM_H = 2.57V}}$$