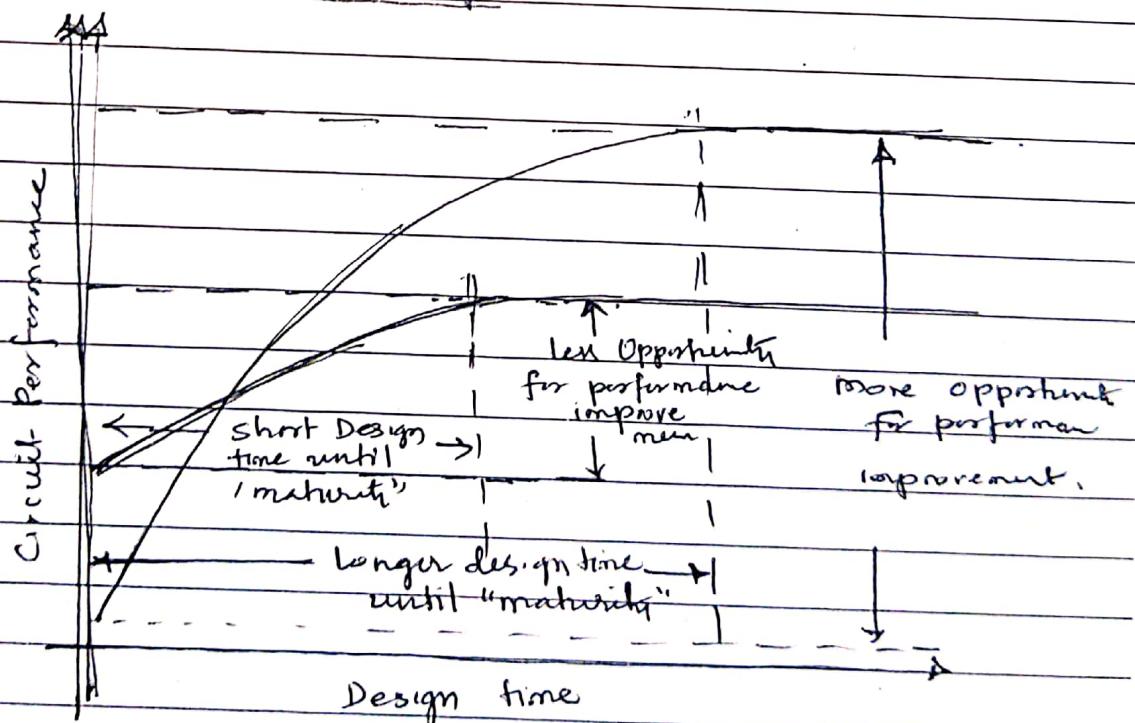


* Overview of Design methodologies :

- Complexity of integrated chip varies based on logic chips like microprocessor chips, digital signal processor (DSP) and Memory chips.
- DSP chips will have more complexity as they will have computation blocks as well as memory.
- Basically design complexity of logic chips increase almost exponentially with number of transistors to be integrated. This is translated into an increase into design cycle time.
- Design cycle time is the time period from start of chip development until the mask-type delivery time. In this, majority of time is devoted to achieving the desired level of chip performance at an acceptable cost, which is needed for economical success of any competitive commercial product.
- During the course of design cycle the circuit performance can be increased also by adapting improved designs. This happens more rapidly in the beginning and then more gradually until the performance finally saturates for a particular design style and technology used.
- The design cycle time and achievable ckt performance depends on VLSI design style used. Let us consider two different design styles and w.r.t cycle time & performance. The two design styles considered are:
 - i) Full custom design style → In this, the geometry and the placement of every transistor can be optimized individually.
 - ii) This requires longer time until design maturity can be reached. But, the inherent flexibility in geometry and placement so on allows more opportunity for ckt performance improvement during the design cycle.

- b) The final product typically has a high level of performance
i.e. high processing speed, low power dissipation
- c) The silicon area is relatively small because of better area utilization
- ii) Semi-custom design style - In this, designer use standard cells or FPGA for design. This allows
- Then A shorter design time until design maturity can be achieved.
 - In the early design phase, the design performance can be even higher than that of full custom design since some components will be already optimized
 - But, the semi custom design style offers less opportunity for performance improvement, and the overall performance of the final product will inevitably be less than that of a full - custom design.



The above graph shows impact of design style chosen on design time and performance. The choice of design style depends

i) Performance requirements.

ii) technology being used,

iii) Expected life time of product & cost of the project

On the other hand, if the design time is kept excessively longer to achieve the higher possible performance for the current generation of technology, there is danger of

i) Missing the next technology window, ~~but might~~ but, might be having better performance w.r.t the product designed with short design time for only short duration. as the product with short design time can be updated w.r.t next higher technology to improve performance. The upgradation of product designed using longer ~~to~~ designs time is not acceptable as it must be in market for certain time in order to recover the development costs. \therefore Advantages brought by next generation manufacturing technology cannot be utilized & the product becomes incompetitive.

- In reality

"design of next generation chip usually overlaps with production cycle of the current generation chip, thereby assuring continuity."

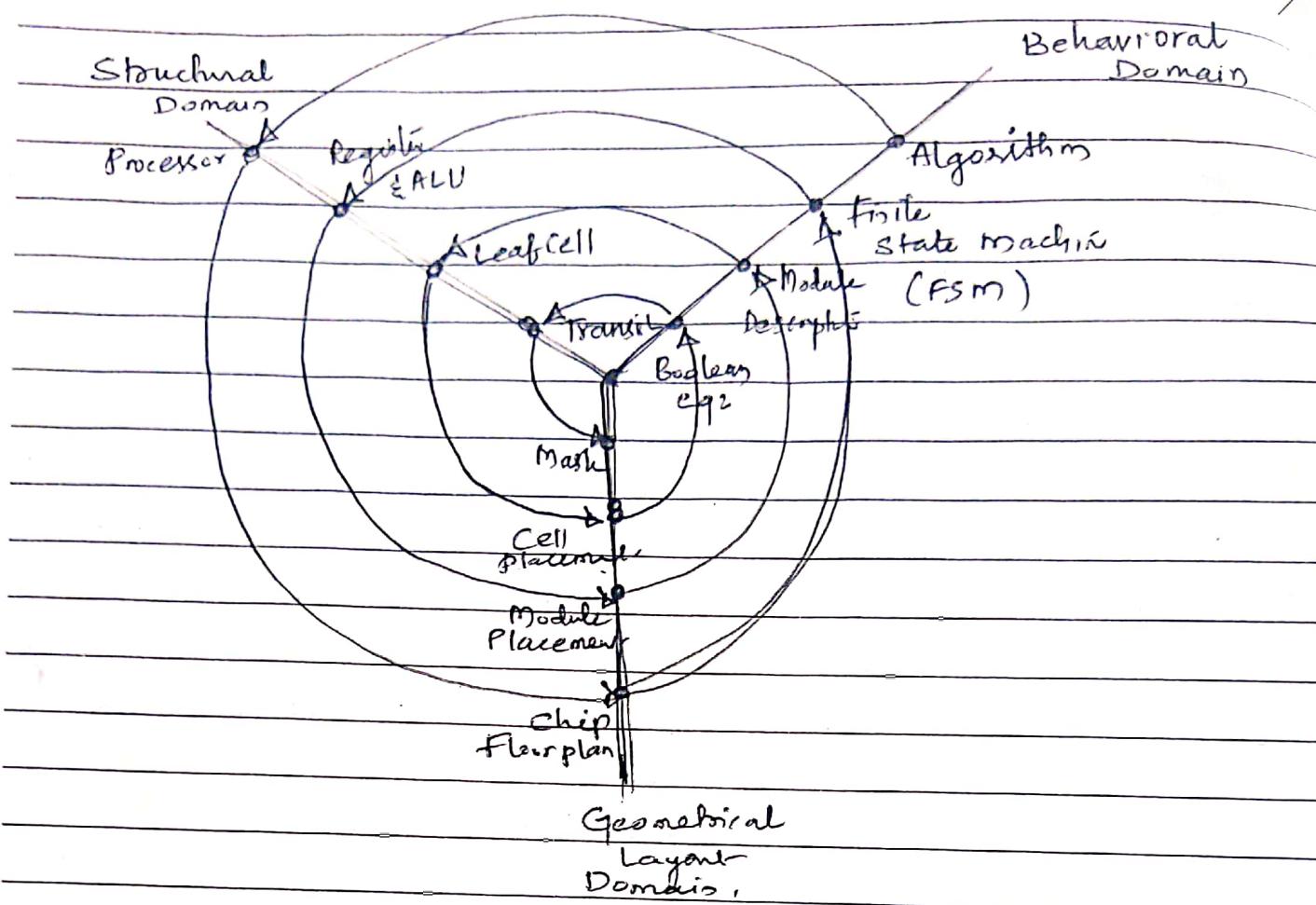
* VLSI Design Flow -

Y-chart illustrates a simplified design flow for most logic chips, using different design activities on three axes (domains) which resembles the letter 'Y'

Y chart consists of three domains of representation namely

- Behavioral domain
- Structural domain and
- Geometrical layout domain.

\rightarrow The design flows starts from the algorithm that describes the behavior of the target chip. (System specification). It is followed by corresponding architecture of the processor is first defined. & then mapped onto chip surface by floor planning.

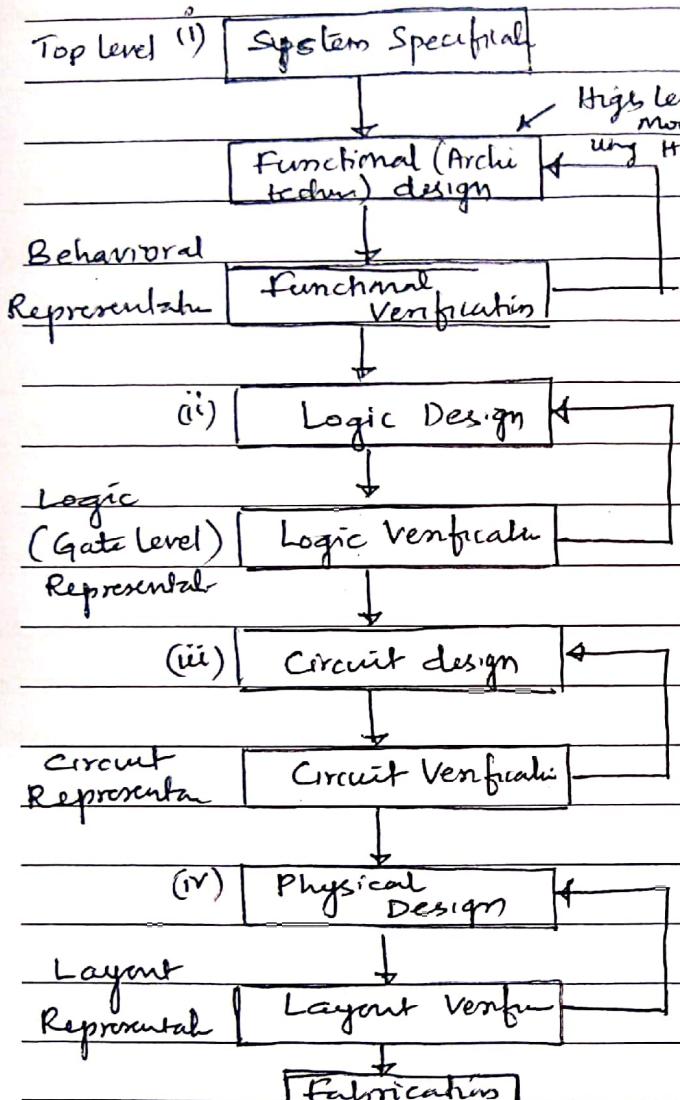


- Next design evolution is the behavioral domain defines FSM which are structurally implemented with functional modules as registers and ALUs. These modules are then geometrically placed onto ^{the} chip surface using CAD tools - for automatic module placement followed by routing with a goal of minimizing the interconnects area and signal delays.

- The third evolution starts with a behavioral module - description. Individual modules are then implemented with leaf cells. At this stage chip is described in terms of logic gates, which can be placed and interconnected using a cell placement and routing programs.

- The last evolution starts with detail boolean description of leaf cells followed by transistor level implementation of leaf cells of mask generation.

More simplified view of the VLSI design flow, taking into account the various representations, or abstractions of designs: behavioral, logic, circuit and mask layout.



- i) - A product is defined in both specific & general terms that provide design targets such as functions, speed, size, etc. for entire project.
- The system specifications are used to create an abstract, high level model using HDL & the functional verification is done.
- The abstract model contains information on behaviour of each block and interaction among the blocks in the system.
- The model is subjected extensive verification steps to ensure that it is correct.
- ii) The next level is to provide the logical design of the network by specifying the primitive gate and units needed to build each unit, and goes through logical verification to ensure that it is correct.
- iii) The logic level is design is basis for transforming the design to the electronic circuit level where bottom transistors are used as switches level and boolean variables are treated as varying voltage signals.

- iv) To create transistor, we move down to another level i.e physical design. In this level the network is built on a tiny area of silicon using complex mapping schemes that translated to transistors and wires into extremely fine line pattern of metals and other materials. and the physical design goes through verification process in which design rules (DRC), Layout Vs schematic (LVS), parasitic extraction so on is done to meet the given specification in number of iterations. and then finally sent for fabrication.

DATE

- Although the top-down design flow appears for design process, in reality, there is no truly truly uni-directional top-down design flow.

- Both, top-down and bottom-up approaches have to be combined for successful design

Ex: If a chip designer defines an architecture without close estimation of the corresponding chip area, then it very likely that the resulting chip layout exceeds the area limit of the available technology.

In such cases, in order to fit the architecture into allowable chip area, some functions may have to be removed and the design process must be repeated.

Such changes may require significant modifications of the original requirements.

Thus, it is very important to feed forward low level information to high level (bottom-up) as early as possible.

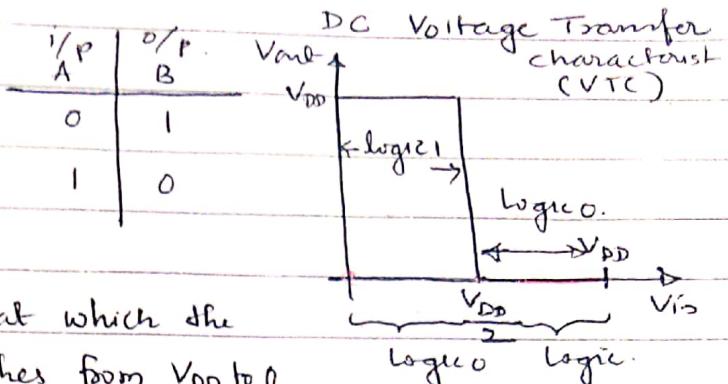
MOS Inverters

Ideal Inverter



V_{th} - threshold voltage.

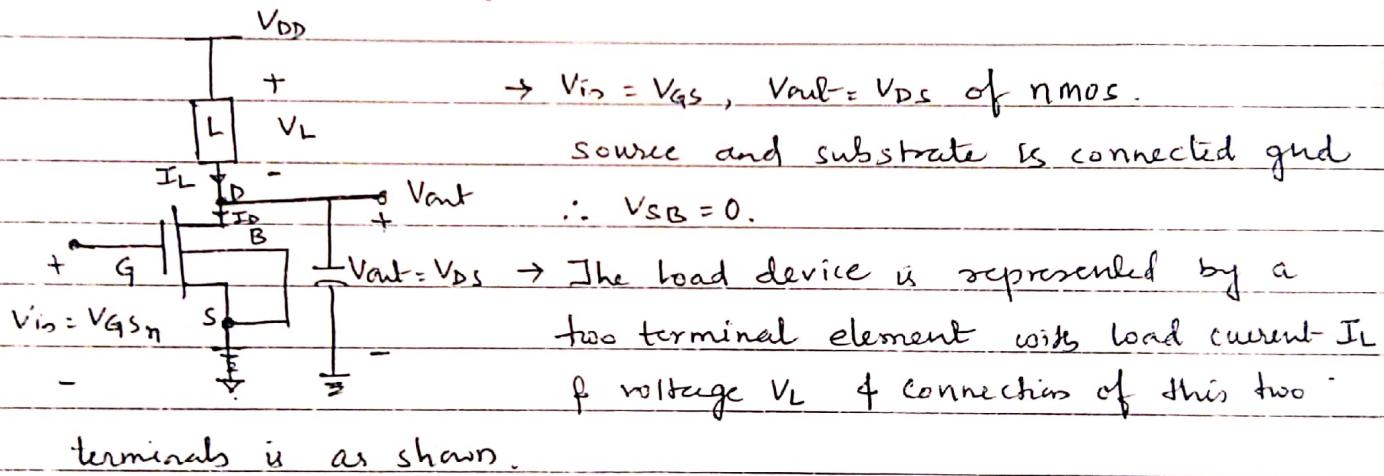
It is the ^{input} voltage level at which the output of inverter switches from V_{DD} to 0.



We can see that is ideal VIC

- i) $0 < V_{in} < \frac{V_{DD}}{2}$ — $V_{out} = V_{DD}$. and
 - ii) $\frac{V_{DD}}{2} \leq V_{in} \leq V_{DD}$ — $V_{out} = 0$
 - iii) $V_{in} = \frac{V_{DD}}{2} = V_{th}$ — the output inverter switches from V_{DD} to 0.
ideally $V_{th} = V_{DD}/2$.

Let us consider a generalized structure of a nmos Inverter.



Voltage transfer characteristics (VTC)

- (i) $V_{DS} = \text{Low}$; the driver nmos is in cutoff & does not conduct ie it is open circuited. \therefore does not conduct any current hence $I_D = 0$.

Consequently voltage drop across the load is very small in magnitude and output V_{out} is HIGH.

- (ii) As the input voltage increases, the driver nmos device starts conducting a certain drain current and the output eventually starts decreasing. This drop in output voltage does not occur abruptly; it gradually reduces with a finite slope.

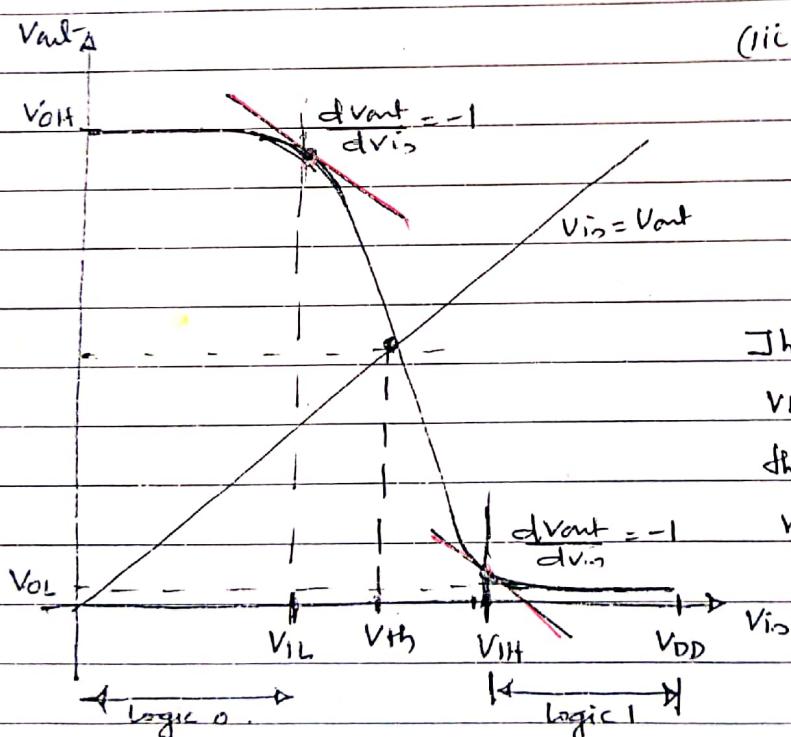
There is a critical voltage which is identified on the graph, decreasing curve at a point where slope of $V_{out}(V_{in})$ char. becomes (-1). i.e

$$\frac{dV_{out}}{dV_{in}} = -1 \quad (1)$$

Thus During the transitions from $V_{out} = \text{HIGH}$ to LOW , there are two points identified on the curve i.e the

(a) Smaller voltage value satisfying cond $z \frac{dV_{out}}{dV_{in}} = -1$
which is referred as V_{IL} (Input Low voltage)

(b) Larger voltage value satisfying cond $z \frac{dV_{out}}{dV_{in}} = -1$
which is referred as V_{IH} (Input High voltage)



(iii) As the input is further increased, V_{out} continues to drop and reach a value of output Low voltage (V_{OL}) when $V_{in} = V_{DD}$.

The inverter threshold voltage V_{th} , which is considered as the inverter threshold transition voltage is defined at a point when $V_{in} = V_{out}$ on VTC

(ii) Thus, we find that there are 5 critical voltages which can be identified by VTC

i) V_{OH} - Maximum output voltage when the output level is logic 1.

ii) V_{OL} - Minimum " " " " " " is logic 0.

iii) V_{IL} - Maximum I/p voltage which can be interpreted as logic '0' i.e $0 \leq V_{in} < V_{IL}$ - logic 0

iv) V_{IH} - minimum I/p voltage which can be interpreted as logic 1.

v) V_{th} - Invertor threshold voltage, transition voltage taken at a point where $V_{in} = V_{out}$

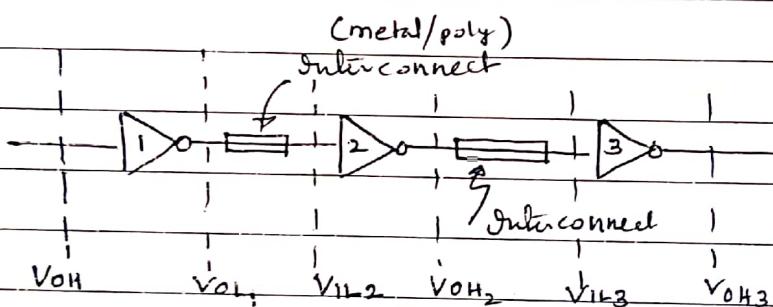
- \therefore i) Input logic '0' is any input voltage level between the lowest available voltage in the system [ground potential] and V_{IL}
- ii) Input logic '1' is any input voltage level between the highest available voltage in systems [V_{DD}] and V_{IH} .
- iii) Output logic '0' is any output voltage level between the lowest available voltage in systems [grnd] and V_{OL}
- iv) Output logic '1' is any output voltage level between the highest available voltage in systems [V_{DD}] to V_{OH} .

* Noise Immunity and Noise margin

Reliability

- Effect of Noise on circuit reliability.

- Let us consider circuit consisting of three identical inverter cascaded



(i) INV1 : Input is V_{DH} and the o/p is V_{OL} (logic 0)

Now, this output of INV1 (V_{OL}) is being transmitted to next inverter^(INV2) through a interconnect (made up of metal/poly).

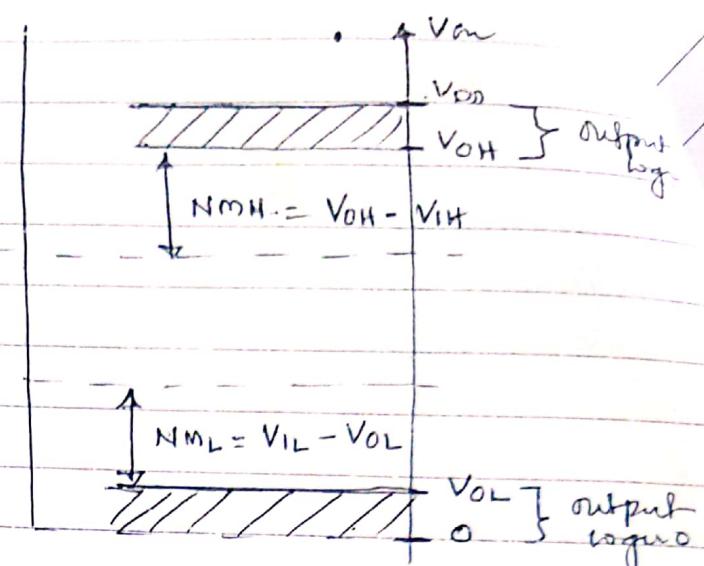
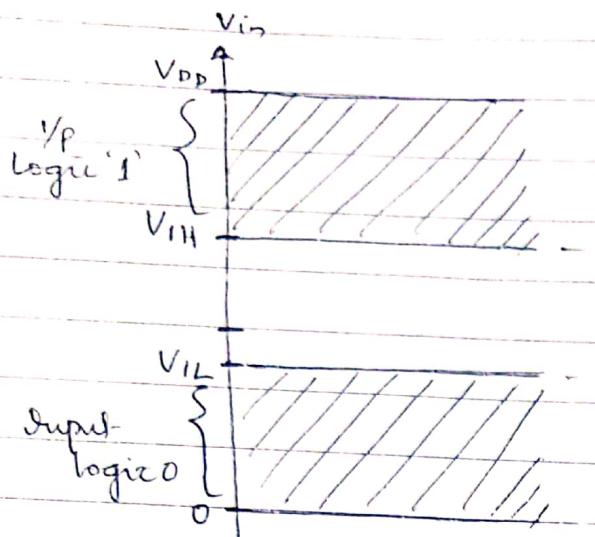
Since on-chip interconnect are generally prone to noise, the output of INV1 (V_{OL}) is unsettled (decrease/increase because of noise). Consequently voltage at the input of INV2 will be either larger or smaller than V_{OL} .

$$V_{IL2} = V_{OL} \pm \text{Noise.}$$

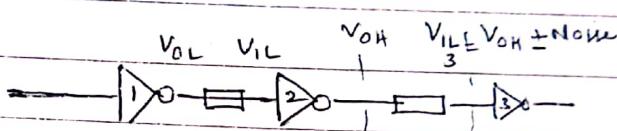
$$\therefore V_{IL2} = V_{OL} - \text{Noise} < V_{OL} \quad (\text{or}) \quad V_{IL2} = V_{OL} + \text{Noise} > V_{OL}$$

a) If input signal to INV2 is smaller than V_{OL} , then it is interpreted as logic 0.

b) If input signal to INV2 is larger than V_{OL} such that it goes beyond the V_{IL2} (max input voltage interpreted as logic 0), then it may not be interpreted as logic 0.



(i)



$$V_{OL} = 0.2V + \text{Noise} = 0.9V.$$

If $V_{IL} = 0.85V$, it means input to INV2 is beyond the max input voltage which can be interpreted as logic 0.

(ii) V_{OH} of INV2 by the time it traverse through interconnection may be added / subtracted.

In this if it adds ie $V_{IH3} = V_{OH} + \text{Noise}$
No issues, it is interpreted as logic 1.

But if $V_{IH3} < V_{OH} + \text{Noise}$

$$= 3V - 1V = 2V$$

If $V_{IH3} = 2.2V$, it means the input is below the defined 'logic 1' $\xrightarrow{\text{to } 2.3}$. It is not interpreted as logic 1 input for INV3.

From this it is clear that for any inverter it is important to define noise margin NML of NMH .

$$(NML = V_{IL} - V_{OL}) - \text{Noise margin Low}$$

It means, If noise added to V_{OL} up to NML there is no issue ie noise immune but if it goes beyond NML the interpretation of input in next stage changes.

If noise margin HIGH $(NMH = V_{OH} - V_{IH})$, it is the maximum noise level which can be added to V_{OH} before it reaches as input to next stage input. If it goes beyond this it is misinterpreted.

The selection of two critical voltage points, V_{IL} and V_{IH} , using the slope cond²

$dV_{out}/dV_{in} = -1$ can now be justified by noise consideration

W.K.T. V_{out} of an inverter under noise free, steady state conditions is a non-linear function of input voltage V_{in} .

$$V_{out} = f(V_{in}) \quad \text{--- (1)}$$

If input V_{in} is unsettled from its nominal value because of external influence such as noise (ΔV_{noise}), the output voltage will deviate from its nominal value

$$V_{out}' = f(V_{in} + \Delta V_{noise}) \quad \text{--- (2)}$$

By simple first order Taylor expansion & by neglecting higher order term, we can express V_{out} as

$$\boxed{V_{out} = f(V_{in}) + \frac{dV_{out}}{dV_{in}} \cdot \Delta V_{noise} + \text{higher order terms}} \quad \text{--- (3)}$$

(neglected)

$f(V_{in})$ - Represents the nominal o/p signal,

$\frac{dV_{out}}{dV_{in}}$ - voltage gain of inverter at a nominal i/p voltage

Thus

$$\begin{matrix} \text{Unsettled} \\ \text{output} \end{matrix} = \begin{matrix} \text{Nominal} \\ \text{output} \end{matrix} + \text{Gain} \times \text{External influence}$$

If the magnitude of the voltage gain at the nominal input voltage V_{in} smaller than unity, then the input influence signal is not amplified and consequently output influence would relatively remain small. Otherwise, with the voltage gain greater than unity, a small influence of external signal in the input voltage level causes larger influence on the output voltage.

Hence, we define the boundaries of valid input signal regions as the voltage points where the magnitude of the inverter voltage gain is equal to unity for $x=a$

$$f(x) = f(a) + f'(a)(x-a) + \frac{f''(a)}{2!}(x-a)^2 + \frac{f'''(a)}{3!}(x-a)^3$$

The voltage range between V_{IL} and V_{IH} corresponds to input with values that may not be processed correctly as logic '0' input or logic '1' input by inverter. This region is called uncertain region or transition region.

Ideally, slope of VTC should be very large between V_{IL} and V_{IH} , because a narrow transition region obviously allows large noise margins. ∴ Reducing the width of the uncertain region is one of the important design objectives.

For any inverter circuit, the five critical voltage points

⇒ Five critical voltage point $V_{IL}, V_{IH}, V_{OL}, V_{OH}$ and V_{th} fully determine the DC input-output voltage behavior, the noise margins, and the width and location of transition region.

* Power and Area Considerations.

Two other issues that play significant roles in inverter design:

i) Power consumption and

ii) Chip area occupied by the inverter ckt.

i) Millions of logic gate integrated in VLSI chip using 0.5 μ m tech. & Each gate on chip dissipates power and thus generates heat, and thus removal of this thermal energy ie cooling of the chip, becomes essential and very expensive task.

The d.c power dissipation of an inverter can be calculated

$$\text{by } [P_{dc} = V_{DD} \cdot I_{DC}] \quad \text{--- (1)}$$

V_{DD} - Power Supply

I_{DC} - Amount of current drawn from power supply during steady or standby mode

DC current drawn by the inverter ckt may vary depending on the input and output voltage level.

Assuming that input voltage level corresponds to logic '0' during 50% of operating time and to logic '1' during other 50%.

The overall DC power consumption of the ckt can be estimated as follows

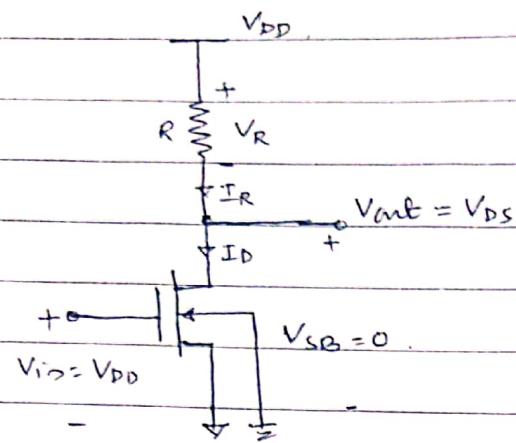
$$P_{DD} = \frac{V_{DD}}{2} [I_{DC}(V_{in}=low) + I_{DC}(V_{in}=High)] \quad \text{--- (2)}$$

Power dissipation varies from inverter to inverter designed.

ii) Chip Area Reduction:

- It is necessary to reduce (W/L) ratio of mos device ie Area of mos device which is product of W & L . ie width to gate Length (W/L) ratio and it is expected to be around unit but contradicts other design criteria ; such as noise margin , current driving capability and dynamic switching speed . ∴ There will be trade off these criteria.

* Resistive Load Inverter



- A passive load R_L is used (linear resistor)

- Analysis concentrates on static behavior

of ckt \therefore output-load cap is not shown in the ckt.

- $ID = IR$, in DC steady state operation, $V_{SD} = 0$ and threshold voltage of driver transistor is always equal to V_{TO} .

Operating regions under steady state cond₂

i) $V_{in} < V_{TO}$ - cutoff

ii) $V_{TO} \leq V_{in} < V_{out} + V_{TO}$. - Saturation.

iii) $V_{in} \geq V_{out} + V_{TO}$ - linear.

T.volt
for 3000
body bias.

i) $V_{in} < V_{TO}$

- The transistor is in cutoff and $ID = 0$.

Since voltage drop acf R_L is zero, the output voltage is equal to V_{DD} ie $V_{out} = V_{DD}$.

ii) - We know that now $V_{DS} = V_{DD}$.

As the input voltage V_{in} is increased beyond V_{TO} , the driver transistor starts conducting a non zero drain current.

Now it is clear that $V_{in} \geq V_{TO}$ and $V_{DS} > V_{GS} - V_{TO}$

$$V_{GS} \leq V_{DS} + V_{TO}$$

As $V_{DS} > V_{GS} - V_{TO}$ - The device is in saturation.

i.e. $V_{TO} \leq V_{GS} < V_{DS} + V_{TO}$. - Device will be in saturation

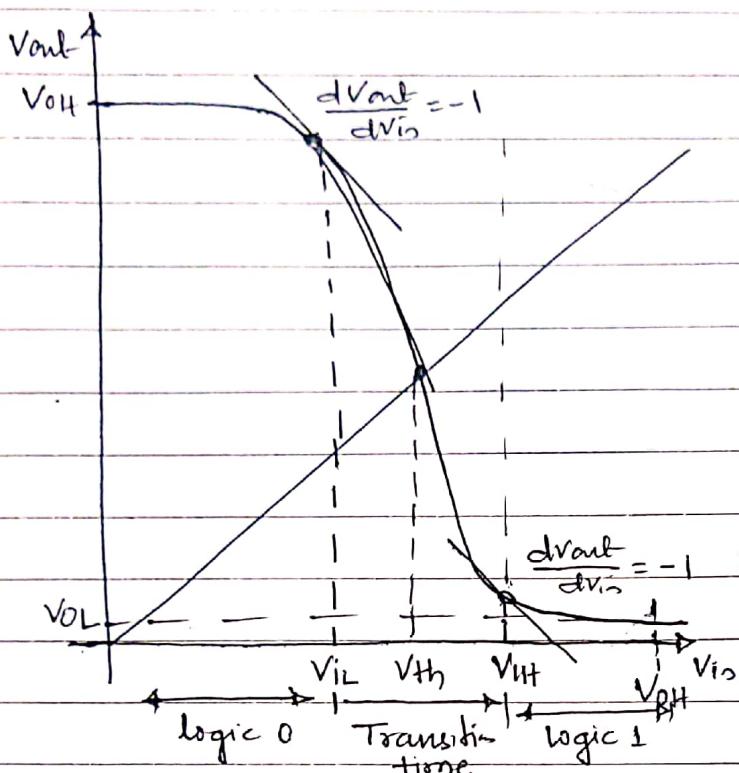
$$V_{TO} \leq V_{in} \leq V_{DS} + V_{TO}$$

$$\therefore I_R = \frac{k_n}{2} (V_{GS} - V_{TO})^2 = \frac{k_n}{2} (V_{in} - V_{TO})^2 \quad (1)$$

iii) With increasing input voltage, I_D increases and V_{out} starts to drop. Eventually for input voltage larger than $V_{DS} + V_{TO}$

$I_R = \frac{k_n}{2} [2(V_{in} - V_{TO})V_{out}] \quad [V_{in} \geq V_{out} + V_{TO}]$ the driver transistor enters in linear region. At larger input voltage transistor remains in linear region.

VTC of Resistive Load Inverter



Note: $\frac{dV_{out}}{dV_{in}} > \text{Unity}$
in transitioning period
∴ Noise (ΔV_{noise}) gets amplified
∴ V_{IL} and V_{IH} are defined as critical voltage as they define the limit for logic 0/1 for V_{in} where the gain $\frac{dV_{out}}{dV_{in}} \leq \text{Unity}$

∴ Immune to Noise.

Calculating critical voltages V_{IL} , V_{IH} , V_{OL} , and V_{DH} .

Note: $V_{to} < V_{gsn} < V_{ds} + V_{to}$ ie $V_{to} < V_{in} < V_{out} + V_{to}$ — nmos is in Sat

As $I_R = I_D$

$$I_R = \frac{k_n}{2} (V_{in} - V_{to})^2 \quad (1) \quad \therefore V_{gsn} = V_{in}$$

and when $V_{in} > V_{out} + V_{to}$ — nmos is in Linear region

$$I_R = \frac{k_n}{2} (2(V_{in} - V_{to})V_{out} - V_{out}^2) \quad \left\{ \begin{array}{l} \because V_{in} = V_{gsn} \\ V_{out} = V_{dsn} \end{array} \right. \quad (2)$$

Case (1) : Calculation of V_{DH}

W.K.T

$$V_{in} = 0/1$$

$$V_{out} = V_{DD} - I_R R_L \quad (3)$$

V_{DH} is obtained when V_{in} is smaller than V_{to} of driver transistor under this condⁿ nmos is in cutoff ∴ $I_D = I_R = 0$.

$$\therefore V_{out} = V_{DD} = V_{DH} \quad \text{ie } V_{out} = V_{DH} = V_{DD}$$

$V_{out} = V_{DD}$

— (4)

Case (ii) : Calculation of V_{OL} -

When To calculate V_{OL} , Let us assume that $V_{in} = V_{DH} = V_{DD}$.

Since $V_{in} \geq V_{out} + V_{TO}$ ie $V_{in} \geq V_{DS} + V_{TO}$

$V_{GS} \geq V_{DS} + V_{TH}$ the device is in linear region and load current I_R is

$$V_{DS} \leq V_{GS} - V_{TH}$$

$$\left[I_R = \frac{V_{DD} - V_{out}}{R_L} = \frac{V_{DD} - V_{OL}}{R_L} \right] \quad \text{--- (5)} \quad \therefore V_{out} = V_{OL}$$

As device is in linear region

$$I_D = I_R = \frac{k_n}{2} (2(V_{in} - V_{TO}) V_{out} - V_{out}^2) \quad \text{--- (6)} \quad \begin{array}{l} V_{GS} = V_{in} \\ V_{DS} = V_{out} \end{array}$$

Now equating (5) and (6) when $V_{in} = V_{DD}$ & $V_{out} = V_{OL}$

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{k_n}{2} (2(V_{DD} - V_{TO}) V_{OL} - V_{OL}^2)$$

By rearranging

$$V_{OL}^2 - 2(V_{DD} - V_{TO}) V_{OL} + \frac{2(V_{DD} - V_{OL})}{k_n R_L} = 0$$

$$V_{OL}^2 - 2(V_{DD} - V_{TO}) V_{OL} + \frac{2V_{DD}}{k_n R_L} - \frac{2V_{OL}}{k_n R_L} = 0$$

$$\textcircled{a} \left[V_{OL}^2 - 2 \left(V_{DD} - V_{TO} + \frac{1}{k_n R_L} \right) V_{OL} + \frac{2V_{DD}}{k_n R_L} = 0 \right] - \textcircled{7}$$

It is a simple quadratic eq² of the form $ax^2 + bx + c$

where $a = 1$, $b = -2(V_{DD} - V_{TO} + \frac{1}{k_n R_L})$, $c = \frac{2V_{DD}}{k_n R_L}$, $x = V_{OL}$

$$\therefore V_{OL} = +2 \left(V_{DD} - V_{TO} + \frac{1}{k_n R_L} \right) \pm \sqrt{\frac{4(V_{DD} - V_{TO} - \frac{1}{k_n R_L})^2 - 4 \times 1 \times \frac{2V_{DD}}{k_n R_L}}{2 \times 1}}$$

$$\boxed{V_{OL} = \left(V_{DD} - V_{TO} + \frac{1}{k_n R_L} \right) - \sqrt{\left(V_{DD} - V_{TO} - \frac{1}{k_n R_L} \right)^2 - \frac{2V_{DD}}{k_n R_L}}} \quad \text{--- (8)}$$

We get two possible solⁿs in which the one which is physically correct for output low is chosen \therefore -ve sign is chosen

Case(iii) - Calculation of V_{IL}

V_{IL} and V_{IH} are defined by defining two points on VTC with slope equal to (-1) ie $dV_{out}/dV_{in} = -1$

In this, V_{IL} is smaller of these two voltages.

From VTC, it is clear that when $V_{in} = V_{IL}$, V_{out} is slightly smaller than V_{in} . Consequently

$$V_{out} > V_{in} - V_{TO} \quad (\text{or}) \quad V_{DS} > V_{GS} - V_{TO} \quad \text{and} \quad V_{GS} < V_{DSS} + V_{TO}$$

the nmos is operating in saturation

$$I_D = \frac{k_n}{2} (V_{GS} - V_{TO})^2$$

$$I_D = \frac{k_n}{2} (V_{in} - V_{TO})^2 \quad \text{--- (9)}$$

$$\text{and } I_R = \frac{V_{DD} - V_{out}}{R_L} \quad \text{--- (10)}$$

Equating (9) and (10) By KCL at o/p node. $I_D = I_R$

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} (V_{in} - V_{TO})^2 \quad \text{--- (11)} \quad \cancel{V_{in} = V_{IV}}$$

By differentiating eq² (11) w.r.t V_{in} on both side of eq² (11)

$$\frac{dV_{out}}{dV_{in}} \left(-\frac{1}{R_L} \right) = \frac{k_n}{2} (V_{in} - V_{TO}) \quad (1)$$

$$\text{w.k.t } \left(\frac{dV_{out}}{dV_{in}} \right) = -1$$

$$(-1) \left(-\frac{1}{R_L} \right) = k_n (V_{in} - V_{TO})$$

$$\boxed{V_{in} = V_{IL}}$$

$$\left(\frac{1}{R_L} \right) = k_n (V_{IL} - V_{TO})$$

$$\left(\frac{1}{R_L} \right) = k_n V_{IL} - k_n V_{TO}$$

$$k_n V_{IL} = \frac{1}{R_L} + k_n V_{TO}$$

$$V_{IL} = V_{TO} + \frac{1}{k_n R_L} \quad \text{--- (12)}$$

V_{out} can also be defined by substituting eq² (12) in (11) & solve for V_{in}

Substituting ⑫ in ⑪

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \left[\left(V_{TO} + \frac{1}{k_n R_L} \right) - V_{TO} \right]^2$$

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \left(\frac{1}{k_n R_L} \right)^2$$

$$\frac{V_{out}}{R_L} = \frac{V_{DD}}{R_L} - \frac{k_n}{2} \left(\frac{1}{k_n R_L} \right)^2$$

$V_{out} = V_{DD} - \frac{k_n}{2 k_n R_L}$ $(V_{in} = V_{TO})$	— ⑬
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Case(iv) : Calculation of V_{IH} .

V_{IH} is the larger of two voltage points on VTC at which slope = (-1)

When $V_{in} = V_{IH}$, the output voltage V_{out} is slightly larger than the output low voltage V_{OL} .

Consequently, $V_{out} < V_{in} - V_{TO}$ & the driver transistor operates in the linear region. ^{The} KCL eq2 for the output node is given by below

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \left[2(V_{in} - V_{TO}) \cdot V_{out} - V_{out}^2 \right] \quad u \quad v \quad — ⑭$$

By differentiating

$$-\frac{1}{R_L} \frac{dV_{out}}{dV_{in}} = \frac{k_n}{2} \left[2(V_{in} - V_{TO}) \frac{dV_{out}}{dV_{in}} + 2V_{out} \cdot \frac{dV_{in}}{dV_{in}} - 2V_{out} \cdot \frac{dV_{out}}{dV_{in}} \right]$$

Now substitute $(dV_{out}/dV_{in}) = (-1)$

$$-\left(\frac{1}{R_L}\right)(-1) = \frac{k_n}{2} \left[2(V_{in} - V_{TO})(-1) + 2V_{out} - 2V_{out}(-1) \right]$$

$$\left(\frac{1}{R_L}\right) = \left(\frac{k_n}{2}\right) [-2V_{in} + 2V_{TO} + 2V_{out} + 2V_{out}]$$

$$\left(\frac{1}{R_L}\right) = k_n \left[(V_{in} - V_{TO})(-1) + 2V_{out} \right] \quad (\text{where } V_{in} = V_{IH})$$

Solving $\frac{1}{R_L} = k_n [-V_{IH} + V_{TO} + 2V_{out}]$

$$1 + k_n V_{IH} = R_L k_n V_{TO} + 2V_{out} k_n R_L$$

$$V_{IH} = R_L V_{TO} + 2V_{out} R_L - \frac{1}{k_n} = V_{TO} + 2V_{out} - \frac{1}{k_n R_L} \quad — ⑮$$

Substituting (5) in (4) V_{out} is derived.

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \left[2 \left(V_{T0} + 2V_{out} - \frac{1}{k_n R_L} - V_{T0} \right) V_{out} - V_{out}^2 \right]$$

$$\frac{V_{DD}}{R_L} - \frac{V_{out}}{R_L} =$$

$$\frac{2}{k_n} \left(\frac{V_{DD} - V_{out}}{R_L} \right) = 2 \left(2V_{out} - \frac{1}{k_n R_L} \right) V_{out} - V_{out}^2$$

$$V_{out}^2 - 2 \left(2V_{out} - \frac{1}{k_n R_L} \right) V_{out} + \frac{2}{k_n} \left(\frac{V_{DD} - V_{out}}{R_L} \right) = 0$$

$$V_{out}^2 - 2 \left(2V_{out} - \frac{1}{k_n R_L} \right) V_{out} + \frac{2V_{DD}}{k_n R_L} - \frac{2V_{out}}{k_n R_L} = 0$$

$$V_{out}^2 - 2 \left(2V_{out} - \frac{1}{k_n R_L} + \frac{V_{out}}{k_n R_L} \right) V_{out} + \frac{2V_{DD}}{k_n R_L} = 0$$

$$V_{out}^2 - 4V_{out}^2 + \frac{2V_{DD}}{k_n R_L} = 0$$

$$-3V_{out}^2 + \frac{2V_{DD}}{k_n R_L} = 0$$

$$V_{out}^2 = \frac{2}{3} \frac{V_{DD}}{k_n R_L}$$

$$\therefore V_{out} (V_{in} = V_{IH}) = \sqrt{\frac{2}{3} \frac{V_{DD}}{k_n R_L}} \quad \text{--- (16)}$$

By substituting (16) in eq (15)

$$V_{IH} = V_{T0} + 2V_{out} - \frac{1}{k_n R_L}$$

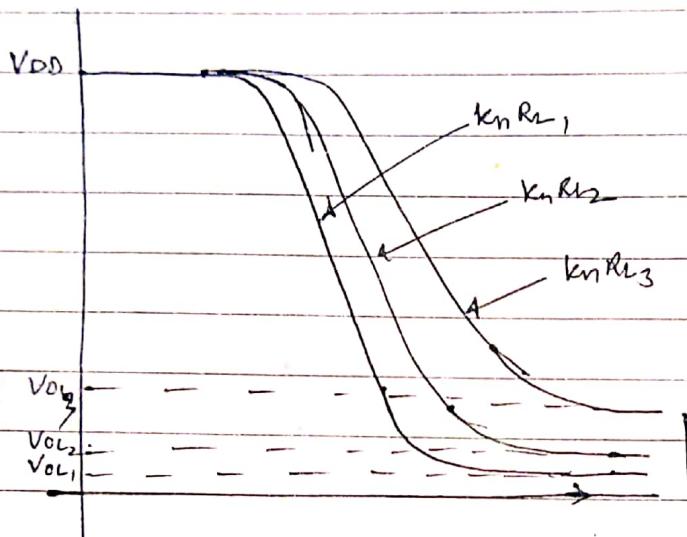
$$= V_{T0} + 2 \sqrt{\frac{2}{3} \frac{V_{DD}}{k_n R_L}} - \frac{1}{k_n R_L}$$

$$\boxed{V_{IH} = V_{T0} + \sqrt{\frac{8}{3} \frac{V_{DD}}{k_n R_L}} - \frac{1}{k_n R_L}} \quad \text{--- (17)}$$

We can see that eq (8) i.e. V_{OL} , eq (12) for V_{IL} and eq (17) for V_{IH} all have a factor $k_n R_L$. $\therefore k_n R_L$ plays important role in determining shape of the VTC

Case (i) : If $k_n R_L$ is larger.

V_{OL} becomes smaller, V_{IL} is smaller and V_{IH} is small.
the slope shape of VTC approaches a ideal inverter with large transition step



$k_n R_L_1 > k_n R_L_2 > k_n R_L_3$
Achieving larger $k_n R_L$ value in design will have other trade offs in a design w.r.t area and power consumption of the ckt

* Power consumption and chip area

- The avg dc power consumption of resistive load inverter ckt is found by two cases, $V_{in} = V_{OL}$ (low) and $V_{in} = V_{OH}$ (High)

- When $V_{in} = V_{OL}$ (Low) - nmos is in cutoff

$I_D = I_R = 0$ & dc power consumption is equal to zero. and $V_{in} = V_{OH}$ (HIGH), both MOSFET & the load resistor conduct nonzero current. Since output voltage is this case is $\approx V_{OL}$, the current drawn from the power supply can be found

$$I_D = I_R = \frac{V_{DD} - V_{out}}{R_L} = \frac{V_{DD} - V_{OL}}{R_L}$$

Assuming 50% duty cycle (Low and HIGH input). As the avg power consumption :

$$\boxed{P_{DC}(\text{avg}) = \left(\frac{V_{DD}}{2}\right) V_{DD} \times I_R = \frac{V_{DD}}{2} \left(\frac{V_{DD} - V_{OL}}{R_L} \right)}$$

(1) Given $V_{DD} = 5V$, $k_n' = 30 \mu A/V^2$, and $V_{TO} = 1V$.

Design a resistive load inverter circuit with $V_{OL} = 0.2V$. Specifically, determine the (W/L) ratio of the driver transistor & the value of R_L that achieves the required V_{OL} .

Sol: To get V_{OL} , $V_{in} = V_{OH} = V_{DD}$ & nmos is operating in linear region.

By KCL at node 1

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{k_n'}{2} \left(\frac{W}{L} \right) \left[2(V_{OH} - V_{TO}) V_{OL} - V_{OL}^2 \right]$$

Assuming $V_{OL} = 0.2V$ & using given values.

$$\frac{5 - 0.2}{R_L} = \frac{30 \times 10^{-6}}{2} \left(\frac{W}{L} \right) \left[2(5 - 1)0.2 - (0.2)^2 \right]$$

$$\frac{4.8}{R_L} = 15 \times 10^{-6} \left(\frac{W}{L} \right) \left[2(4)(0.2) - (0.2)^2 \right]$$

$$\frac{4.8}{R_L} = 15 \times 10^{-6} \left(\frac{W}{L} \right) [1.56]$$

$$\left(\frac{W}{L} \right) R_L = \frac{4.8}{15 \times 10^{-6} \times 1.56} = 2051.28 = 2.05 \times 10^5$$

$$\left| \left(\frac{W}{L} \right) \cdot R_L = 2.05 \times 10^5 \right| = 205 \text{ k}$$

- Now designer have choice of different (W/L) and R_L values such the design specification are met.

- The selection of pair of values to be chosen finally depends other considerations such as power consumption and chip area (silicon).

-	(W/L)	$(R_L) \text{ k}\Omega$	$P_{DC}(\text{avg}) \text{ mW}$
	1	205	$\frac{5}{2} \left(\frac{5 - 0.2}{205 \times 10^3} \right) = 58.5$
	2	102.5	117.1
	3	68.4	175.4
	4	51.3	233.9
	5	41.0	292.7
	6	34.2	350.8

Observations

i) Power consumption increases as the value of the load resistor R_L is decreased. and $(\frac{W}{L})$ is increased.

- ii)
- i) If Power consumption is a concern, $(\frac{W}{L})$ is kept low and a large load resistor (R_L) need to be considered but, area will be more. as fabrication of R_L requires \rightarrow ~~it is more~~ larger silicon-area.
 - from this it is clear that there is a clear trade off between power & area.

(2) Consider a resistive load inverter with

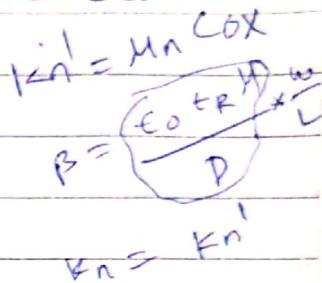
$V_{DD} = 5V$, $k_n' = 20 \mu A/V^2$, $V_{TO} = 0.8V$, $R_L = 200 k\Omega$ and $(W/L) = 2$. Calculate the critical voltage (V_{OL} , V_{OH} , V_{IL} , V_{IH}) on the VTC and find the noise margin of the ckt.

Sol

$$V_{OH} = V_{DD} = 5V$$

$$\beta = k_n = k_n' (W/L) = 20 \times 10^{-6} \times 2 = 40 \times 10^{-6} \mu A/V^2$$

$$k_n R_L = 4 \times 10^{-6} \times 200 \times 10^3 = 8 V^{-1}$$



$$V_{OL} = V_{DD} - V_{TO} + \frac{1}{k_n R_L} - \sqrt{\left(V_{DD} - V_{TO} + \frac{1}{k_n R_L}\right)^2 - \frac{2V_{DD}}{k_n R_L}}$$

$$= 5 - 0.8 + \frac{1}{8} - \sqrt{\left(5 - 0.8 + \frac{1}{8}\right)^2 - \frac{2 \times 5}{8}}$$

$$= 0.147V$$

$$V_L = V_{TO} + \frac{1}{k_n R_L} = 0.8 + \frac{1}{8} = 0.925V$$

$$V_{IH} = V_{TO} + \sqrt{\frac{8}{3} \frac{V_{DD}}{k_n R_L}} - \frac{1}{k_n R_L} = 0.8 + \sqrt{\frac{8}{3} \frac{5}{8}} - \frac{1}{8}$$

$$= 1.97V$$

$$NML = V_{IL} - V_{OL} = 0.925 - 0.147 = \underline{\underline{0.778V}}$$

$$NMH = V_{OH} - V_{IH} = 5.0 - 1.97 = \underline{\underline{3.03V}}$$

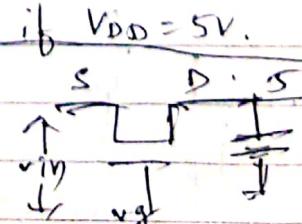
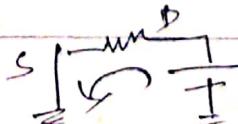
• 925
• 147
• 778

Observation

- The noise margin (NML) found to be quite low and eventually lead to misinterpretation of input signal levels.
- For better noise immunity NML should be atleast 25% of the V_{DD} i.e. $1.25V$ if $V_{DD} = 5V$.

when $V_g = 5$

$$V_{in} = 0, \quad V_o = 5V$$



$$V_{ds} < V_{gs} - V_b$$

$$\frac{V_d - V_s}{T} = 5 - 1$$

$$5 = 4V$$

0/1

atmos acts as strong logic zero.

(3) Design a resistive-load inverter with $R = 1 k\Omega$, such that $V_{OL} = 0.6 V$. The enhancement-type nmos inverter transistor has the following parameters

$$V_{DD} = 5 V, V_{TO} = 1.0 V, \gamma = 0.2 V^{1/2}, \lambda = 0, \text{ and } \text{ln}(C_O X) = 22.0 \mu A/V^2$$

Determine

i) Required aspect ratio, (W/L)

ii) V_{IL} and V_{IH}

iii) Noise margins NM_L and NM_H

Sol: For $V_{OL} = 0.6 V$

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{k_n}{2} \left(\frac{W}{L} \right) \left[2 (V_{GDS} - V_{TO}) V_{OL} - V_{OL}^2 \right]$$

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{k_n}{2} \left(\frac{W}{L} \right) \left[2 (V_{IH} - V_{TO}) V_{OL} - V_{OL}^2 \right]$$

$$\frac{5 - 0.6}{1 \times 10^3} = \frac{22 \times 10^{-6}}{2} \left(\frac{W}{L} \right) \left[2 (5 - 1.0) 0.6 - 0.6^2 \right]$$

$$\left(\frac{W}{L} \right) = 90.1$$

$$\text{ii) } V_{IL} = V_{TO} + \frac{1}{k_n R_L} = 1.0 + \frac{1}{22 \times 10^{-6} \times 90.1 \times 1 \times 10^3} = 1.5 V$$

$$\boxed{V_{IL} = 1.5 V}$$

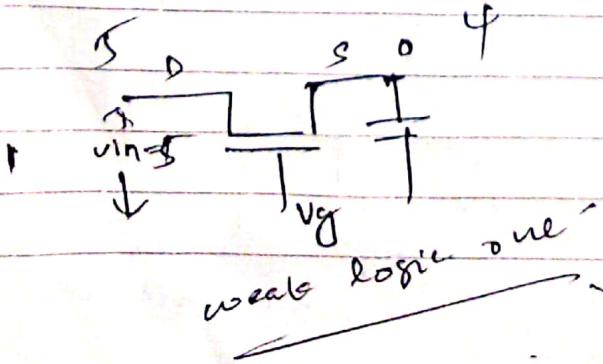
$$V_{IH} = V_{TO} + \sqrt{\frac{8}{3} \frac{V_{DD}}{k_n R_L} - \frac{1}{k_n R_L}} = 1 + \sqrt{\frac{8}{3} \frac{5}{22 \times 10^{-6} \times 90.1 \times 1 \times 10^3}}$$

$$\boxed{V_{IH} = 3.09 V}$$

$$\text{iii) } NM_L = V_{IL} - V_{OL} = 1.5 - 0.6 = 0.9 V$$

$$NM_H = V_{OH} - V_{IH} = 5 - 3.09 = 1.91 V$$

$$v_{gs} = 5$$



$$\begin{aligned} v_{gs} &= v_g - v_s \\ &= 5 - 0 = 5 \\ &= 5 - 1 = 4 \\ &= 5 - 2 = 3 \\ v_{gs} &\geq v_{th} \end{aligned}$$

* Inverter with n-type MOSFET load - nmos inverter

As resistive load inverter have a disadvantage of using more silicon for designing the load resistor, an alternate is nmos load. In this instead of using resistive load nmos loads are used.

The active loads used are

1) Enhancement nmos load - Referred as enhancement load inverters and in this there are two topologies, ie the enhancement nmos load operating in saturation region

(a) linear region

a) Saturated enhancement nmos load nmos inverter.

b) Linear enhancement nmos load nmos inverter

2) Depletion nmos load - Referred as depletion load nmos inverter.

In this, the load used is a depletion nmos transistor. This nmos has a channel implanted at the fabrication level itself because of which it has following properties

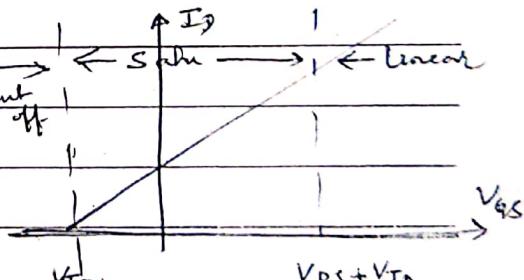
a) It operates even when $V_{GS} = 0$ because of implanted channel with $\text{Grv } V_{DS}$.

b) It has gate threshold voltage V_{TH} cut off

c) It operates in enhancement mode and depletion mode

d) At gate both (+ve or)

(+)ve voltage can be applied. When $V_{GS} = (+)\text{ve}$ it operates in enhancement mode and when $V_{GS} = (-)\text{ve}$ the channel starts depleting & operates in depletion mode



Advantage of using MOSFET as load

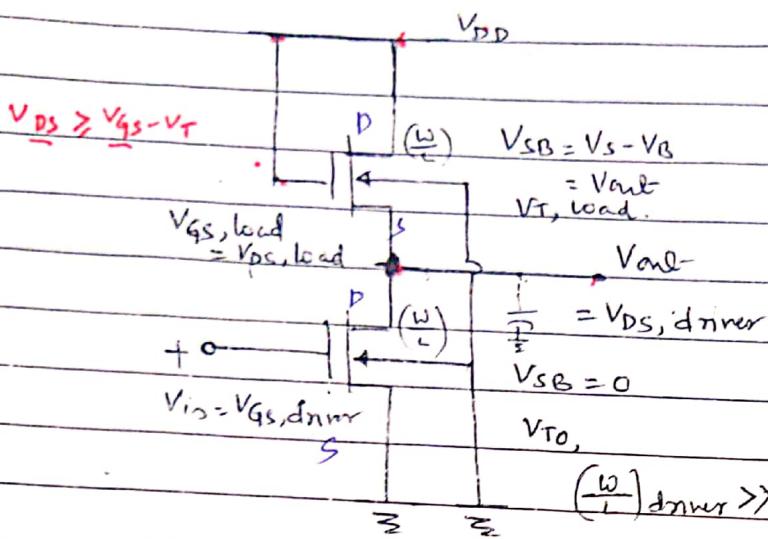
i) Silicon area occupied by the transistor is usually smaller than that occupied by a comparable resistive load

ii) The overall performance of mos load inverter is better than resistive load inverter

∴ nmos load inverters are preferred rather than resistive load inverters.

1) Enhancement load nmos inverter

a) Saturated enhancement load nmos inverter



In this, the enmos used as load operates in saturation region provided V_{GS}

$$V_{GS, load} > V_{T, load} (V_{out})$$

$$V_{T, load} = V_{T_0} + \gamma \sqrt{|2\phi_F|} + V_{out} - \sqrt{|2\phi_F|}$$

$$\frac{W}{L}_{driver} \gg \frac{W}{L}_{load} \rightarrow \text{body effect coefficient}$$

ϕ_F - Bulk coefficient

As $V_{GS, load} = V_{DS, load}$, always e-nmos load satisfies the cond² $V_{DS, load} \geq V_{GS} - V_{T, load}$ as a result it is ~~sat~~ V_{DS} always in saturation

a) When $V_{in} = 0$, driver nmos is cutoff and load nmos is conducting (saturation)

$V_{in} < V_{T, driver}$, driver nmos is OFF (cutoff), load transient is ~~sat~~ V_{out}

$$V_{out} = V_{DD} - V_{T, load}$$

$$V_{DS} \geq V_{GS} - V_T \quad | \quad V_{out} = V_{DD} - V_{out} - V_{T, load}$$

As V_{in} increases the driver nmos gets in saturation region and load nmos is also in saturation.

$$k_{\text{driver}} (V_{in} - V_{T_0})^2 = k_{\text{load}} (V_{GS, load} - V_{T, load})^2$$

$$= k_{\text{load}} (V_{DD} - V_{out} - V_{T, load})^2$$

$$V_{in} \sqrt{\frac{k_{\text{driver}}}{k_{\text{load}}}} (V_{in} - V_{T_0}) = (V_{DD} - V_{out} - V_{T, load})$$

With $V_{in} = V_{DD}$,

$$V_{out} = V_{DD} - V_{T, load} - \sqrt{\frac{k_{\text{driver}}}{k_{\text{load}}}} (V_{in} - V_{T_0}) \quad \text{①}$$

Magnitude of slope depends on $\frac{k_{\text{driver}}}{k_{\text{load}}}$ $\therefore k_{\text{driver}} \gg k_{\text{load}}$

$$(\frac{W}{L})_{\text{dr.}} \gg (\frac{W}{L})_{\text{load}}$$

simplicity in structure as both are e-nmos / fabrication process will be easy.

From ① it is clear that as V_{in} increases, V_{out} starts decreasing (where slope depends on $\sqrt{k_{\text{driver}}/k_{\text{load}}}$) and at some point when $V_{out} = V_{in} - V_{T, driver}$ i.e.

$$V_{DS, driver} = V_{GS, driver} - V_{T, driver}$$

The driver nmos gets into triode

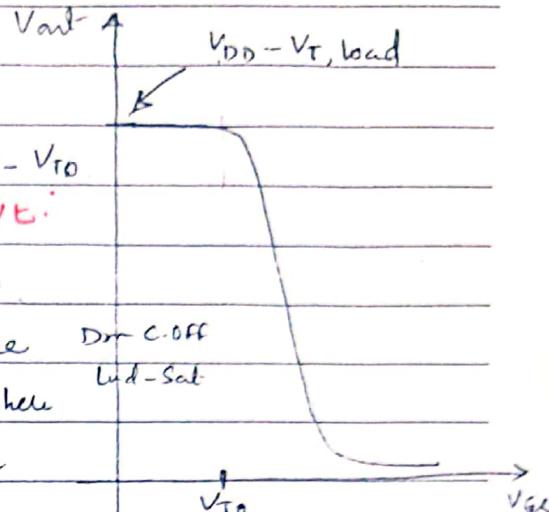
As V_{out} starts decreasing from $(V_{DD} - V_{T, load})$, At some point

it becomes equal $V_{out} = V_{GS, driver} - V_{TO}$
 $V_{out} \approx V_{DS, driver}$. $V_{DS} < v_{GS} - V_T$.

$V_{DS, driver} < V_{GS, driver} - V_{TO}$

the driver nmos gets into triode region. If $V_{in} = V_{DD}$ the $V_{out} = 0$ when

~~the~~ driver nmos will be in linear region.



$$V_{DS} = v_{GS} - V_T$$

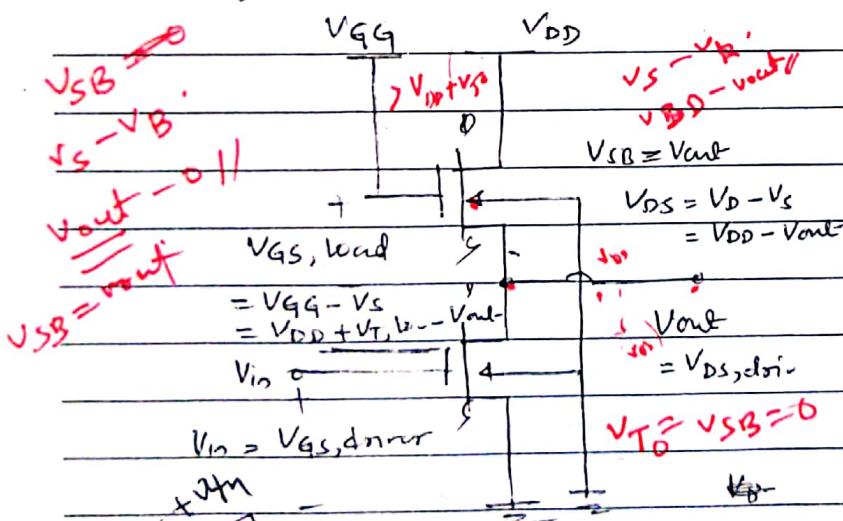
Adv: i) As both load & driver are e-nmos, the fabrication

of saturated load nmos is easier will be easy

ii) It requires only one V_{DD} source pin for both drain and gate of load nmos.

v_{GS}

b) Linear Enhancement load nmos inverter



In this case, instead of connecting gate of load nmos to V_{DD} , it is connected separately

source whose magnitude will be set as V_{GG}

$$[V_{GG} \geq V_{DD} + V_{T, load}]$$

$$V_{DS} < V_{GS} - V_T \quad (\text{for device to be in linear})$$

$$V_{DD} < V_{DD} + V_{T, load}$$

$$V_{DD} - V_{out} < V_{DD} + V_{T, load} - V_{out}$$

$$5 \quad V_{DD} < V_{DD} + V_{T, load}$$

\therefore load nmos will be always in linear region.

In this case when $V_{in} = 0$; driver nmos will be in cutoff and load nmos is linear and $V_{out} = V_{DD}$.

\therefore when $V_{out} = V_{DD}$

$$V_{GS, load} = V_{GG} - V_S = V_{GG} - V_{out}$$

$$= V_{DD} + V_{T, load} - V_{DD}$$

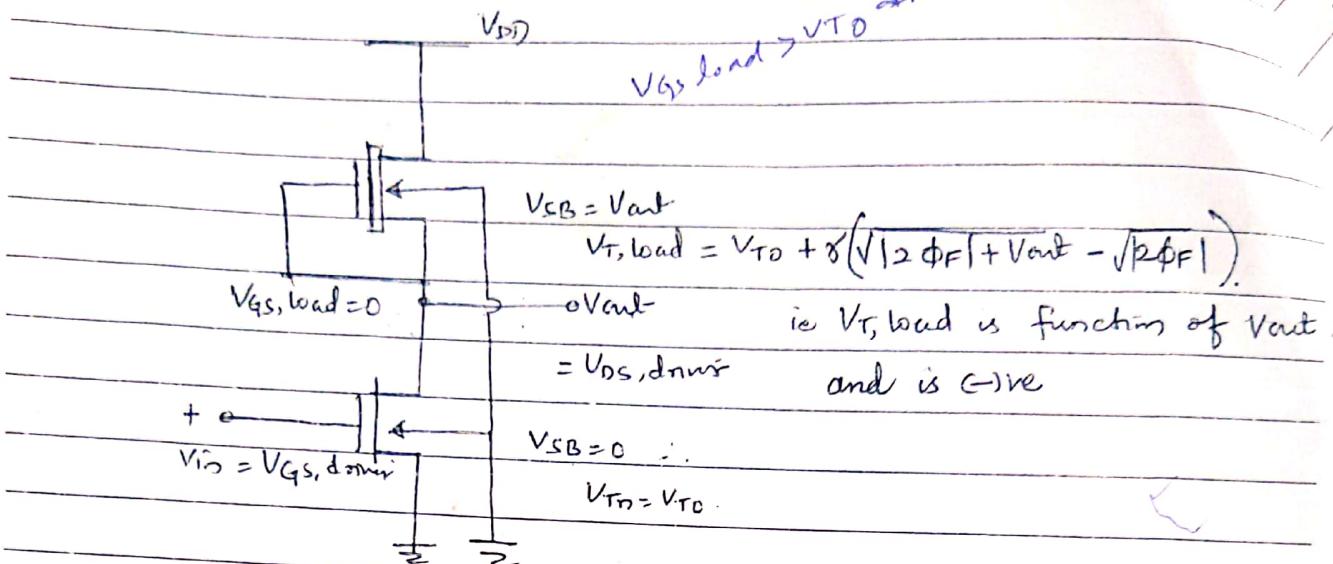
$$= V_{T, load} \quad (\text{Gets into cut-off})$$

$$r = \sqrt{\frac{2\sigma H_{Ae}}{C_{ox}}} \quad (\# F) \text{ form potential of material} = \frac{kT}{q} \ln \left(\frac{n_i}{n} \right)$$



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2) Depletion type nmos Inverter



- The drain current eq²s used for D-nmos is same as that of enhancement-nmos
- From the connection shown it is clear that gate and source of depletion-nmos load is shorted ie $V_{GS,load} = 0$ and the device operates either in saturation / linear based on the condition satisfied $[V_{DS} \geq V_{GS} - V_{T,load} - \text{Saturation else is broken}]$
- The threshold value of depletion nmos load is function of V_{out} as $V_{SB} \neq 0$. where threshold voltage is given by

$V_{T,load} = V_{TD} + \gamma(\sqrt{|2\phi_F|} + V_{out} - \sqrt{2\phi_F}) \quad \text{--- (1)}$

$\phi_F \rightarrow$ Consideration
Fermi potential and as device is operating either in saturation / linear

of nMOS regions the I_D can be expressed with V_{GS} - ckt cond² as below.

$\theta \rightarrow$ Body effect - saturation region, $V_{GS,load} = 0$ & $V_{Tn} = V_{T,load}(V_{out})$

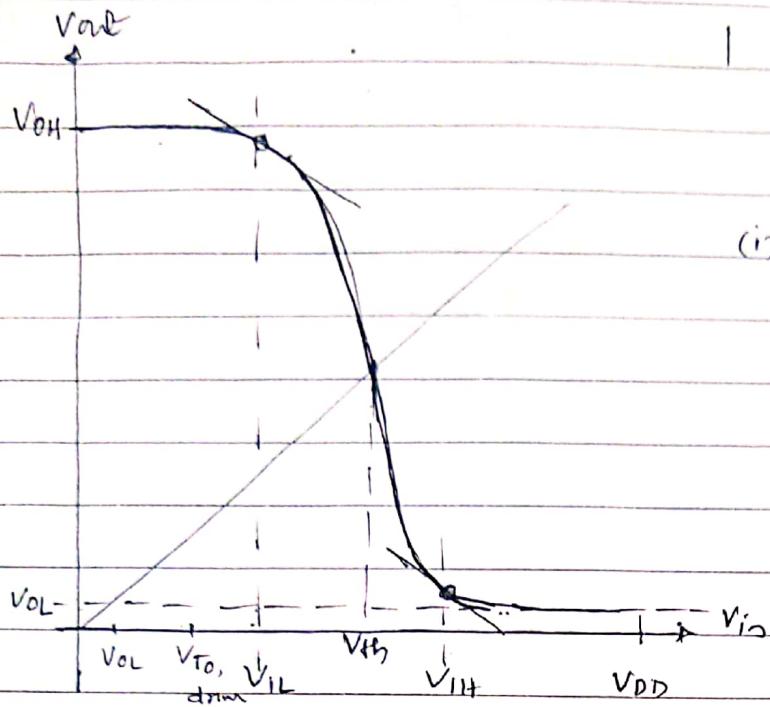
$$I_D, \text{load} = \frac{k_n, \text{load}}{2} [V_{GS,load} - V_{Tn}]^2 = \frac{k_n, \text{load}}{2} [0 - V_{T,load}(V_{out})]^2 \quad \text{--- (2)}$$

$$\phi_F = \left(\frac{V_T}{2} \right) \ln \left(\frac{n_A}{n_D} \right) - \text{Linear region}, \quad V_{GS,load} = 0, \quad V_{Tn} = V_{T,load}(V_{out})$$

$$V_{DS} = V_D - V_S = V_{DD} - V_{out}$$

$$I_D, \text{load} = \frac{k_n, \text{load}}{2} [2(V_{GS,load} - V_{Tn})] V_{DS, \text{load}} = V_{DS, \text{load}}^2$$

$$I_D, \text{load} = \frac{k_n, \text{load}}{2} [2[-V_{T,load}(V_{out})](V_{DD} - V_{out}) - (V_{DD} - V_{out})^2]$$



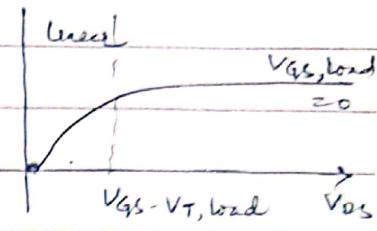
$$V_{in} = V_{OL},$$

Driver nmos - cutoff

Load nmos - linear

- (i) $V_{in} < V_{TO,driven}$, driver nmos, driver is in cut off, nmos, load is in linear

$$\begin{aligned} V_{DS} &= V_D - V_S \\ &= V_{DD} - V_{OH} \end{aligned}$$



$$V_{DS,load} = V_D - V_S$$

$$= V_{DD} - V_{DD} = 0$$

Saturation Region

$$V_{DS,load}$$

V_{in}	V_{out}	E-nmos, driver	D-nmos, load	$\geq V_{DS,load} - V_{T,load}$
V_{OL}	V_{OH}	Cutoff	Linear.	$V_{DD} - V_{out} \geq -V_{T,load}$
V_{IL}	$\approx V_{OH}$	Saturation	Linear	$V_{DD} + V_{T,load} \geq V_{out}$
V_{IH}	Small	Linear	Saturation.	$V_{out} \leq V_{DD} + V_{T,load}$
V_{OLT}	V_{OL}	Linear	Saturation.	Linear [$V_{out} > V_{DD} + V_{T,load}$]

- (ii) $V_{in} \geq V_{TO,driven}$, driver nmos starts conducting and it will be in saturation region and it remains in saturation as long as $V_{TO,driven} \leq V_{in} < V_{DS,driven} + V_T$

and load nmos will be in linear

i.e. for $V_{in} = V_{IL}$, driver nmos is in saturation and load nmos is linear. and V_{out} gradually starts decreasing.

- (iii) $V_{in} = V_{IH}$, driver nmos will be in linear region and load nmos is saturation and V_{out} will be small.

- (iv) $V_{in} = V_{OH}$, driver nmos is in saturation and load nmos is saturation and $V_{out} = V_{OL}$.

$$V_{DS,load} \geq V_{GS,load} - V_{T,load}(V_{out})$$

$$V_{out} \leq V_{DD} + V_{T,load}$$

$\text{if } V_{out} > V_{DD} + V_{T,load}$

$$V_{DD} - V_{out} \geq Q - V_{T,load}(V_{out}).$$

$$V_{DD} + V_{T,load} \geq V_{out}.$$

Calculation of V_{out}

When $V_{in} < V_{TO}$ (ie threshold of nmos with $V_{SB}=0$) of nmos then, nmos (driver) is in cutoff and load nmos is in linear region.

$$I_{D, \text{driver}} = I_{D, \text{load}} = 0$$

$$V_{out} = V_{OH} = V_{DD}$$

Calculation of V_{OL}

To calculate V_{OL} , we assume that input $V_{in} = V_{OH} = V_{DD}$

$$\text{When } V_{in} = V_{OH} = V_{DD}$$

driver nmos is in linear region while depletion load is in saturation

$$I_{D, \text{driver}} = k_{\text{driver}} \left[\frac{2(V_{GS} - V_{TO}) V_{DS} - V_{DS}^2}{2} \right]$$

$$= k_{\text{driver}} \left[\frac{2(V_{in} - V_{TO}) V_{DL} - V_{DL}^2}{2} \right] \quad (1)$$

$$\text{and } I_{D, \text{load}} = k_{\text{load}} \left[\frac{2(V_{GS} - V_{T, \text{load}})(V_{out})}{2} \right]$$

$$V_{GS, \text{load}} = 0$$

$$\therefore I_{D, \text{load}} = k_{\text{load}} \left[-V_{T, \text{load}}(V_{out}) \right]^2 \quad (2)$$

$$\text{where } V_{T, \text{load}} = V_{TO} + 2 \sqrt{|2\phi_F| + V_{out} - \sqrt{|2\phi_F|}} \quad (3)$$

$$\text{By equating eq (1) + (2)} \quad I_{D, \text{driver}} = I_{D, \text{load}}$$

$$\frac{k_{\text{driver}}}{2} \left[2(V_{OH} - V_{TO}) V_{OL} - V_{OL}^2 \right] = \frac{k_{\text{load}}}{2} \left[-V_{T, \text{load}}(V_{out}) \right]^2$$

By rearrangement

$$V_{OL}^2 - [2(V_{OH} - V_{TO}) V_{OL}] + \frac{k_{\text{load}}}{k_{\text{driver}}} [-V_{T, \text{load}}(V_{out})]^2 = 0$$

find root

$$V_{OL} = \frac{2(V_{OH} - V_{TO}) V_{OL}}{2 \times 1} \pm \sqrt{\frac{4(V_{OH} - V_{TO})^2 - 4 \times 1 \times \frac{k_{\text{load}}}{k_{\text{driver}}} [-V_{T, \text{load}}(V_{out})]^2}{2 \times 1}}$$

$$V_{OL} = (V_{OH} - V_{TO}) - \sqrt{(V_{OH} - V_{TO})^2 - \frac{k_{\text{load}}}{k_{\text{driver}}} |V_{T, \text{load}}(V_{out})|^2} \quad (4)$$



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As $V_{T,load}$ is function of V_{out} (i.e. $V_{out} = V_{OL}$), the actual value of V_{OL} can be found by solving the two equations (3) and (4) using numerical iterations. The iterative method converges rapidly because the actual value of V_{OL} is relatively small.

Calculation of V_{IL}

When $V_{in} = V_{IL}$, driver transistor operates in saturation if load transistor operates in linear region.

By applying KCL at o/p node

$$I_{D,driver} = \frac{k_n,driver}{2} [V_{gs,driver} - V_{TO}]^2$$

$$= \frac{k_n,driver}{2} [V_{IL} - V_{TO}]^2 \quad \text{--- (1)}$$

$$I_{D,load} = \frac{k_n,load}{2} \left[2(V_{gs,load} - V_{T,load}(V_{out})) (V_{DS,load}) - (V_{DS,load})^2 \right]$$

$$V_{gs,load} = 0 \quad \text{and} \quad V_{DS,load} = V_D - V_{out} = (V_{DD} - V_{out})$$

$$\therefore I_{D,load} = \frac{k_n,load}{2} \left[2(-V_{T,load}(V_{out})) (V_{DD} - V_{out}) - (V_{DD} - V_{out})^2 \right] \quad \text{--- (2)}$$

Equating (1) and (2)

$$\frac{k_n,driver}{2} (V_{IL} - V_{TO})^2 = \frac{k_n,load}{2} \left[2(-V_{T,load}(V_{out})) (V_{DD} - V_{out}) - (V_{DD} - V_{out})^2 \right] \quad \text{--- (3)}$$

As V_{IL} is defined at a slope $= -1$ ($dV_{out}/dV_{in} = -1$), we differentiate eq 2 (3) w.r.t V_{in}

$$\frac{k_n,driver}{2} 2(V_{IL} - V_{TO}) = \frac{k_n,load}{2} \left[2(-V_{T,load}(V_{out})) \cdot \left(-\frac{dV_{out}}{dV_{in}} \right) + 2(V_{DD} - V_{out}) \left(-\frac{dV_{T,load}(V_{out})}{dV_{in}} \right) - 2(V_{DD} - V_{out}) \left(-\frac{dV_{out}}{dV_{in}} \right) \right]$$

Assume

Substitute $(dV_{out}/dV_{in}) = -1$ and $(dV_{T,load}(V_{out})/dV_{in})$ is very small compared to other values.

$$\frac{2(V_{in} - V_{T0})}{2} \cdot$$

$$2(V_{in} - V_{T0}) = \frac{k_{nload}}{k_{ndriver}} \left[2(-V_{T,load}(V_{out})) \left(-\frac{dV_{out}}{dV_{in}} \right) \right]$$

$$+ 2(V_{DD} - V_{out}) \left(-\frac{d(+V_{T,load}(V_{out}))}{dV_{out}} \right) \left(\frac{dV_{out}}{dV_{in}} \right) - 2(V_{DD} - V_{out}) \left(-\frac{dV_{out}}{dV_{in}} \right)$$

In this

$$\frac{d(V_{T,load}(V_{out}))}{dV_{out}} = \gamma \quad \text{by Implicit differentiation}$$

When $V_{in} = V_{IL}$, $V_{out} \approx V_{olt}$ (Assume $V_{out} = 4.81V$) and $\gamma = 0.4$ and $\phi = 0.3$.

$$\frac{d(V_{T,load}(V_{out}))}{dV_{out}} = \frac{0.4}{2\sqrt{0.6 + 4.81}} = 0.0860$$

& the term

$$2(V_{DD} - V_{out}) \frac{dV_{T,load}(V_{out})}{dV_{out}} = 2(5 - 4.81)(0.0860) \\ = 0.0327V$$

This value is ^{very} small compared other values so the term $\frac{dV_{T,load}(V_{out})}{dV_{out}}$ is neglected

$$\frac{dy^2(x)}{dx} = \frac{dy^2}{dy} \cdot \frac{dy}{dx} = 2y \cdot \frac{dy}{dx} \quad \because y(x) \text{ when } y \text{ depends on } x$$

Now eq² (4) by substituting $\frac{dV_{out}}{dV_{in}} = -1$ and assuming $\frac{dV_{T,load}(V_{out})}{dV_{in}}$ is very small, it is neglected.

$$\frac{d(V_{in} - V_{T0})}{2} = \frac{k_{nload}}{k_{ndriver}} \left[\gamma(-V_{T,load}(V_{out})) (1) + 0 - \gamma^2(V_{DD} - V_{out}) (1) \right]$$

$$V_{in} = V_{T0} + \frac{k_{nload}}{k_{ndriver}} \left[V_{out} - V_{DD} + |V_{T,load}(V_{out})| \right]$$

$$V_{IL} = V_{T0} + \frac{k_{nload}}{k_{ndriver}} \left[V_{out} - V_{DD} + |V_{T,load}(V_{out})| \right] \quad (5)$$

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Calculation of V_{in}

- V_{IH} is larger of the two voltage points on VTC at which slope is equal to (-1)
- At $V_{in} = V_{IH}$, the output V_{out} corresponds to the operating point which is relatively small and the driver transistor is linear region and load transistor is in saturation
- By KCL at the output node

$$\frac{k_n \text{driver}}{2} [2(V_{gs, \text{drive}} - V_{TO})(V_{DS, \text{drive}}) - (V_{DS, \text{drive}})^2] = \frac{k_n \text{load}}{2} [V_{gs, \text{load}} - V_{T, \text{load}}(V_{at})]^2$$

$$\frac{k_n \text{driver}}{2} [2(V_{in} - V_{TO}) V_{out} - V_{out}^2] = \frac{k_n \text{load}}{2} [-V_{T, \text{load}}(V_{at})]$$
-(1)

By differentiating w.r.t V_{in} as V_{IH} is defined at slope = -1

$$\begin{aligned} & \left[2(V_{in} - V_{TO}) \cdot \frac{dV_{at}}{dV_{in}} + 2V_{out}(1) - 2V_{out} \cdot \frac{dV_{at}}{dV_{in}} \right] \\ &= \left(\frac{k_n \text{load}}{k_n \text{driver}} \right) \frac{d(V_{T, \text{load}}(V_{at}))}{dV_{out}} \cdot \left(-\frac{dV_{at}}{dV_{in}} \right) \end{aligned} \quad -(2)$$

Substitute $(dV_{at}/dV_{in} = -1)$ and $d(V_{T, \text{load}}(V_{at})) / dV_{out}$ gives larger value so not neglected

$$\cancel{2(V_{in} - V_{TO})(-1)} + \cancel{2V_{out}} - \cancel{2V_{out}(-1)} = \left(\frac{k_n \text{load}}{k_n \text{driver}} \right) \frac{dV_{T, \text{load}}(V_{at})}{dV_{at}}$$

$$-V_{in} + V_{TO} + 2V_{out} = \left(\frac{k_n \text{load}}{k_n \text{driver}} \right) [-V_{T, \text{load}}(V_{at})] \cdot \frac{dV_{T, \text{load}}}{dV_{at}}$$

$$\boxed{V_{in} = V_{TO} + 2V_{out} + \left(\frac{k_n \text{load}}{k_n \text{driver}} \right) [-V_{T, \text{load}}(V_{at})] \cdot \frac{dV_{T, \text{load}}}{dV_{at}}}$$

where $dV_{T, \text{load}} = \gamma$

$$\frac{dV_{T, \text{load}}}{dV_{out}} = \frac{\gamma}{2\sqrt{12\phi_F} + V_{out}} \quad -(4)$$

$$V_{T, \text{load}}(V_{at}) = V_{TO} + \gamma \sqrt{12\phi_F} + V_{out} - \sqrt{12\phi_F}$$



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The actual value of V_{IH} and corresponding output voltage are determined by solving eq² (4) together with eq(1) and eq¹ (3) using numerical iterations.

From the expression obtained for V_{OL} , V_{IL} , and V_{IH} it is clear that they depend on terms like

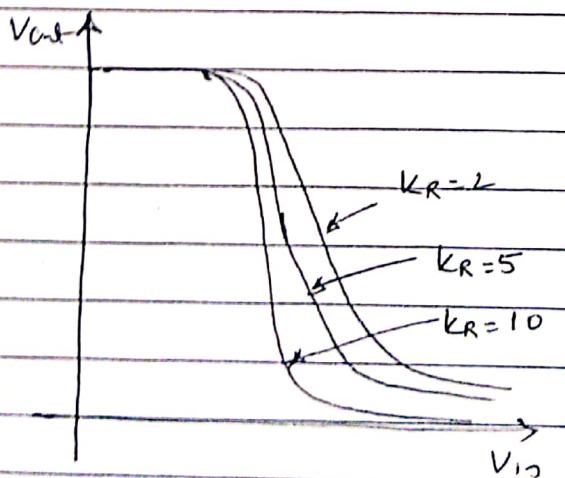
- a) threshold voltages of driver and load transistor
- b) Ratio of (k_{load}/k_{driver})

In these, threshold values are set by fabrication process. ∴ driver to load ratio is primary design parameter which can be adjusted to achieve desired VTC shape.

As in $(k_{load}/k_{driver}) \neq \frac{k_n'(\omega/L)_{load}}{k_n'(\omega/L)_{driver}}$ where -

$k_n'_{load} \approx k_n'_{driver}$. Therefore control voltages depend solely on (ω/L) ratio of the ~~transistor~~ driver and load transistor.

$(k_R = \frac{k_{driver}}{k_{load}})$ ie driver to load ratio has the effect on VTC.



By In the ~~#~~ critical voltage $V_{OH} = V_{DD}$ and is the remains three V_{OL} is the most significant critical voltage design constraint. Designing the inverter to achieve a certain V_{OL} value will automatically set the other two critical voltages,

V_{IL} and V_{IH} and KCL eq² of V_{OL} can be rearranged to calculate the driver to Load ratio that achieves a target V_{OL} .

$$k_R = \left(\frac{k_{driver}}{k_{load}} \right) = \frac{|V_{T,load}(V_{OL})|^2}{2(V_{OH} - V_{TO})V_{OL} - V_{OL}^2} \quad \text{--- (1)}$$

$$k_R = \frac{k_n'_{\text{driver}} (W/L)_{\text{driver}}}{k_n'_{\text{load}} (W/L)_{\text{load}}} \quad (2)$$

Since the channel doping densities and consequently, the channel electron mobilities of enhancement type driver transistor and depletion type load transistor are not equal, i.e. $k_n'_{\text{driver}} \neq k_n'_{\text{load}}$ in general.
Only if $k_n'_{\text{driver}} = k_n'_{\text{load}}$ then

$$k_R = \frac{(W/L)_{\text{driver}}}{(W/L)_{\text{load}}} \quad (3)$$

Design procedure thus for determines the ratio of the driver and the load transconductances, but not specific (W/L) ratio of each transistor.

Number of designs with different (W/L) ratios to satisfy the driver to load ratio cond.

The actual sizes of driver and load transistor determined by other design constraints, such as current-drive capability, the steady state power dissipation and the transient switching speed.

* Power and Area considerations

Steady state DC power consumption of depletion type load inverter can be easily found by

- i) Amount of current being drawn from the power supply, during the input-low state and input high state.

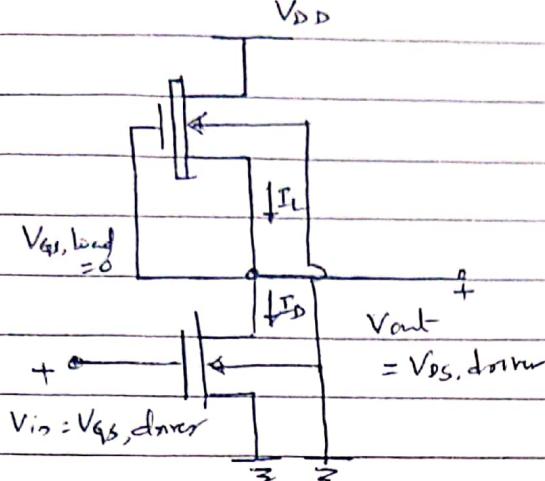
When $V_{in} = 0$ When $V_{in} = \text{low}$, driver is cut-off and $V_{out} = V_{OH} = V_{DD}$
low for 50% of time & high for the driver & load branch. Consequently no DC power dissipation for time.

$P_{DC} = V_{DD} \cdot I_{load}$. Load conduct current significantly of given by

$$\frac{k_{load}}{2} \left[\frac{-V_{T,load}}{V_{OL}} \right]^2 I_D (V_{in} = V_{DD}) = \frac{k_{load}}{2} \left[\frac{-V_{T,load}}{V_{OL}} \right]^2$$

$$= \frac{k_{load}}{2} \left[2(V_{OH} - V_{TO}) V_{OL} - V_{OL}^2 \right]$$

Calculate the critical voltages (V_{OL} , V_{OH} , V_{IL} , V_{IH}) and find the noise margins of the following depletion-load inverter circuit.



$$V_{DD} = 5V$$

$$V_{TO, \text{driver}} = 1.0V$$

$$V_{T, \text{load}} = -3.0V$$

$$(W/L)_{\text{driver}} = 2$$

$$(W/L)_{\text{load}} = 1/3$$

$$k_n'_{\text{driver}} = k_n'_{\text{load}} = 25 \mu A/V^2$$

$$\gamma = 0.4 V^{1/2}, \phi_F = -0.3V$$

Sol:

$$V_{OH} = V_{DD} = 5V$$

Calculation of V_{OL}

- for calculation of V_{OL} we need to calculate V_{OL} and $V_{T, \text{load}}$ for number of iteration.

- Start by assuming output voltage equal to zero

$$\therefore V_{T, \text{load}} = V_{TO, \text{load}} + \gamma (\sqrt{12\phi_F} + V_{out} - \sqrt{12\phi_F})$$

$$V_{T, \text{load}} = V_{TO, \text{load}} \phi = -3.0V$$

Now, first order estimation of V_{OL}

$$V_{OL} = V_{OH} - V_{TO} - \sqrt{(V_{OH} - V_{TO})^2 - \left(\frac{k_{\text{load}}}{k_{\text{driver}}} \right) |V_{T, \text{load}}(V_{OL})|^2}$$

$$= 5 - 1.0 - \sqrt{(5-1)^2 - \left(\frac{25 \times 10^{-6} \times (1/3)}{25 \times 10^{-6} \times 2} \right) (-3)^2}$$

$$V_{OL} = 0.192V$$

Now, $V_{T, \text{load}}(V_{out})$ is calculated by substituting $V_{out} = V_{OL}$

$$V_{T, \text{load}} = V_{TO, \text{load}} + \gamma (\sqrt{12\phi_F} + V_{out} - \sqrt{12\phi_F})$$

$$= -3 + 0.4 (\sqrt{0.6 + 0.192} - \sqrt{0.6})$$

$$= -2.95V$$

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Using the new value of $V_{T,load}$, we calculate V_{OL} again

$$V_{OL} = V_{OH} - V_{TO} - \sqrt{(V_{OH} - V_{TO})^2 - \left(\frac{k_{load}}{k_{dsin}}\right) |V_{T,load}(V_{OL})|^2}$$

$$= 5 - 1 - \sqrt{(5 - 1)^2 - (1/6) |2.95|^2}$$

$$V_{OL} = \underline{0.186 \text{ V}}$$

and now, $V_{T,load}(V_{OL})$ is calculated with respect to new value of V_{OL}

$$\begin{aligned} V_{T,load} &= V_{TO,load} + \gamma \left(\sqrt{|2\phi_F| + V_{out}} - \sqrt{|2\phi_F|} \right) \\ &= -3.0 + 0.4 \left(\sqrt{0.6 + 0.186} - \sqrt{0.6} \right) \\ &= -2.95 \text{ V} \end{aligned}$$

At this point, we can stop the iteration process since the threshold voltage of the load device has not changed in the two significant digit after the decimal point.

Continuing iteration would not produce a perceptible improvement of V_{OL} .

Calculation of V_{IL}

- When $V_{IN} = V_{IL}$, we expect V_{out} slightly lower than the output high voltage V_{OH} .

- As first order approximation assume $V_{T,load} \cdot V_{out} = V_{OH}$.

For $V_{IN} = V_{IL}$, if $V_{T,load}(V_{out})$ is calculated with $V_{out} = 5 \text{ V}$,

$$\begin{aligned} V_{T,load} &= V_{TO,load} + \gamma \left(\sqrt{|2\phi_F| + V_{out}} - \sqrt{|2\phi_F|} \right) \\ &= -3 + 0.4 \left(\sqrt{0.6 + 5} - \sqrt{0.6} \right) = \underline{-2.36 \text{ V}} \end{aligned}$$

Now

$$\begin{aligned} V_{IL}(V_{out}) &= V_{TO} + \left(\frac{k_{load}}{k_{dsin}} \right) [V_{out} - V_{DD} + |V_{T,load}(V_{out})|] \\ &= 1 + (1/6) (V_{out} - 5 + 2.36) \end{aligned}$$

$$V_{IL} = 0.167 V_{out} + 0.56$$

$$\text{By rearranging } \boxed{V_{out} = 6V_{IL} - 3.35}$$



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No substitute this in KCL eq² of V_{IL} calculation.

$$\frac{K_{DD}}{2} (V_{IL} - V_{TO})^2 = \frac{k_{load}}{2} [2 |V_{T,load}(V_{out})| (V_{DD} - 6V_{IL} + 3.35) - (V_{DD} - 6V_{IL} + 3.35)^2]$$

$$2(V_{IL} - 1)^2 = \frac{1}{2} [2(2.36)(5 - 6V_{IL} + 3.35) - (5 - 6V_{IL} + 3.35)^2]$$

Solution of 2nd order eq² yields two possible values

$$V_{IL} = \begin{cases} 0.98V \\ 1.36V \end{cases}$$

Note: V_{IL} must be larger than threshold voltage V_{TO} of the driver transistor, hence V_{IL} = 1.36V is chosen as V_{TO} = 1V.

$$\therefore V_{out} = 6V_{IL} - 3.36 = 6 \times 1.36 - 3.36 = 4.81V$$

$| V_{out} = 4.81V |$

which significantly improves our initial assumption of V_{out} = 5V

Iteration 2: Recalculate V_{T,load} w.r.t new value of V_{out}

$$\begin{aligned} V_{T,load} &= V_{TO,load} + \gamma (\sqrt{|2\phi_F|} + V_{out} - \sqrt{|2\phi_F|}) \\ &= -3 + 0.4 (\sqrt{0.6} + 4.81 - \sqrt{0.6}) \\ &= -2.379 \approx -2.38 \end{aligned}$$

This value is slightly higher by 20mV than previous iteration

\therefore We can terminate the iteration at the stage of V_{IL} = 1.36

Calculation of V_{IH}

For calculation of V_{IH} we need to calculate ($dV_{T,load}/dV_{out}$)

When input voltage V_{in} = V_{IH} and output is expected to be low.

At first order approximation ~~start~~ assume the output voltage level V_{out} = V_{OL} = 0.2V. When V_{in} = V_{IH} & the load threshold voltage of the load device can be estimated as ~~V_{T,load}~~.

$$V_{T,load} (V_{out} = 0.2V) = -2.95V$$

$$\begin{aligned} V_{T,load} &= V_{TO,load} + \gamma (\sqrt{|2\phi_F|} + V_{out} - \sqrt{|2\phi_F|}) \\ &= -3.0 + 0.4 (\sqrt{0.6} + 0.2 - \sqrt{0.6}) \\ &= -2.95 \end{aligned}$$

$$\frac{dV_{T, \text{load}}}{dV_{\text{out}}} = \frac{\gamma}{2\sqrt{|2pF| + V_{\text{out}}}} = \frac{0.4}{2\sqrt{0.6 + 0.2}} = 0.22$$

Now calculate V_{IH} as function of the output voltage.

$$V_{IH}(V_{\text{out}}) = V_{TO} + 2V_{\text{out}} + \frac{k_{\text{load}}}{k_{\text{drive}}} \left[-V_{T, \text{load}}(V_{\text{out}}) \right] \frac{dV_{T, \text{load}}}{dV_{\text{out}}}$$

$$= 1 + 2V_{\text{out}} + \left(\frac{1}{6}\right) [2.95 \times 0.22]$$

$$V_{IH} = 2V_{\text{out}} + 1.108$$

$$\boxed{V_{\text{out}} = 0.5V_{IH} - 0.55}$$

Now, substitute V_{out} in KCL eq^o of V_{IH} calculation.

$$\frac{k_{\text{load}}}{2} [2(V_{IH} - V_{TO})(V_{\text{out}}) - (V_{\text{out}})^2] = \frac{k_{\text{load}}}{2} [-V_{T, \text{load}}(V_{\text{out}})]^2$$

$$2 [2(V_{IH} - 1)(0.5V_{IH} - 0.55) - (0.5V_{IH} - 0.55)^2] = \frac{2}{3}(2.95)$$

$$2 [2[0.5V_{IH}^2 - 0.55V_{IH} - 0.5V_{IH} + 0.55] - [(0.5V_{IH})^2 + (0.55)^2]]$$

$$- 2 \times 0.5V_{IH} \times 0.55] = 2.90$$

By simplifying quadratic eq^o

$$V_{IH} = \begin{cases} -0.35 \text{ V} \\ 2.43 \text{ V} \end{cases}$$

where $V_{IH} = 2.43 \text{ V}$ is physically correct sol^e.

The output voltage at this point

$$V_{\text{out}} = 0.5(2.43) + 0.55 = 0.665 \text{ V}$$

$$\boxed{V_{\text{out}} = 0.67 \text{ V}}$$

With this V_{out} updated V_{out} value we can calculate threshold voltage $V_{T, \text{load}}(V_{\text{out}} = 0.67 \text{ V})$

$$V_{T, \text{load}} = V_{TO, \text{load}} + 0.4(\sqrt{0.6} + 0.67 - \sqrt{0.6})$$

$$= -2.9 \text{ V} \quad \text{and}$$

$$\frac{dV_{T, \text{load}}}{dV_{\text{out}}} = \frac{0.18}{\text{---}} ;$$

$$NM_H = V_{OH} - V_{IH} = 5 - 2.43 = 2.57 \text{ V}$$

$$NM_L = V_{IL} - V_{OL} = 1.36 - 0.186 = 1.17 \text{ V}$$

Calculate the critical voltage (V_{IL} , V_{IH} , V_{OL} , V_{OH}) and find the noise margin of the following depletion-load nmos inverter

$$V_{DD} = 5V$$

$$V_{TO, \text{driver}} = 1.0$$

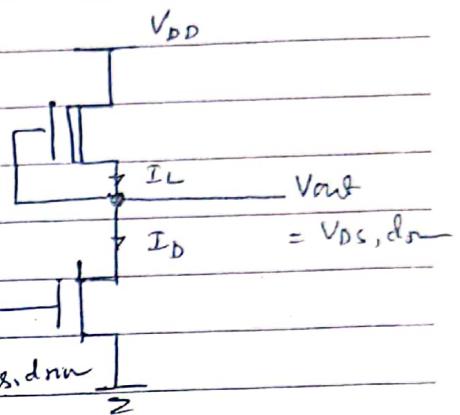
$$V_{TO, \text{load}} = -3.0$$

$$(W/L)_{\text{driver}} = 2, (W/L)_{\text{load}} = (1/3)$$

$$k_n'_{\text{driver}} = k_n'_{\text{load}} = 25 \mu A/V^2$$

$$\gamma = 0.4 V^{1/2}$$

$$\phi_F = -0.3V$$



SOL:

i) $V_{OH} = V_{DD} = 5V$.

ii) To calculate V_{OL} number of iterations are used as
 V_{OL} depends $V_{T, \text{load}}(V_{out})$

Iteration 1 : Start $V_{T, \text{load}} = V_{TO, \text{load}} = -3.0$

$$V_{OL} = V_{OH} - V_{TO} - \sqrt{(V_{OH} - V_{TO})^2 - \left(\frac{k_{\text{load}}}{k_{\text{driver}}} \right) |V_{T, \text{load}}(V_{OL})|^2}$$

$$= (5 - 1) - \sqrt{(5 - 1)^2 - \left(\frac{25 \times 10^6 \times 1/3}{25 \times 10^6 \times 2}\right) |3|^2}$$

$$= \underline{\underline{0.192V}}$$

Now, $V_{T, \text{load}}(V_{out})$ ie $V_{T, \text{load}}(V_{OL})$ is calculated

$$V_{T, \text{load}} = V_{TO, \text{load}} + \gamma \sqrt{2\phi_F} + V_{OL} - \sqrt{2\phi_F}$$

$$= -3 + 0.4 \sqrt{2 \times 0.3 + 0.192} - \sqrt{0.3}$$

$$= \underline{\underline{-2.95V}}$$

Iteration 2 : Using new value of $V_{T, \text{load}} = -2.95$, V_{OL} is calculated

$V_{OL} = 0.186V$ and then $V_{T, \text{load}}(V_{OL})$ is calculated (ie $V_{T, \text{load}}$ w.r.t new V_{OL} is calculated)

$$V_{T, \text{load}} = -2.95V$$

since the threshold $V_{T,load}$ has not changed in two significant digits after decimal point, the iterations can be stopped.

(iii) Calculation of V_{IL}

V_{IL} calculation need to be done using number of iterations by repeating the calculation of V_{IL} and $V_{T,load}(V_{out})$

when $V_{in} = V_{IL}$, we expect V_{out} slightly less $V_{OH} = V_{DD}$

As a first order approximation, assume $V_{out} = V_{OH} = 5V$ for $V_{IL} = V_{IL}$.

$$\begin{aligned}
 V_{T,load} &= V_{TO,load} + (\sqrt{|2\phi_F|} + V_{out} - \sqrt{|2\phi_F|}) \\
 &= -3.0 + 0.4(\sqrt{2 \times 0.3} + 5 - \sqrt{2 \times 0.3}) \\
 &= -3.0 + 0.4(2.3664) - 0.7745 \\
 &= -3.0 + 0.94656 - 0.7745 \\
 &= -3 + 0.4(2.3664 - 0.7745) \\
 &= -3 + 0.6367 \\
 \boxed{V_{T,load}(V_{out}) = -2.363V}
 \end{aligned}$$

$$\begin{aligned}
 V_{IL}(V_{out}) &= V_{TO} + \frac{k_{load}}{k_{dunner}} [V_{out} - V_{DD} + |V_{T,load}(V_{out})|] \\
 &= 1 + \left(\frac{1}{6}\right) (V_{out} - 5 + 2.36) \\
 &= 1 + 0.1667 V_{out} - 0.44
 \end{aligned}$$

$$V_{IL}(V_{out}) = 0.56 + 0.1667 V_{out} -$$

$$0.1667 V_{out} = V_{IL} - 0.56$$

$$\boxed{V_{out} = 6V_{IL} - 3.35}$$

By substituting V_{out} in ϵ

$$I_L = I_D$$

$$\frac{k_{dunner}(V_{IL} - V_{TO})^2}{2} = \frac{k_{load}}{7} [2|V_{T,load}(V_{out})|] \frac{(V_{out})}{(V_{DD} - V_{out})^2}$$

$$\frac{k_{dunner}(V_{IL} - V_{TO})^2}{2} = \frac{k_{load}}{2} \left[\frac{2|V_{T,load}(V_{out})|}{6V_{IL} - 3.35} \right] - \left[\frac{6V_{IL} - 3.35}{2} \right]$$

$$\frac{25 \times 10^6 \times (2)}{2}$$

DATE

$$\frac{k_{\text{driver}} (V_{IS} - V_{TO})^2}{2} = \frac{k_{\text{load}}}{2} [2|V_{T,\text{load}}(V_{AFT})| (V_{DD} - V_{out}) - (V_{DD} - V_{out})^2]$$

$$(V_{IL} - V_{TO})^2 = \frac{k_{\text{load}}}{k_{\text{driver}}} [2 \times 2.36 \times (5 - 6V_{IL} + 3.35) - (5 - 6V_{IL} + 3.35)^2]$$

$$(V_{IL} - V_{TO})^2 = \left(\frac{1}{2}\right) \left[2 \times 2.36 (5 - 6V_{IL} + 3.35) - (5 - 6V_{IL} + 3.35)^2 \right]$$

By solving

$$V_{T,\text{load}} = V_{TO,\text{load}} + \gamma \sqrt{|2dF| + V_{AFT}} - \sqrt{2dF}.$$

$$\frac{dV_{T,\text{load}}}{dV_{IS}} =$$

$$V_{IS} = V_{IL}$$

$$\frac{dV_{T,\text{load}}}{dV_{AFT}} = \frac{\gamma}{2 \sqrt{|2dF| + V_{AFT}}}$$

$$V_{IS} = V_{IH}$$

$$\frac{dV_{T,\text{load}}}{dV_{AFT}} = \frac{\gamma}{2 \sqrt{|2dF| + V_{AFT}}}$$

$$V_{AFT} = V_{OL}$$

$$\frac{0.4}{2 \sqrt{0.6 + 5}}$$

$$\frac{0.4}{2 \sqrt{0.6 + 0.2}}$$

$$0.08451$$

$$0.2236$$

As $V_{T, \text{load}} (V_{\text{out}})$

$$\text{When } V_{in} = V_{IL} \quad V_{\text{out}} \approx V_{OH}$$

$$\frac{d(V_{T, \text{load}})}{dV_{in}} = \frac{d(V_{T, \text{load}}) \times dV_{\text{out}}}{dV_{in}} \\ = \frac{\gamma}{2\sqrt{|2\phi_F| + V_{\text{out}}}} \times \frac{dV_{\text{out}}}{dV_{in}}$$

$$\text{If } \gamma = 0.4 \quad \phi_F = -0.3$$

$$\frac{dV_{T, \text{load}}}{dV_{\text{out}}} = \frac{0.4}{2\sqrt{0.6} + V_{\text{out}}} \quad (-1)$$

$$\text{If } \boxed{V_{in} = V_{IL}} \quad \boxed{V_{\text{out}} = V_{OH} \approx 5V}$$

$$\frac{dV_{T, \text{load}}}{dV_{\text{out}}} = \frac{0.4}{2\sqrt{0.6} + 5} = \frac{0.4}{2\sqrt{5.6}} = 0.0845$$

$$\text{If } \boxed{V_{in} = V_{IH}} \quad , \quad \boxed{V_{\text{out}} = V_{OL} \approx 0.2}$$

$$\frac{dV_{T, \text{load}}}{dV_{\text{out}}} = \frac{0.4}{2\sqrt{0.6} + 0.2} = 0.22$$

$$\text{When } V_{in} = V_{IL}$$

0.0845^1 can be neglected w.r.t $(dV_{\text{out}}/dV_{in})$
whereas 0.22 when $V_{in} = V_{IH}$

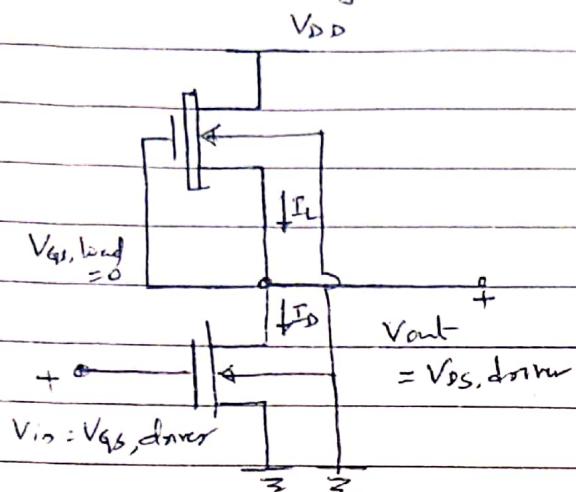
$$V_{IL} = V_{TO} + \left(\frac{k_{\text{load}}}{k_{\text{channel}}} \right) [V_{\text{out}} - V_{DS} + V_{T, \text{load}}]$$

$$\cancel{V_{DS}} = \dots$$

Body effect refers to the change in the VT of the device when there is a diff b/w sub and source voltage.

Thus it may increases the min. gate voltage needed to achieve channel inversion.

Calculate the critical voltages (V_{OL} , V_{OH} , V_{IL} , V_{IH}) and find the noise margins of the following depletion-load inverter circuit



$$V_{DD} = 5V$$

$$V_{TO, \text{driver}} = 1.0V$$

$$V_{T, \text{load}} = -3.0V$$

$$(W/L)_{\text{driver}} = 2$$

$$(W/L)_{\text{load}} = 1/3$$

$$k_n'_{\text{load}} = k_p'_{\text{load}} = 25 \mu A/V^2$$

$$\gamma = 0.4 V^{1/2}, \phi_F = -0.3V.$$

So:

$$V_{OH} = V_{DD} = 5V.$$

Calculation of V_{OL}

- for calculation of V_{OL} we need to calculate V_{OL} and $V_{T, \text{load}}$ for number of iteration.

- Start by assuming output voltage equal to zero

$$\therefore V_{T, \text{load}} = V_{TO, \text{load}} + \gamma (\sqrt{1/2 \phi_F} + V_{out} - \sqrt{1/2 \phi_F})$$

$$V_{T, \text{load}} = V_{TO, \text{load}} \phi = \pm 3.0V.$$

Now, first order estimation of V_{OL}

$$V_{OL} = V_{OH} - V_{TO} - \sqrt{(V_{OH} - V_{TO})^2 - \left(\frac{k_{\text{load}}}{k_{\text{driver}}} \right) |V_{T, \text{load}}(V_{OL})|^2}$$

$$= 5 - 1.0 - \sqrt{(5-1)^2 - \left(\frac{25 \times 10^{-6} \times (1/3)}{25 \times 10^{-6} \times 2}\right) (3)^2}$$

$$V_{OL} = 0.192V$$

Now, $V_{T, \text{load}}$ (V_{out}) is calculated by substituting V_{OL} $V_{out} = V_{OL}$

$$V_{T, \text{load}} = V_{TO, \text{load}} + \gamma (\sqrt{1/2 \phi_F} + V_{out} - \sqrt{1/2 \phi_F})$$

$$= -3 + 0.4 (\sqrt{0.6} + 0.192 - \sqrt{0.6})$$

$$= -2.95V$$

Using the new value of $V_{T,load}$, we calculate V_{OL} again.

$$V_{OL} = V_{OH} - V_{TD} - \sqrt{(V_{OH} - V_{TD})^2 - \left(\frac{k_{load}}{i_{load}}\right) |V_{T,load}(V_{OL})|}$$

$$= 5 - 1 - \sqrt{(5 - 1)^2 - \left(\frac{1}{6}\right) |2.95|^2}$$

$$V_{OL} = 0.186 \text{ V}$$

and now, $V_{T,load}(V_{OL})$ is calculated with respect to new value of V_{OL}

$$\begin{aligned} V_{T,load} &= V_{TD,load} + \gamma \left(\sqrt{|12\phi_F| + V_{out}} - \sqrt{|12\phi_F|} \right) \\ &= -3.0 + 0.4 \left(\sqrt{0.6} + 0.186 - \sqrt{0.6} \right) \\ &= -2.95 \text{ V} \end{aligned}$$

At this point, we can stop the iteration process since the threshold voltage of the load device has not changed in the two significant digit after the decimal point.

Continuing iteration would not produce a perceptible improvement of V_{OL} .

Calculation of V_{IL}

- When $V_{in} = V_{IL}$, we expect V_{out} slightly lower than the output high voltage V_{OH}

- As first order approximation assume ~~$V_{out} = V_{in}$~~ : $V_{out} = V_{in}$.

for $V_{in} = V_{IL}$. & $V_{T,load}(V_{out})$ is calculated with $V_{out} = 5 \text{ V}$

$$\begin{aligned} V_{T,load} &= V_{TD,load} + \gamma \left(\sqrt{|12\phi_F| + V_{out}} - \sqrt{|12\phi_F|} \right) \\ &= -3 + 0.4 \left(\sqrt{0.6 + 5} - \sqrt{0.6} \right) = -2.36 \text{ V} \end{aligned}$$

Now

$$\begin{aligned} V_{IL}(V_{out}) &= V_{TD} + \left(\frac{k_{load}}{i_{load}} \right) [V_{out} - V_{DD} + |V_{T,load}(V_{out})|] \\ &= 1 + \left(\frac{1}{6} \right) (V_{out} - 5 + 2.36) \end{aligned}$$

$$V_{IL} = 0.167 V_{out} + 0.56$$

$$\text{By rearranging } |V_{out} = 6V_{IL} - 3.35|$$

Now substitute this in KCL eq^o of V_{IL} calculation

$$\frac{V_{DD}}{2} \cdot (V_{IL} - V_{TO})^2 = \text{load} \left[\frac{1}{2} |V_{T, \text{load}}(V_{out})| (V_{DD} - 6V_{IL} + 3.35) - (V_{DD} - 6V_{IL} + 3.35)^2 \right]$$

$$2(V_{IL} - 1)^2 = \frac{1}{3} [2(2.36)(5 - 6V_{IL} + 3.35) - (5 - 6V_{IL} + 3.35)^2]$$

Solution of 2nd order eq^o yields two possible values

$$V_{IL} = \begin{cases} 0.98 \text{ V} & 6(V_{IL}^2 + 1 - 2V_{IL}) = [4.12(8.36) \\ & - (8V_{IL}) - (8.36 - 6V_{IL})^2] \\ 1.36 \text{ V} & \end{cases}$$

Note: V_{IL} must be larger than threshold voltage V_{TO} of the driver transistor, hence V_{IL} = 1.36 V is chosen as V_{TO} = 1 V.

$$\therefore V_{out} = 6V_{IL} - 3.36 = 6 \times 1.36 - 3.36 = 4.81 \text{ V}$$

$$V_{out} = 4.81 \text{ V}$$

which significantly improves our initial assumption of
V_{out} = 5 V

Iterations 2: Recalculate V_{T, load} w.r.t new value of V_{out}

$$\begin{aligned} V_{T, \text{load}} &= V_{TO, \text{load}} + \gamma (\sqrt{12\phi_F} + V_{out} - \sqrt{12\phi_F}) \\ &= -3 + 0.4 (\sqrt{0.6 + 4.81} - \sqrt{0.6}) \\ &= -2.379 \approx -2.38 \end{aligned}$$

This value is slightly higher by 20mV than previous iteration.
∴ We can terminate the iteration at the stage of V_{IL} = 1.36

Calculation of V_{IH} (Start with 1st order approximation V_{out} = V_{OL} = 0.2 V)

For calculation of V_{IH} we need to calculate (dV_{T, load} / dV_{out})

When input voltage V_{in} = V_{IH} and output is expected to be low.

At first order approximation start assume the output voltage level V_{out} = V_{OL} = 0.2 V, when V_{in} = V_{IH} & the load threshold voltage of the load device can be estimated as V_{T, load}.

$$V_{T, \text{load}} (V_{out} = 0.2 \text{ V}) = -2.95 \text{ V}$$

$$V_{T, \text{load}} = V_{TO, \text{load}} + \gamma (\sqrt{12\phi_F} + V_{out} - \sqrt{12\phi_F})$$

$$= -3.0 + 0.4 (\sqrt{0.6 + 0.2} - \sqrt{0.6})$$

$$= -2.95$$

$$\frac{dV_{T, \text{load}}}{dV_{\text{out}}} = \frac{\gamma}{2\sqrt{|2\beta F| + V_{\text{out}}}} = \frac{0.4}{2\sqrt{0.6 + 0.2}} = 0.22$$

Now calculate V_{IH} as function of the output voltage.

$$V_{IH}(V_{\text{out}}) = V_{TO} + 2V_{\text{out}} + \frac{k_{\text{load}}}{k_{\text{drive}}} \left[-V_{T, \text{load}}(V_{\text{out}}) \right] \left[\frac{dV_{T, \text{load}}}{dV_{\text{out}}} \right]$$

$$= 1 + 2V_{\text{out}} + \left(\frac{1}{6} \right) [2.95 \times 0.22]$$

$$V_{IH} = 2V_{\text{out}} + 1.108$$

$$V_{\text{out}} = 0.5V_{IH} - 0.55$$

Now, substitute V_{out} in KCL eq^o of V_{IIH} calculation.

$$\frac{k_{\text{load}}}{2} \left[2(V_{IH} - V_{TO})(V_{\text{out}}) - (V_{\text{out}})^2 \right] = \frac{k_{\text{load}}}{2} \left[-V_{T, \text{load}}(V_{\text{out}}) \right]^2$$

$$2 \left[2(V_{IH} - 1)(0.5V_{IH} - 0.55) - (0.5V_{IH} - 0.55)^2 \right] = \left(\frac{1}{3} \right) (2.95)^2$$

$$2 \left[2[0.5V_{IH}^2 - 0.55V_{IH} - 0.5V_{IH} + 0.55] - [(0.5V_{IH})^2 + (0.55)^2] \right. \\ \left. - 2 \times 0.5V_{IH} \times 0.55 \right] = 2.90.$$

By simplifying quadratic eq^o $V_{IH}^2 - 1.1V_{IH} - 1.1V_{IH} + 1.1 - 0.25V_{IH}^2 + 0.55V_{IH} - 0.3025$

$$V_{IH} = \begin{cases} -0.35 \text{ V} \\ 2.43 \text{ V} \checkmark \end{cases} \quad \frac{0.75V_{IH}^2 - 1.55V_{IH} - 0.6529 = 0}{0.5 \times 2} = 1.450.$$

where $V_{IH} = 2.43 \text{ V}$ is physically correct sol^e.

The output voltage at this point

$$V_{\text{out}} = 0.5(2.43) + 0.55 = 0.665 \text{ V} \checkmark$$

$$(V_{\text{out}} = 0.67 \text{ V})$$

With this V_{out} updated V_{out} value we can calculate threshold voltage $V_{T, \text{load}}(V_{\text{out}} = 0.67 \text{ V})$

$$V_{T, \text{load}} = V_{TO, \text{load}} + 0.4(\sqrt{0.6 + 0.67} - \sqrt{0.6}) \\ = -2.9 \text{ V}$$

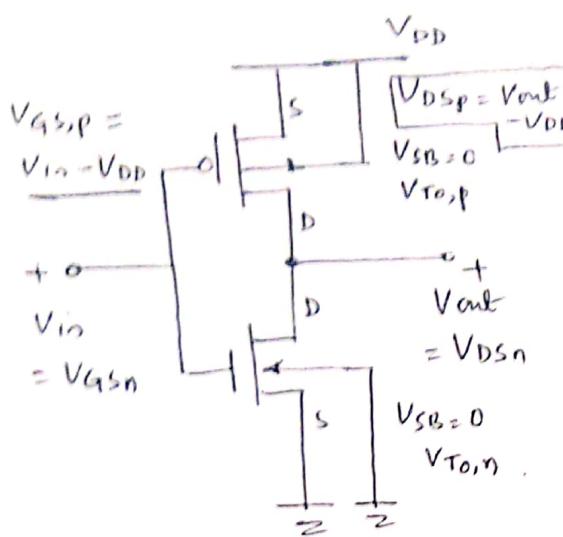
$$\frac{dV_{T, \text{load}}}{dV_{\text{out}}} = 0.18$$

$$NM_H = V_{OH} - V_{IH} = 5 - 2.43 = 2.57 \text{ V} \checkmark$$

$$NM_L = V_{IL} - V_{OL} = 1.36 - 0.186 = 1.17 \text{ V} \checkmark$$

CMOS Inverter

It consists of enhancement type nmos and pmos transistor - operating in complementary mode. ∴ the configuration is called complementary mos (cmos)



i.e. for HIGH input, the nmos transistor drives (pulls down) the output node while pmos acts as the load, and for LOW input the pmos drives (pulls up) the output node while the nmos acts as the load.

Adv:

- i) Steady state power dissipation of cmos inverter circuit is virtually negligible except for small power dissipation due to leakage current.

- ii) The VTC (Voltage Transfer curve) exhibit a full output voltage swing between 0 to V_{DD} , and VTC transition is usually very sharp.

Drawback

- i) Fabrication of cmos inverter is more complex as pmos & nmos need to be fabricated side by side

∴ cmos process must provide an n-type substrate for pmos and p-type substrate for nmos transistor. i.e. N-well (or) p-well fabrication process to be used based on substrate type

- ii) Close proximity of pmos and nmos transistor may lead to the formation of two parasitic bipolar transistors, causing latch up condition. This is prevented by addition fabrication processes.

Circuit Operation

- Input voltage is connected back to gate of both nmos and pmos transistor. Thus both transistors are driven directly by the input signal V_{in} .
- Substrate of nmos is connected to ground while substrate of pmos connected to power supply voltage, V_{DD} , ∵ $V_{SB} = 0$ for both devices, thus no substrate bias effect (No body effect) for either device. ∵ threshold values

From the ckt diagram,

$$\left. \begin{array}{l} V_{GS,n} = V_{in} \\ V_{DS,n} = V_{out} \end{array} \right\} \quad (1)$$

and

$$V_{GS,p} = V_G - V_S = V_{in} - V_{DD}$$

$$V_{GS,p} = -(V_{DD} - V_{in})$$

$$V_{DS,p} = V_D - V_S = V_{out} - V_{DD}$$

$$V_{DS,p} = -(V_{DD} - V_{out})$$

$$\left. \begin{array}{l} V_{GS,p} = -(V_{DD} - V_{in}) \\ V_{DS,p} = -(V_{DD} - V_{out}) \end{array} \right\} \quad (2)$$

Let us start analysis by
consider the two simple cases

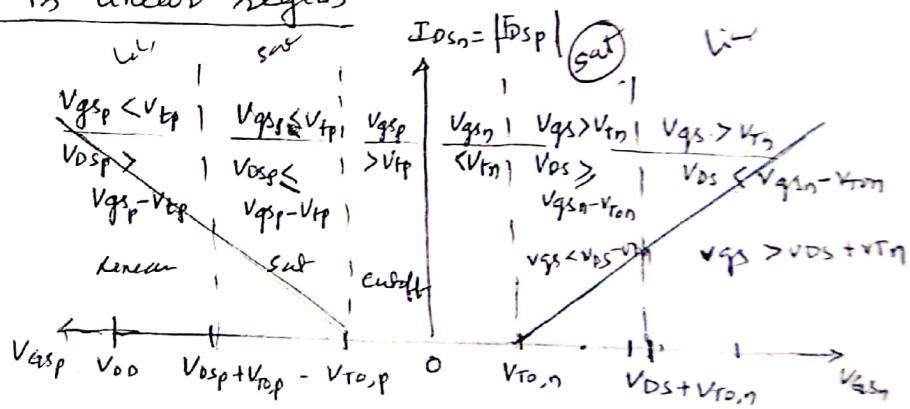
(i) When ($V_{in} < V_{Tn}$) : When input voltage is less than the nmos threshold voltage.

then, nmos is cutoff. At the same pmos is ON.

and operating in linear region

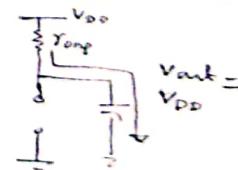
Since drain current of both transistors are approximately equal to zero

$$I_{DSn} = I_{Dsp} = 0$$



The drain-to-source voltage of the pmos transistor is equal to zero and the voltage V_{out} is equal to the power supply voltage

$$V_{out} = V_{opf} = V_{DD}$$

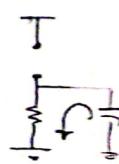


(ii) When V_{in} exceeds ($V_{DD} + V_{rop,p}$)

$$V_{Gsp} = V_G - V_S = V_{in} - V_S = (V_{DD} + V_{rop,p}) - V_{DD} = V_{rop,p}$$

$$\therefore V_{Gsp} = -(V_{DD} - V_{in}) = -(V_{DD} - V_{DD} - V_{rop,p}) = +V_{rop,p}$$

Hence, pmos transistor gets into cutoff & nmos transistor will be operating in linear region and its drain-to-source voltage is equal to zero $\therefore [V_{out} = V_{OL} = 0]$



Operating modes of nmos and pmos transistor depends on input and output voltages.

The nmos transistor is said to operate in saturation region

if a) $V_{in} > V_{TO,n}$ and

$$V_{DSn} \geq V_{GSn} - V_{TO,n} \Leftrightarrow V_{out} \geq V_{in} - V_{TO,n}$$

$$V_{out} \geq V_{in} - V_{TO,n}$$

The pmos transistor is said to operate in saturation region

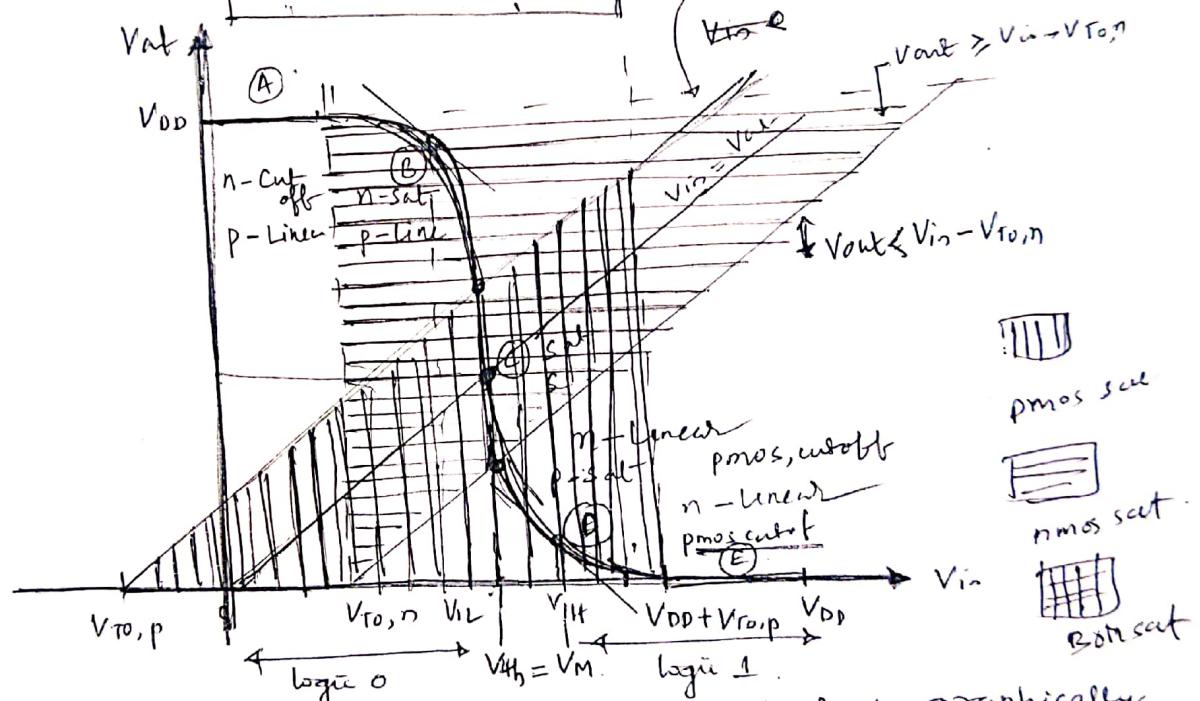
if b) $V_{in} < (V_{DD} + V_{TO,p})$ and

$$V_{DSp} \leq V_{GSp} - V_{TO,p} \Leftrightarrow V_{out} \leq V_{in} - V_{TO,p}$$

$$V_{out} - V_{DD} \leq V_{in} - V_{DD} - V_{TO,p}$$

$$V_{out} \leq V_{in} - V_{TO,p}$$

$$V_{out} = V_{in} - V_{TO,p}$$



Device saturation conditions are illustrated graphically with shaded area on $V_{out} - V_{in}$ plane. and VTC is also superimposed for easy reference. We can identify five regions of operations in Regions A, B, C, D and E corresponding to different set of operating cond^rs

Region	V_{in}	$V_{out} - V_{in}$	nmos	pmos
A	$< V_{TO,n}$	High $\approx V_{DD}$	Cutoff	Linear
B	V_{IL}	High $\approx V_{DD}$	Saturation	Linear
C	V_{TH}	V_{TH}	Saturation	Saturation
D	V_{IH}	Low $\approx V_{DD}$	Linear	Saturation
E	$> (V_{DD} + V_{TO,p})$	V_{DD}	Ideal	Cutoff

Region A

When $V_{in} < V_{TO,n}$

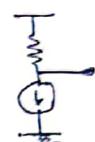
NMOS is in cutoff and } $V_{out} = V_{OH} = V_{DD}$.
PMOS is in linear



* Colvin

Region B

- As V_{in} is increased beyond $V_{TO,n}$, the NMOS transistor starts conducting in saturation region and the output voltage starts decreasing
- Critical voltage V_{IL} defined at $dV_{out}/dV_{in} = -1$ is located in within region B.



Region C

- As V_{in} is further increased, V_{out} decreases further as a result PMOS moves into saturation region at the boundary of region C.

- The inverter threshold voltage V_{th} , where $V_{in} = V_{out}$ is located in Region C.

- In region C, both transistors are operating in saturation region.

Region D

- When V_{out} falls below $(V_{in} - V_{TO,n})$, the NMOS transistor starts operating in linear region (still PMOS is in saturation)
- V_{IH} defined at $(dV_{out}/dV_{in} = -1)$ is located in Region D.

Region E

- When $V_{in} > V_{DD} + V_{rop}$, the PMOS transistor cutoff

$$\therefore V_{GSp} = V_g - V_s = V_{in} \Leftrightarrow V_s = V_{DD} + V_{rop} - V_{DD} = V_{TO,p}$$

$\therefore V_{GSp} > V_{TO,p}$ (PMOS is cutoff)

and $V_{out} = V_{OL} = 0$

Significant feature of CMOS Inverter

- The current drawn from the power supply in both of these regions A and E (steady state operating points) is nearly equal to zero as one of the device is in cutoff.
- The only current that flows in either case is because small leakage current of reverse biased source and drain junctions
- CMOS Inverter can be driven loads like interconnect capacitor or fan-out devices logic gates connected to output node, either by supply driving signal or remove from the load

* Calculation of V_{IL}

V_{IL} is input voltage defined at a point where $\frac{dV_{out}}{dV_{in}} = -1$ on VTC.
 & When $V_{in} = V_{IL}$, nmos is in saturation region and pmos is in the linear region.

$$I_{D,n} = I_{D,p}$$

$$\frac{k_n}{2} (V_{GS,n} - V_{TO,n})^2 = \frac{k_p}{2} [2(V_{GS,p} - V_{TO,p}) V_{DS,p} - V_{DS,p}^2] \quad (1)$$

w.k.t
 $V_{GS,n} = V_{in}$; $V_{GS,p} = V_{in} - V_{DD}$; $V_{DS,p} = (V_{out} - V_{DD})$ — By substituting

these in above eq²

$$\frac{k_n}{2} (V_{in} - V_{TO,n})^2 = \frac{k_p}{2} [2(V_{in} - V_{DD} - V_{TO,p}) (V_{out} - V_{DD}) - (V_{out} - V_{DD})^2] \quad (2)$$

As V_{IL} is defined at $\frac{dV_{out}}{dV_{in}} = -1$, in order to satisfy this condition we differentiate the eq² w.r.t V_{in} on both side.

$$k_n 2(V_{in} - V_{TO,n}) = \left(\frac{k_p}{k_n} \right) \left[2(V_{in} - V_{DD} - V_{TO,p}) \cdot \left(\frac{dV_{out}}{dV_{in}} \right) + 2(V_{out} - V_{DD}) \cdot (1) \right. \\ \left. - 2(V_{out} - V_{DD}) \left(\frac{dV_{out}}{dV_{in}} \right) \right] \quad (3)$$

Substitute $\left(\frac{dV_{out}}{dV_{in}} = -1 \right)$ in eq¹ (3)

$$k_n (V_{in} - V_{TO,n}) = \left(\frac{k_p}{k_n} \right) \left[2(V_{in} - V_{DD} - V_{TO,p}) (-1) + 2(V_{out} - V_{DD}) \right. \\ \left. - 2(V_{out} - V_{DD}) (-1) \right]$$

$$\underline{V_{in} = V_{IL}}$$

$$k_n (V_{IL} - V_{TO,n}) = \left(\frac{k_p}{k_n} \right) \left[-V_{IL} + V_{DD} + V_{TO,p} + V_{out} - V_{DD} + V_{out} \right. \\ \left. - V_{DD} \right]$$

$$k_n (V_{IL} - V_{TO,n}) = k_p [2V_{out} - V_{IL} + V_{TO,p} - V_{DD}]$$

$$k_n V_{IL} + k_p V_{IL} = k_p 2V_{out} + k_p V_{TO,p} - k_p V_{DD} + k_n V_{TO,n}$$

$$V_{IL} (k_n + k_p) = k_p (2V_{out} + V_{TO,p} - V_{DD}) + k_n V_{TO,n}$$

$$V_{IL} = \frac{k_p (2V_{out} + V_{TO,p} - V_{DD}) + k_n V_{TO,n}}{(k_n + k_p)}$$

$$V_{IL} = \frac{2V_{out} + V_{TO,p} - V_{DD} + \left(\frac{k_n}{k_p} \right) V_{TO,n}}{\left(1 + \frac{k_n}{k_p} \right)} = \frac{2V_{out} + V_{TO,p} - V_{DD}}{\left(1 + K_R \right)} + K_R V_{TO,p}$$

where $K_R = \frac{k_n}{k_p}$

Calculation

Eq²(4) should be solved along with KCL eq²(2) to obtain the numerical value of V_{IL} and corresponding It does not require any iterations as is none of the transistor is subject to substrate bias effect

Calculation of V_{IH}

When $V_{in} = V_{IH}$; nmos is in linear region and pmos is in saturation.

Apply KCL to the o/p node

$$\frac{k_n}{2} [2(V_{gs,n} - V_{To,n}) V_{DS,n} - V_{DS,n}^2] = \frac{k_p}{2} [V_{gs,p} - V_{To,p}]^2 \quad (1)$$

$$V_{gs,n} = V_{in}, V_{DS,n} = V_{out}, V_{gs,p} = V_{in} - V_{DD}, \quad \#$$

$$\frac{k_n}{2} [2(V_{in} - V_{To,n}) V_{out} - V_{out}^2] = \frac{k_p}{2} [V_{in} - V_{DD} - V_{To,p}]^2 \quad (2)$$

As V_{IH} is defined at $\frac{dV_{out}}{dV_{in}} = -1$; differentiate eq²(2) wrt V_{in}

$$k_n \left[\cancel{\frac{d}{dV_{in}}(V_{in} - V_{To,n})} \left(\frac{dV_{out}}{dV_{in}} \right) + \cancel{\frac{d}{dV_{in}}(1)} - \cancel{\frac{d}{dV_{in}}(V_{out})} \left(\frac{dV_{out}}{dV_{in}} \right) \right] \\ = k_p \cancel{\frac{d}{dV_{in}}(V_{in} - V_{DD} - V_{To,p})} \quad (3)$$

Substitute $V_{in} = V_{IH}$ & $\left(\frac{dV_{out}}{dV_{in}} = -1 \right)$

$$k_n \left[(V_{IH} - V_{To,n})(-1) + V_{out} - V_{out}(-1) \right] = k_p [V_{IH} - V_{DD} - V_{To,p}]$$

$$k_n [-V_{IH} + V_{To,n} + V_{out} + V_{out}] = k_p [V_{IH} - V_{DD} - V_{To,p}]$$

$$k_p V_{IH} + k_n V_{IH} = k_n [2V_{out} + V_{To,n}] + k_p [V_{DD} + V_{To,p}]$$

$$\therefore V_{IH} = \frac{k_n [2V_{out} + V_{To,n}] + k_p [V_{DD} + V_{To,p}]}{[k_n + k_p]}$$

$$\therefore = \frac{(k_n/k_p) [2V_{out} + V_{To,n}] + [V_{DD} + V_{To,p}]}{[1 + k_n/k_p]}$$

$$\boxed{V_{IH} = \frac{V_{DD} + V_{To,p} + k_p (2V_{out} + V_{To,n})}{(1 + k_p)}} \quad (4)$$

Eq²(4) must be solved along with eq²(2) to get sol² for

Calculation of V_{th}

- The inverter threshold is defined as $V_{th} = V_{in} = V_{out}$.
- for $V_{in} = V_{out}$ both transistors are expected to be in saturation region.
- By applying KCL at o/p node

$$\frac{k_n}{2} (V_{GS,n} - V_{TO,n})^2 = \frac{k_p}{2} (V_{GS,p} - V_{TO,p})^2$$

$$(V_{in} - V_{TO,n})^2 = \frac{k_p}{k_n} ((V_{DD} - V_{in}) - V_{TO,p})^2 = \frac{k_p}{k_n} (V_{in} - V_{DD} + V_{TO,p})$$

$$(V_{in} - V_{TO,n})^2 = \left(\frac{k_p}{k_n}\right) (-V_{DD} + V_{in} - V_{TO,p})^2$$

Square root on both sides gives

$$(V_{in} - V_{TO,n}) = \pm \sqrt{\left(\frac{k_p}{k_n}\right) (-V_{DD} + V_{in} - V_{TO,p})} \quad \begin{array}{l} \text{(By definition} \\ x^2 = 4 \\ x = \pm \sqrt{4} \end{array}$$

$$(V_{in} - V_{TO,n}) = \pm \sqrt{\left(\frac{k_p}{k_n}\right) (-V_{DD} + V_{in} - V_{TO,p})}$$

In order to get correct sol can be obtained by taking (-) sign

$$V_{in} - \sqrt{\frac{k_p}{k_n}} V_{in} = V_{TO,n} - \sqrt{\left(\frac{k_p}{k_n}\right) (-V_{DD} - V_{TO,p})}$$

$$\text{when } V_{in} = \frac{V_{TO,n} - \sqrt{\left(\frac{k_p}{k_n}\right) (V_{DD} + V_{TO,p})}}{1 \pm \sqrt{\frac{k_p}{k_n}}}$$

for correct sol $+ \sqrt{k_p/k_n}$ is considered as denominator can't be zero (when $k_p = k_n$)

$$\boxed{V_{in} = \frac{V_{TO,n} + \sqrt{\left(\frac{k_p}{k_n}\right) (V_{DD} + V_{TO,p})}}{1 + \sqrt{\frac{k_p}{k_n}}}}$$

$$k_R = \frac{k_n}{k_p}$$

$$\boxed{V_{in} = \frac{V_{TO,n} + \sqrt{\frac{1}{k_R}} (V_{DD} + V_{TO,p})}{1 + \sqrt{\frac{k_p}{k_n}}}}$$

$$\frac{k_n}{k_p} = 1$$

Inverter threshold voltage is defined as $V_{th} = V_{in} = V_{out}$.

$$k_n = k_p \quad \text{and} \quad V_{th} = -V_{TO,p}$$

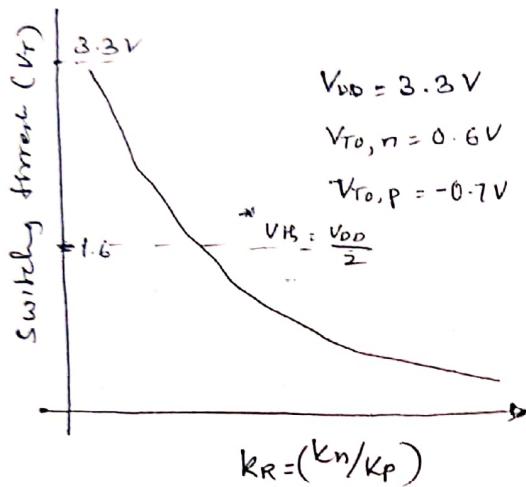
$$V_{in} = \frac{V_{DD}}{2}$$

When $V_{in} = V_{th}$,

We find that output voltage can attain any value between $(V_{th} - V_{To,n})$ and $(V_{th} + V_{To,p})$ without violating the voltage constraint used in analysis.

Note: (k_n/k_p) is transconductance ratio.

As transconductance ratio increases, V_{th} of inverter decreases. For fixed value of V_{DD} , $V_{To,n}$, & $V_{To,p}$



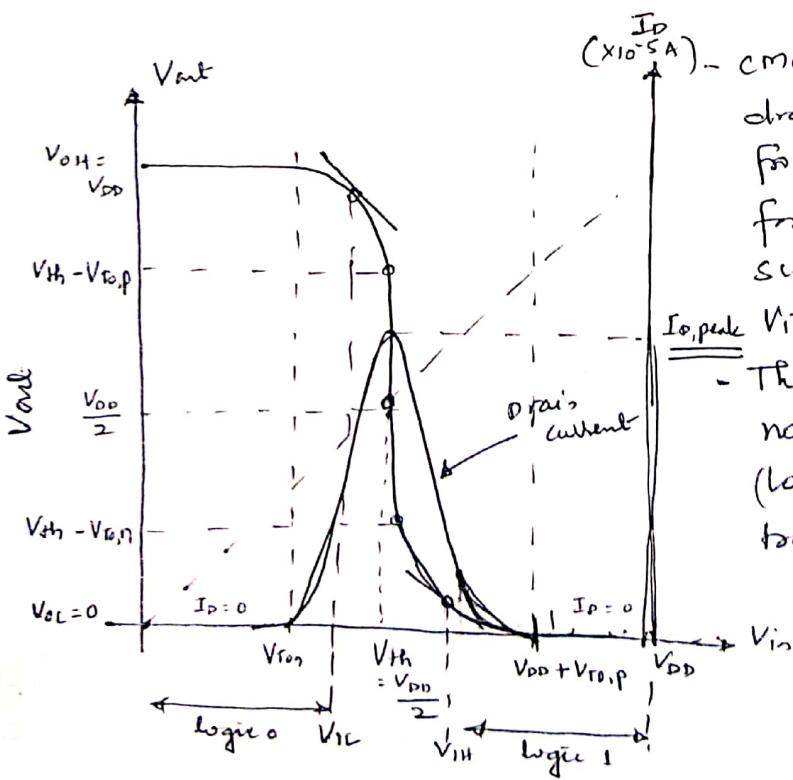
of $V_{To,n} \approx |V_{To,p}|$ (assumed)

then

$$V_{in} = V_{th} = \frac{V_{DD} + V_{To,n} + V_{To,p}}{1+1}$$

$$V_{th} = \frac{V_{DD}}{2}$$

VTC and power supply current of CMOS Inverter



$(\times 10^{-5} A)$ - CMOS Inverter does not draw significant current from power source, except for small leakage and subthreshold currents, when $V_{in} < V_{To,n}$ and $V_{in} > (V_{DD} + V_{To,p})$

- The NMOS & PMOS conduct non-zero current during (low to high) or (high to low) transition i.e. Regions B, C & D

- The current draw from power source is at its peak when $V_{in} = V_{th}$ i.e. when both are in saturation.

$$V_{th} = \frac{V_{DD}}{2} \text{ iff } k_n = k_p, \text{ Symmetric}$$

- Also we can see that when $V_{in} = V_{th}$, V_{out} can attain any value between $(V_{th} - V_{To,p})$ and $(V_{th} + V_{To,n})$

Design of CMOS Inverter

- V_{th} is one of important parameter that characterizes the steady state input-output behavior of CMOS inverter.
- It provides full output voltage swing between $(0 - V_{DD})$ ∴ Noise margin are relatively large wide.
- By setting the inverter threshold to desired level is important aspect of designing CMOS inverter.

We have,

$$V_{in} = \frac{V_{TO} + \sqrt{\frac{k_n}{K_R}} (V_{DD} + V_{TO,p})}{(1 + \sqrt{\frac{k_n}{K_R}})}$$

By rearranging

$$- V_{in} \left(1 + \sqrt{\frac{1}{K_R}} \right) = V_{TO} + \sqrt{\frac{1}{K_R}} (V_{DD} + V_{TO,p})$$

$$(V_{in} - V_{TO,n}) = \sqrt{\frac{1}{K_R}} (V_{DD} + V_{TO,p}) - V_{in} \sqrt{\frac{1}{K_R}}$$

$$= \sqrt{\frac{1}{K_R}} [(V_{DD} + V_{TO,p}) - V_{in}]$$

$$\sqrt{\frac{1}{K_R}} = \frac{(V_{in} - V_{TO,n})}{(V_{DD} + V_{TO,p} - V_{in})} \quad \checkmark$$

$$\frac{1}{K_R} = \frac{(V_{in} - V_{TO,n})^2}{(V_{DD} + V_{TO,p} - V_{in})^2}$$

$$K_R = \left(\frac{V_{DD} + V_{TO,p} - V_{in}}{V_{in} - V_{TO,n}} \right)^2$$

when $V_{in} = V_{th} = \frac{V_{DD}}{2}$ for a ideal inverter (symmetric) -

$$K_R = \left(\frac{V_{DD} + V_{TO,p} - V_{DD}/2}{V_{DD}/2 - V_{TO,n}} \right)$$

$$K_R = \left(\frac{0.5 V_{DD} + V_{TO,p}}{0.5 V_{DD} - V_{TO,n}} \right)^2$$

A symmetric inverter can be obtained by setting $V_{TO,n} = V_{TO,p}$

$$K_R = \left(\frac{k_n}{k_p} \right) = 1$$

$$= \frac{m_{ox} (k)}{2} \mu$$

$$V_{TO,n} = -V_{TO,p}$$

$$\frac{\frac{M_n \text{lo}x}{Z} \left(\frac{w}{L}\right)_n}{\frac{M_p \text{lo}x}{Z} \left(\frac{w}{L}\right)_p} = 1$$

$$\frac{\left(\frac{w}{L}\right)_n}{\left(\frac{w}{L}\right)_p} = \frac{M_p \text{lo}x}{M_n \text{co}x}$$

By substituting $M_p = 230 \text{ cm}^2/\text{V.s}$ $M_n = 580 \text{ cm}^2/\text{V.m}$
are typical values.

$$\frac{\left(\frac{w}{L}\right)_n}{\left(\frac{w}{L}\right)_p} = \frac{230 \text{ cm}^2/\text{V.m.s}}{580 \text{ cm}^2/\text{V.m.s}}$$

$\frac{1}{0.3965}$

$$\frac{\left(\frac{w}{L}\right)_n}{\left(\frac{w}{L}\right)_p} \approx 2/5 \quad 0.3965 \quad \therefore \frac{\left(\frac{w}{L}\right)_p}{\left(\frac{w}{L}\right)_n} \approx \underline{\underline{2.52}}$$

$$\boxed{\left(\frac{w}{L}\right)_p \approx 2.5 \left(\frac{w}{L}\right)_n}$$

* Effect of $(k_R = \frac{k_n}{k_p})$ on VTC

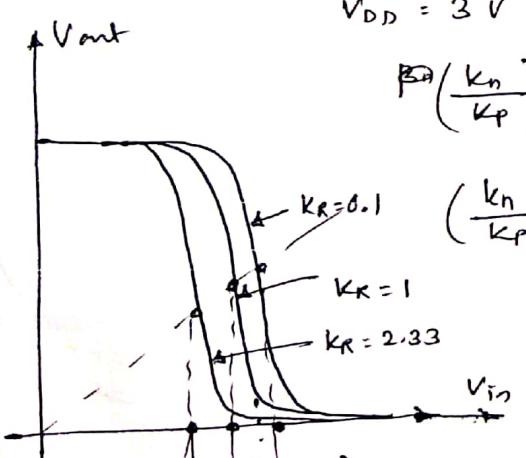
$$V_{in} = V_{TO} + \frac{\sqrt{1/k_R} (V_{DD} + V_{TO,p})}{(1 + \sqrt{1/k_R})}$$

As k_R increases, $V_{TH} = V_m$ decreases towards 0 volts (left)

\therefore As k_R increase, Dr term decreases

$$V_{DD} = 3 \text{ V} \quad V_{TH} = |V_{TP}| = 0.7 \text{ V}$$

$$\begin{array}{ll} 0.66 & 1.5 \quad k_R = 4 \\ 0.58 & 1.7 \quad k_R = 2 \end{array}$$



$$\text{For } \left(\frac{k_n}{k_p}\right) = 1 \quad V_{in} = \frac{0.7 + \sqrt{1} (3 - 0.7)}{(1 + \sqrt{1})} = \frac{3}{2} = \underline{\underline{1.5}}$$

$$\begin{aligned} V_{in} &= \frac{0.7 + \sqrt{1/2.33} (3 - 0.7)}{1 + \sqrt{1/2.33}} \\ &= \frac{0.7 + 0.655 (2.3)}{1 + 0.655} = \underline{\underline{1.33 \text{ V}}} \end{aligned}$$

$$V_{in} = \frac{0.7 + 3.16 (2.3)}{1 + 3.16} = \underline{\underline{1.92 \text{ V}}}$$

As k_R increases, V_{TH} decreases

for symmetric Inverter (CMOS) with

$V_{TO,n} = |V_{TO,p}|$ and $k_R = 1$ the critical voltage V_{IL} is

$$V_{IL} = \frac{1}{8} (3V_{DD} + 2V_{TO,n})$$

and critical voltage V_{IH} is

$$V_{IH} = \frac{1}{8} (5V_{DD} - 2V_{TO,n})$$

In a symmetric inverter sum of V_{IL} and V_{IH} is equal to V_{DD}

$$V_{IL} + V_{IH} = V_{DD}$$

Noise margin

$$NM_L = V_{IL} - V_{OL} = V_{IL}$$

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{IH}$$

$$\therefore NM_L = NM_H = V_{IL}$$

$$V_{out} = (V_{in} - V_{top}) \pm \sqrt{(V_{in} - V_{top})^2 - 2V_{PP} \left[\frac{V_{in} - V_{top}}{2} - \frac{V_{DD}}{2} - \frac{B_D}{B_P} (V_{in} - V_{top}) \right]}$$

$$V_{in} = \underline{\underline{V_{IL}}} \quad V_{top} = \underline{\underline{V_{IH}}}$$

regarding $\underline{\underline{B}}$.

$$V_{out} = \underline{\underline{V_{out}}}$$

$$V_{IL} =$$

$$\frac{3V_{IP} + 2V_{TO,n}}{8} + \frac{5V_{PP} - 2V_{TO,n}}{8}$$

$$\frac{3V_{IP} + 2V_{TO,n}}{8} = \frac{-5V_{PP} + 2V_{TO,n}}{8}$$

Region A

$$0 \leq v_{in} \leq v_{tn}$$

Region B

$$v_{tn} < v_{in} < \frac{VDD}{2}$$

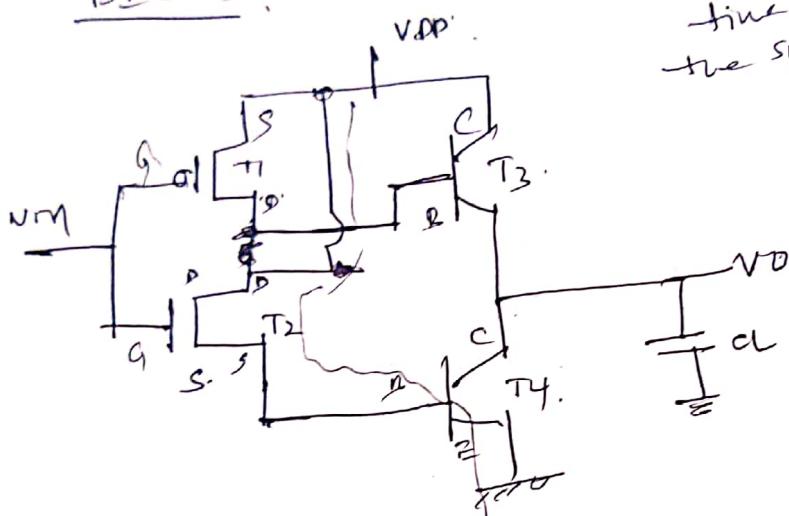
Region C

$$v_{in} - v_{tn} < v_{out} < v_{in} - v_{top}$$

Region D

$$\frac{VDD}{2} < v_{in} \leq VDD + v_{top}$$

BiCMOS



To reduce reverse recovery time of transistor or to increase the speed of transistor the following
BJT current gain ↑
cmos I_{DSS} is not.

Case-1. $v_{in} = 0$. T_1 is on, T_2 is off
 T_3 is on, T_4 is off
cap charges through T_3 .

$$V_{DP} - V_{BE} = V_0$$

$$5 - 0.7$$

$$= 4.3V$$

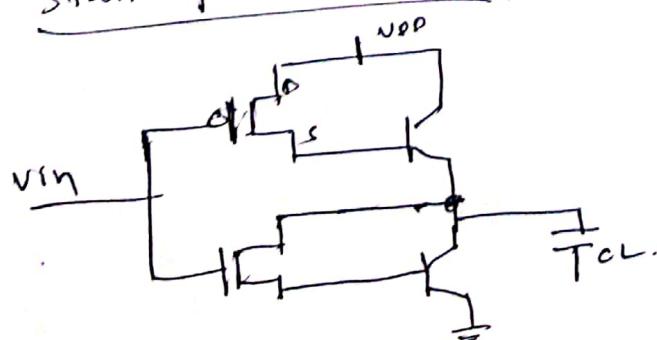
Signal degradation

Case-2 $v_{in} = 1$

T_1 is off, T_2 is on, T_4 is on - saturation. $V_{sat} = 0.2$
 $V_0 = V_{sat} = 0.3V$.

$v_{in} = 0$
 T_1 off, T_3 on.
 $V_0 = V_{DP}$

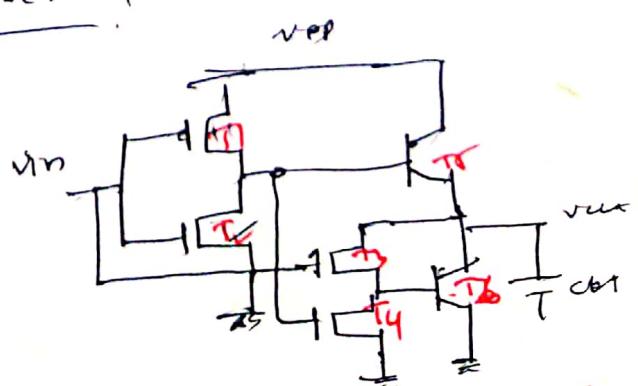
Static power dissipation



Low static power and driving capability,

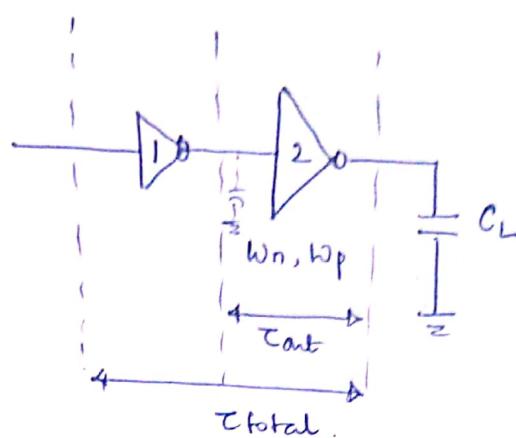
$v_{in} = 1, T_2$ off, T_5 off
 T_3 off, T_6 off //

To avoid



NMOS

Consider a case of driving large onchip / offchip capacitive load using CMOS inverter ckt, which is intern driven by another CMOS inverter



T_{out} - Propagation delay of output buffer

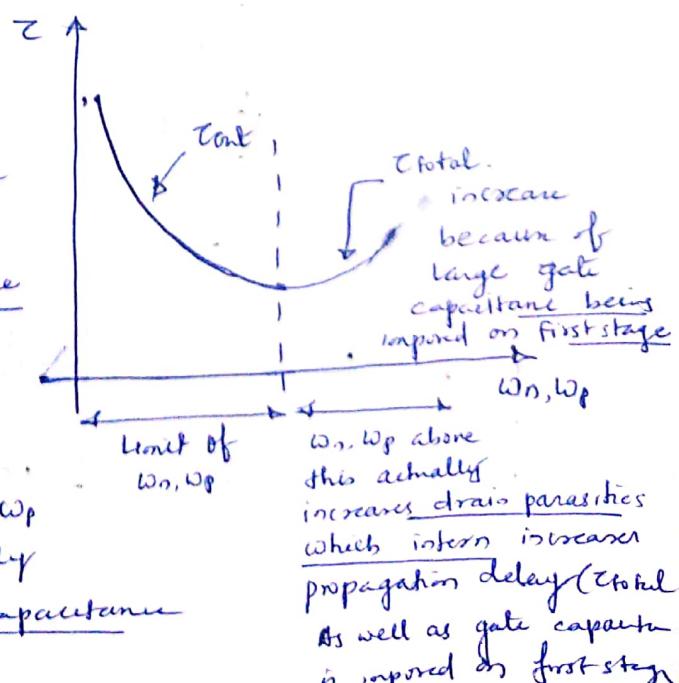
T_{total} - Propagation delay of entire two stage structure

To drive large capacitive loads with specified propagation delay using CMOS can be done by

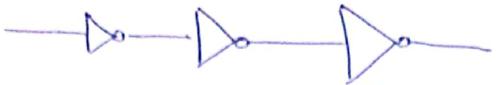
- Designing the output buffer with sufficiently large transistor widths W_n and W_p . (Area of silicon used increases)
- Simply increasing channel width of NMOS & PMOS is not sufficient as the increase in width increases the drain capacitance parasitics and eventually destroys the switching speed improvement to be gained by increase in large transistor size.
- T_{out} (output stage propagation delay) can not be reduced beyond certain limit due to increase in drain parasitics due to increase in width of channel.

In fact T_{total} (overall delay) of two stages increases with large value of W_n and W_p , because of large gate capacitance being imposed on the first stage.

i.e. Increase in W_n, W_p of output buffer actually leads to larger gate capacitance driven by first stage.



The only feasible soln for driving large capacitors obtained by scaled buffer chain



but, it uses larger silicon area.

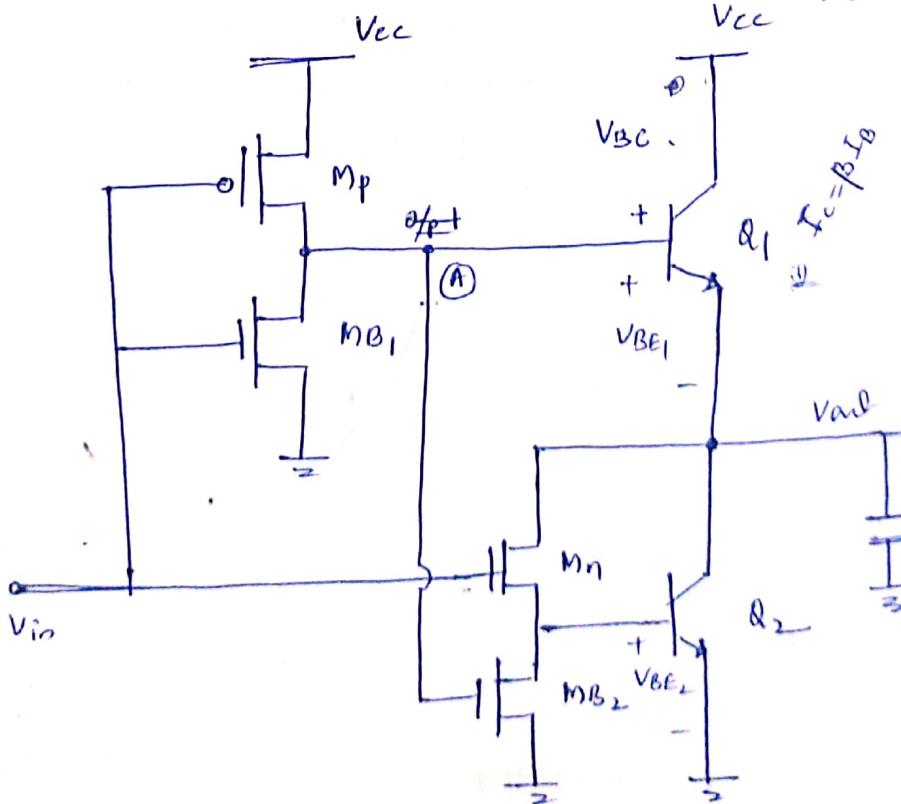
∴ BiCMOS ckt are used. In BiCMOS it uses advantages of BJT and MOS devices.

1) Bipolar devices have more driving capability and hence ^{speed} overcomes bottleneck using lesser area.
but BJT have more power dissipation than CMOS.

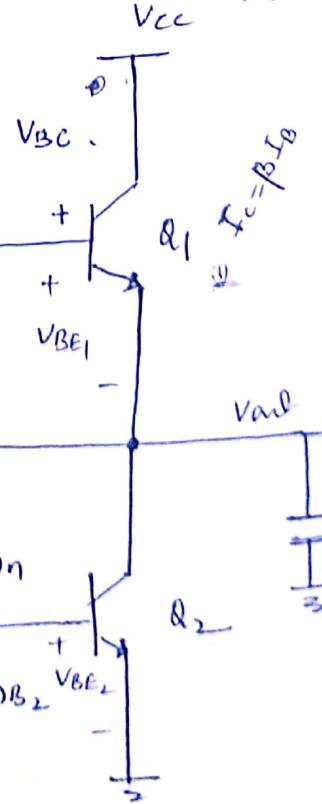
2) CMOS have low static power dissipation but less driving capacity & slow speed (large propagation delay as W_n, W_p increases).

∴ BiCMOS use advantages of Bipolar & MOS devices to overcome the bottleneck of driving large capacitive loads with less propagation delay keeping area minimum of power dissipation minimum

* BiCMOS Inverter



$V_{BE} < 0$, 1) Cutoff
 $V_{BC} < 0$, 2) Forward Active ($V_{BE} > 0$)
 $V_{BC} > 0$, 3) Saturation ($V_{BE} < 0$)

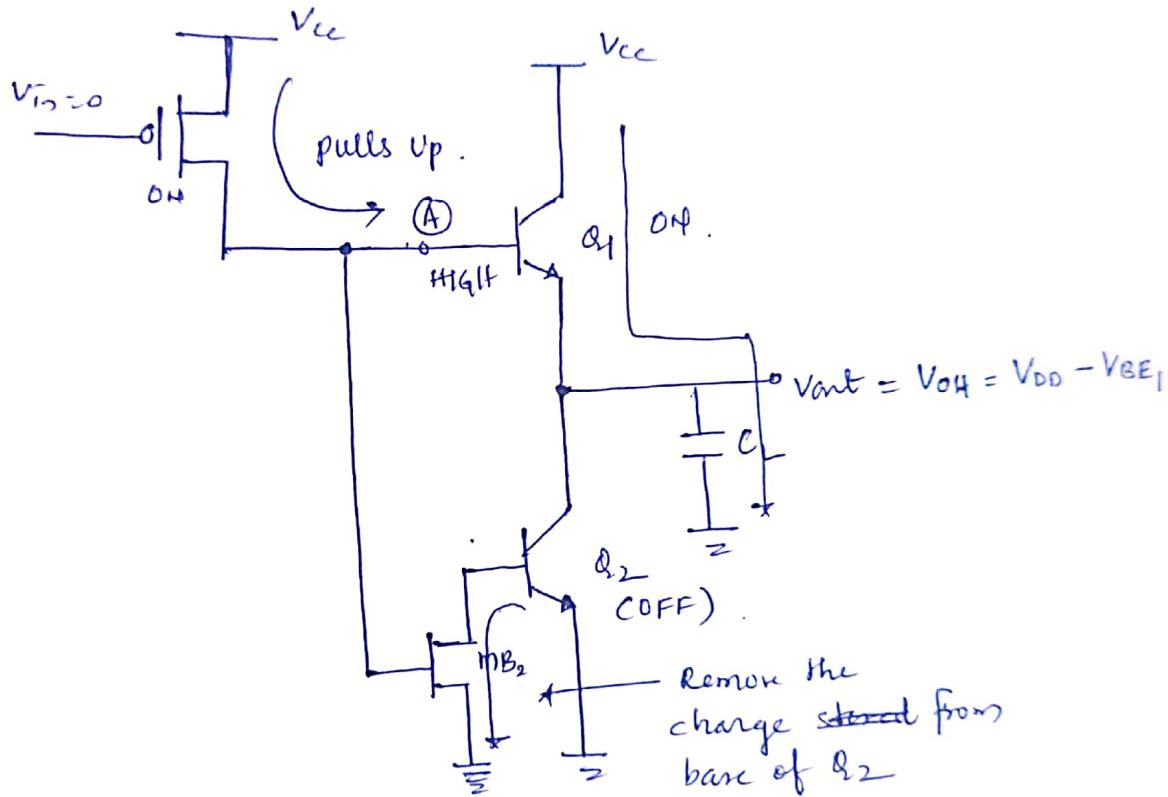


M_{B1}, M_{B2} are used to remove the charge from bare terminal of $\&_1$ and $\&_2$ resp

This speeds up the switching of the ckt enhancing its use as an output driver.

advantages of
capacitor
area.

in-OFF, MB1-OFF and MP is ON
since MP and MB1 form a inverter, the o/p is HIGH. This
high output drives the base of Q1 at and Q1 turns ON
ie active and also high o/p at point A also makes MB2
ON. which grounds base of Q2 (ie makes the helps to remove
charge from base of Q2)

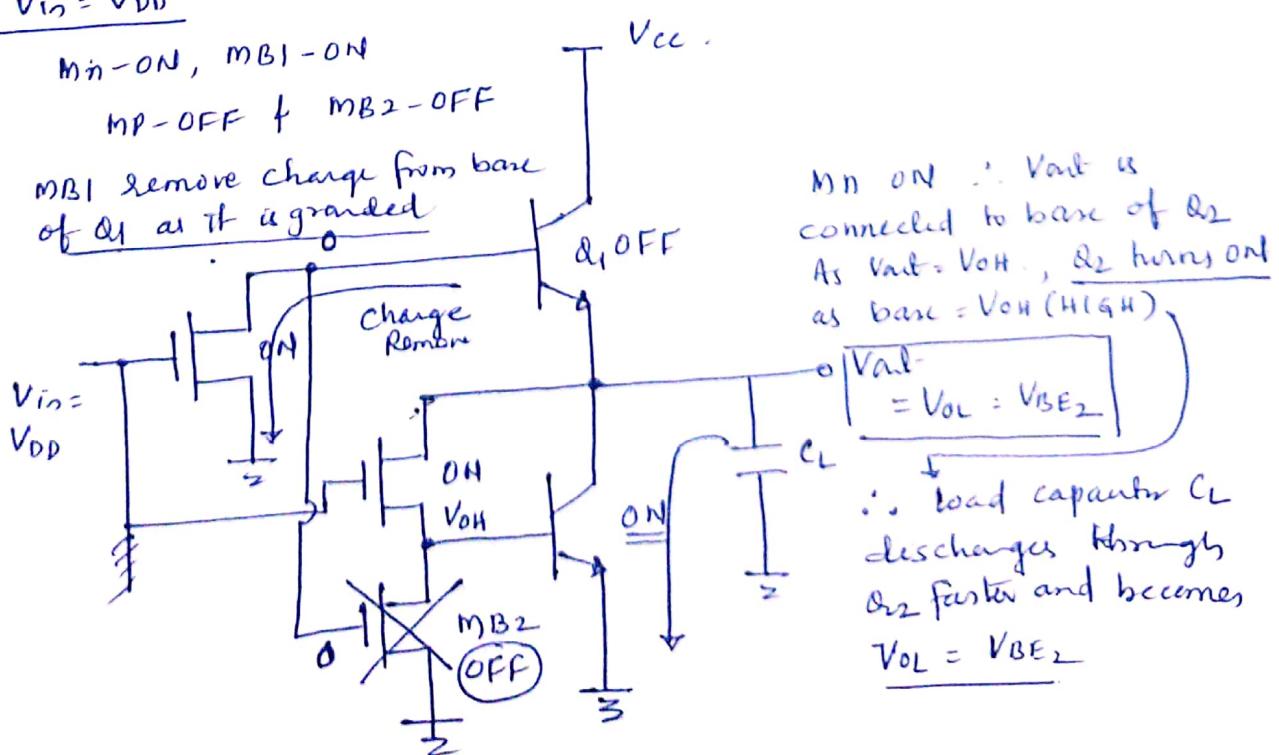


$$V_{in} = V_{DD}$$

in-ON, MB1-ON

MP-OFF + MB2-OFF

MB1 remove charge from base
of Q1 as it is grounded



in ON ∵ Vout is
connected to base of Q2
As Vout = Voh, Q2 turns ON
as base = Voh (HIGH)

$$V_{out} = V_{oh} = V_{BE2}$$

∴ load capacitor CL
discharges through
Q2 faster and becomes
 $V_{OL} = V_{BE2}$