PROJECT 1
VLSI

Name: Jacob V Sanoj
SRN: PES1UG20EC083

QUESTION 3

Aim : Solve the following Boolean expression using CMOS realization
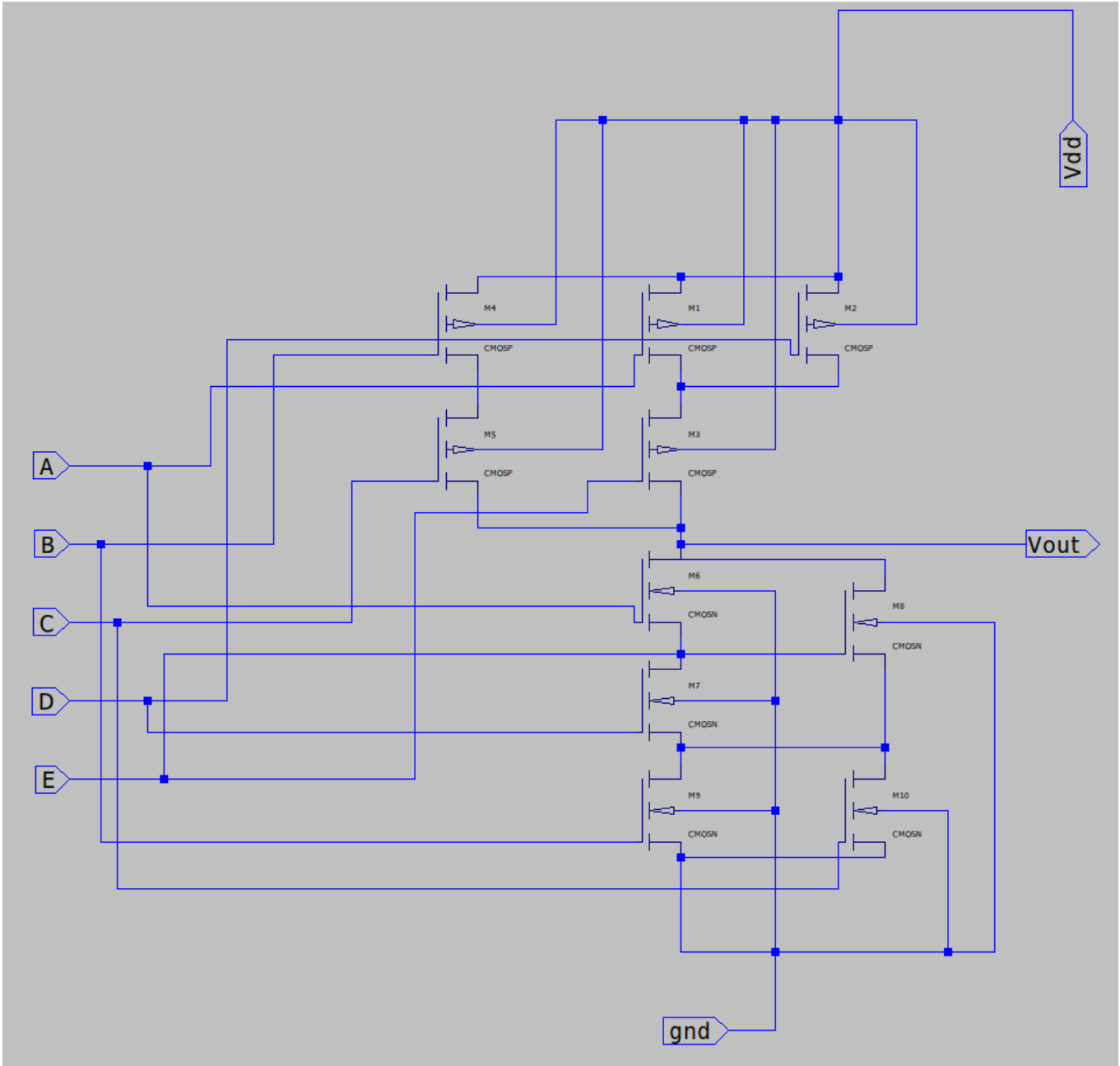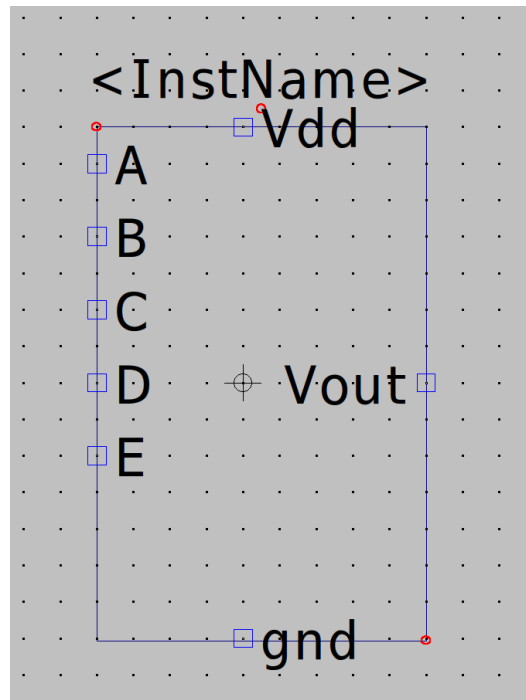
Expression :

$$Z = \overline{(AD + E).\ (B + C)}\ .$$

Truth Table:

A	B	C	D	E	Z
0	0	0	0	0	1
0	0	0	0	1	1
0	0	0	1	0	1
0	0	0	1	1	1
0	0	1	0	0	1
0	0	1	0	1	1
0	0	1	1	0	1
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	0	1	1
0	1	0	1	0	1
0	1	0	1	1	0
0	1	1	0	0	1
0	1	1	0	1	0
0	1	1	1	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	0	0	1	1
1	0	0	1	0	1
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	0	1	0
1	0	1	1	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	1
1	1	0	1	0	0
1	1	0	1	1	0
1	1	1	0	0	0
1	1	1	0	1	0

1	1	1	1	0	0
1	1	1	1	1	0

Schematic :

Symbol :

Test Bench :
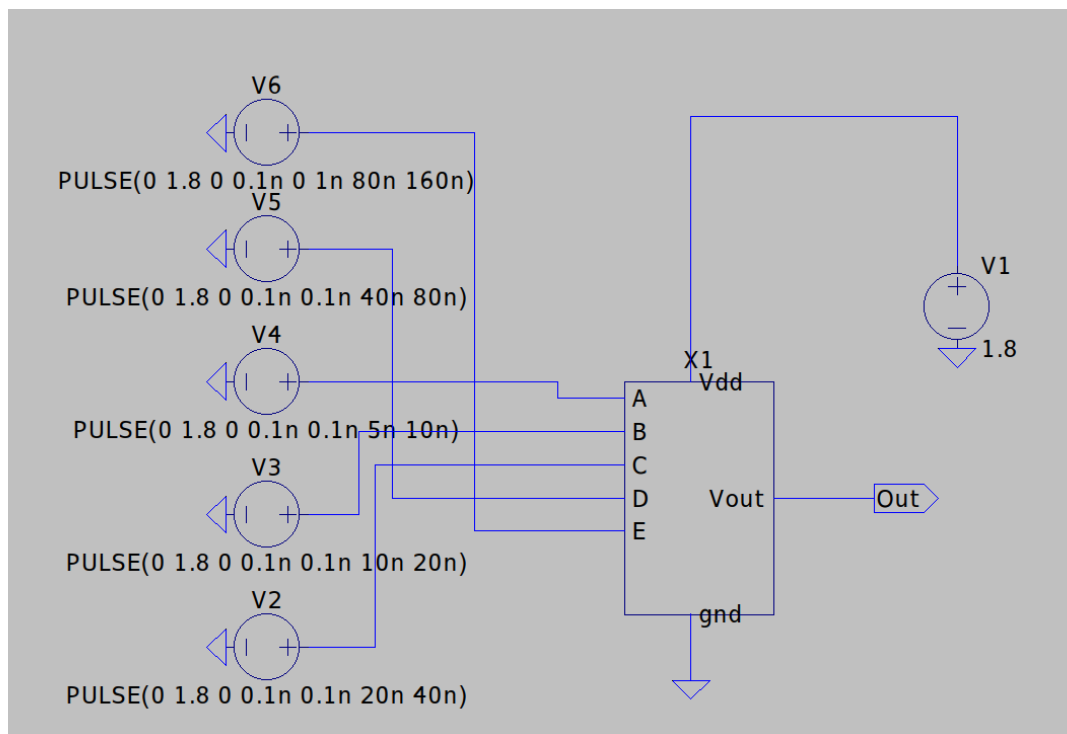
ANY INPUT	Z	DELAY
RISING	FALLING	62.75 ps

INPUT	EDGE	Z	DELAY (in ns)
A	FALLING	RISING	4.996
B	FALLING	RISING	9.929
C	FALLING	RISING	10.058
D	FALLING	RISING	20.077
E	FALLING	RISING	25.069

Waveform :
BLUE : A, PINK : B, CYAN : C, RED : D, GOLD : E, GREEN : Vout
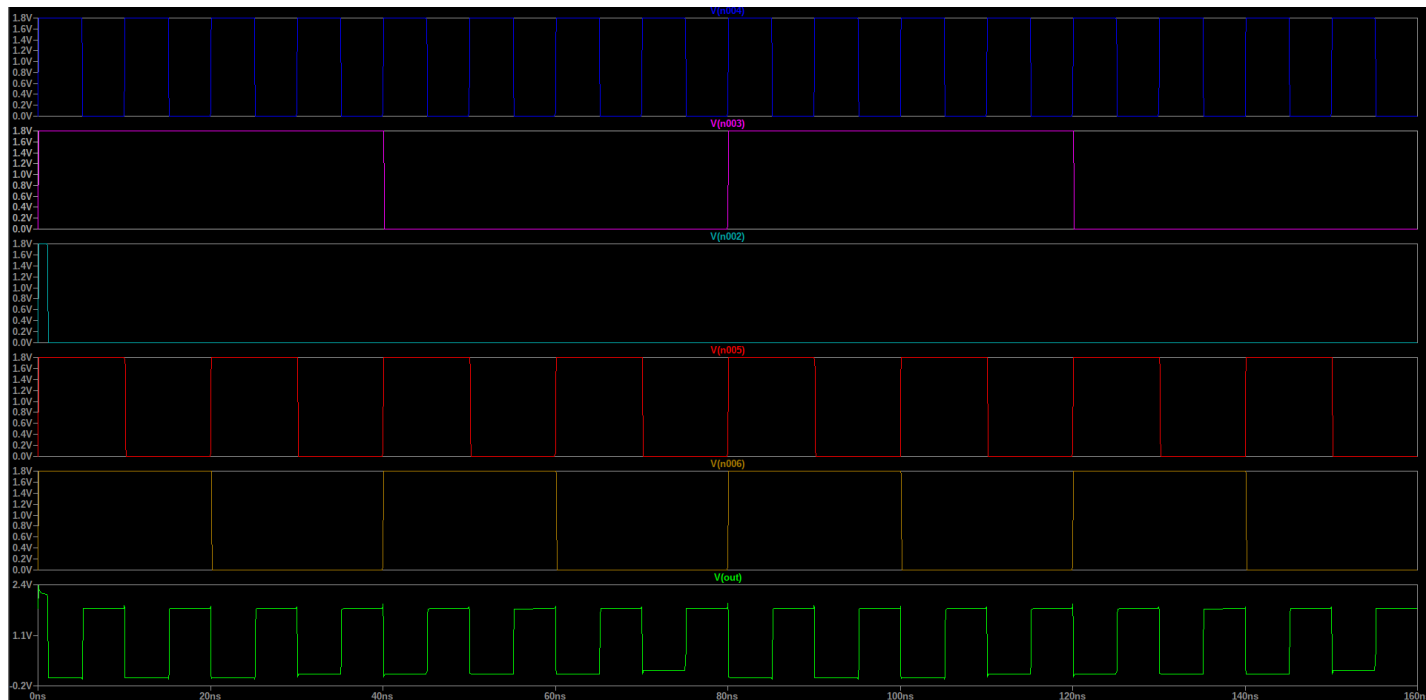
RESULT:

THE EXPRESSION IS SOLVED USING CMOS REALIZATION WHICH CAN BE VERIFIED BY ANALYZING THE WAVEFORM AND COMPARING WITH THE TRUTH TABLE.