RISC V Architecture

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RISC V ARCHITECTURE

UNIT 4: Arithmetic for Computers

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Signed Division:

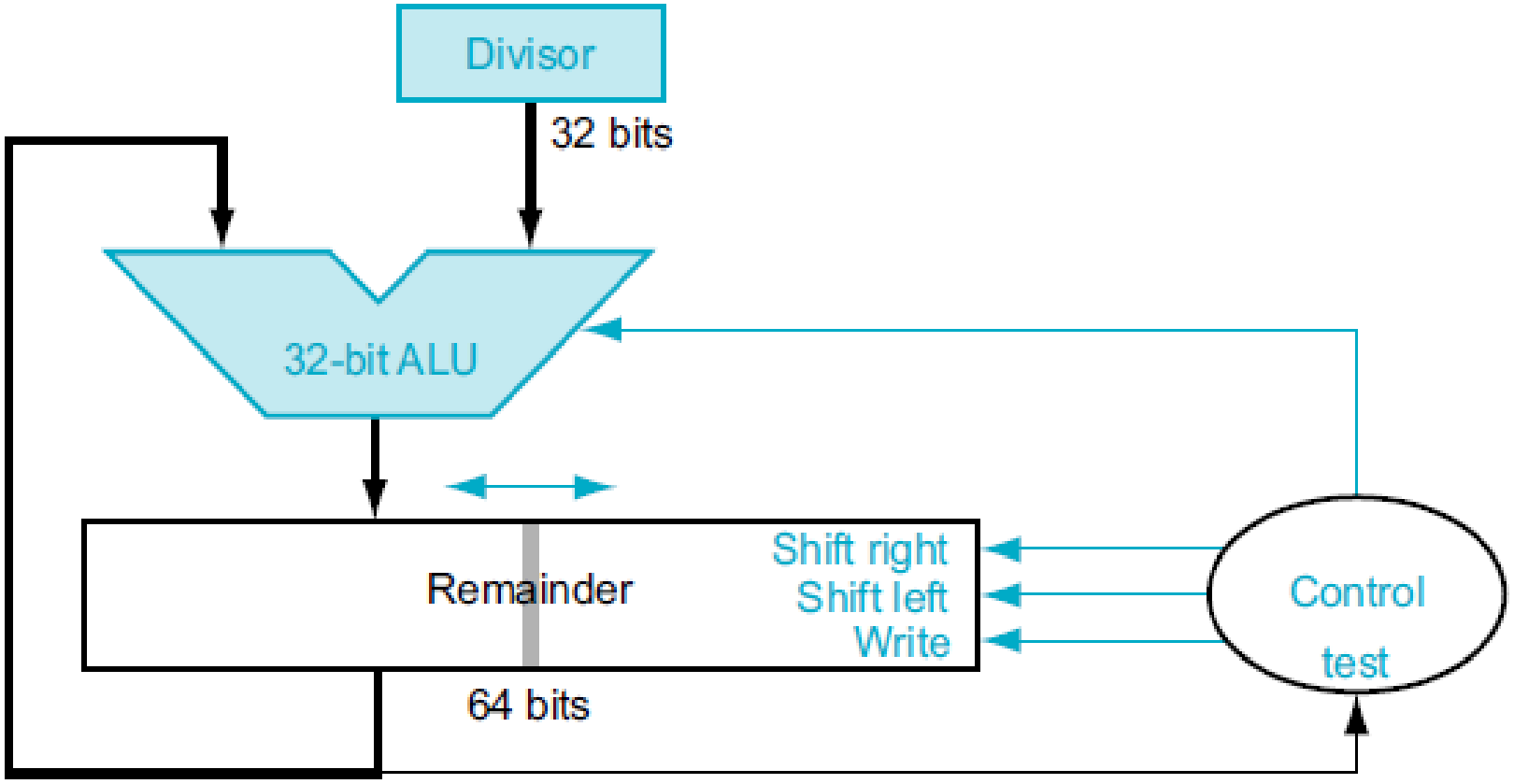
Remember the signs of the divisor and dividend and then negate the quotient if the signs disagree.
complication of signed division is that we must also set the sign of the remainder.
The following equation must always hold:
Dividend = Quotient x Divisor + Remainder

Example: ±7ten by ±2ten:
Case 1: +7 /+2: Quotient =+ 3, Remainder = + 1: check - + 7 3 x 2+ (+1)= 6 + 1
Case 2: -7 / +2: Quotient = - 3, Remainder = -1
Case 3: +7 /-2 : Quotient =- 3, Remainder= + 1
Case 4: -7 /- 2 : Quotient =+3, Remainder= -1

Signed Division:

Dividend	Divisor	Sign of Quotient	Sign of Remainder
+ve	+ve	+ve	+ve
+ve	-ve	-ve	+ve
-ve	+ve	-ve	-ve
-ve	-ve	+ve	-ve

Improved Hardware



An improved version of the division hardware:

- The Divisor register, ALU, and Quotient register are all 32 bits wide.
- Compared to previous design, the ALU and Divisor registers are halved and the remainder is shifted left.
- This version also combines the Quotient register with the right half of the Remainder register.
- The remainder register has grown to 65 bits to make sure the carry out of the adder is not lost.

Faster Division:

Restoring division:

we need to know the sign of the difference before we can perform the next step of the algorithm, whereas with multiply we could calculate the 32 partial products immediately.

To produce more than one bit of the quotient per step.

The (SRT) Sweeney–Robertson–Tocher division technique tries to predict several quotient bits per step, using a table lookup based on the upper bits of the dividend and remainder. It relies on subsequent steps to correct wrong predictions.

Non restoring division -*adds the dividend to the* shifted remainder, takes one clk cycle per step

$$(r + d) \times 2 - d = r - 2 + d \times 2 - d = r \times 2 + d.$$

Nonperforming division algorithm -doesn't save the result of the subtract if it's negative -averages one-third fewer arithmetic operations

Divide in RISC-V:

Same sequential hardware can be used for both multiply and divide
The only requirement is a 64-bit register that can shift left or right and a 32-bit ALU that adds or subtracts.

To handle both signed integers and unsigned integers, RISC-V has two instructions for division and two instructions for remainder:
divide (div), divide
unsigned (divu),
remainder (rem),
remainder unsigned (remu).

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RISC-V assembly language

Category	Instruction	Example	Meaning	Comments
Arithmetic	Add	add x5, x6, x7	x5 = x6 + x7	Three register operands
	Subtract	sub x5, x6, x7	x5 = x6 - x7	Three register operands
	Add immediate	addi x5, x6, 20	x5 = x6 + 20	Used to add constants
	Set if less than	slt x5, x6, x7	x5 = 1 if x5 < x6, else 0	Compare two registers
	Set if less than, unsigned	sltu x5, x6, x7	x5 = 1 if x5 < x6, else 0	Compare two registers
	Set if less than, immediate	slti x5, x6, x7	x5 = 1 if x5 < x6, else 0	Comparison with immediate
	Set if less than immediate, unsigned	sltiu x5, x6, x7	x5 = 1 if x5 < x6, else 0	Comparison with immediate
	Multiply	mul x5, x6, x7	x5 = x6 × x7	Lower 32 bits of 64-bit product
	Multiply high	mulh x5, x6, x7	x5 = (x6 × x7) >> 32	Upper 32 bits of 64-bit signed product
	Multiply high, unsigned	mulhu x5, x6, x7	x5 = (x6 × x7) >> 32	Upper 32 bits of 64-bit unsigned product
	Multiply high, signed-unsigned	mulhsu x5, x6, x7	x5 = (x6 × x7) >> 32	Upper 32 bits of 64-bit signed-unsigned product
	Divide	div x5, x6, x7	x5 = x6 / x7	Divide signed 32-bit numbers
	Divide unsigned	divu x5, x6, x7	x5 = x6 / x7	Divide unsigned 32-bit numbers
	Remainder	rem x5, x6, x7	x5 = x6 % x7	Remainder of signed 32-bit division
	Remainder unsigned	remu x5, x6, x7	x5 = x6 % x7	Remainder of unsigned 32-bit division

RISC-V software must check the divisor to discover division by 0 as well as overflow.

THANK YOU

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