DIGITAL VLSI DESIGN

Annapurna K Y
Electronics and Communication Engineering

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Unit 2: Fabrication of MOSFETs & Circuit Design Process

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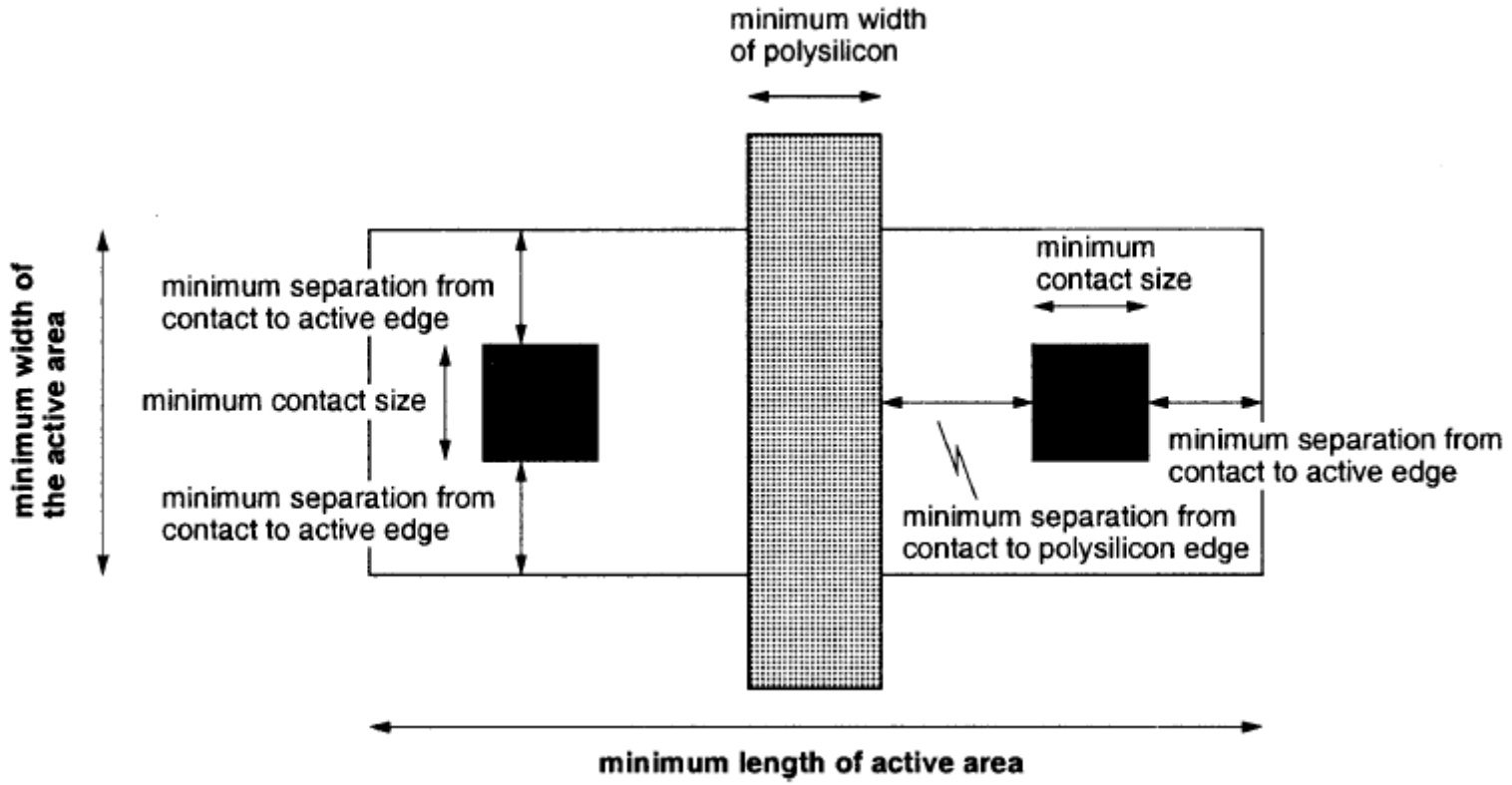
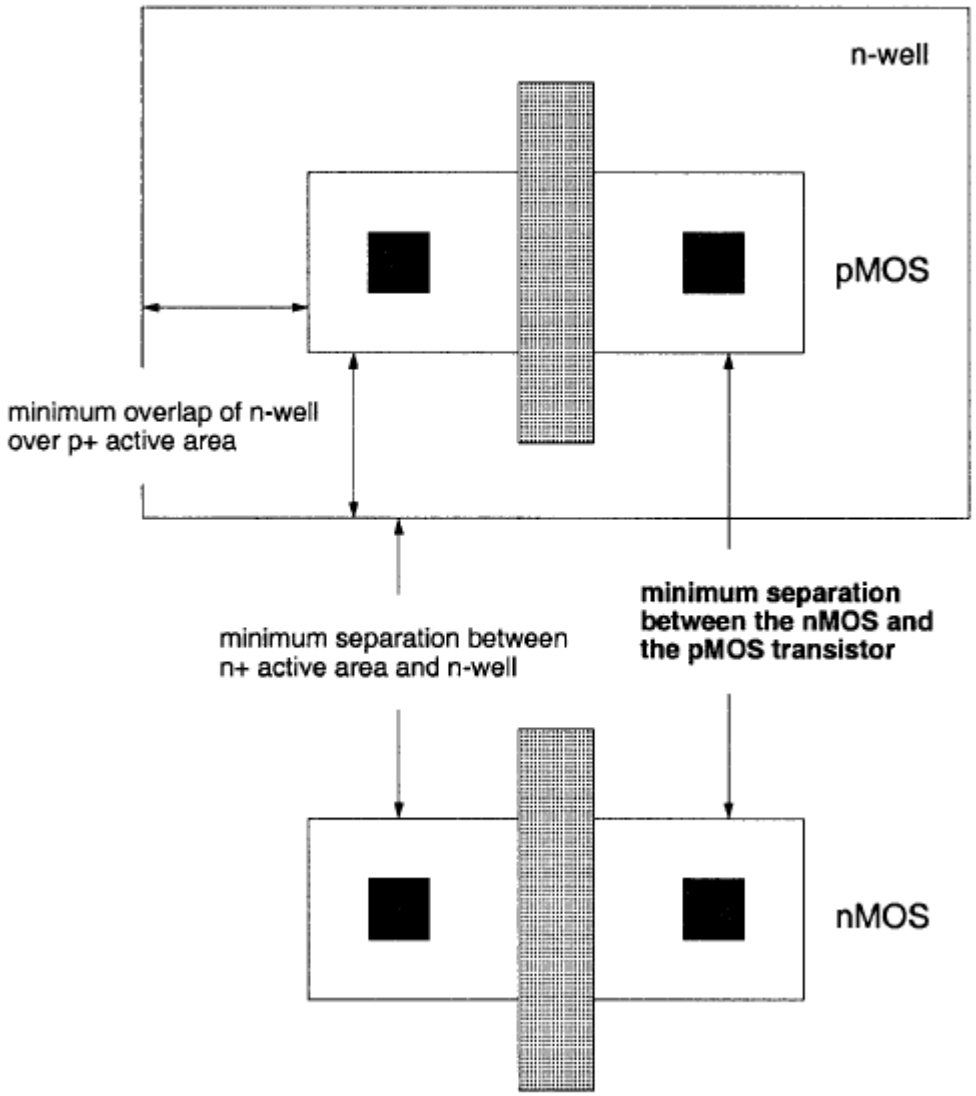
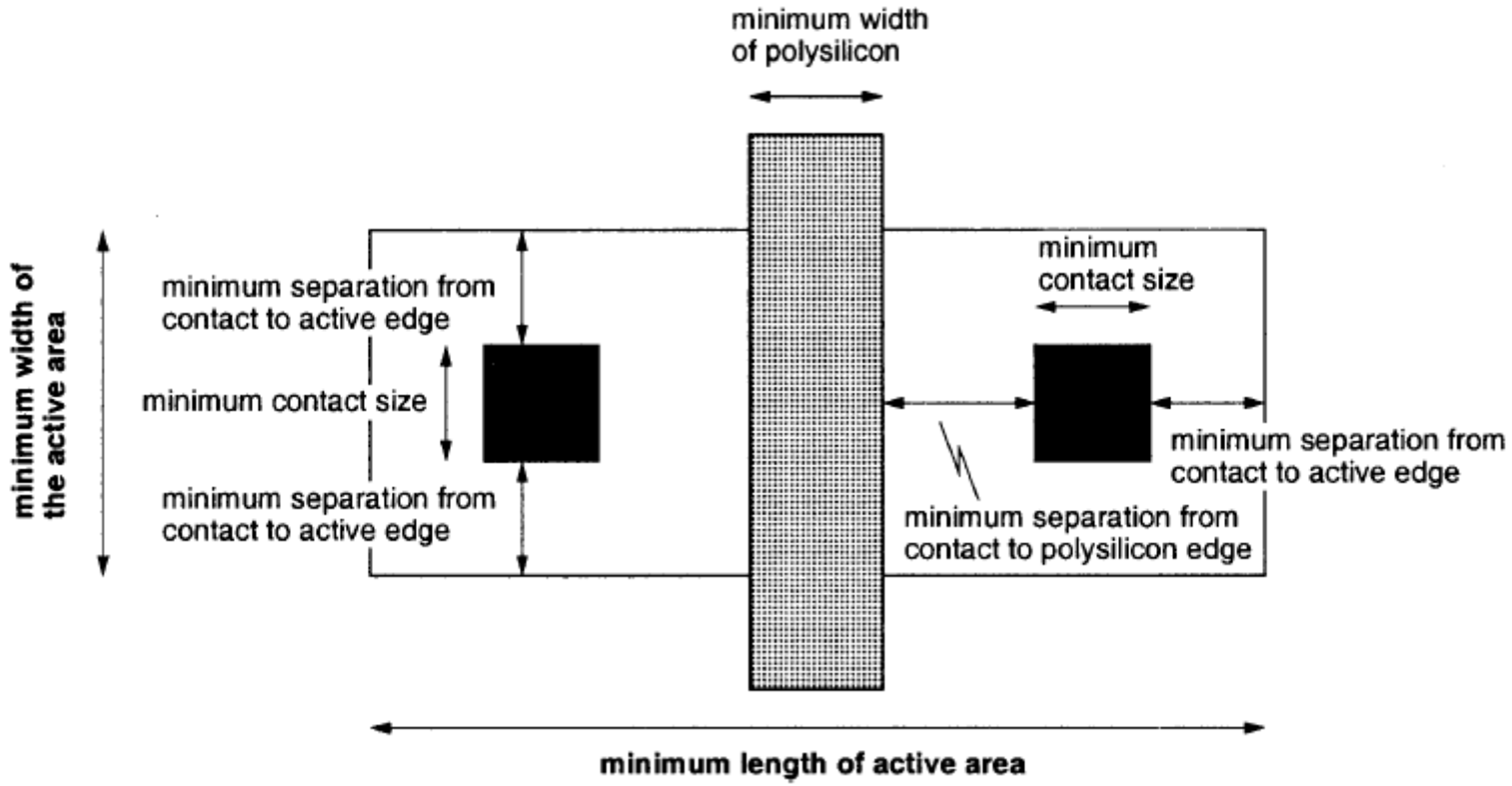
Layout Rules of a Minimum-Size MOSFET



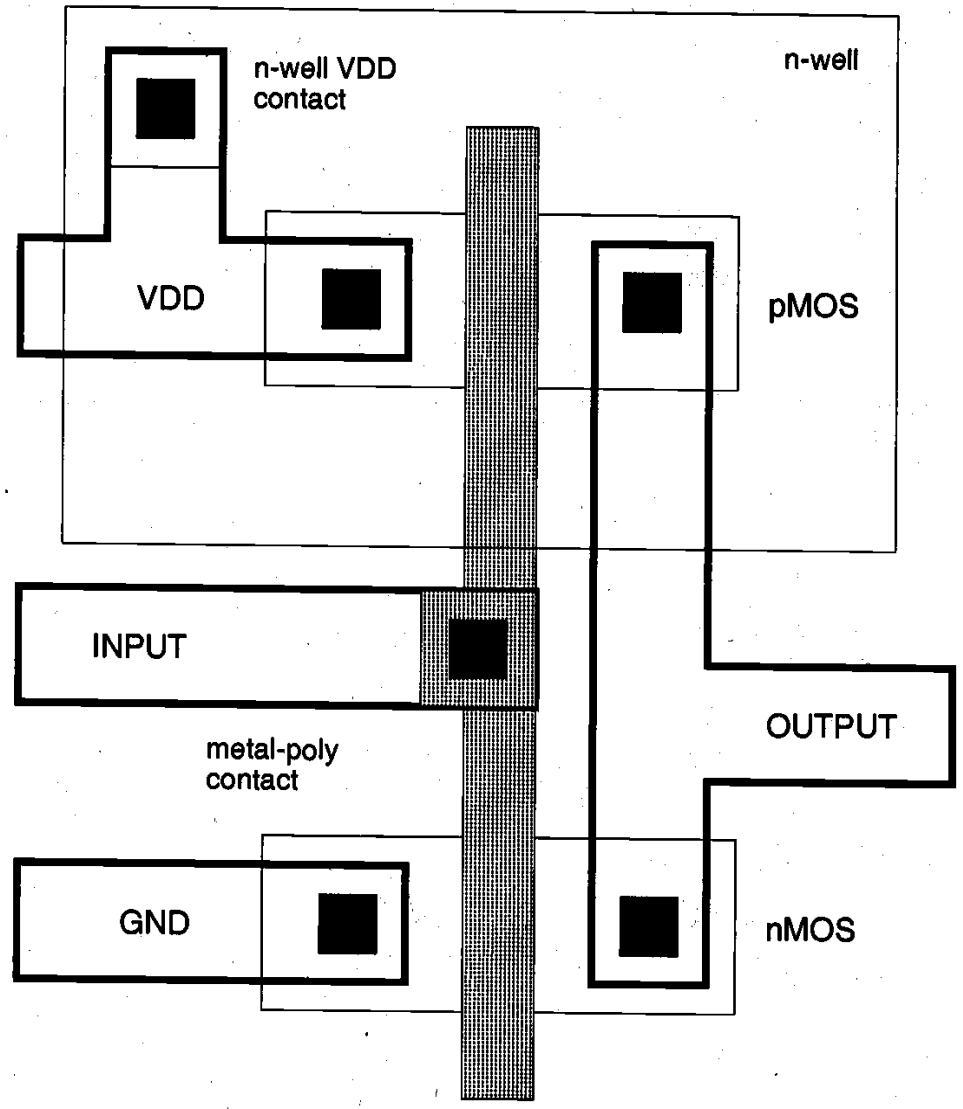
Layout Rules of a Minimum-Size MOSFET



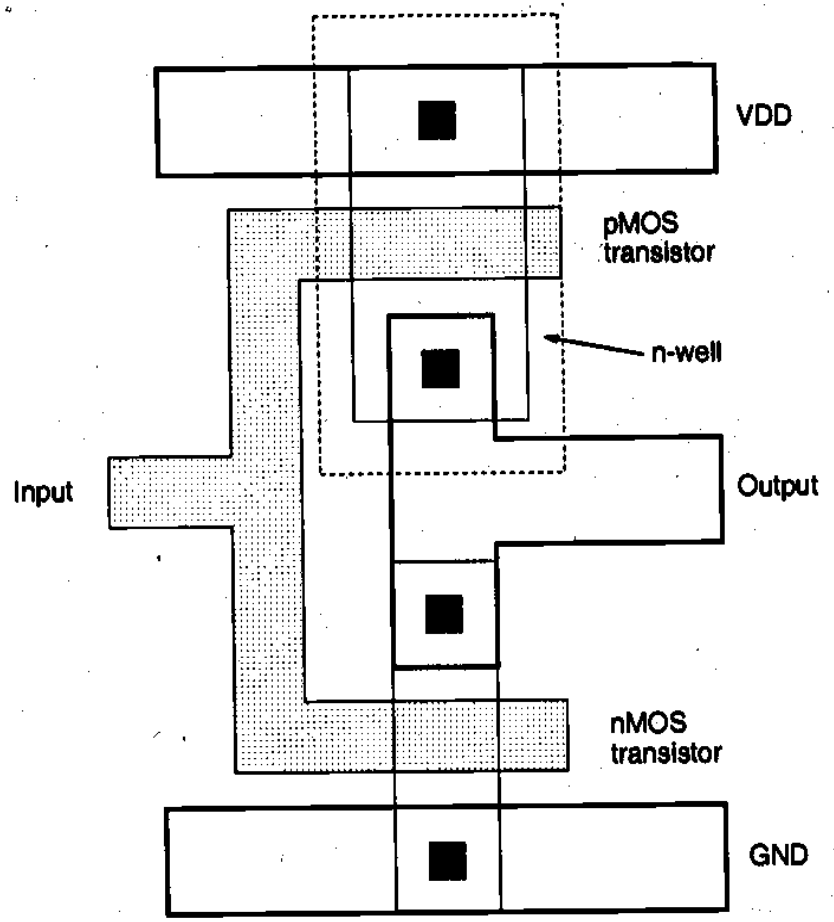
Layout Rules of a Minimum-Size MOSFET

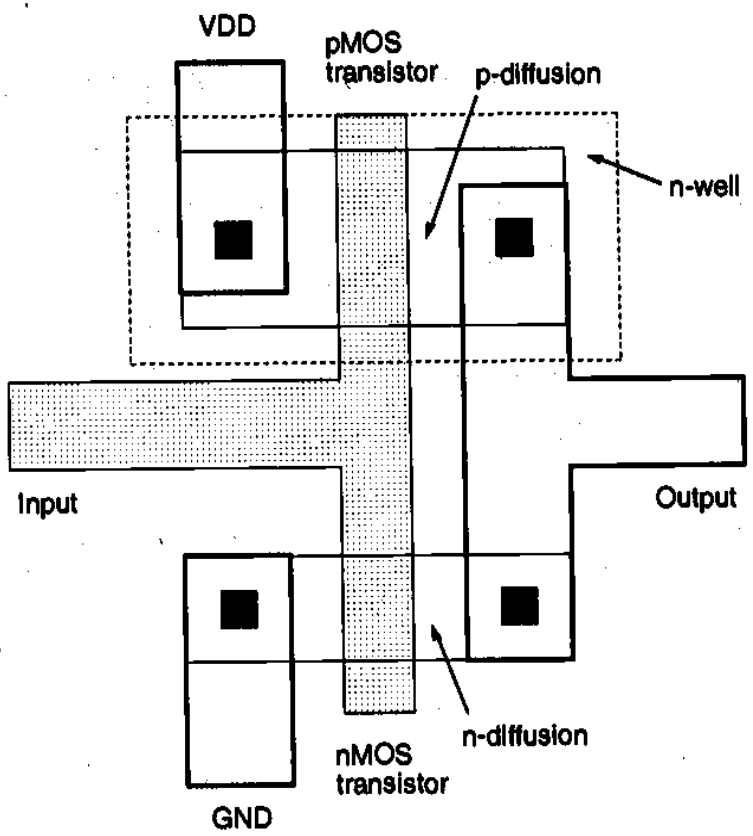


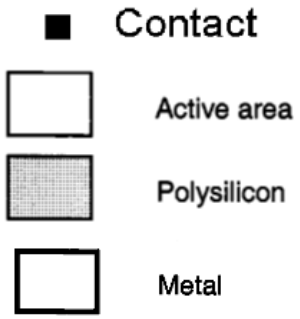
Complete mask layout of the CMOS inverter.



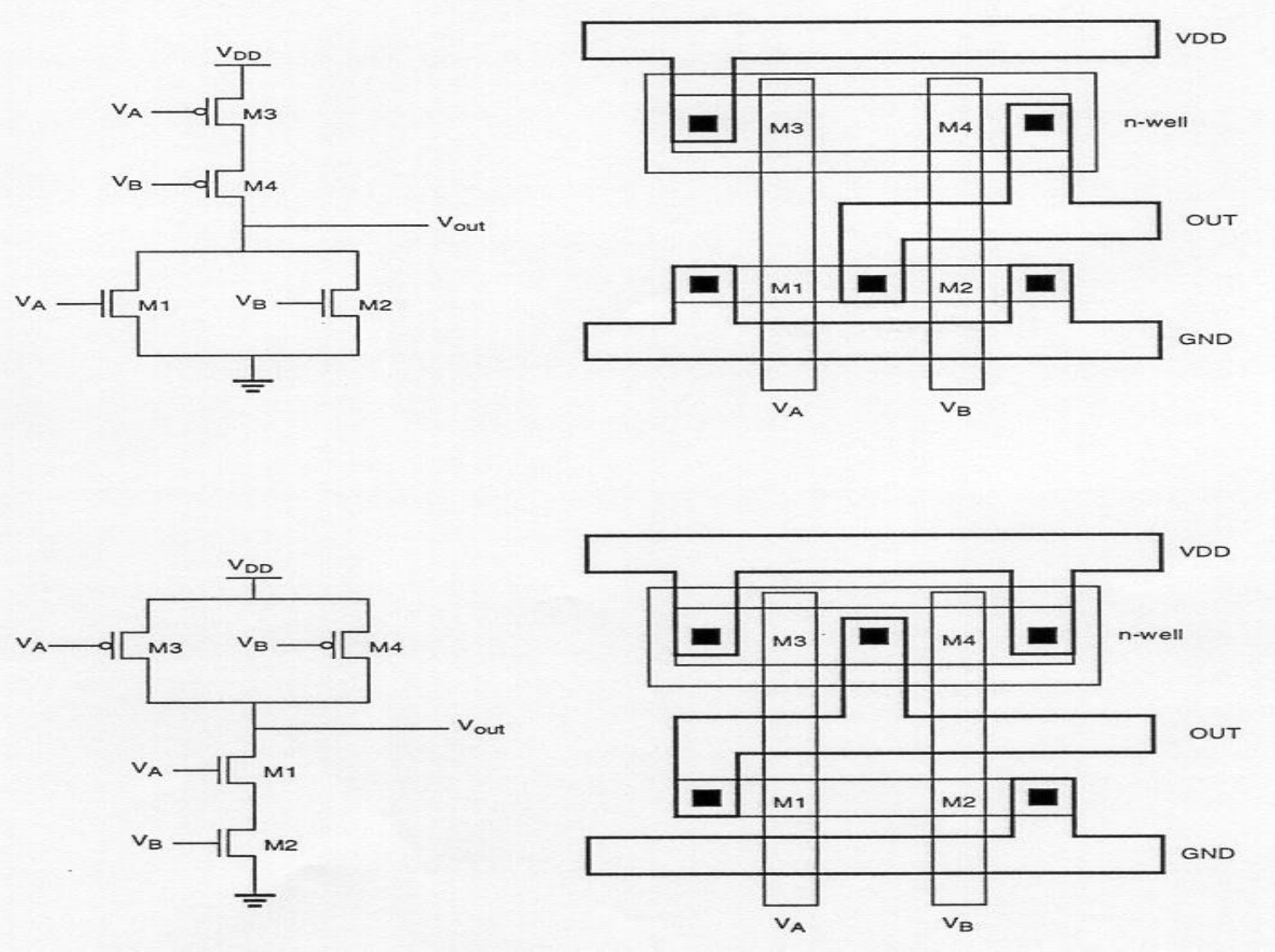
Two sample layouts of CMOS inverter circuits (for p-type substrate)

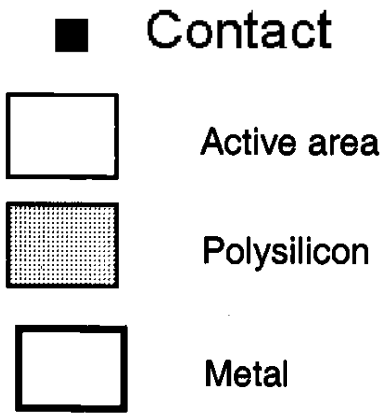






Layout of the CMOS 2 input NAND and NOR gate





THANK YOU

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