DIGITAL VLSI DESIGN

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Electronics and Communication Engineering

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Unit 2: Fabrication of MOSFETs & Circuit Design Process

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DIGITAL VLSI DESIGN - Course content

Unit 2: Fabrication of MOSFETs & Layout Design Concepts				
R1: Chap 2 (2.1 – 2.5) **R1: Chap 7 (7.4), Chap 3(3.5)**	NMOS fabrication, CMOS fabrication, p-well, n-well, twin-tub process (2.2 & 2.3)	20%	41%	
	MOS layers, Lambda based design rules, contact cuts (2.4)			
	Combinational Logic Circuits and Layout: NAND2 gate and NOR2 gate, Boolean functions of multiple input variables. (7.4)			
	MOSFET scaling and small geometry effects and scaling models (3.5)			

Reference Books:

R1: CMOS Digital Integrated Circuits Analysis And Design, Sung-Mo (Steve) Kang

Categories of Materials

Materials can be categorized into three main groups regarding their electrical conduction properties:

- **Insulators**
- **Conductors**
- **Semiconductors**

Semiconductors

While there are numerous semiconductor materials available, by far the most popular material is **Silicon**.

GaAs, InP and SiGe are compound semiconductors that are used in specialized devices.

The success of a semiconductor material depends on how easy it is to process and how well it allows reliable high-volume fabrication.

Introduction

- There are very strong links between the fabrication process, the circuit design process, and the performance of the resulting chip.

- Hence, circuit designers must have a working knowledge of chip fabrication to create effective designs and to optimize the circuits with respect to various manufacturing parameters.

- Also, the circuit designer must have a clear understanding of the roles of various masks used in the fabrication process, and how the masks are used to define various features of the devices on-chip.

Introduction

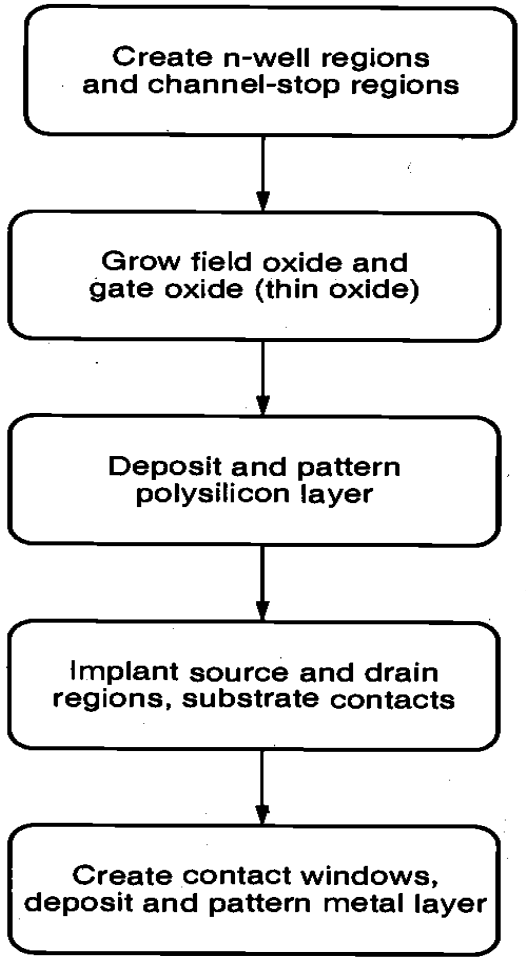


Figure 2.1. Simplified process sequence for the fabrication of the n-well CMOS integrated circuit with a single polysilicon layer, showing only major fabrication steps.

Fabrication Process Flow: Basic Steps

Note that each processing step requires that certain areas are *defined* on chip by appropriate *masks.* Consequently, the integrated circuit may be viewed as a set of patterned layers of doped silicon, polysilicon, metal, and insulating silicon dioxide.

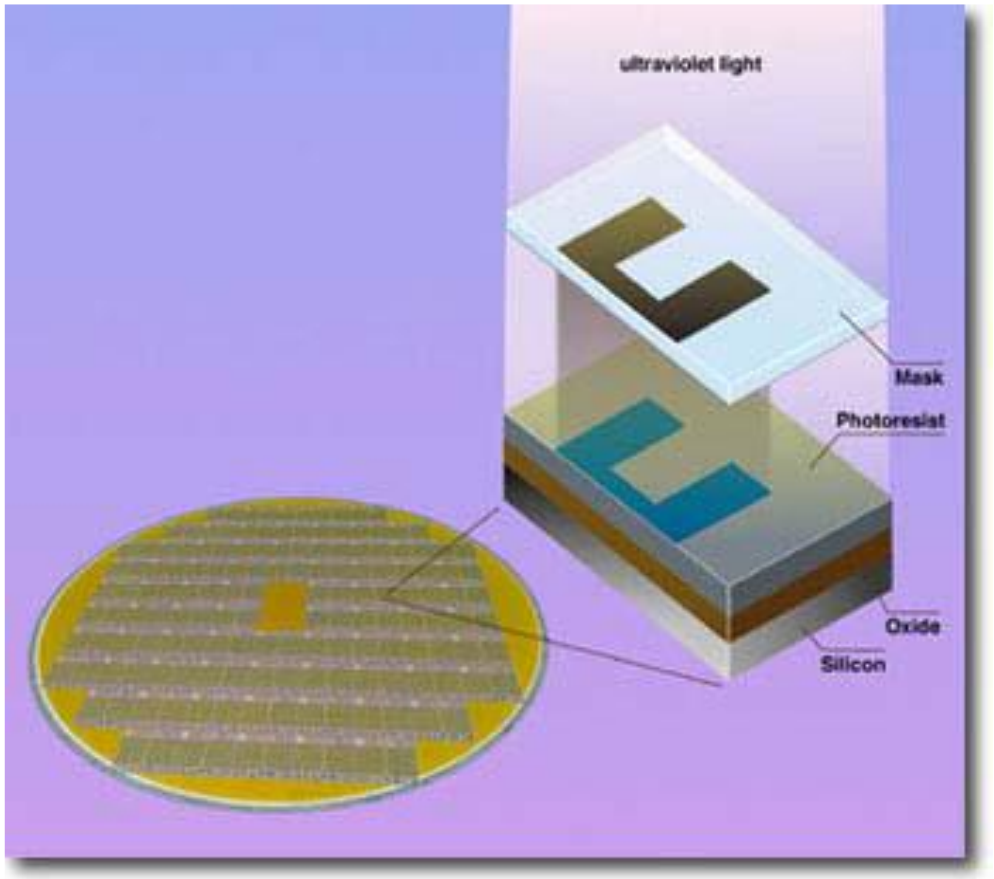
In general, a layer must be patterned before the next layer of material is applied on the chip.

The process used to transfer a pattern to a layer on the chip is called *lithography.* Since each layer has its own distinct patterning requirements, the lithographic sequence must be repeated for every layer, using a different mask.

Lithography

An IC consists of several layers of material that are manufactured in successive steps.

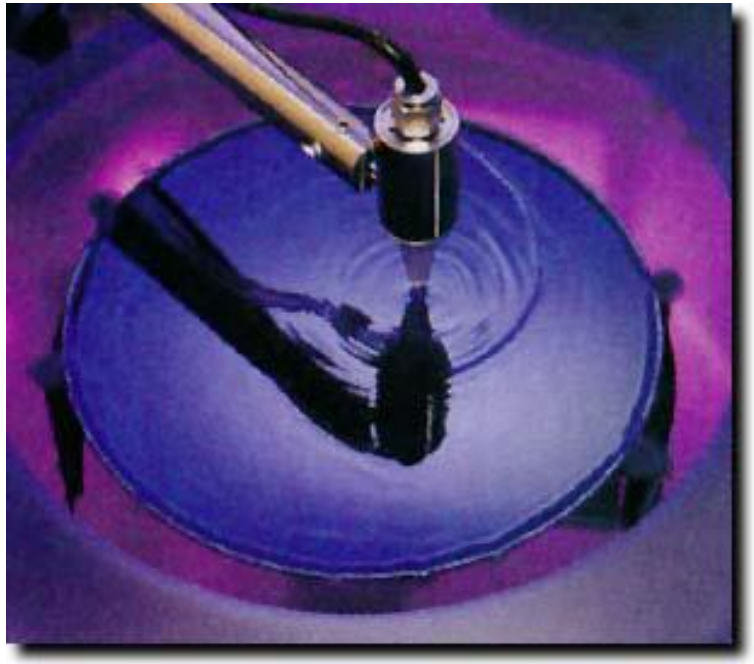
Lithography is used to selectively process the layers, where the 2-D mask geometry is copied on the surface.



Lithography

The surface of the wafer is coated with a photosensitive material, the **photoresist**. The mask pattern is developed on the photoresist, with UV light exposure.

Depending on the type of the photoresist (negative or positive), the exposed or unexposed parts of the photoresist change their property and become resistant to certain types of solvents.



Photoresist Application
(Ontrak)

Subsequent processing steps remove the undeveloped photoresist from the wafer. The developed pattern (usually) protects the underlying layer from an etching process. The photoresist is removed after patterning on the lower layer is completed.

Lithography

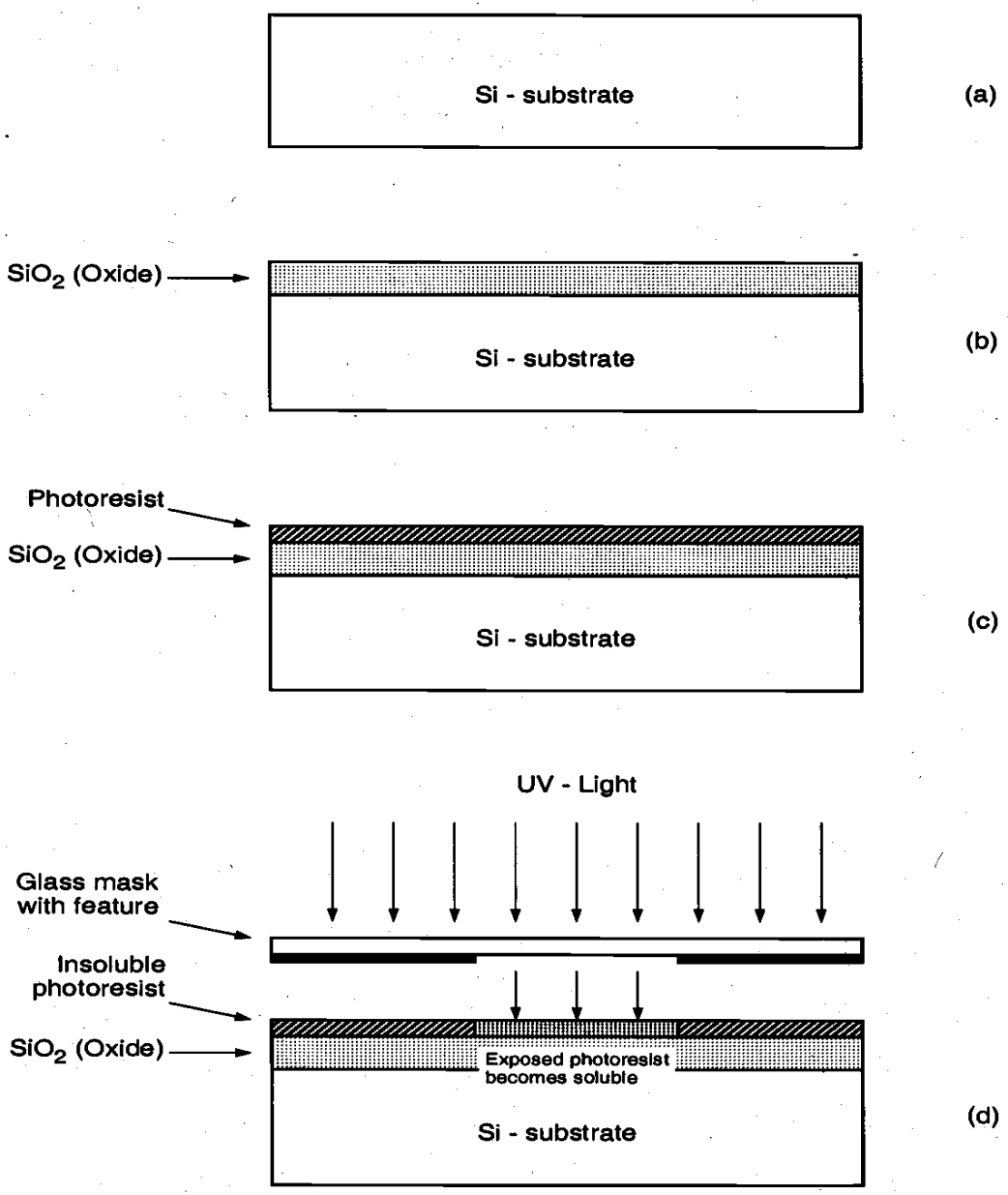
- The type of photoresist which is initially insoluble and becomes soluble after exposure to UV light is called *positive photoresist.* The process sequence shown in Fig. uses positive photoresist.

- There is another type of photoresist which is initially soluble and becomes insoluble (hardened) after exposure to UV light, called *negative photoresist.*

- If negative photoresist is used in the photolithography process, the areas which are not shielded from the UV light by the opaque mask features become insoluble, whereas the shielded areas can subsequently be etched away by a developing solution.

- Negative photoresists are more sensitive to light, but their photolithographic resolution is not as high as that of the positive photoresists. Therefore, negative photoresists are-used less commonly in the manufacturing of high-density integrated circuits.

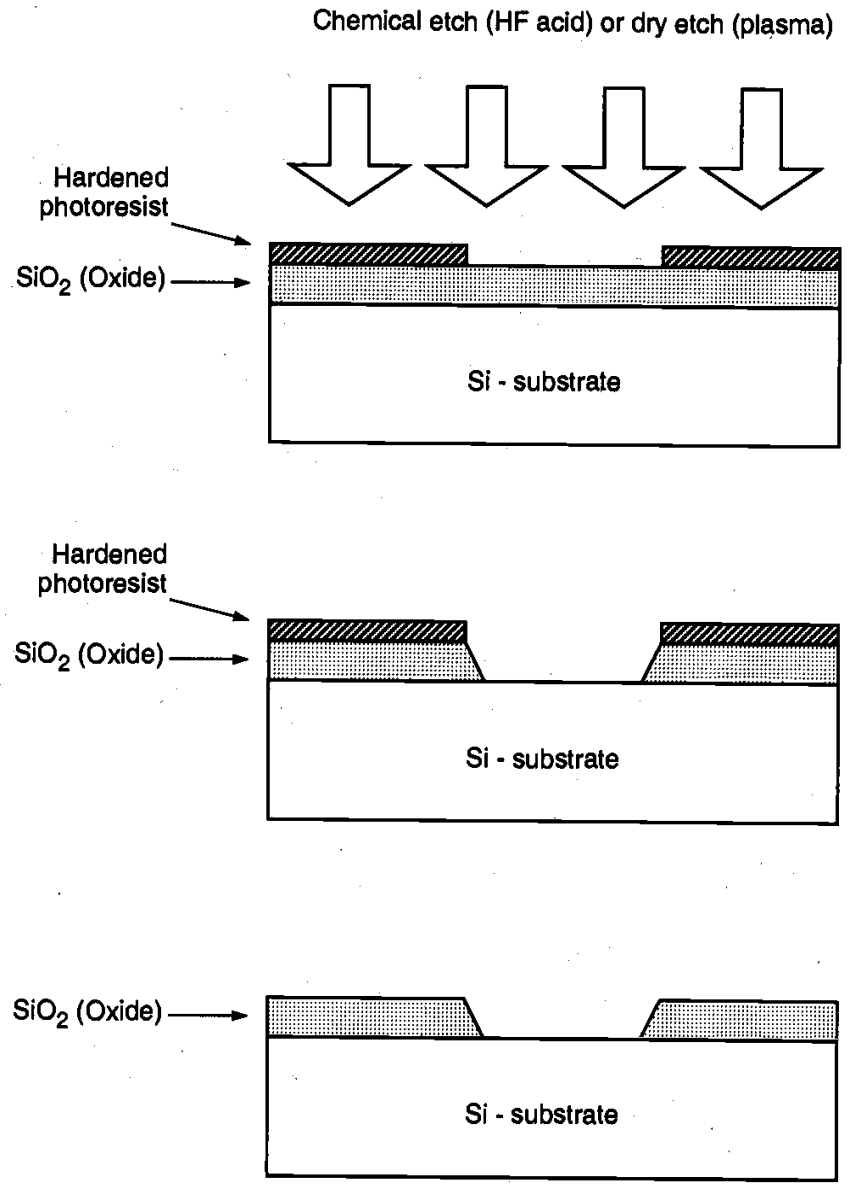
Patterning of Features on SiO2



Fabrication Process Flow: Basic Steps

- The sequence starts with the thermal oxidation of the silicon surface, by which an oxide layer of about 1 m thickness, is created on the substrate.
- The entire oxide surface is then covered with a layer of *photoresist,* which is essentially a light-sensitive, acid - resistant organic polymer, initially insoluble in the developing solution (Fig.(c)).
- If the photoresist material is exposed to ultraviolet (UV) light, the exposed areas become soluble so that they are no longer resistant to etching solvents. To selectively expose the photoresist, we have to cover some of the areas on the surface with a *mask* during exposure.
- Thus, when the structure with the mask on top is exposed to UV light, areas which are covered by the opaque features on the mask are shielded.
- In the areas where the UV light can pass through, on the other hand, the photoresist is exposed and becomes soluble.

Patterning of Features on SiO2



- Following the UV exposure step, the unexposed portions of the photoresist can be removed by a solvent.
- Now, the silicon dioxide regions which are not covered by hardened photoresist can be etched away either by using a chemical solvent (HF acid) or by using a dry etch (plasma etch) process (Fig. (e)).
- Note that at the end of this step, we obtain an oxide window that reaches down to the silicon surface (Fig. (f)).
- The remaining photoresist can now be stripped from the silicon dioxide surface by using another solvent, leaving the patterned silicon dioxide feature on the surface as shown in Fig. (g).

Patterning of Features on SiO2

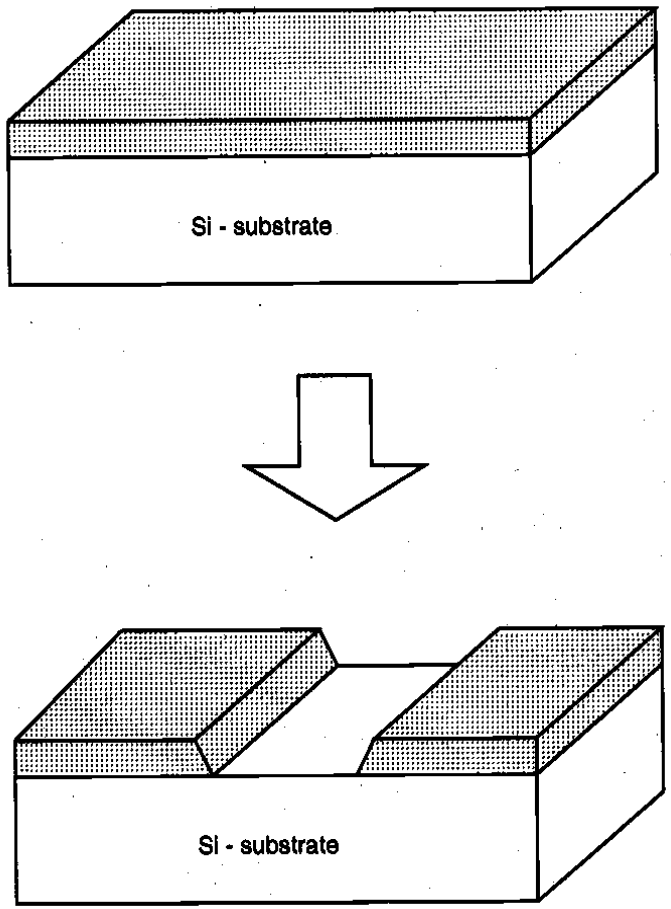


Figure 2.3. **The result of a single lithographic patterning sequence on silicon dioxide, without showing the intermediate steps.**

THANK YOU

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