RISC V Architecture

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RISC V ARCHITECTURE

UNIT 4: Arithmetic for Computers

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Graphics and audio applications can take advantage of performing simultaneo operations on short vectors

Example: 128-bit adder:

Sixteen 8-bit adds

Eight 16-bit adds

Four 32-bit adds

----By partitioning the carry chains within a 128-bit adder, a processor could use **parallelism to perform simultaneous operations on short vectors of sixteen 8-bit** operands, eight 16-bit operands, four 32-bit operands, or two 64-bit operands

Also called data-level parallelism, vector parallelism, or Single Instruction, Multiple Data (SIMD)

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Real Stuff: Streaming SIMD Extensions and Advanced Vector Extensions in x86

** Instructions to use subword parallelism are still under development by RISC-V International

X86: Extended Instruction with 64 bit registers -The SSE/SSE2 floating-point instructions

Data transfer	Arithmetic	Compare
MOV[AU]{SS|PS|SD|PD} xmm, {mem|xmm}	ADD{SS|PS|SD|PD} xmm,{mem|xmm}	CMP{SS|PS|SD|PD}
	SUB{SS|PS|SD|PD} xmm,{mem|xmm}	
MOV[HL]{PS|PD} xmm, {mem|xmm}	MUL{SS|PS|SD|PD} xmm,{mem|xmm}	
	DIV{SS|PS|SD|PD} xmm,{mem|xmm}	
	SQRT{SS|PS|SD|PD} {mem|xmm}	
	MAX{SS|PS|SD|PD} {mem|xmm}	
	MIN{SS|PS|SD|PD} {mem|xmm}	

xmm means one operand is a 128-bit SSE2 register
{mem|xmm} means the other operand is either in memory or it is an SSE2 register.
Regular expressions to show the variations of instructions:
MOV[AU]{SS|PS|SD|PD} represents the eight instructions MOVASS,MOVAPS,MOVASD,MOVAPD,MOVUSS,MOVUPS,MOVUSD and MOVUPD.

Square brackets [] to show single-letter alternatives:
A means the 128-bit operand is aligned in memory;
U means the 128-bit operand is unaligned in memory;
H means move the high half of the 128-bit operand;
L means move the low half of the 128-bit operand.

Curly brackets {} with a vertical bar | to show multiple letter variations of the basic operations:
SS stands for Scalar Single precision floating point, or one 32-bit operand in a 128-bit register;

PS stands for Packed Single precision floating point, or four 32-bit operands in a 128-bit register;

SD stands for Scalar Double precision floating point, or one 64-bit operand in a 128-bit register;

PD stands for Packed Double precision floating point, or two 64-bit operands in a 128-bit register.

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16 Registers of 128-bit - data transfers can load and store multiple operands per instruction.

packed floating-point format supports Four -- singles (PS) or two doubles (PD).

2011, Intel doubled the width of the registers again, now called YMM, with ’Advanced Vector Extensions (AVX).---a single operation can now specify eight 32-bit floating-point operations or four 64-bit floating-point operations.

The legacy SSE and SSE2 instructions now operate on the lower 128 bits of the YMM registers-from 128- and 256-bit operations

Example: the SSE2 instruction to perform two 64-bit floating-point additions

```
addpd %xmm0, %xmm4
```

Becomes

```
vaddpd %ymm0, %ymm4
```

Unit 4: Arithmetic for Computers -Streaming SIMD Extension 2 (SSE2)

AVX512/AVX1024 ---Intel extns
AVX also added three address instructions to x86
,Ex: vaddpd can now specify 3 operands
vaddpd %ymm0, %ymm1, %ymm4 // %ymm4 = %ymm0 + %ymm1

instead of the standard, two address version
addpd %xmm0, %xmm4 // %xmm4 = %xmm4 + %xmm0

(Unlike RISC-V, the destination is on the right in x86.) Three addresses can reduce the number of registers and instructions needed for a computation.

THANK YOU

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