DIGITAL VLSI DESIGN

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Unit 2: Fabrication of MOSFETs & Circuit Design Process

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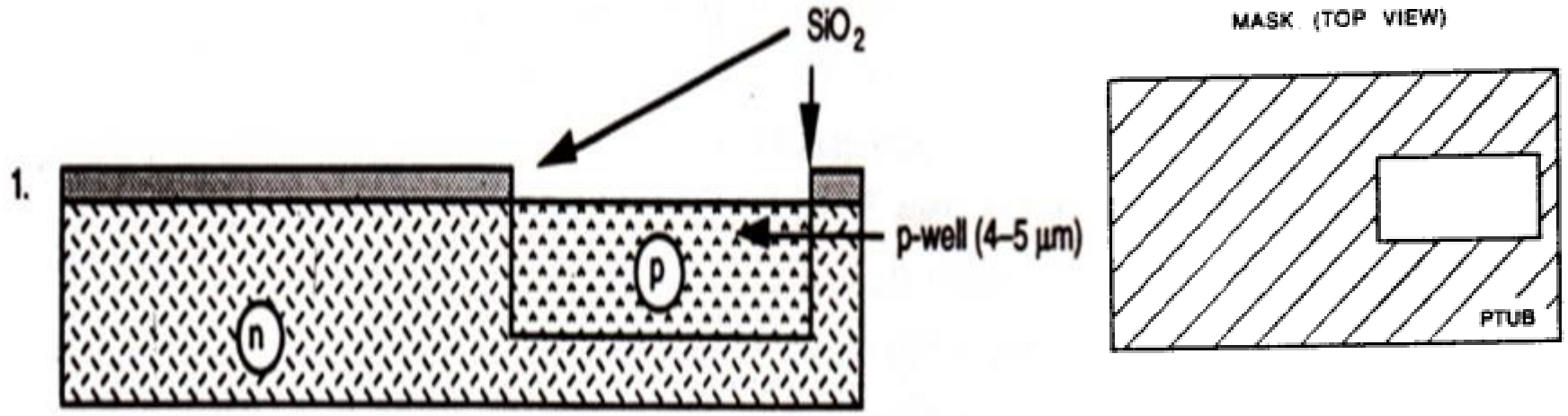
CMOS Fabrication

- Four dominant cmos technologies are:
  - p-well process
  - n-well process
  - Twin-tub process
  - Silicon-on-Insulator

- **P-Well Process**
  - Start with a moderately doped n-type substrate
    - In which p-devices may be formed by suitable masking and diffusion
  - Create the p-type well for n-channel devices
    - by means of diffusion
    - This diffusion must be carried out with special care since the p-well doping concentration and depth will affect the threshold voltages and breakdown voltages of the n-transistors.
    - To achieve low threshold voltages (0.6 to 1.0 V) we need either deep-well diffusion or high-well resistivity
  - Build the p-channel devices in the native n-substrate.

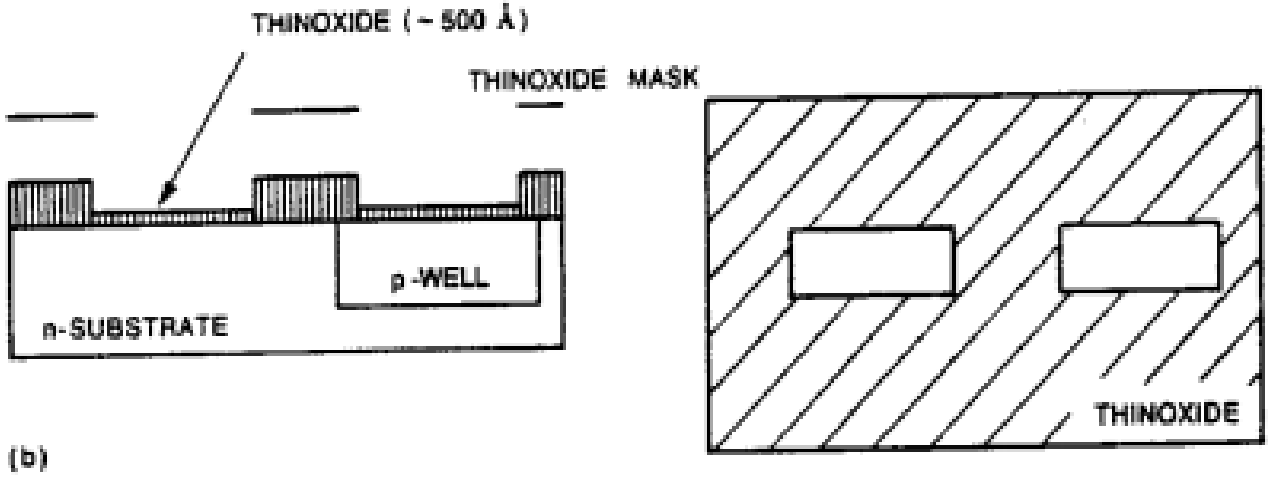
p-well process



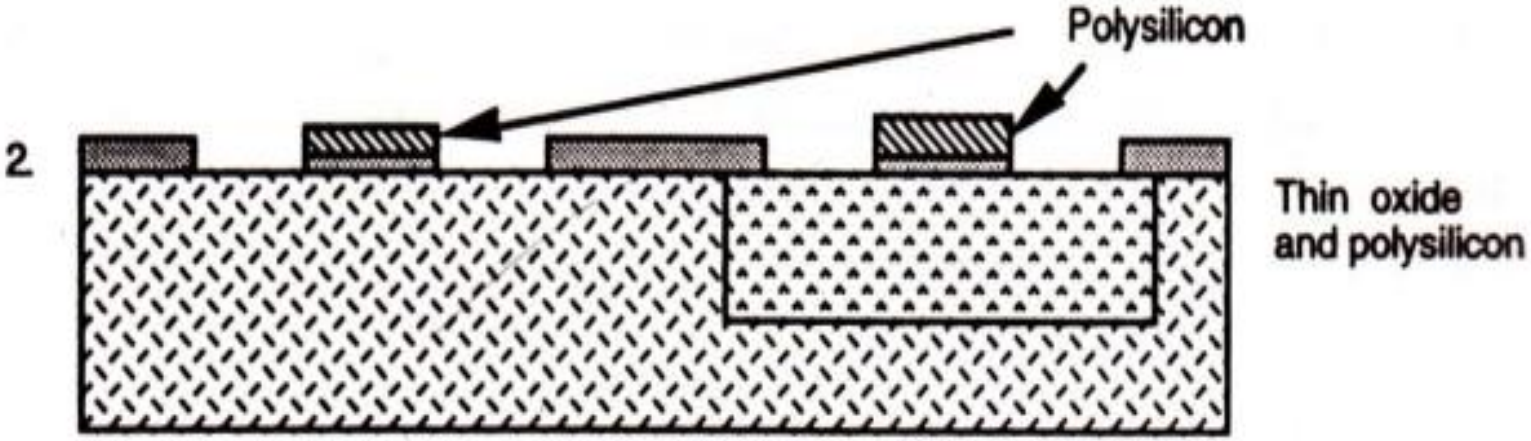
- The first mask defines the p-well. i.e., this mask defines the areas in which the deep p-well diffusions are to take place.

- The field oxide is etched away to allow deep diffusion.

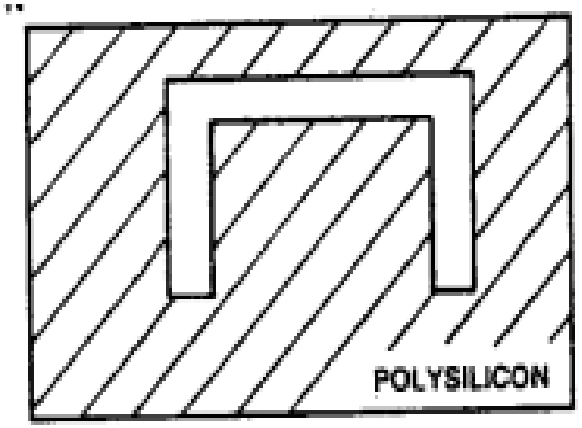
- Depth of this well is usually 4-5um.

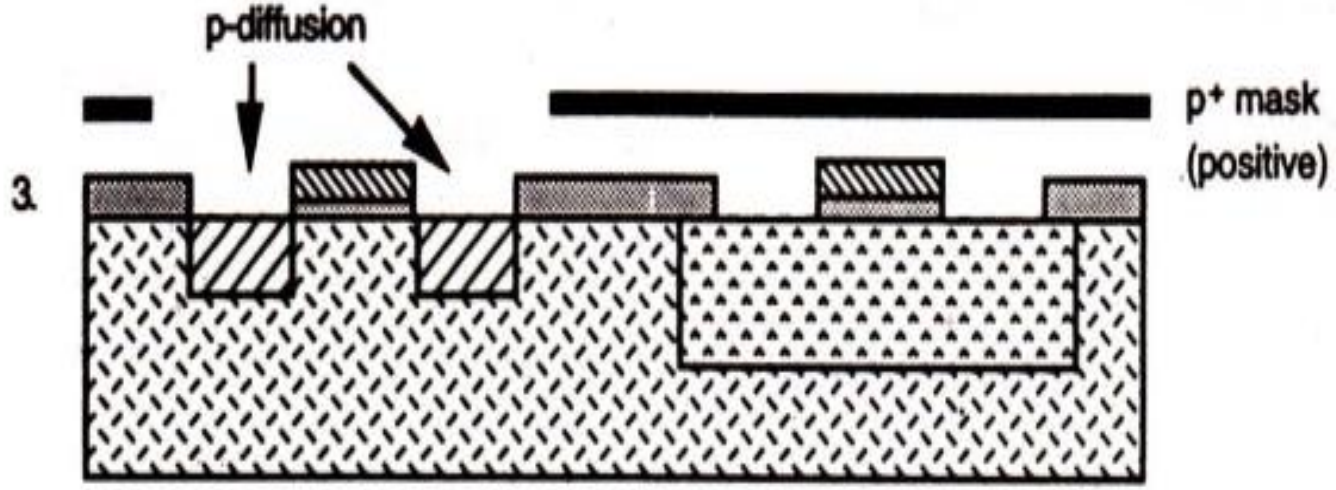


- The next mask is called ‘thinox ’ or ‘thin oxide’ mask.
- It defines the areas, where thin oxide are needed to implement transistor gates and allow implantation to form p- or n- type diffusions for drain/source regions.
- The field oxide areas are etched to the silicon surface and then the thin oxide is grown on these areas.
- *In nmos fabrication, this is called diffusion mask.*

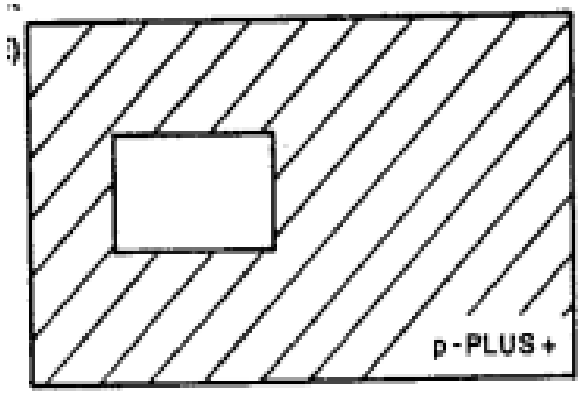


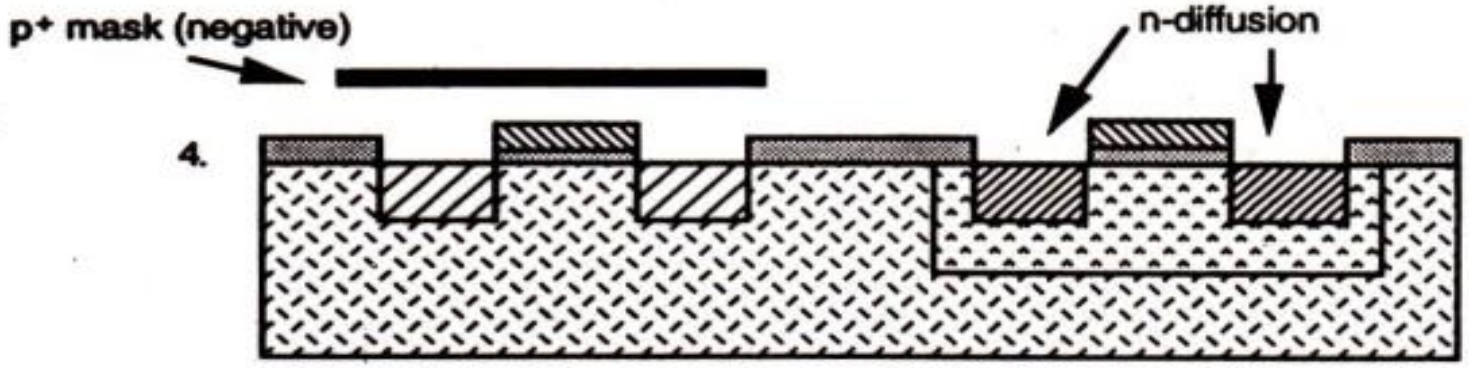
- Polysilicon gate definition is then completed.
- This involves covering the surface with polysilicon and then etching the required pattern.
- The poly gate regions lead to “self-aligned” source and drain regions



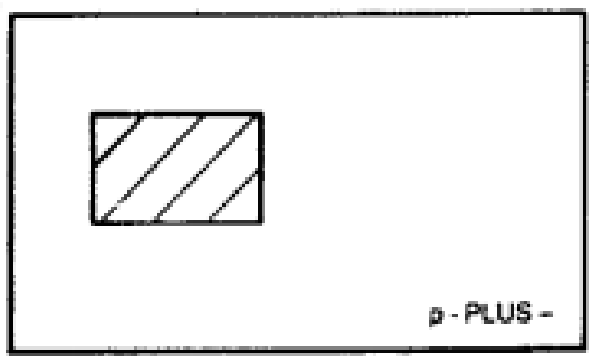


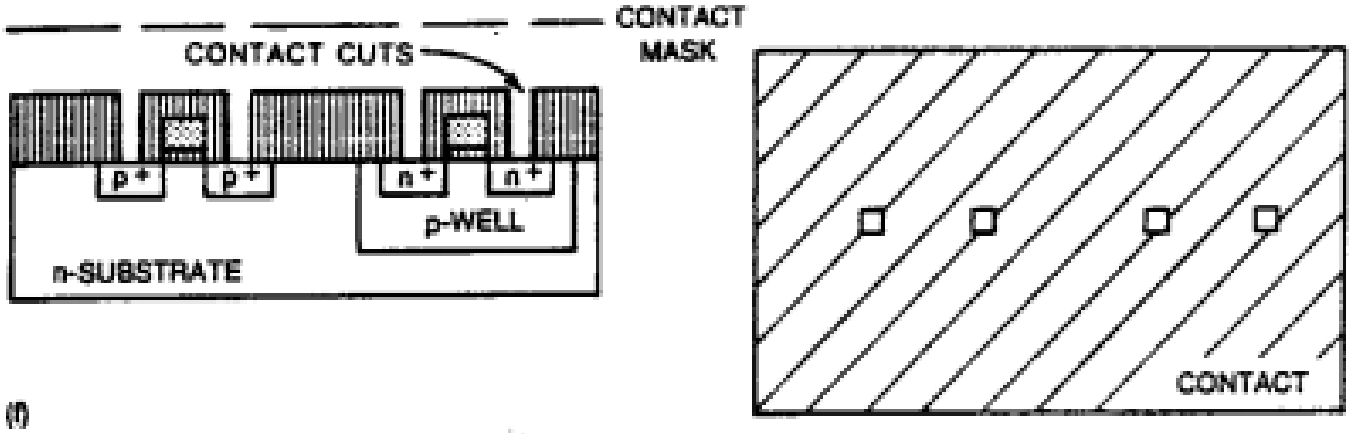
•A p-plus mask is now used (to be in effect "Anded" with Mask 2) to define all areas where p-diffusion is to take place.
•This mask is sometimes called the select mask as it selects those transistor regions that are to be p-type.





•This is usually performed using the **negative form of the p-plus mask** and defines those areas where n-type diffusion is to take place.
•*Complement of the p-plus mask*





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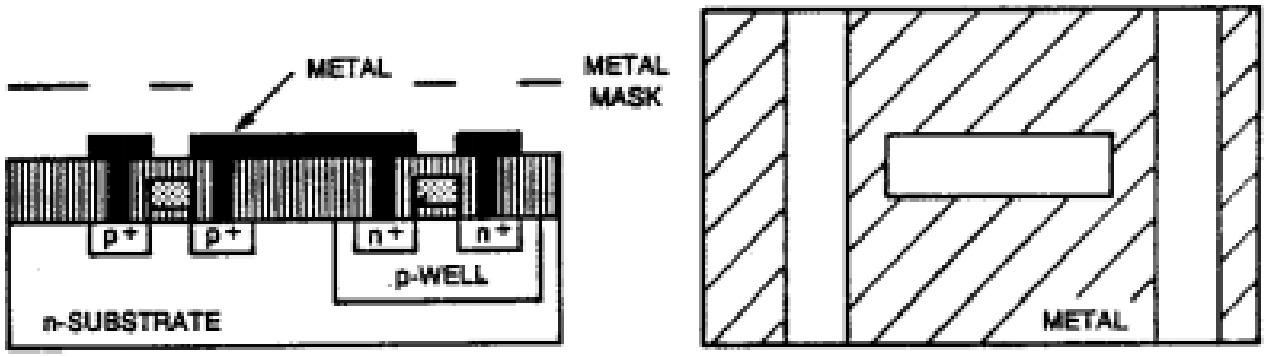
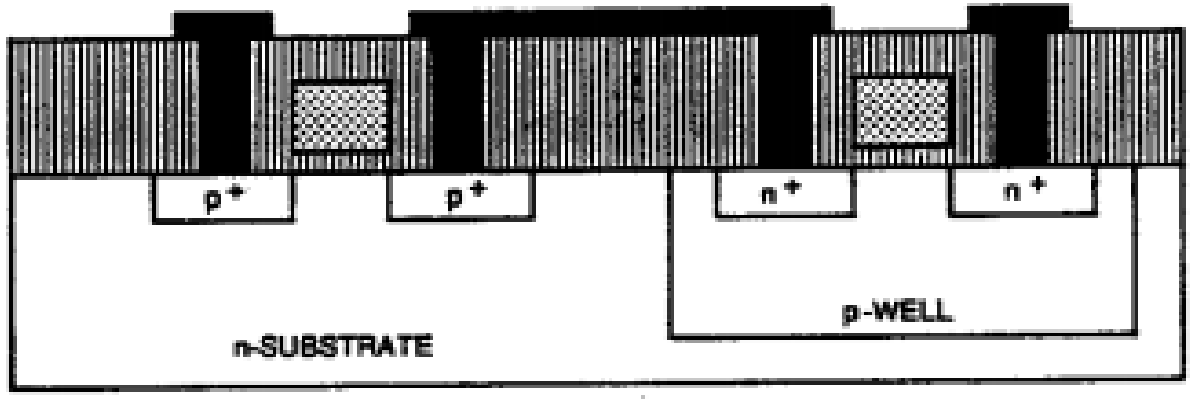
•Contact Cuts are then defined.
•This involves etching any SiO2 down to the contacted surface.
•These allow metal (next step) to contact diffusion regions and polysilicon regions.

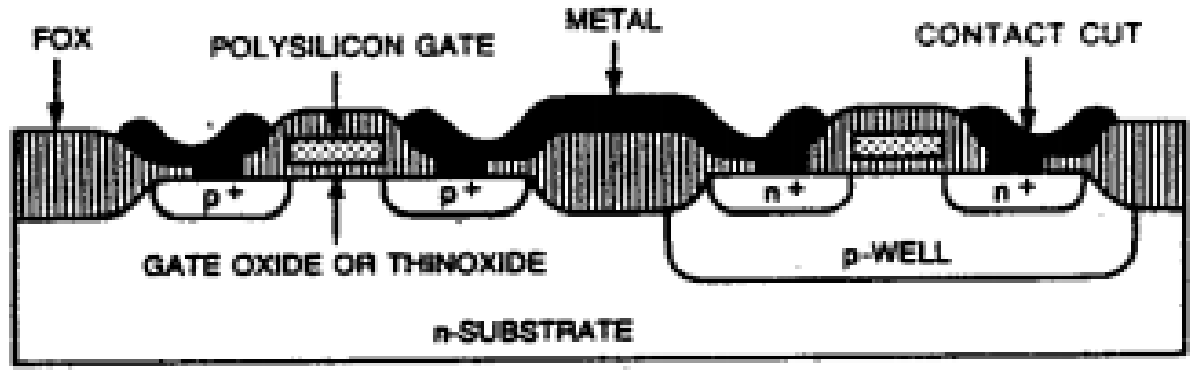


(g)

Matallization is then applied to the surface and selectively etched.

•As a final step, the wafer is passivated and openings to the bonding pads are etched to allow for wire bonding.
•Passivation protects the silicon surface against the ingress of contaminants that can modify circuit behaviour.
This passivation layer is called overglass layer.





Summary of p-well process

In all other respects—masking, patterning, and diffusion—the process is similar to nMOS fabrication. In summary, typical processing steps are:

- *Mask* 1 — defines the areas in which the deep p-well diffusions are to take place.
- *Mask 2* — defines the thinox regions, namely those areas where the thick oxide is to be stripped and thin oxide grown to accommodate p- and n-transistors and wires.
- *Mask* 3 — used to pattern the polysilicon layer which is deposited after the thin oxide.
- *Mask* 4 — A p-plus mask is now used (to be in effect "Anded" with Mask 2) to define all areas where p-diffusion is to take place.
- *Mask* 5 — This is usually performed using the negative form of the p-plus mask and defines those areas where n-type diffusion is to take place.
- *Mask* 6 — Contact cuts are now defined.
- *Mask* 7 — The metal layer pattern is defined by this mask.
- *Mask* 8 — An overall passivation (overglass) layer is now applied and Mask 8 is needed to define the openings for access to bonding pads.

- The p-wells act as substrates for the n-devices within the parent n-substrate.
- Provided that voltage polarity restrictions are observed, the two areas are electrically isolated.
- Since there are now in effect two substrates, two substrate connections (*VDD* and *VSS)* are required

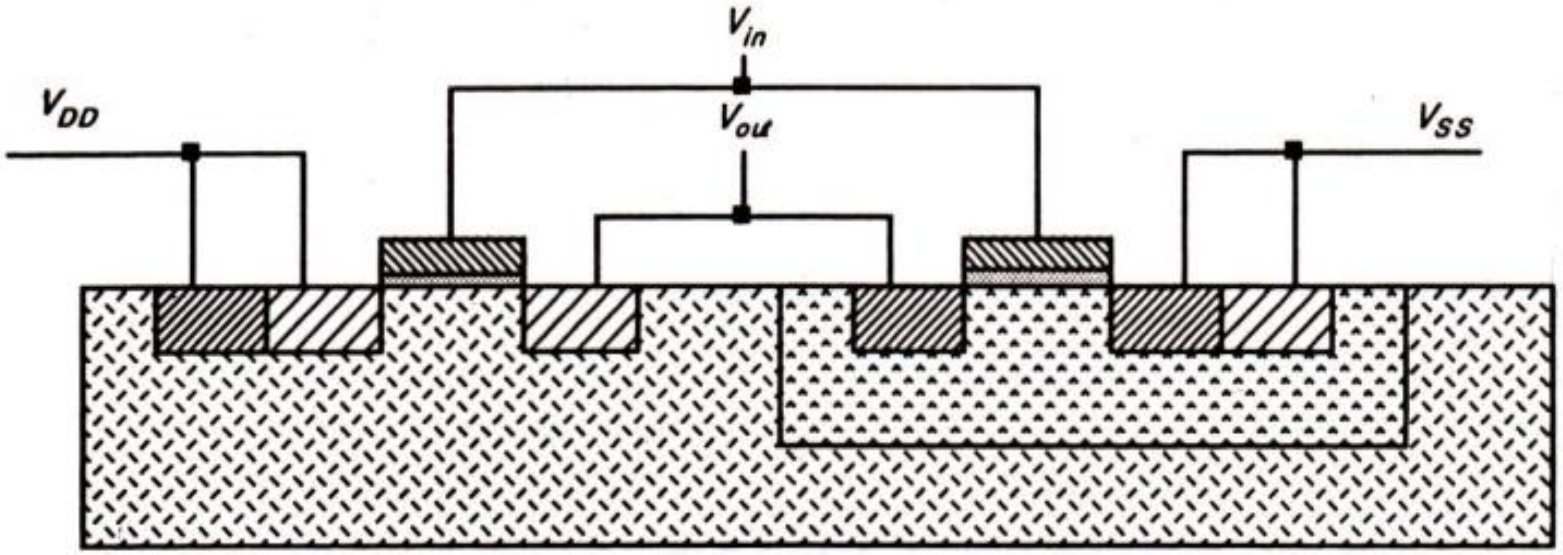


FIGURE 1.10 CMOS p-well inverter showing V_{DD} and V_{SS} substrate connections.

THANK YOU

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