DIGITAL VLSI DESIGN

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Unit 2: Fabrication of MOSFETs & Circuit Design Process

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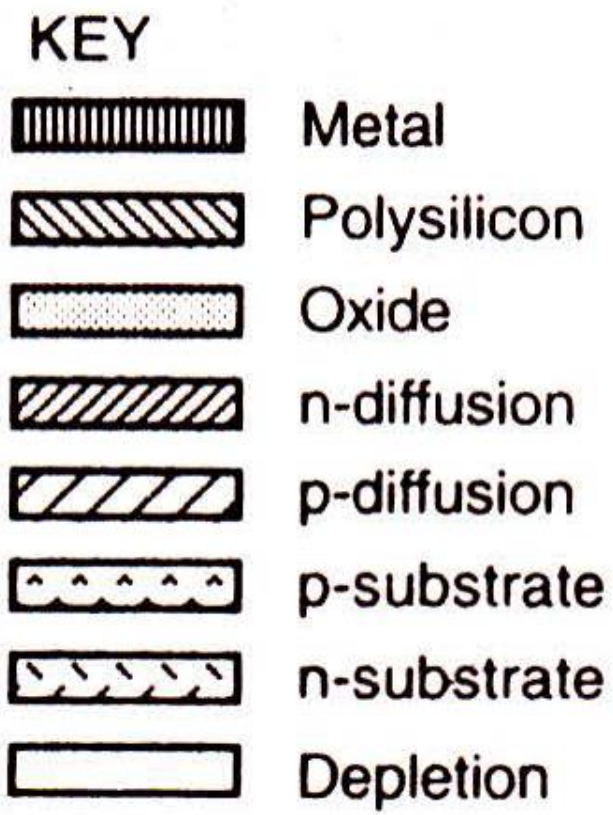
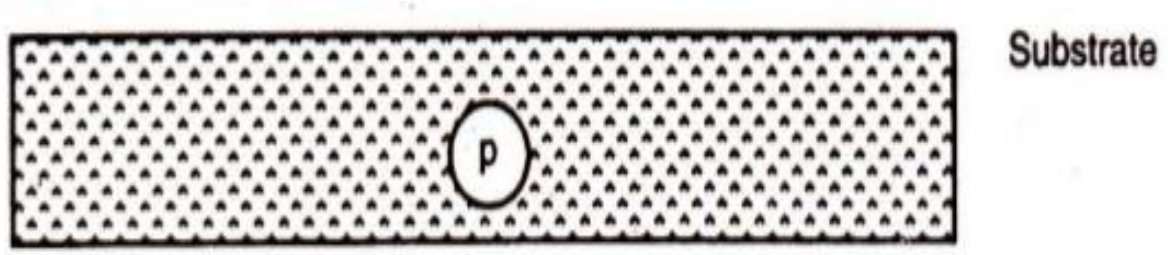
nMOS Fabrication

Different layer representation used in MOS layout is as shown below



nMOS Fabrication – Step 1

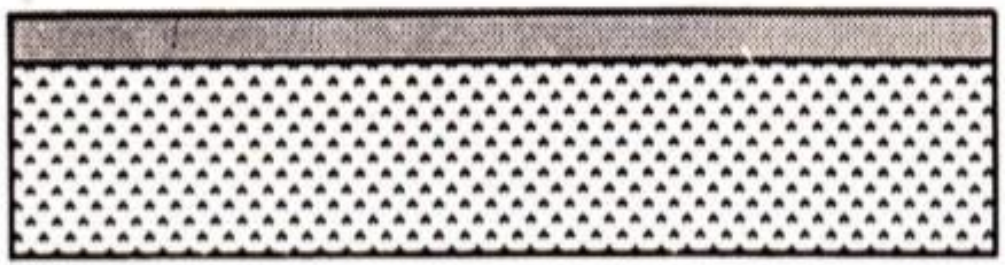
- Processing is carried out on a thin wafer cut from a single crystal of silicon of high purity into which the required p-impurities are introduced as the crystal is grown.
- Such wafers are typically 75 to 150 mm in diameter and 0.4 mm thick
- Doped with(say, boron) to impurity concentrations of 10^{15}/cm3 to 10^{16}/cm^3, giving resistivity in the approximate range 25 ohm cm to 2 ohm cm.



polysilicon gate self-aligning nMOS fabrication process

Step 2

- A layer of silicon dioxide (Si02), typically 1µm thick, is grown all over the surface of the wafer to
  - protect the surface,
  - act as a barrier to dopants during processing, and
  - provide a generally insulating substrate on to which other layers may be deposited and patterned.

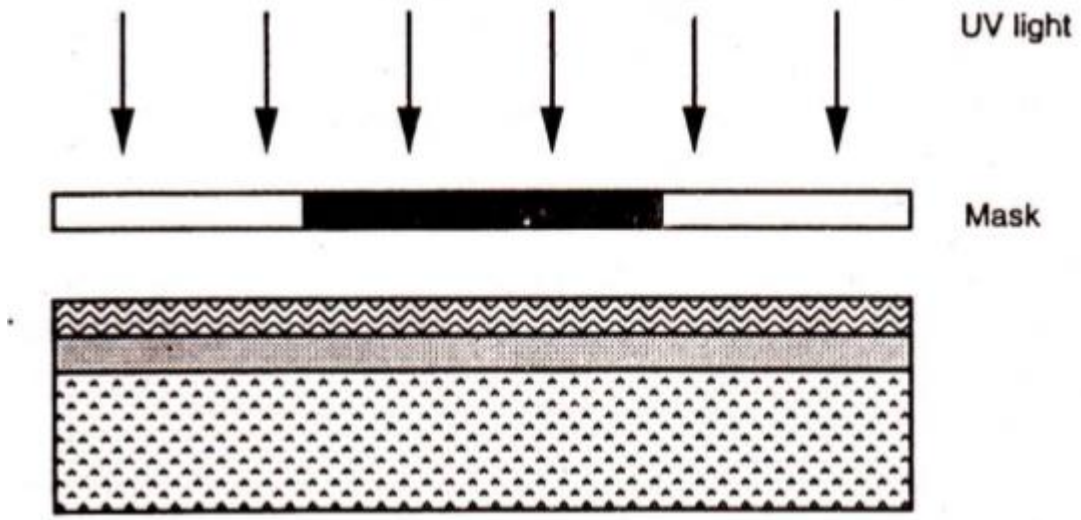


Step 3

- The surface is now covered with a photoresist which is deposited onto the wafer and spun to achieve an even distribution of the required thickness.

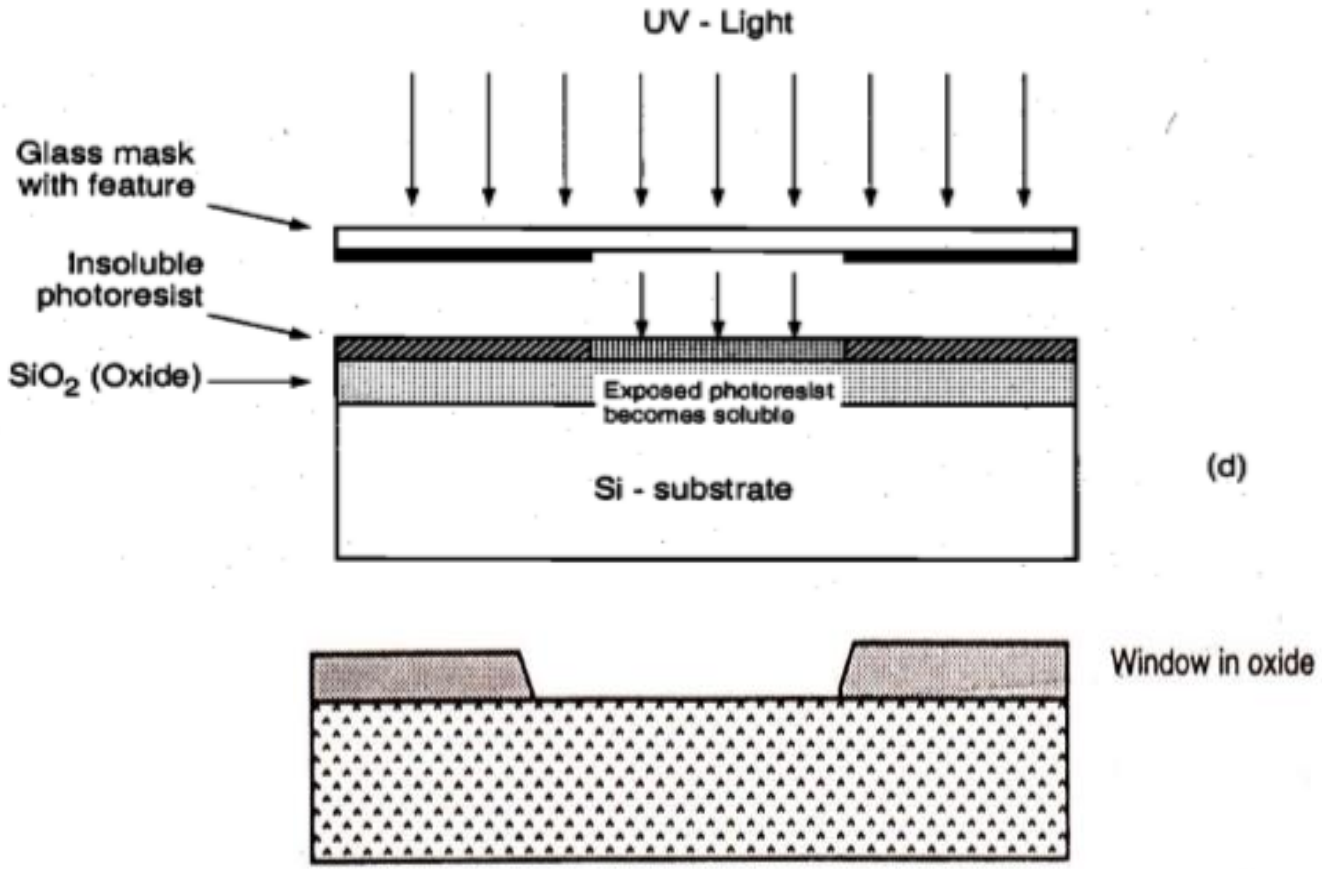
Step 4

- The photoresist layer is then exposed to ultraviolet light through a mask which defines those regions into which diffusion is to take place together with transistor channels.
  - Example: Those areas exposed to ultraviolet radiation are polymerized (hardened), but the areas required for diffusion are shielded by the mask and remain unaffected.



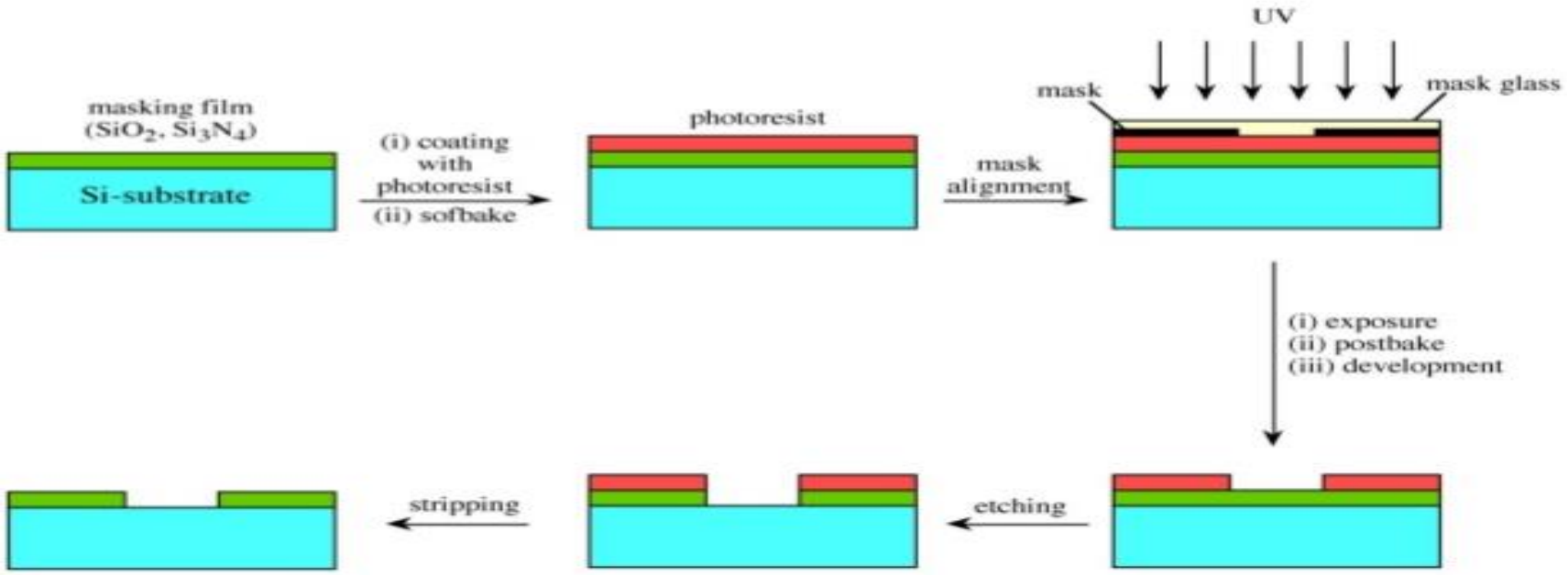
Step 5

- These areas are subsequently readily etched away together with the underlying silicon dioxide so that the wafer surface is exposed in the window defined by the mask

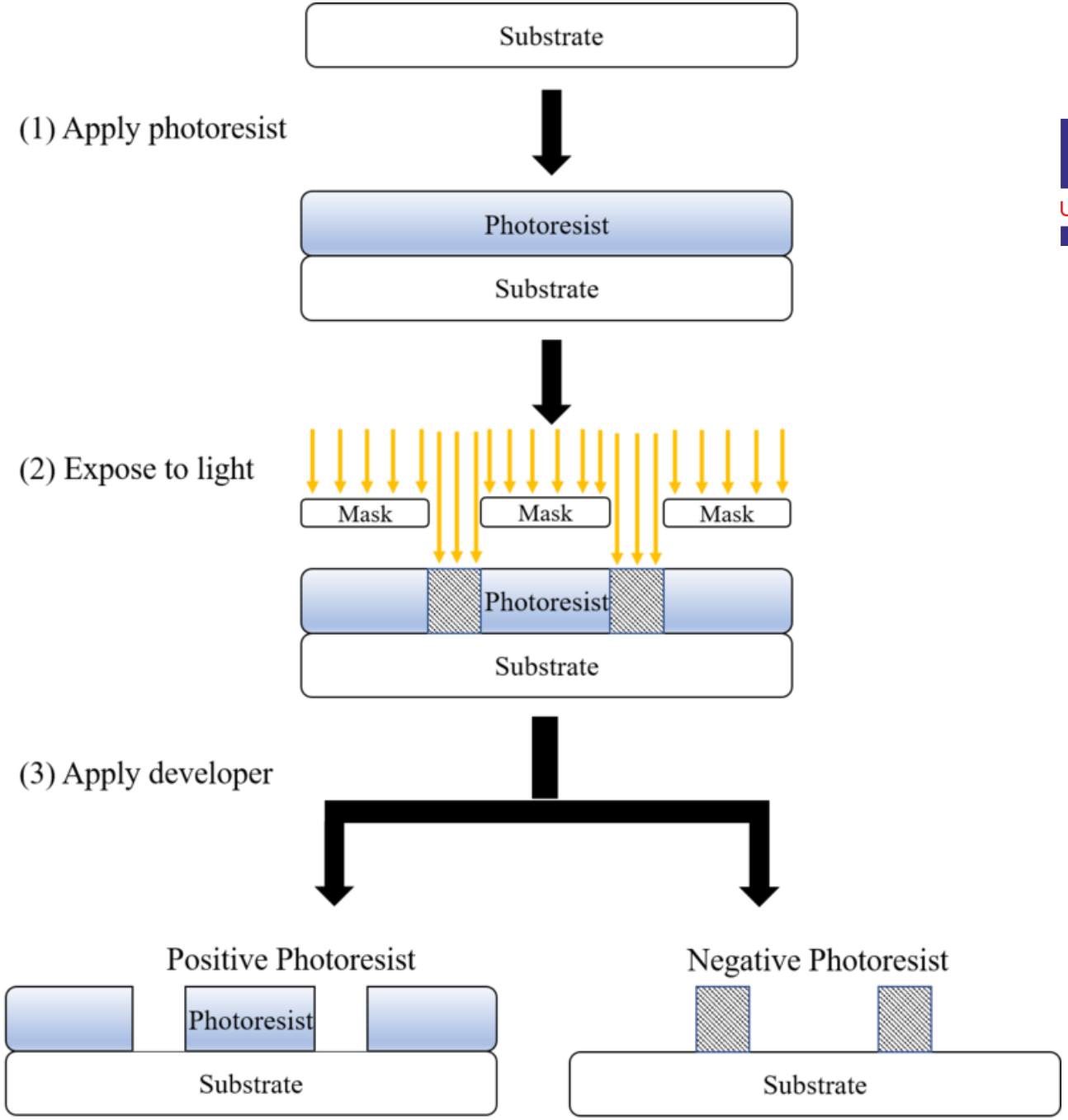


Photolithography

- One of the most important technology in the production of advanced integrated circuits
- It is through photolithography that semiconductor surfaces are patterned and the circuits formed.
- To make extremely small features, in the order of wavelength of light, advanced optical techniques are used to transfer a pattern from a mask onto the surface.
- A polymeric film or *resist*, is modified by the light and records the information in a process not dissimilar to ordinary photography.

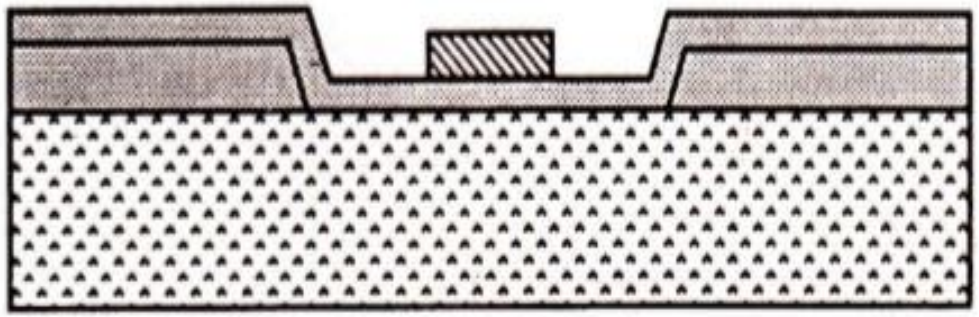


- In the case of a positive photoresist, the photo-sensitive material is degraded by light and the developer will dissolve away the regions that were exposed to light, leaving behind a coating where the mask was placed.
- In the case of a negative photoresist, the photosensitive material is strengthened (either polymerized or cross-linked) by light, and the developer will dissolve away only the regions that were not exposed to light, leaving behind a coating in areas where the mask was not placed.


Substrate
(1) Apply photoresist
Photoresist
Substrate
(2) Expose to light
Mask
Mask
Mask
Photoresist
Substrate
(3) Apply developer
Positive Photoresist
Photoresist
Substrate
Negative Photoresist
Substrate

Step 6

- The remaining photoresist is removed and a thin layer of Si02 (0.1µm typical) is grown over the entire chip surface.
- Polysilicon is then deposited on top of this to form the gate structure.
- The polysilicon layer consists of heavily doped polysilicon deposited by chemical vapor deposition (CVD).
- In the fabrication of fine pattern devices, precise control of thickness, impurity concentration, and resistivity is necessary.
- Further photoresist coating and masking allows the polysilicon to be patterned



Patterned poly. (1–2 µm)
on thin oxide (800–1000 Å)

Step 7

- The thin oxide is removed to expose areas into which n-type impurities are to be diffused to form the source and drain.
- Diffusion is achieved by heating the wafer to a high temperature and passing a gas containing the desired n-type impurity (for example, phosphorus) over the surface.

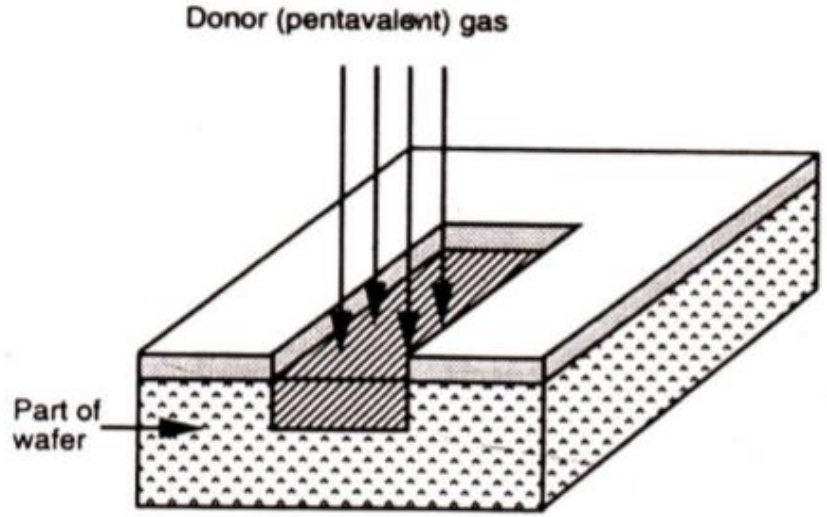
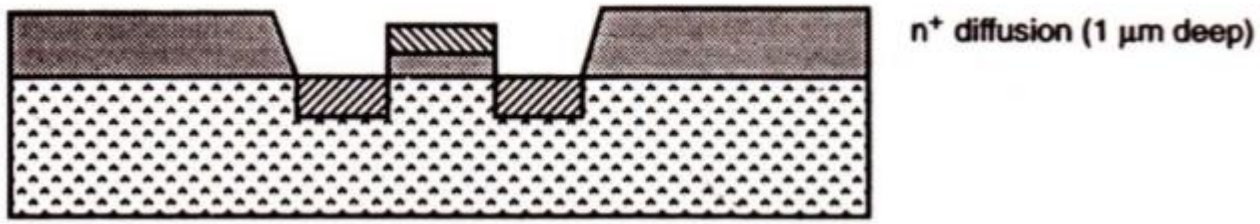


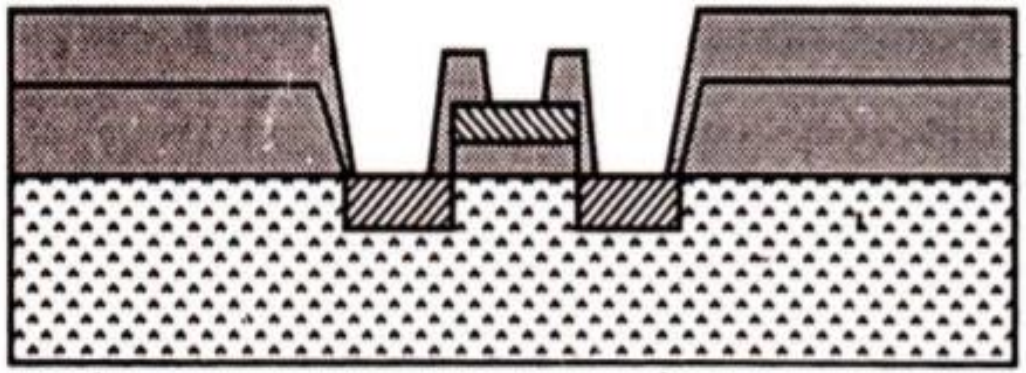
FIGURE 1.8 Diffusion process.

•Note that the polysilicon with underlying thin oxide act as masks during diffusion →the process is self-aligning.



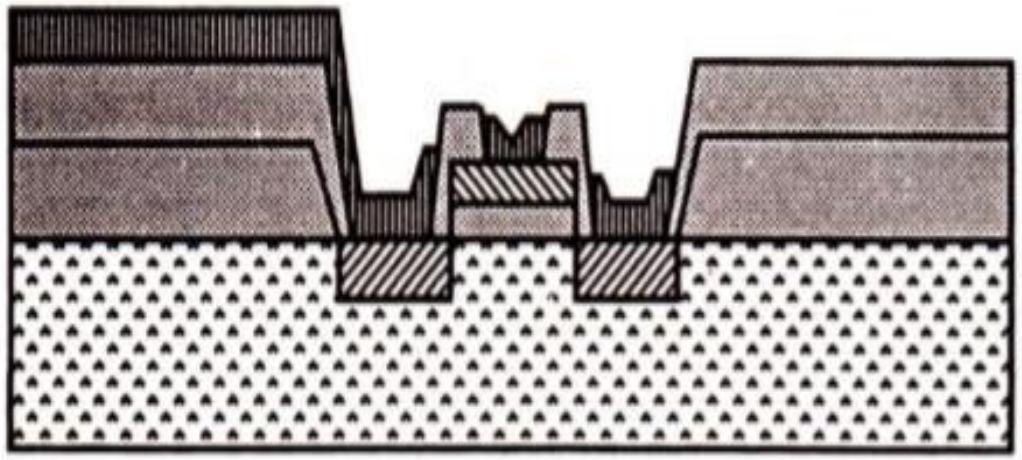
Step 8

- Thick oxide (SiO_2) is grown over all again and is then masked with photoresist and etched to expose selected areas of the polysilicon gate and the drain and source areas where connections (i.e. contact cuts) are to be made.



Step 9

- The whole chip then has metal (aluminium) deposited over its surface to a thickness typically of 1µm.
- This metal layer is then masked and etched to form the required interconnection pattern.



Summary of an nMOS Process

- Processing takes place on a p-doped silicon crystal wafer on which is grown a 'thick' layer of SiO_2.
- *Mask* 1—Pattern SiO_2 to expose the silicon surface in areas where paths in the diffusion layer or gate areas of transistors are required. Deposit thin oxide over all. For this reason, this mask is often known as the *'thinox' mask* but some texts refer to it as the *diffusion mask*.
- *Mask* 2—Pattern the ion implantation within the thinox region where depletion mode devices are to be produced—*self-aligning*.
- *Mask* 3—Deposit polysilicon over all (1.5 μm thick typically), then pattern using Mask 3. Using the same mask, remove thin oxide layer where it is not covered by polysilicon.
- Diffuse n^+ regions into areas where thin oxide has been removed. Transistor drains and sources are thus self-aligning with respect to the gate structures.
- *Mask* 4—Grow thick oxide over all and then etch for contact cuts.
- *Mask* 5—Deposit metal and pattern with Mask 5.
- *Mask* 6—Would be required for the overglassing process step.

THANK YOU

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