DIGITAL VLSI DESIGN

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MODULE 4

Sequential MOS Logic circuits

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Introduction

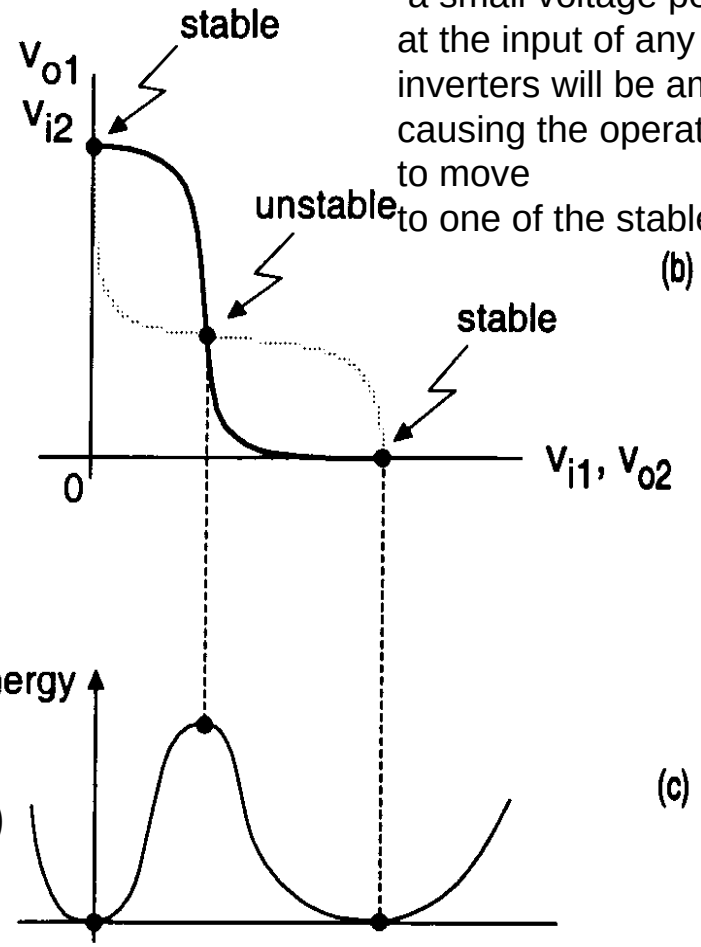
- Sequential Circuit
- Behavior of Bistable Elements
- SR Latch Circuit
- Clocked Latch and Flip Flop Circuits
- CMOS D-Latch and Edge-Triggered Flip-Flop

Classification of logic circuits based on temporal behaviour

Sequential circuit

BiStable

Voltage gain of inverters is larger than unity at unstable Point, a small voltage perturbation at the input of any of the inverters will be amplified, causing the operation point to move to one of the stable points.



simple analogy the energy function ***P (x)*** could be the potential energy of some one-dimensional mechanical system. The gradient of ***P (x)*** is a *"force"*

Bistable

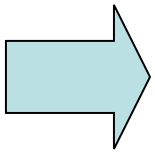
At $V_{01} = V_{02}$ → Unstable condition

$$i_{g1} = i_{d2} = g_m v_{g2}$$

$$i_{g2} = i_{d1} = g_m v_{g1}$$

where $g_m = (g_{mN} + g_{mP})$: *All four Transistor are in saturation*

Output Expectation (exponential!!!)

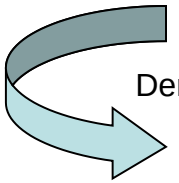


Direction is determined by initial perturbation polarity.

Continue…

Gate Capacitance >>> Drain Capacitance

Gate Charges



Derivative of small-signal gate voltages

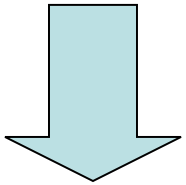
Continue…

$$\frac{dq_1}{dt} = ig_1$$

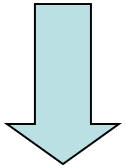
$$i_{g1} = g_m v_{g2}$$

Combination above three equations

Continue…



Combination of two equation yields 2nd order differential equation



Time behaviour of gate charge q1

Continue…

Continue…

$$q_1(0) = C_g \cdot v_{g1}(0)$$

Continue…

Assume ~ Large t

SR Latch Circuit

Gate-level Schematic/Block Diagram.

Truth Table

Operation Mode

Capacitance

$$C_Q = C_{gb,2} + C_{gb,5} + C_{db,3} + C_{db,4} + C_{db,7} + C_{sb,7} + C_{db,8}$$

$$C_{\overline{Q}} = C_{gb,3} + C_{gb,7} + C_{db,1} + C_{db,2} + C_{db,5} + C_{sb,5} + C_{db,6}$$

Circuit with Capacitance

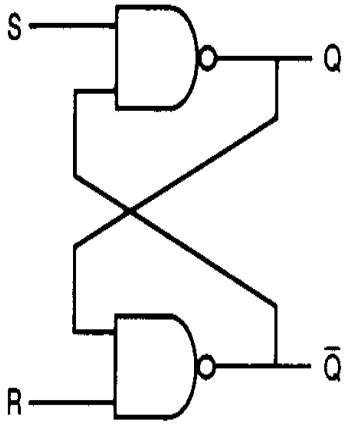
Rise Time

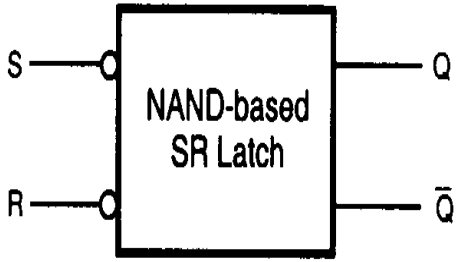
$$\tau_{rise,Q}(SR-latch) = \tau_{rise,Q}(\text{NOR2}) + \tau_{fall,\overline{Q}}(\text{NOR2})$$

Depletion Load nMOS (NOR2)

CMOS SR Latch circuit (NAND2)

Gate Schematic(NAND)





Truth Table

Depletion Load nMOS (NAND)

Clocked Latch and Flip-Flop Circuits

Sample Input-Output Waveforms

AOI Implementation (NOR)

Gate Schematic (NAND), active low

Gate Schematic (NAND), active high

Partial Block Diagram

Gate Schematic

Block Diagram

All NAND Implementation

Detailed Truth Table

- J, K Compliments Q will go to J value at the next clock edge. J, K HIGH, the output will reverse its state after each clock pulse.

NOR-based JK Latch

AOI Realization(NOR)

Toggle Switch

Master-Slave Flip Flop

Master-Slave Flip Flop

Master-Slave Flip Flop (NOR)

- CLK is HIGH MASTER is enable. Slave is disable and retains its previous state.
- CLK is LOW is disconnected while input of slaves are simultaneously coupled to the output of the slaves.

CMOS D-Latch and Edge-Triggered Flip Flop

CMOS Implementation

Simplified Schematic View

Timing Diagram

2nd CMOS Implementation

CMOS –ve Edge-triggered

Simulated Input-Output

Timing Violation

Layout

CMOS +ve Edge-triggered

Timing Diagram

References

- S-M. Kang and Y. Leblebici ,*CMOS Digital Integrated Circuits: Analysis and Design*,, 3rd edition