DVLSI PROJECT

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CLASS: 4 B

TOPIC: TRANSMISSION GATE

Introduction:

A transmission gate (TG) is an analog gate similar to a relay that can conduct in both directions or block by a control signal with almost any voltage potential. It is a CMOS-based switch, in which PMOS passes a strong 1 but poor 0, and NMOS passes strong 0 but poor 1. Both PMOS and NMOS work simultaneously.

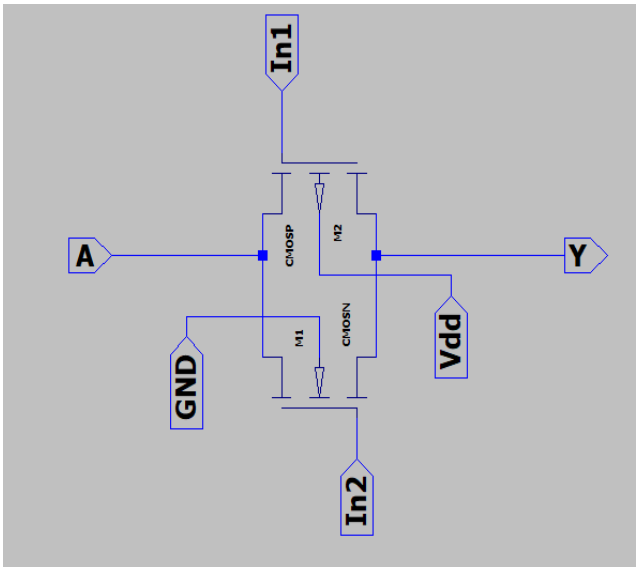
Theory:

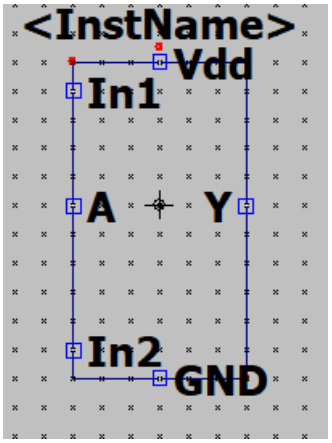
When the control input is a logic zero is given the gate of the n-channel MOSFET is also at a negative supply voltage potential. The gate terminal of the p-channel MOSFET is caused by the inverter, to the positive supply voltage potential. Regardless of which switching terminal of the transmission gate voltage is applied, the gate-source voltage of the n-channel MOSFETs is always negative, and the p-channel MOSFETs is always positive. Accordingly, neither of the two transistors will conduct and the transmission gate turns off.

Now using transmission gate, we are going to realise 2:1 MUX

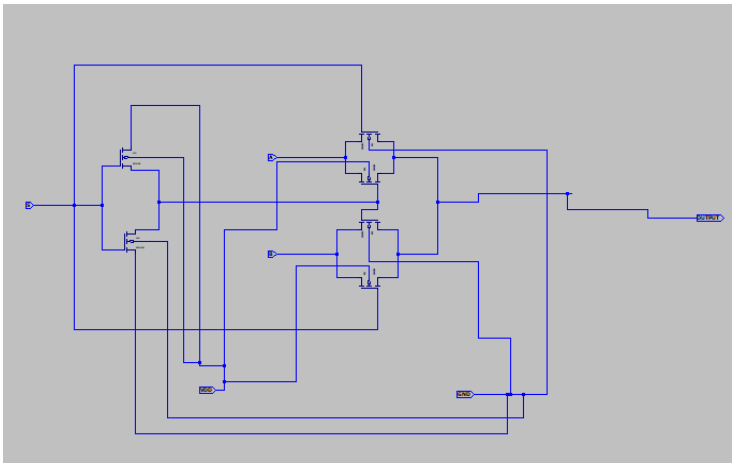
Which has three inputs. A, B, and select line S. when S is 0, Y=A and S=1, Y=B

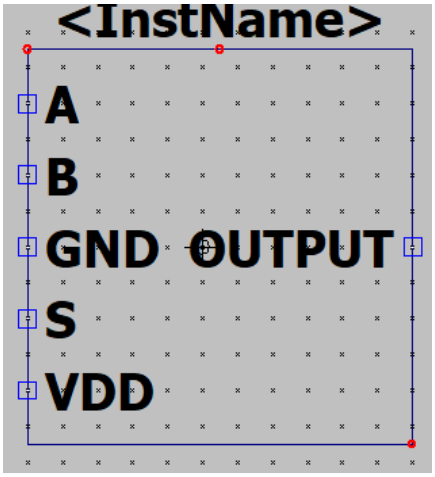
Schematic and Symbol

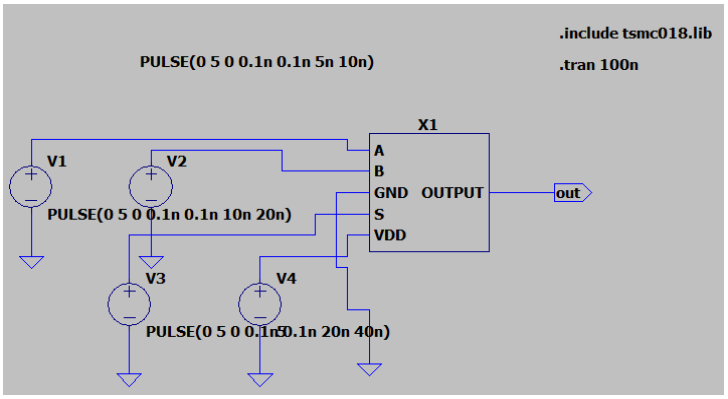


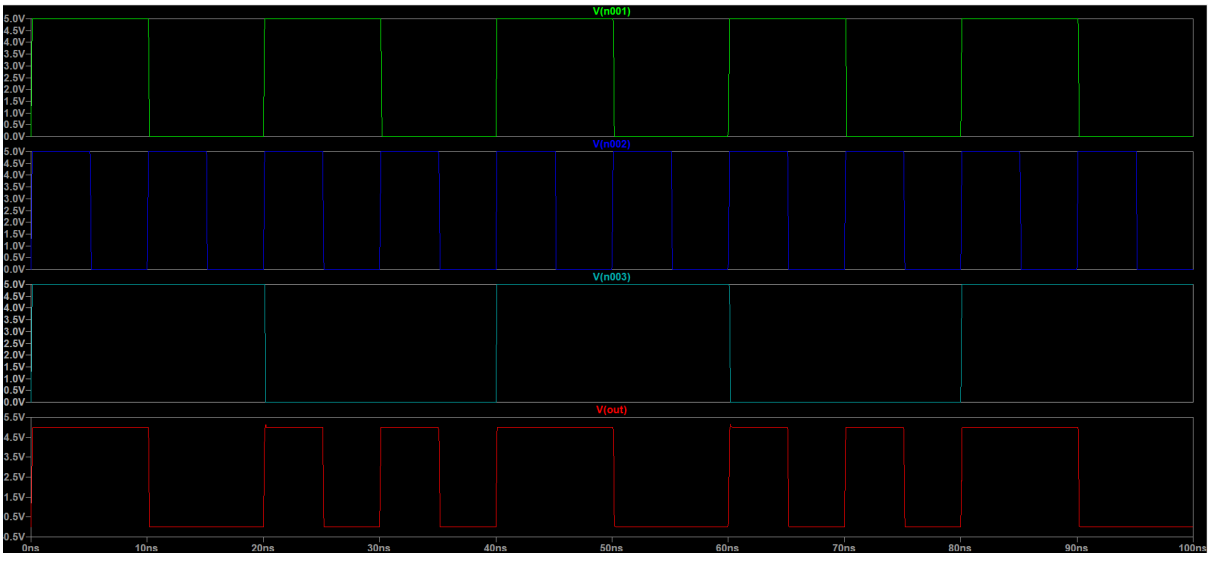


2:1 mux schematic symbol and test bench with graph









We have successfully implemented a 2:1mux using transmission gate

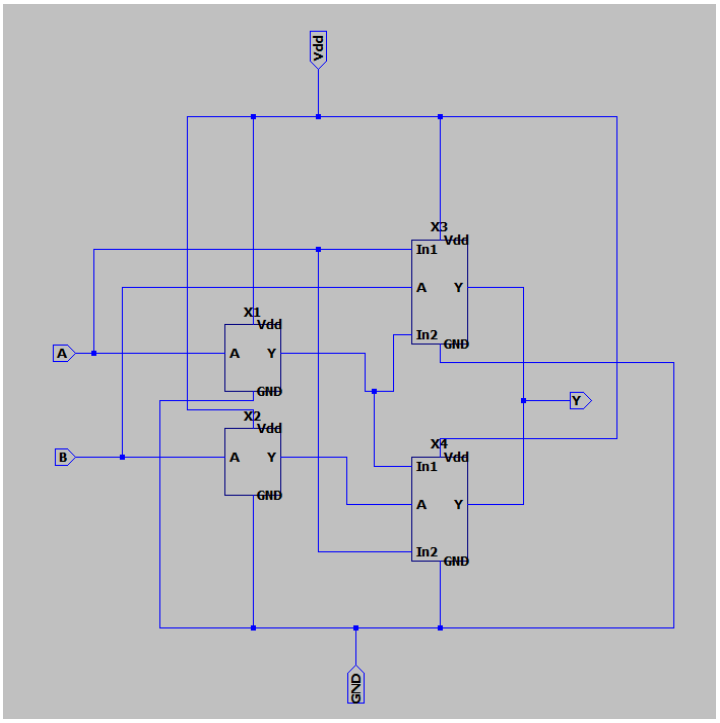
Power dissipation =15.907 uW

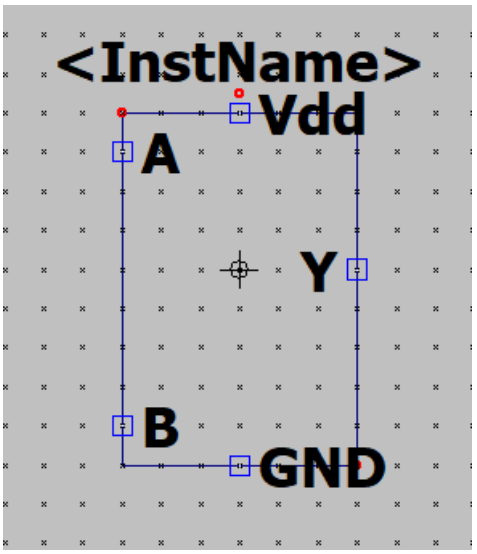
Number of cmos utilized = 6

Now we are going to realise 3 input full adder

But to implement it, first we design a 2 input xor gate using TG and then a 3 input xor gate which gives the sum expression and then we realise carry part of the full adder

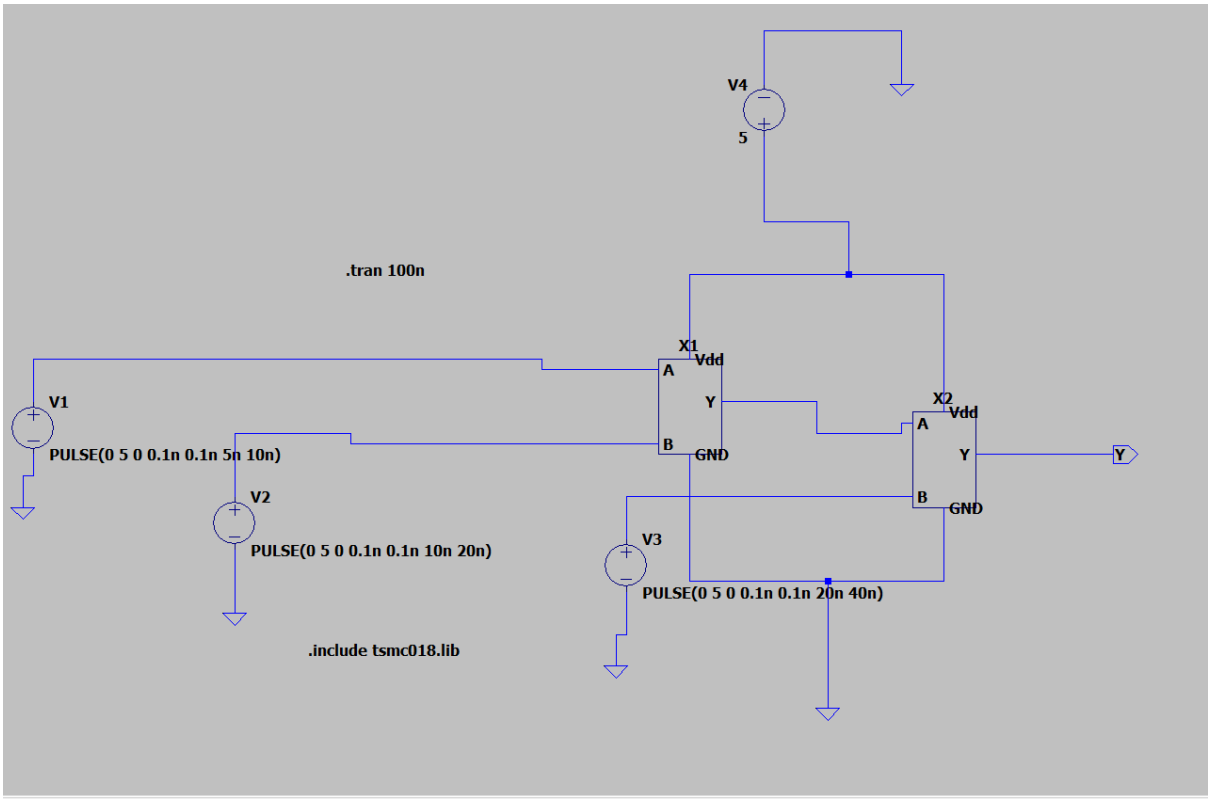
2 input XOR using TG schematic and symbol

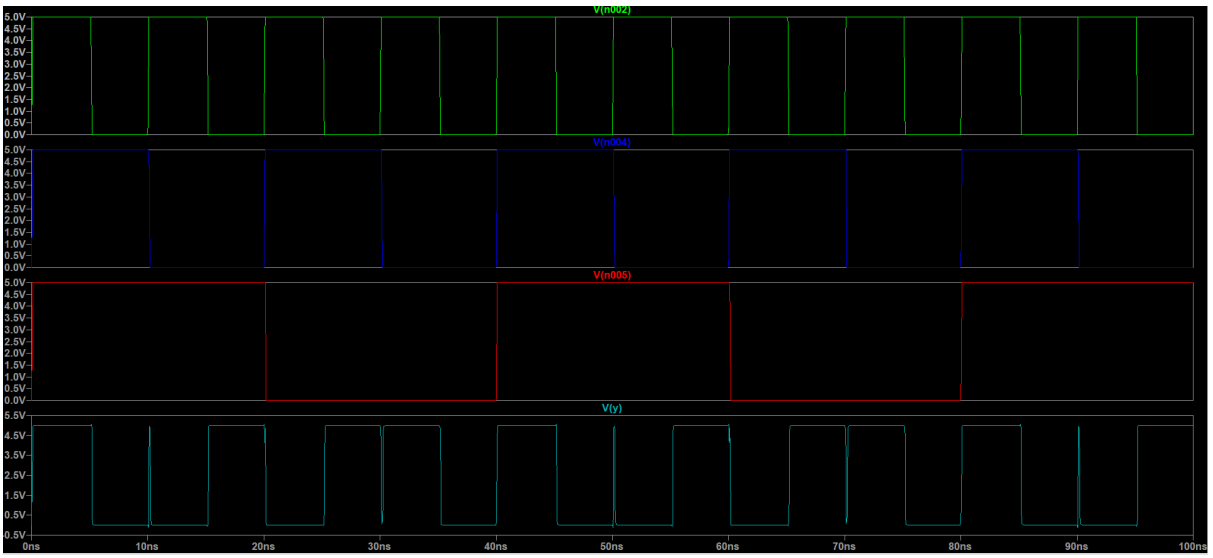




2 input xor gate uses 8 cmos

3 input XOR gate schematic/testbench (SUM PART)





We have realised 3 input xor gate for each case possible

Truth table for verification

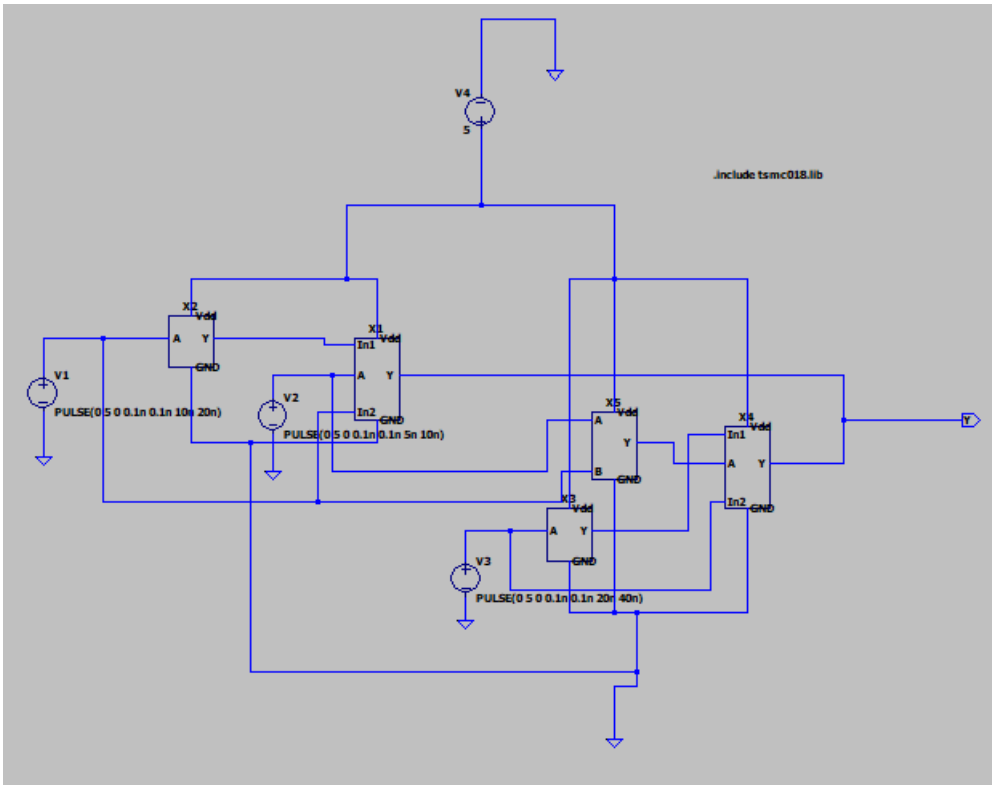
Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

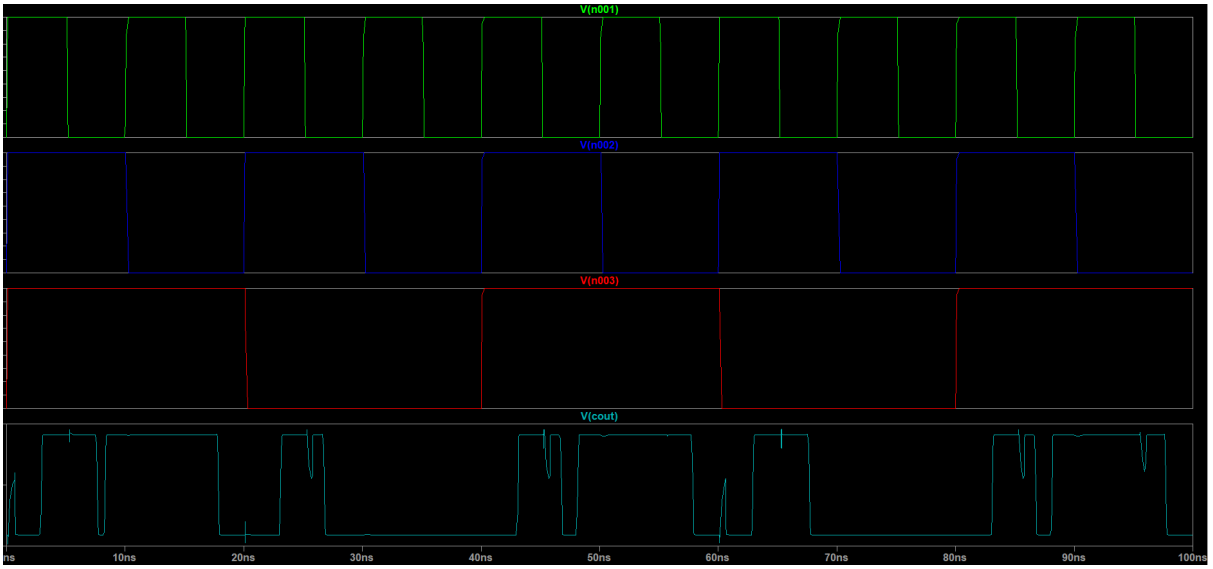
Power dissipation =255.71uW

No of cmos used =16

Now we implement for the carry part of the full adder

Schematic/ testbench with graph





We can verify with each case.

Therefore, we have successfully implemented full adder using TG

Power dissipation =156.23uW

No of cmos used for carry part = 16

The number of cmos used in full adder while using TG circuit is lesser than when we try to realise a full adder using cmos directly

Result:

We have successfully designed and implemented 2:1 MUX, FULL ADDER