DVLSI PROJECT

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ECE
Sem 4
B Section
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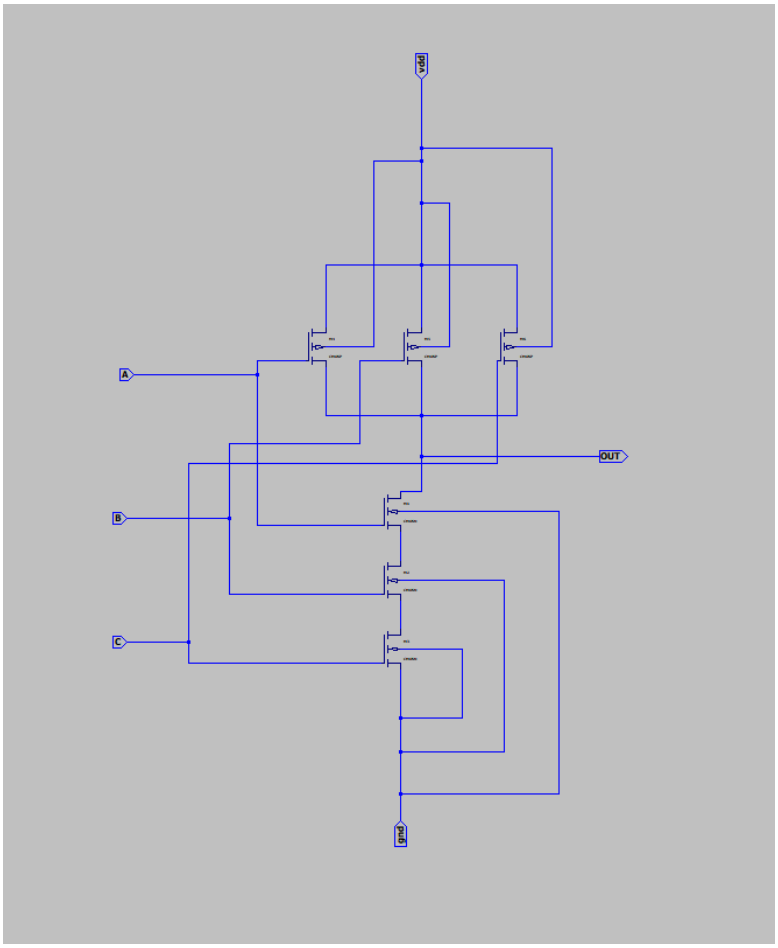
TOPIC : D FLIP FLOP

Overview

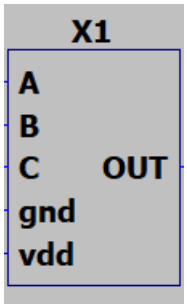
The D flip-flop is a clocked flip-flop with a single digital input ‘D’. Each time a D flip-flop is clocked, its output follows the state of ‘D’. The D Flip Flop has only two inputs D and Clock Pulse. The D inputs go precisely to the S input and its complement is used to the R input.

It is a rising edge flip-flop which means that the output is decided when the clock reached 50% of its final value.

Schematic



Symbol



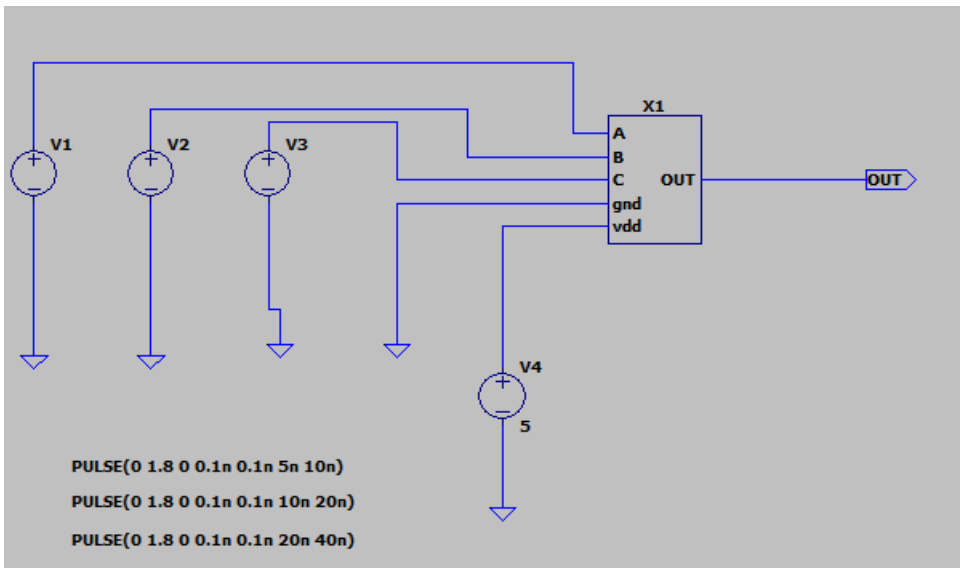
Specifications

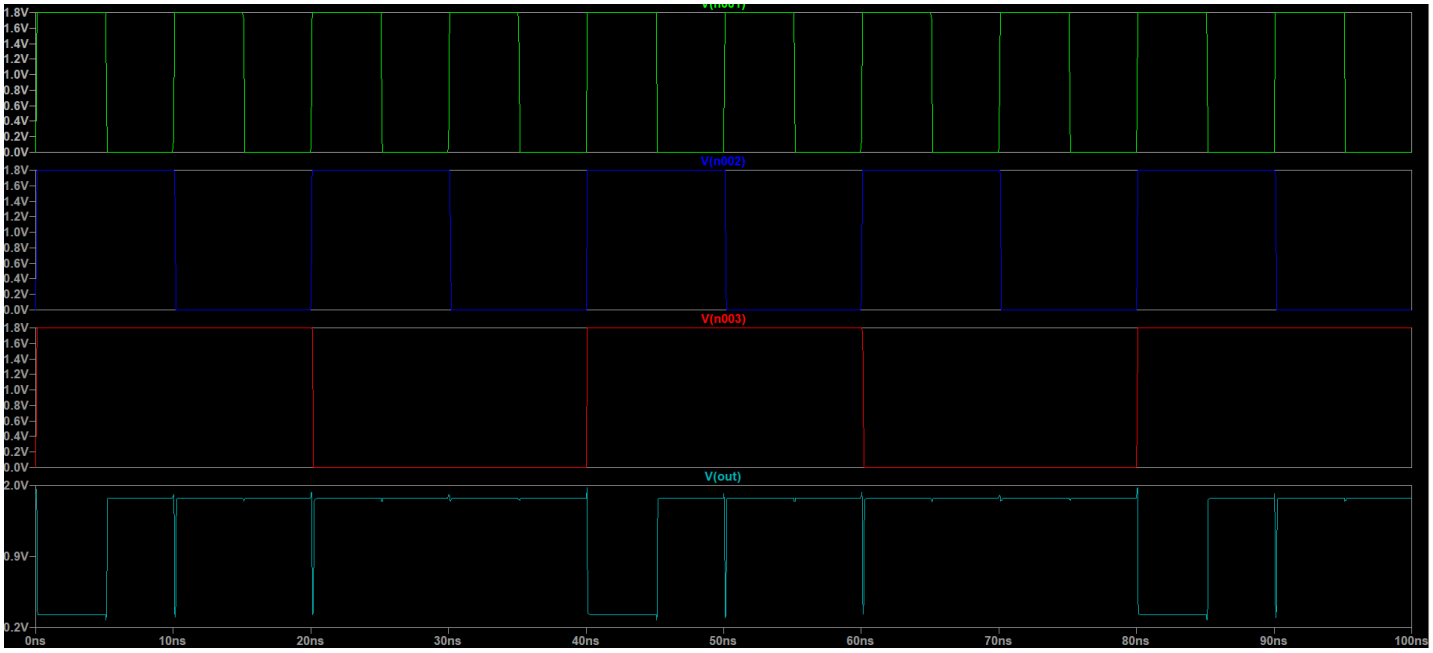
I. Number of CMOS Used is 6

II. Length of the CMOS 180 nm

III. Width of the CMOS 2 µm

Testbench





Observations

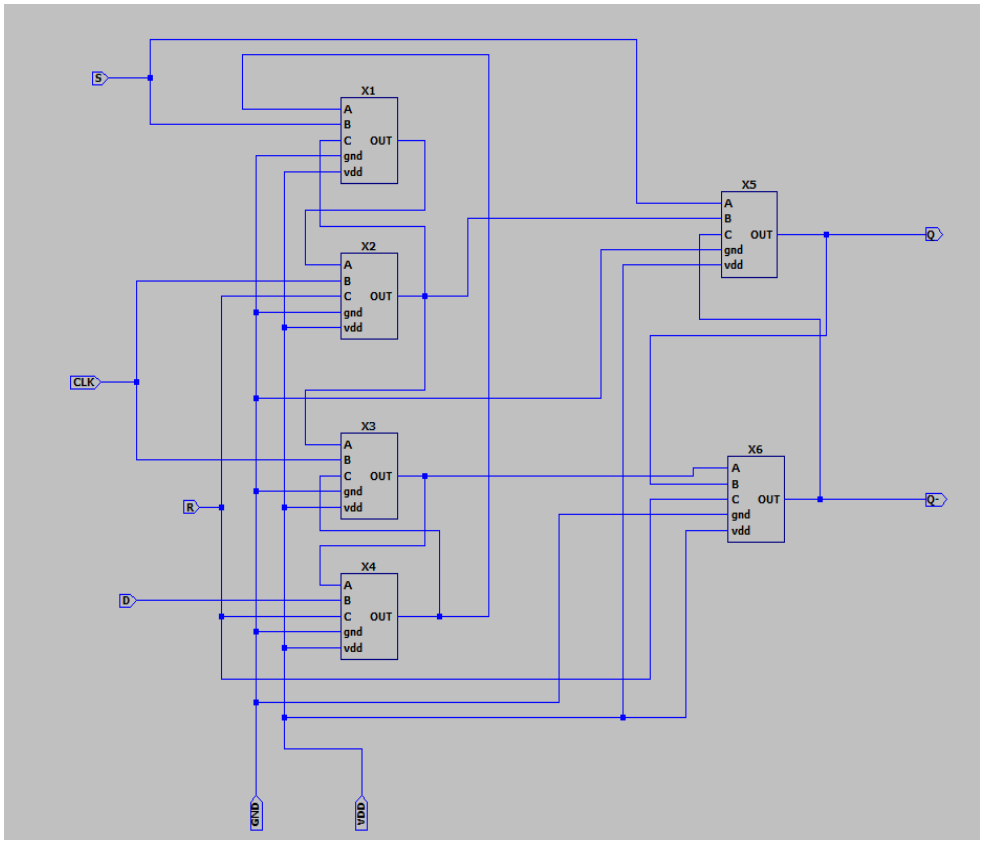
For A = B = C = 1, the output of the NAND Gate is 0 V

Power Dissipated is 467.93 µW

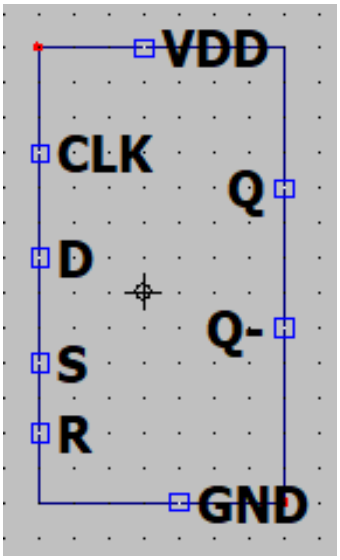
Delay is 2.14 ns

D Flip-Flop

Schematic



Symbol



Specifications

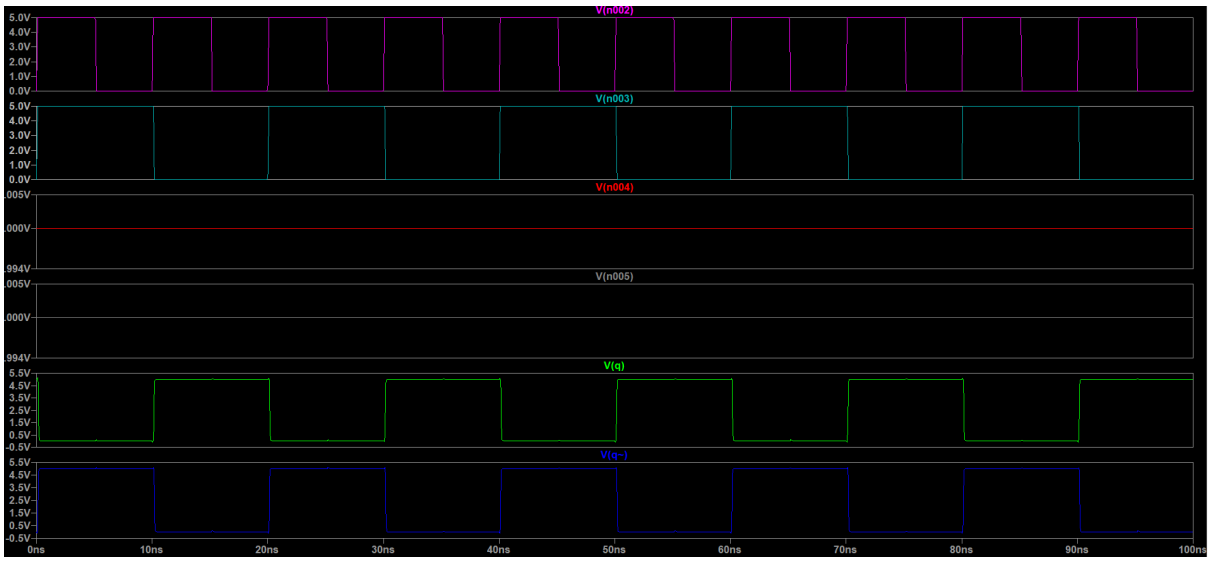
Number of CMOS Used is 36

Length of the CMOS 180 nm

Width of the CMOS 2 µm

Test Parameters

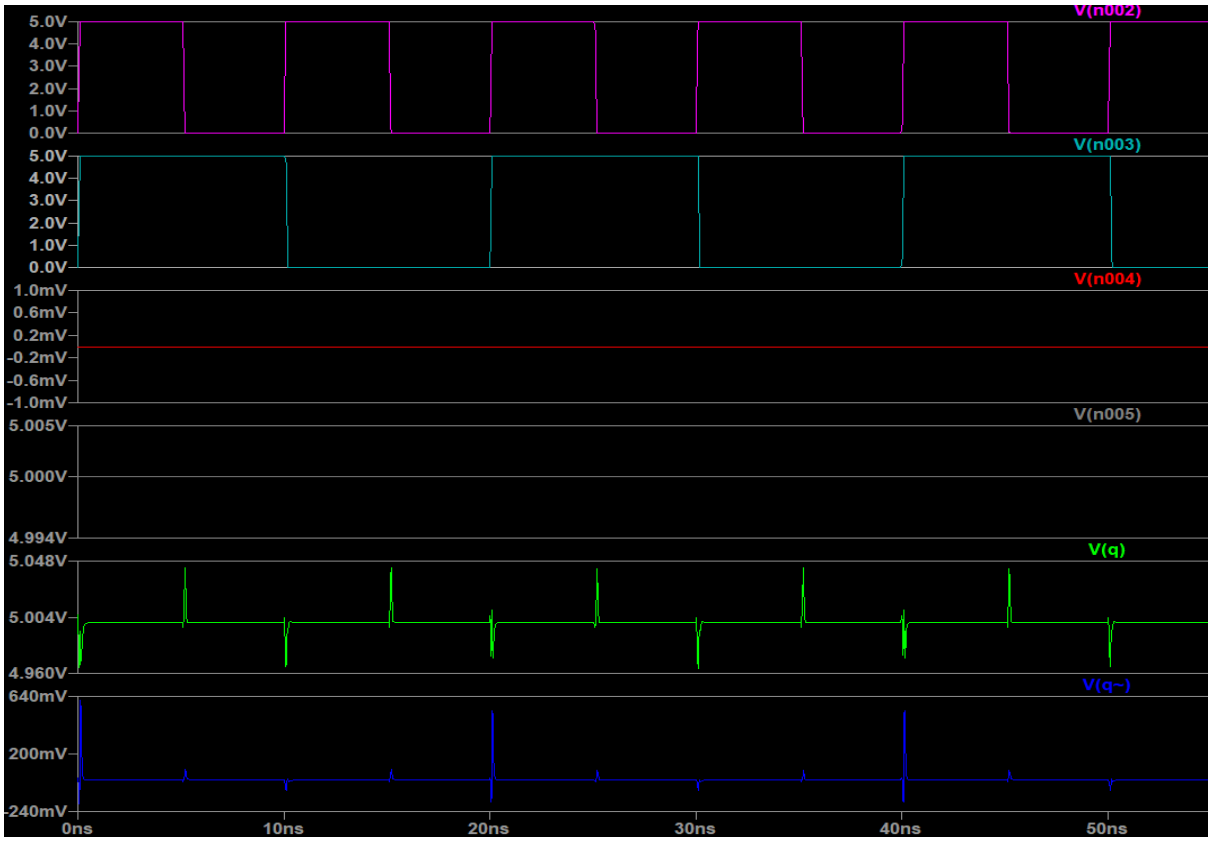
I. When S=1 and R=1



Power Dissipation = -332.05 µW

II. When S=0 and R=1

Expected Output Q=1 AND Q'=0

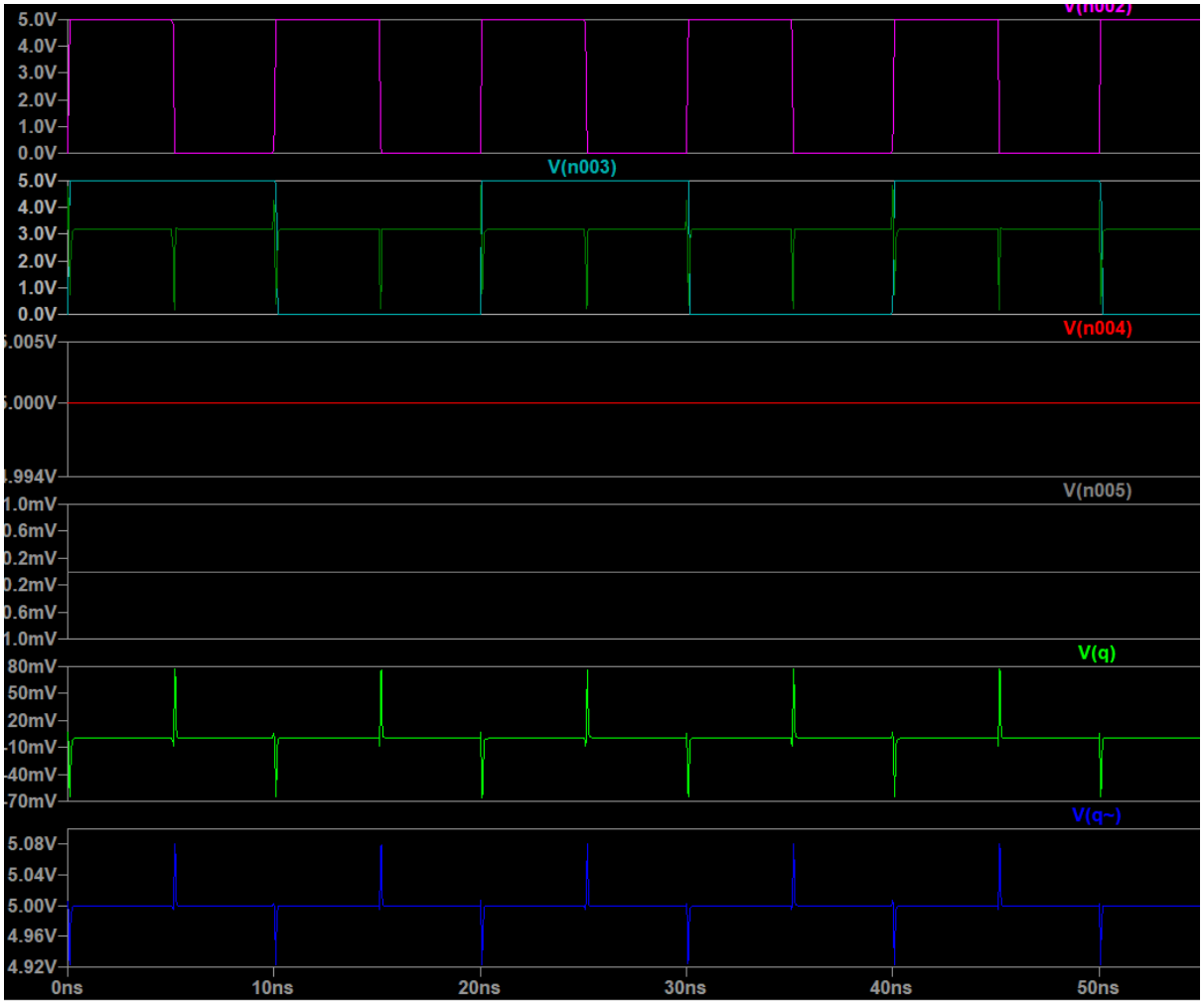


Q=4.889 V AND Q'=2 mV

Power Dissipation = 209.35 µW

III. When S=1 and R=0

Expected Output Q=0 AND Q'=1



Power Dissipation = 86.03 µW

Results

We have successfully a designed and implement D Flip-Flop using CMOS Structure