DIGITAL VLSI DESIGN

Annapurna K Y
Electronics and Communication Engineering

DIGITAL VLSI DESIGN

Unit 2: Fabrication of MOSFETs & Circuit Design Process

Annapurna K Y

Electronics and Communication Engineering

MOSFET Scaling and Small-Geometry Effects

- The reduction of the size, i.e., the dimensions of MOSFETs, is commonly referred to as *scaling.*
- Some physical limitations eventually restrict the extent of scaling that is practically achievable.

- There are two basic types of size-reduction strategies:
  full scaling (also called constant-field scaling) and *constantvoltage scaling.*

- Scaling of MOS transistors is concerned with systematic reduction of overall dimensions of the devices as allowed by the available technology, while preserving the geometric ratios found in the larger devices.

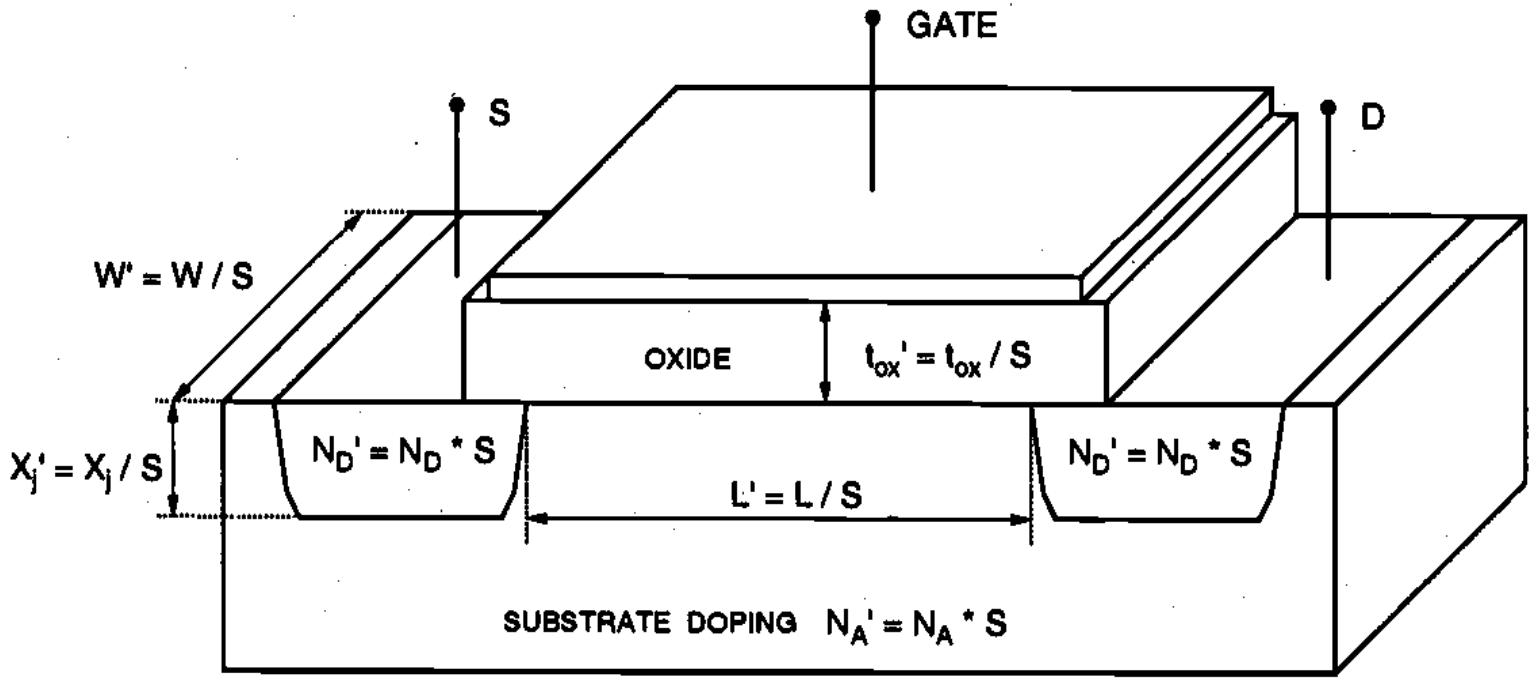
- The proportional scaling of all devices in a circuit would certainly result in a reduction of the total silicon area occupied by the circuit, thereby increasing the overall functional density of the chip.

- To describe device scaling, we introduce a constant *scaling factor* $S > 1$.

- All horizontal and vertical dimensions of the *large-size* transistor are then divided by this scaling factor to obtain the scaled device.

- The extent of scaling that is achievable is obviously determined by the fabrication technology and more specifically, by the minimum feature size.

- We consider the proportional scaling of all three dimensions by the same scaling factor S.
- The below figure shows the reduction of key dimensions on a typical MOSFET, together with the corresponding increase of the doping densities.



Full Scaling (Constant Field)

- The following quantities are altered during fabrication
- We use a prime (‘) to denote the new scaled quantity

Full scaling of MOSFET dimensions, potentials, and doping densities.

Quantity	Before Scaling	After Scaling
Channel length	L	$L' = L / S$
Channel width	W	$W' = W / S$
Gate oxide thickness	t_{ox}	$t_{ox}' = t_{ox} / S$
Junction depth	x_j	$x_j' = x_j / S$
Power supply voltage	V_{DD}	$V_{DD}' = V_{DD} / S$
Threshold voltage	V_{T0}	$V_{T0}' = V_{T0} / S$
Doping densities	N_A N_D	$N_A' = S \cdot N_A$ $N_D' = S \cdot N_D$

- This scaling option attempts to preserve the magnitude of internal electric fields in the MOSFET, while the dimensions are scaled down by a factor of S.
- To achieve this goal, all potentials must be scaled down proportionally, by the same scaling factor.
- Note that this potential scaling also affects the threshold voltage V_{T0}.
- Finally, the Poisson equation describing the relationship between charge densities and electric fields dictates that the charge densities must be *increased* by a factor of S in order to maintain the field conditions.

Effects of full scaling upon key device characteristics

Quantity	Before Scaling	After Scaling
Oxide capacitance	C_{ox}	$C_{ox}' = S \cdot C_{ox}$
Drain current	I_D	$I_D' = I_D / S$
Power dissipation	P	$P' = P / S^2$
Power density	$P / Area$	$P' / Area' = P / Area$

$$P = I_D \cdot V_{DS}$$

$$P' = I_D' \cdot V_{DS}' = \frac{1}{S^2} \cdot I_D \cdot V_{DS} = \frac{P}{S^2}$$

$$I_D'(lin) = \frac{k_n'}{2} \cdot \left[2 \cdot (V_{GS}' - V_T') \cdot V_{DS}' - V_{DS}'^2\right]$$

$$= \frac{S \cdot k_n}{2} \cdot \frac{1}{S^2} \cdot \left[2 \cdot (V_{GS} - V_T) \cdot V_{DS} - V_{DS}^2\right] = \frac{I_D(lin)}{S}$$

$$I_D'(sat) = \frac{k_n'}{2} \cdot (V_{GS}' - V_T')^2 = \frac{S \cdot k_n}{2} \cdot \frac{1}{S^2} \cdot (V_{GS} - V_T)^2 = \frac{I_D(sat)}{S}$$

THANK YOU

Annapurna K Y

Electronics & Communication Engineering

annapurnaky@pes.edu