DIGITAL VLSI DESIGN

Unit 2: Fabrication of MOSFETs & Circuit Design Process

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Electronics and Communication Engineering

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Layout Design Rules

- To allow reliable fabrication of each structure, the mask layers must conform to a set of geometric layout design rules.
- Usually, the rules (for example: minimum distance and/or separation between layers) are expressed as multiples of a scaling factor – lambda (λ).
- For each different fabrication technology, lambda factor can be different.

Layout Design Rules

N-Well

1.1	Min. width	10 λ
1.2	Min. spacing (diff. potential)	9 λ
1.3	Min. spacing (same potential)	6 λ

Active

2.1	Min. width	3 λ
2.2	Min. spacing	3 λ
2.3	S/D active to well edge	5 λ
2.4	Sub. C. active to well edge (*)	3 λ
2.5	Min. spac. different implant (*)	4 λ

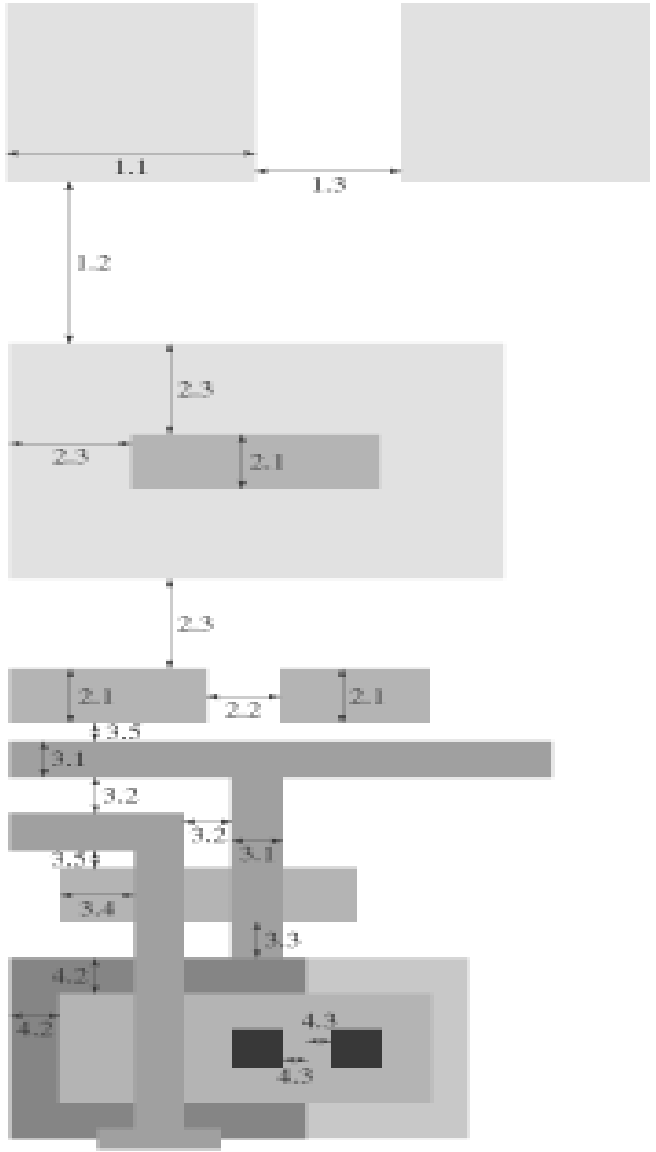
Poly

3.1	Min. width	2 λ
3.2	Min. spacing	2 λ
3.3	Min. gate extension	2 λ
3.4	Min. active extension to poly	3 λ
3.5	Min. field poly to active	1 λ

Select

4.1	Min. select spacing to gate (*)	3 λ
4.2	Min. overlap of active	2 λ
4.3	Min. overlap of contact	1 λ
4.4	Min. width and spacing (*)	2 λ

(*) Not Drawn



Layout Design Rules

Contact

5.1	Exact contact size	2 λ
5.2	Min. poly overlap	1.5 λ
5.3	Min. spacing	2 λ
5.4	Min. spacing to gate	2 λ
6.1	Exact contact size	2 λ
6.2	Min. active overlap	1.5 λ
6.3	Min. spacing	2 λ
6.4	Min. spacing to gate	2 λ

Metal 1

7.1	Min. width	3 λ
7.2.a	Min. spacing	3 λ
7.3	Min. overlap of any contact	1 λ

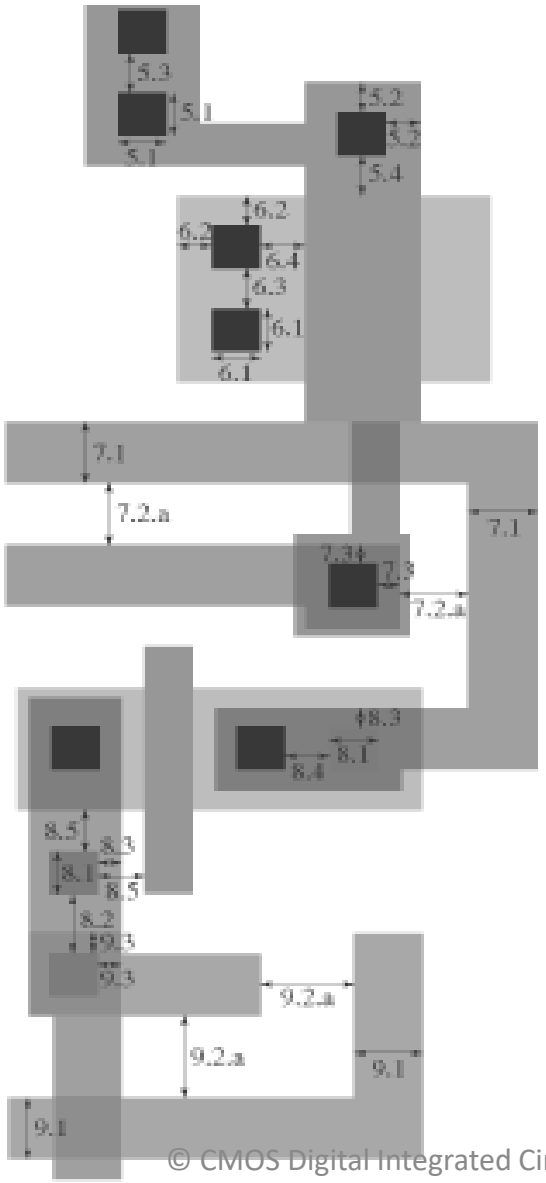
Via 1

8.1	Exact size	2 λ
8.2	Min. spacing	3 λ
8.3	Min. overlap by metal1	1 λ
8.4	Min. spacing to contact	2 λ
8.5	Min. spac. to poly or act. edge	2 λ

Metal2

9.1	Min. width	3 λ
9.2.a	Min. spacing	4 λ
9.3	Min. overlap to via1	1 λ

(*) Not Drawn



THANK YOU

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