Digital VLSI Design

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MOS INVERTERS: SWITCHING CHARACTERISTICS AND INTERCONNECT EFFECTS

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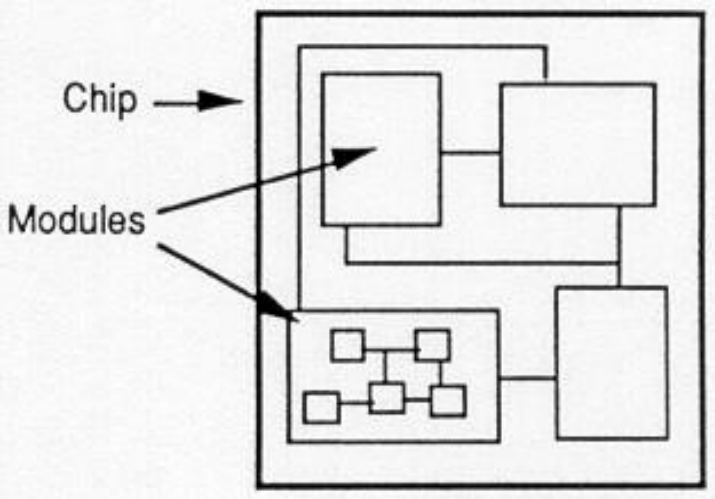
Estimation of Interconnect Parasitics

CHIPs are made of wires called interconnects

- MOS devices are connected by interconnects (Intra Module connection). Relatively large number of local connections between its functional blocks, logic gates, and transistors.
- Interconnects are used for connecting one subsystem to another subsystem sitting on chip.



Estimation of Interconnect Parasitics

- A simple delay models for logic gates with purely capacitive load at the output node was used to estimate the transient behavior
- Determining the Capacitive load is important in estimating transient behavior
- The three main components of the load (assumed to be purely capacitive) are
  1. internal parasitic capacitances of the transistors,
  2. Interconnect (line) capacitances, and
  3. Input capacitances of the fan-out gates.

$$C_{load} = C_{input} + C_{int} + C_g$$

- Among all these , the load conditions **imposed by the interconnection lines present serious problems**.

Estimation of Interconnect Parasitics

- Let us consider an inverter is driving three other inverters, linked over interconnection lines of different length and geometry.

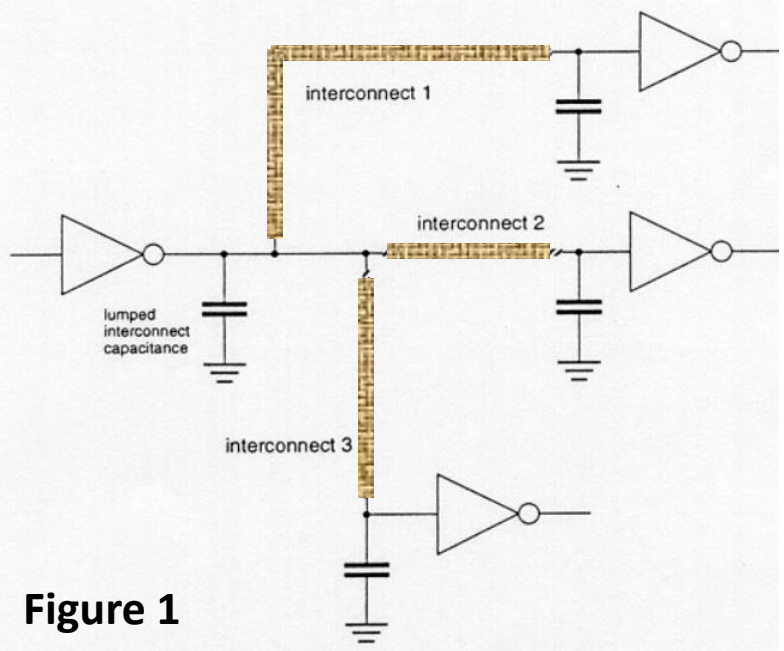


Figure 1

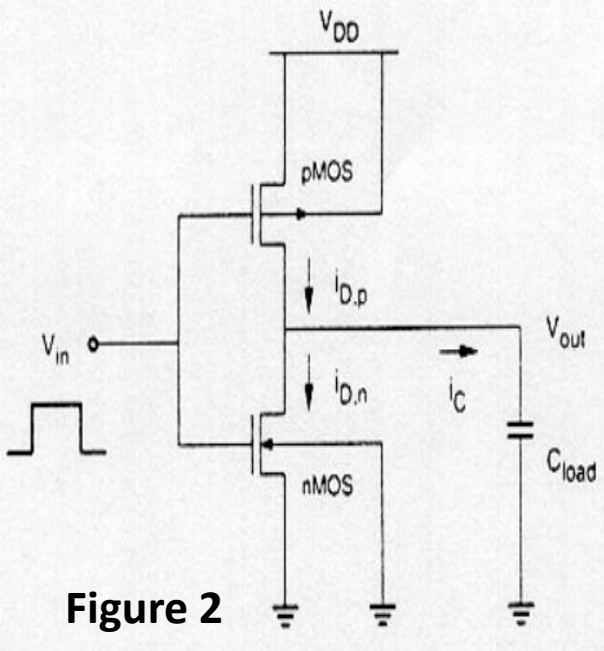
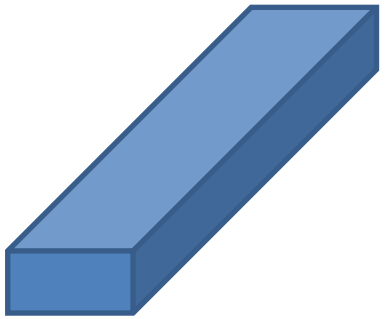


Figure 2



- Let the total load of each interconnection line is approximated by a lumped capacitance, then the total load seen by the primary inverter **is simply the sum of all capacitive components described above** as show in Figure 2.

Estimation of Interconnect Parasitics

- The line, itself a **three-dimensional structure in metal and/or polysilicon**, usually has a **non-negligible resistance** in addition to **its capacitance**. The (length/width) ratio of the wire usually dictates that the parameters are distributed, making the interconnect a true transmission line.

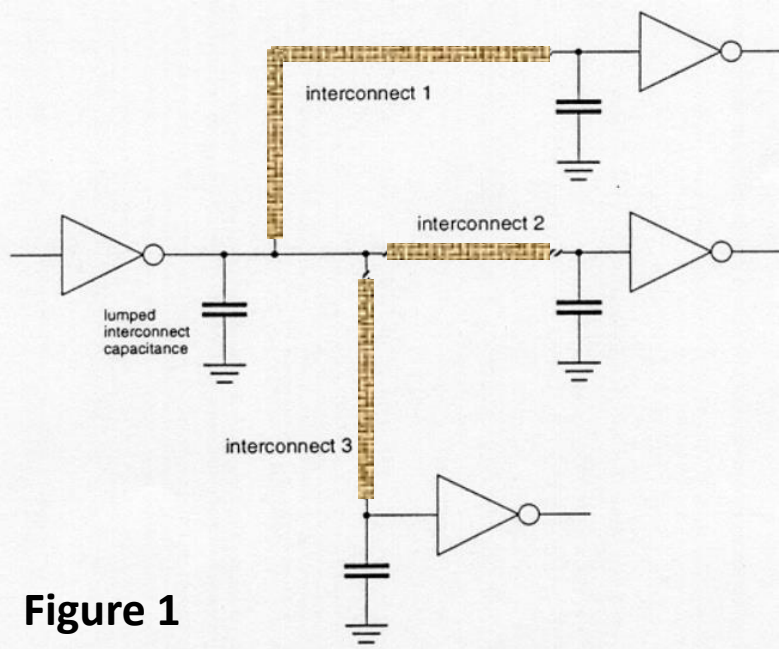
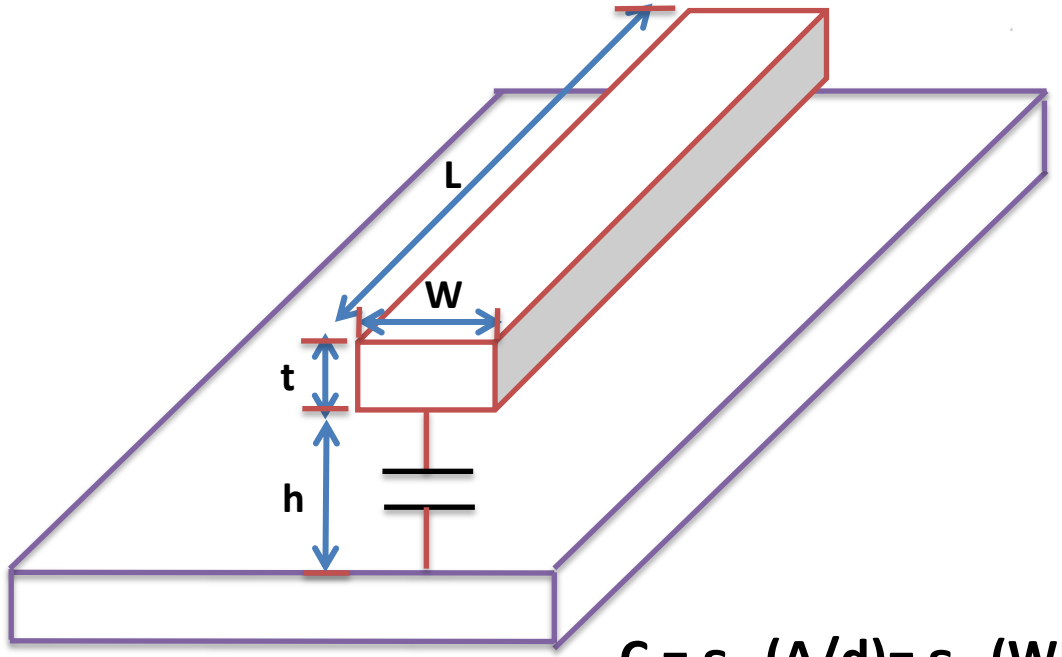


Figure 1

$$R_{wire} = \rho \cdot \frac{l}{w \cdot t} = R_{sheet}\left(\frac{l}{w}\right)$$

$$R_{sheet} = \frac{\rho}{t}$$



$C = \varepsilon_{ox}(A/d) = \varepsilon_{ox}(WL/h)$
$=$Unit Area Capacitance(WxL)

Estimation of Interconnect Parasitics

Time of flight is the measurement of the time taken by an object, particle or wave to travel a distance through a medium.
In VLSI it is time of flight of Signal travelling through Interconnect wire.

- **In general, if the time of flight across the interconnection line (as determined by the speed of light) is shorter than the signal rise/fall times,** then the wire can be modeled as a capacitive load, or as a lumped or distributed RC network.
- If the **interconnection lines are sufficiently long** and the rise times of the signal waveforms are comparable to the time of flight across the line, then the inductance also becomes important, and the interconnection lines must be modeled as transmission lines.

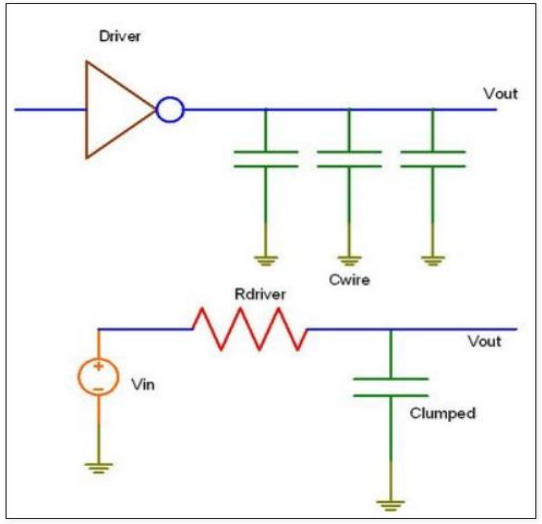
$$C_{line} = Cl \quad R_{line} = Rl \quad L_{line} = Ll$$

Estimation of Interconnect Parasitics

- The **(Length/Width) ratio of the wire usually dictates that the parameters are distributed,** making the interconnect a true transmission line.

Lumped Capacitor Model

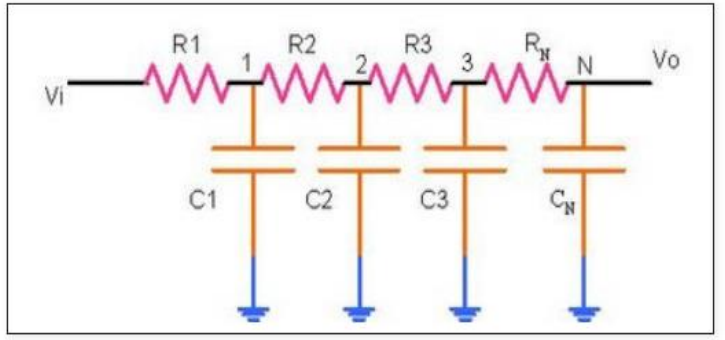
As long as the **resistive component of the wire is small, and switching frequencies are in the low to medium range, it is meaningful to consider only the capacitive component of the wire**, and to lump the distributed capacitance into a single capacitance.



Lumped RC Model

If wire length is more than a few millimeters, the lumped capacitance model is inadequate and a resistive capacitive model has to be adopted.

In lumped RC model the total resistance of each wire segment is lumped into one single R, combines the global capacitive into single capacitor C.



Transmission Line Model

When frequency of operation increases to a larger extent, rise (or fall) time of the signal becomes comparable to time of flight of the net, then inductive effects starts dominating over RC values.

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Estimation of Interconnect Parasitics

- The **different models defined with following conditions**.

$$\tau_{rise}\left(\tau_{fall}\right) < 2.5\times\left(\frac{l}{v}\right) \Rightarrow \{\text{transmission} - \text{line modeling}\}$$

$$2.5\times\left(\frac{l}{v}\right) < \tau_{rise}\left(\tau_{fall}\right) < 5\times\left(\frac{l}{v}\right) \Rightarrow \begin{Bmatrix}\text{either transmission} - \text{line} \\ \text{or lumped modeling}\end{Bmatrix}$$

$$\tau_{rise}\left(\tau_{fall}\right) > 5\times\left(\frac{l}{v}\right) \Rightarrow \{\text{lumped modeling}\}$$

l is the interconnect line length, and v is the propagation speed.

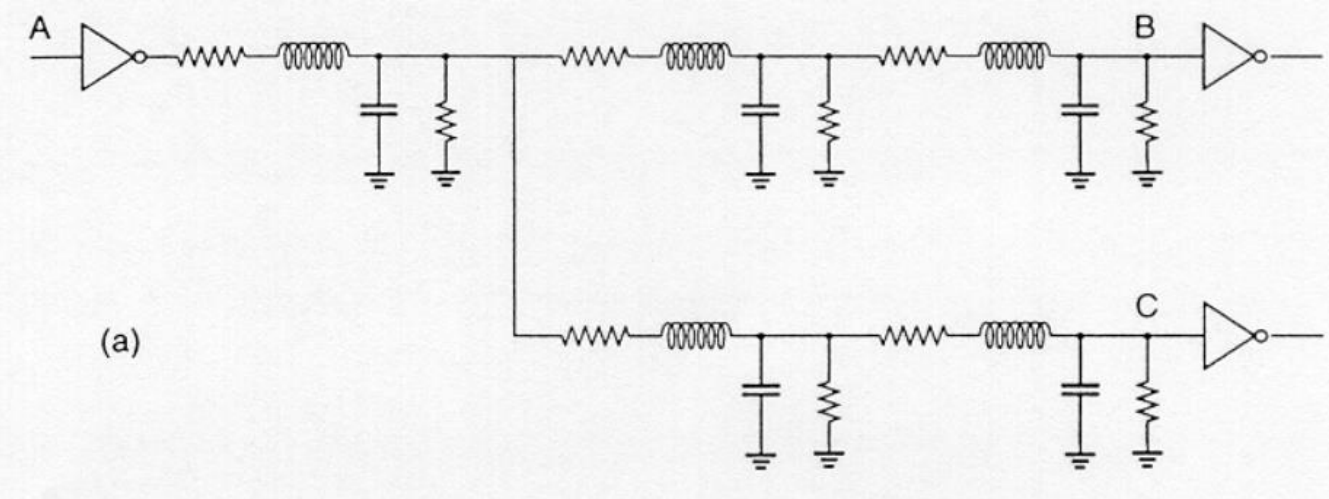
For example, **The longest wire on a VLSI chip may be about 2 cm. The time of flight of a signal across this wire is approximately 133 ps, which is shorter than typical on-chip signal rise/fall times.** Thus, either lumped capacitive or RC model is adequate for the wire.

On the other hand, **the time of flight across a 10 cm multichip module (MCM) interconnect in an alumina substrate.is approximately 1 ns,** which is of the **same order of magnitude as the rise times of signals generated by some drivers**. In this case, the interconnection lines should be **modeled by taking into consideration the RLCG**

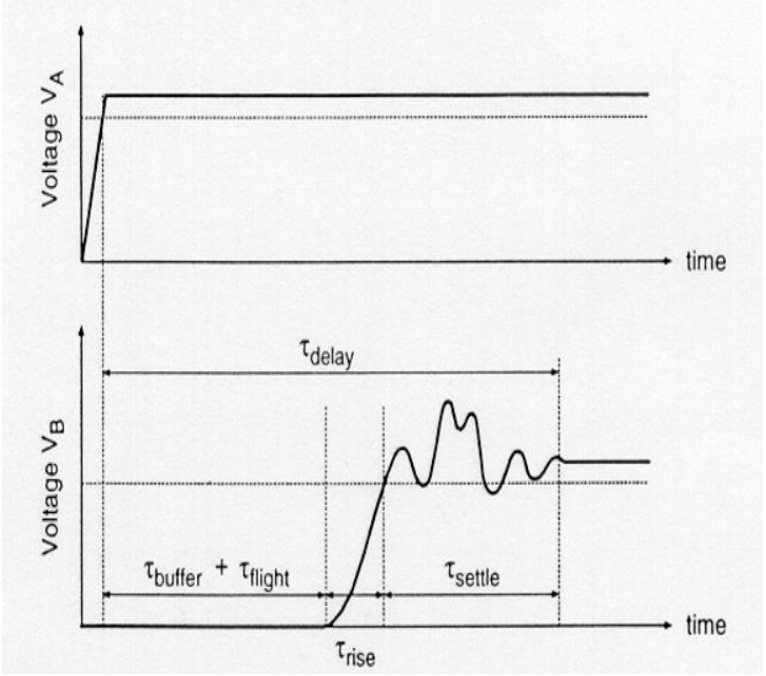
Estimation of Interconnect Parasitic

The Reality with Interconnections

Let us consider an inverter is driving two other inverters, over long interconnection lines.



Taking into consideration the RLCG (resistance, inductance, capacitance, and conductance) parasitic, the signal transmission across the wire becomes a very complicated matter, compared to the relatively simplistic lumped- load case.

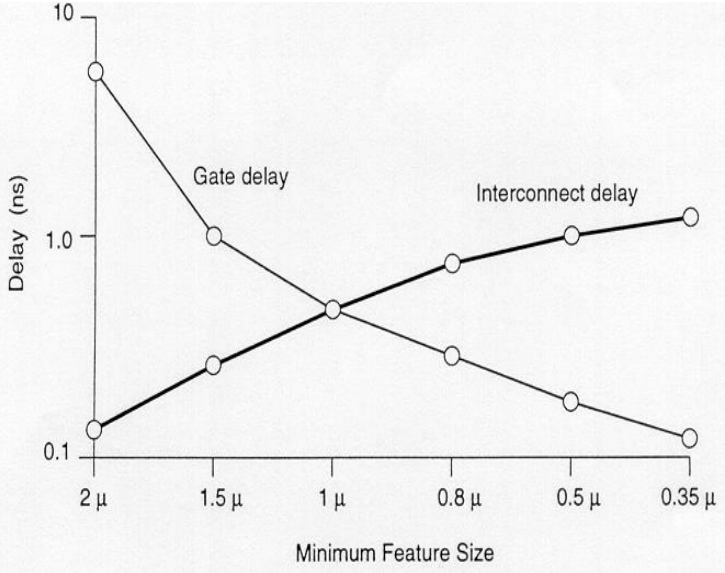


Typical signal waveforms at the nodes A and B, showing the signal delay and the various delay components.

Estimation of Interconnect Parasitic

The Reality with Interconnections

- The interconnect delay are plotted qualitatively, for different technologies.
- From the graph it is clear that for sub-micron technologies, **the interconnect delay starts to dominate the gate delay.**
- In order to deal with the implications and to optimize a system for speed, the designers must have reliable and efficient means of
  - **(1) Estimating the interconnect parasitics in a large chip**, and
  - (2) Simulating the time- domain effects.
- Neither of these tasks is simple – these tow tasks are the most difficult problems in physical design of VLSI circuits today.



Estimation of Interconnect Parasitic

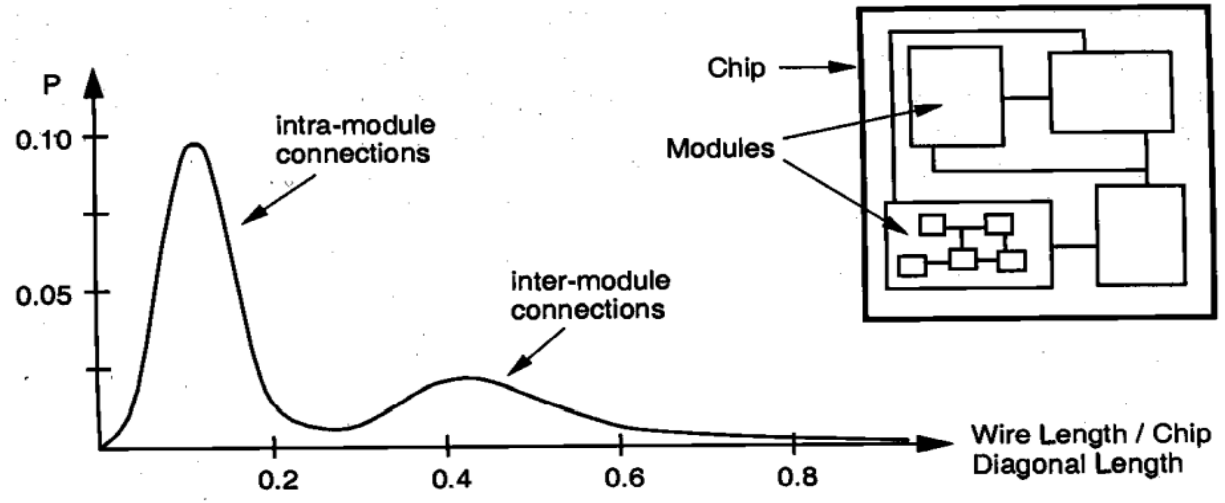
Statistical distribution of interconnection length on a typical chip

Intra Module connection and Delays

- In a chip consisting of several functional modules, each module contains a relatively large number of local connections between its functional blocks, logic gates, and transistors.
- The intra-module connections are usually made over short distances, their influence on speed can be simulated easily with conventional models.

Inter Module connection and Delays

- The Inter Module connections have fairly longer connections.
- It is usually these inter-module connections which should be scrutinized in the early design phases for possible timing problems.



Estimation of Interconnect Parasitic

Statistical distribution of interconnection length on a typical chip

To summarize, we state that :

1. Interconnection delay is becoming the **dominating factor which determines the dynamic performance** of large-scale systems, and
2. **Interconnect parasitics are difficult to model and to simulate**.

Therefore. It becomes important to understand various aspects of on-chip parasitics like capacitive and resistive components.

THANK YOU

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