DIGITAL VLSI DESIGN

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Unit 2: Fabrication of MOSFETs & Circuit Design Process

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Layout Design Rules

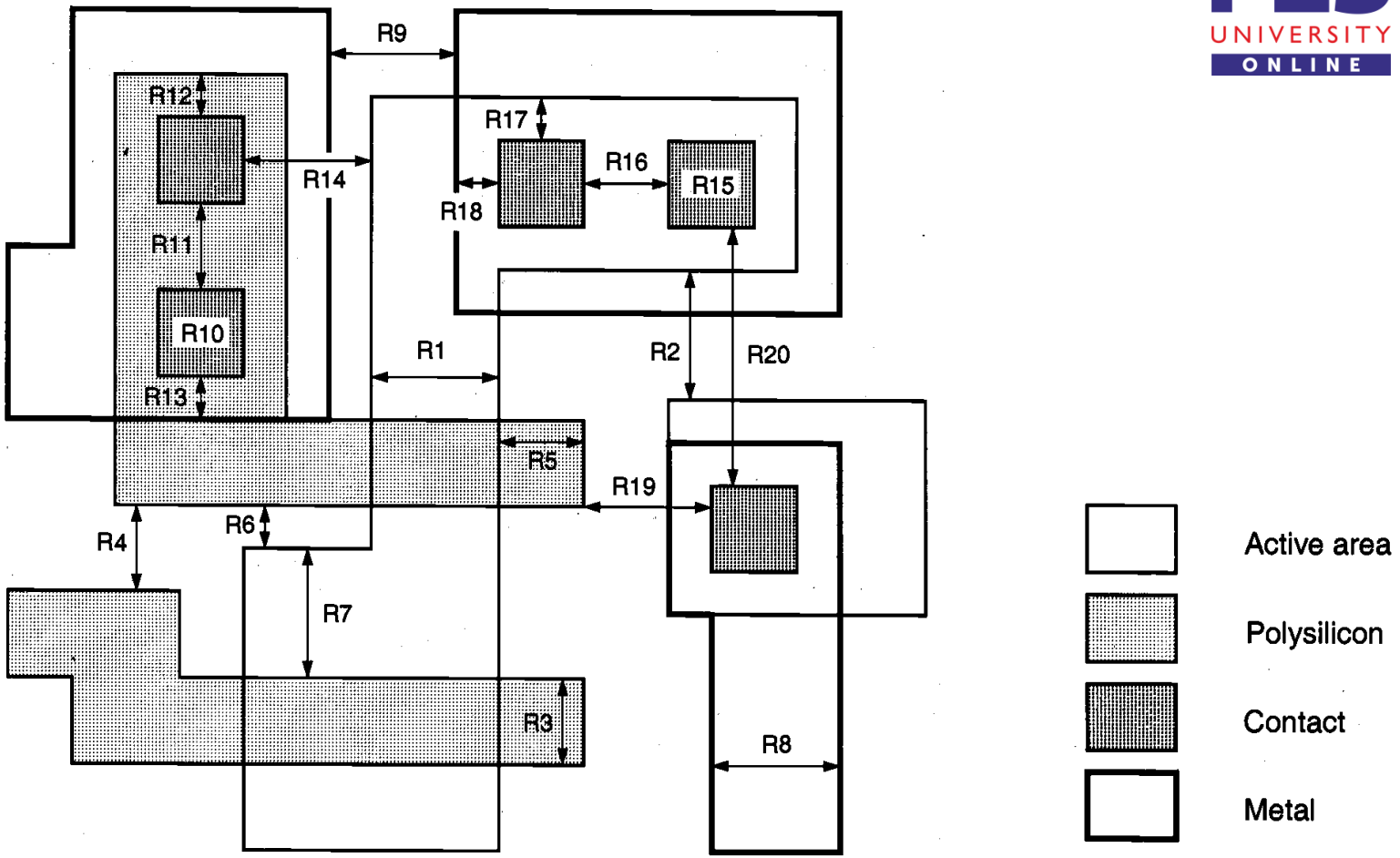
- To allow reliable fabrication of each structure, the mask layers must conform to a set of geometric layout design rules.
- Usually, the rules (for example: minimum distance and/or separation between layers) are expressed as multiples of a scaling factor – lambda (λ).
- For each different fabrication technology, lambda factor can be different.

Layout Design Rules

MOSIS Layout Design Rules (sample set)

Rule number	*Description*	*λ-Rule*
	Active area rules	
R1	Minimum active area width	3λ
R2	Minimum active area spacing	3λ
	Polysilicon rules	
R3	Minimum poly width	2λ
R4	Minimum poly spacing	2λ
R5	Minimum gate extension of poly over active	2λ
R6	Minimum poly-active edge spacing (poly outside active area)	1λ
R7	Minimum poly-active edge spacing (poly inside active area)	3λ
	Metal rules	
R8	Minimum metal width	3λ
R9	Minimum metal spacing	3λ
	Contact rules	
R10	Poly contact size	2λ
R11	Minimum poly contact spacing	2λ
R12	Minimum poly contact to poly edge spacing	1λ
R13	Minimum poly contact to metal edge spacing	1λ
R14	Minimum poly contact to active edge spacing	3λ
R15	Active contact size	2λ
R16	Minimum active contact spacing (on the same active region)	2λ
R17	Minimum active contact to active edge spacing	1λ
R18	Minimum active contact to metal edge spacing	1λ
R19	Minimum active contact to poly edge spacing	3λ
R20	Minimum active contact spacing (on different active regions)	6λ

Illustration of some of the typical MOSIS (MOS Implementation System) layout design rules



THANK YOU

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