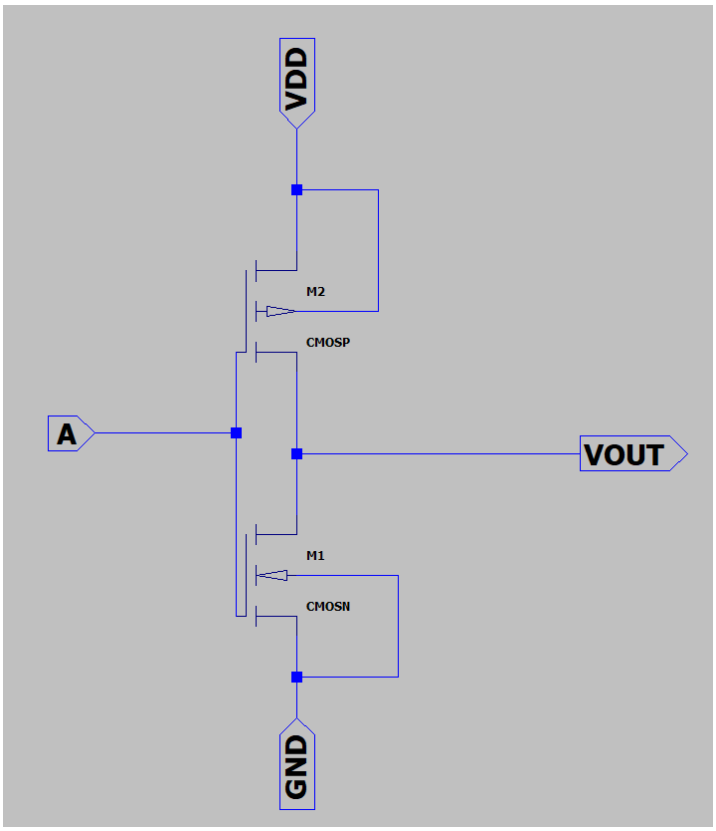
DVLSI PROJECT 2

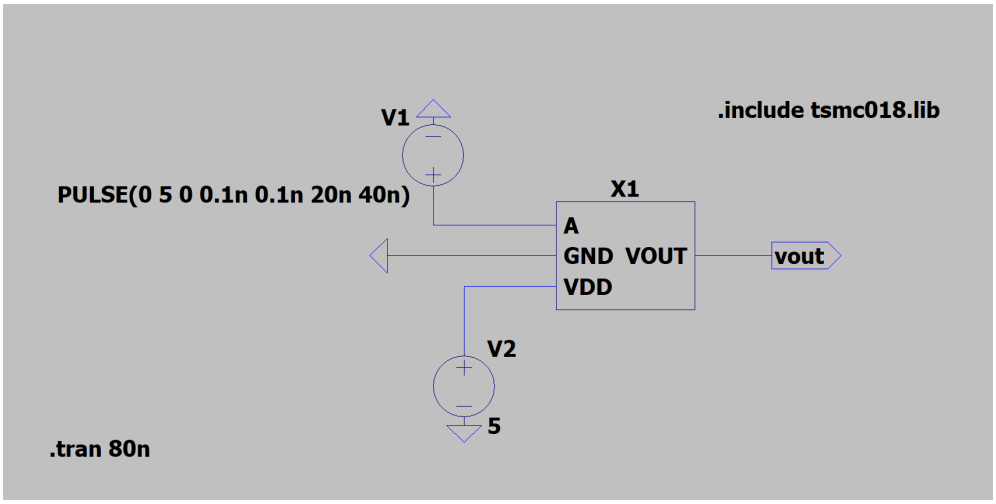
28.03.2022

Jacob V Sanoj
PES1UG20EC083

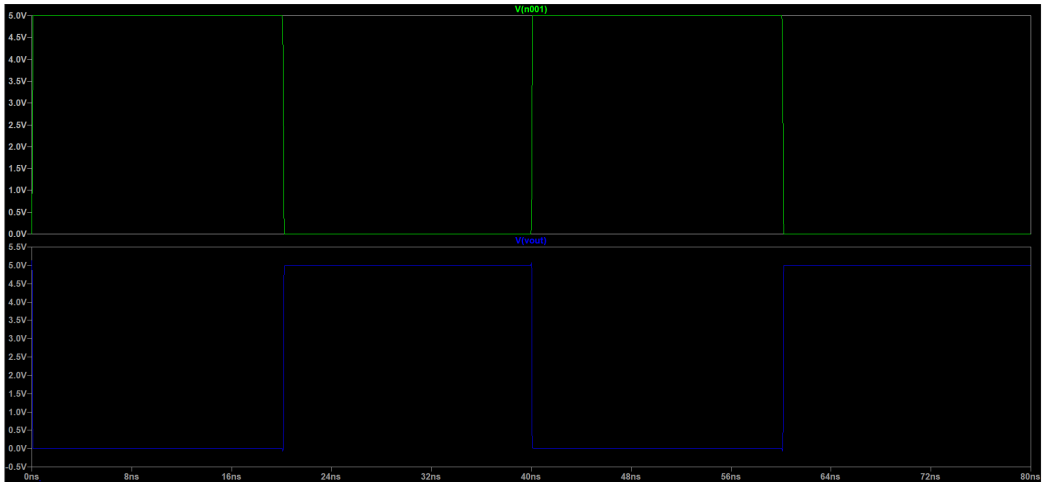
Content

Inverter

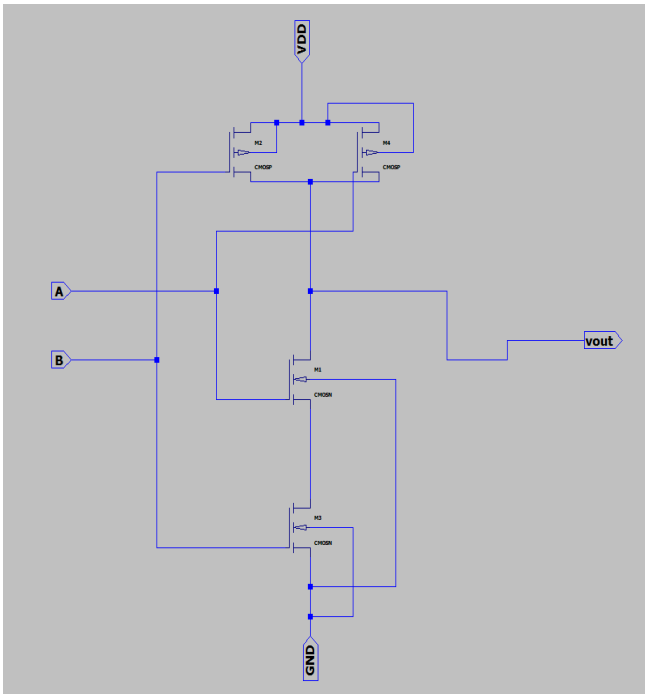


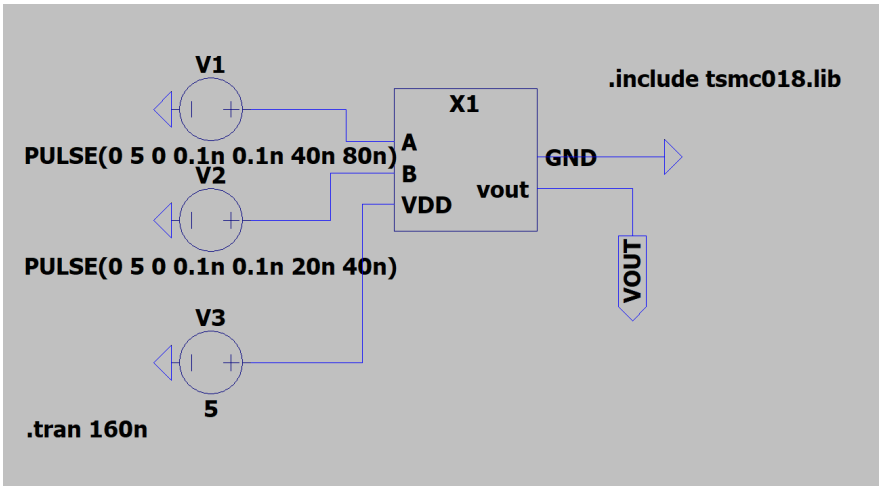

V1
.include tsmc018.lib
PULSE(0 5 0 0.1n 0.1n 20n 40n)
X1
A
GND VOUT
VDD
vout
V2
5
.tran 80n

Test Bench

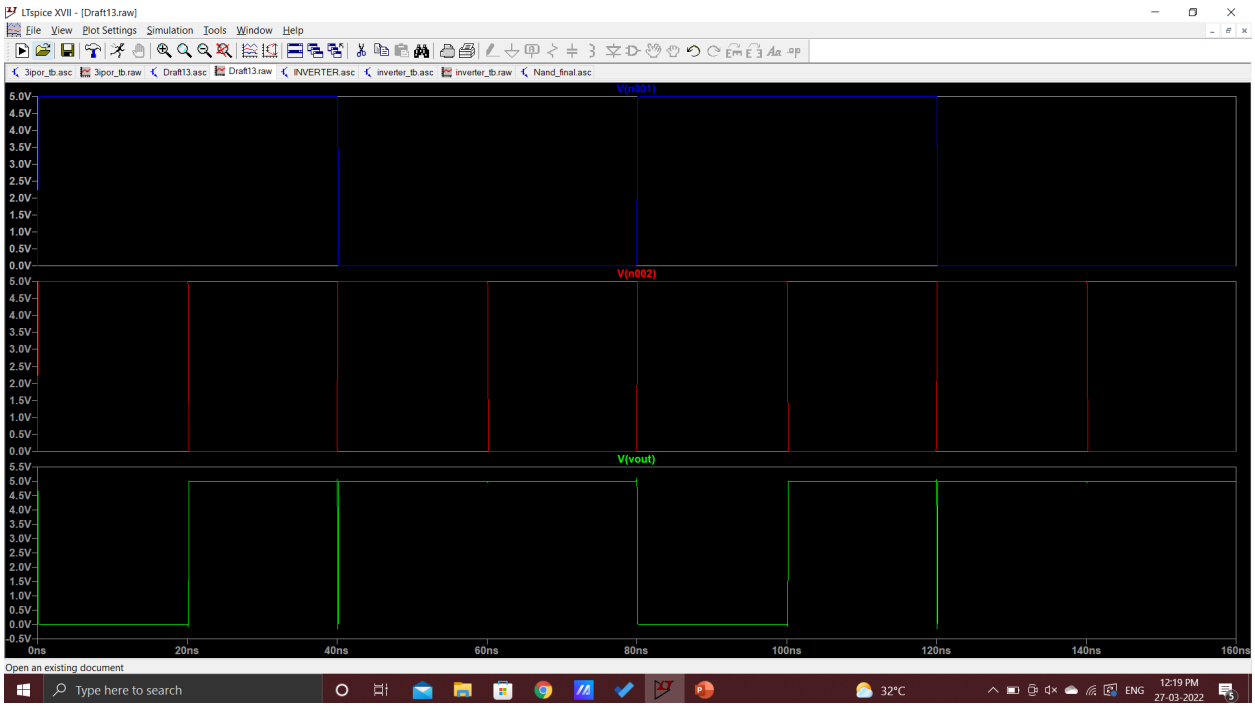

V(n001)
V(vout)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
-0.5V
0ns
8ns
16ns
24ns
32ns
40ns
48ns
56ns
64ns
72ns
80ns

NAND Gate

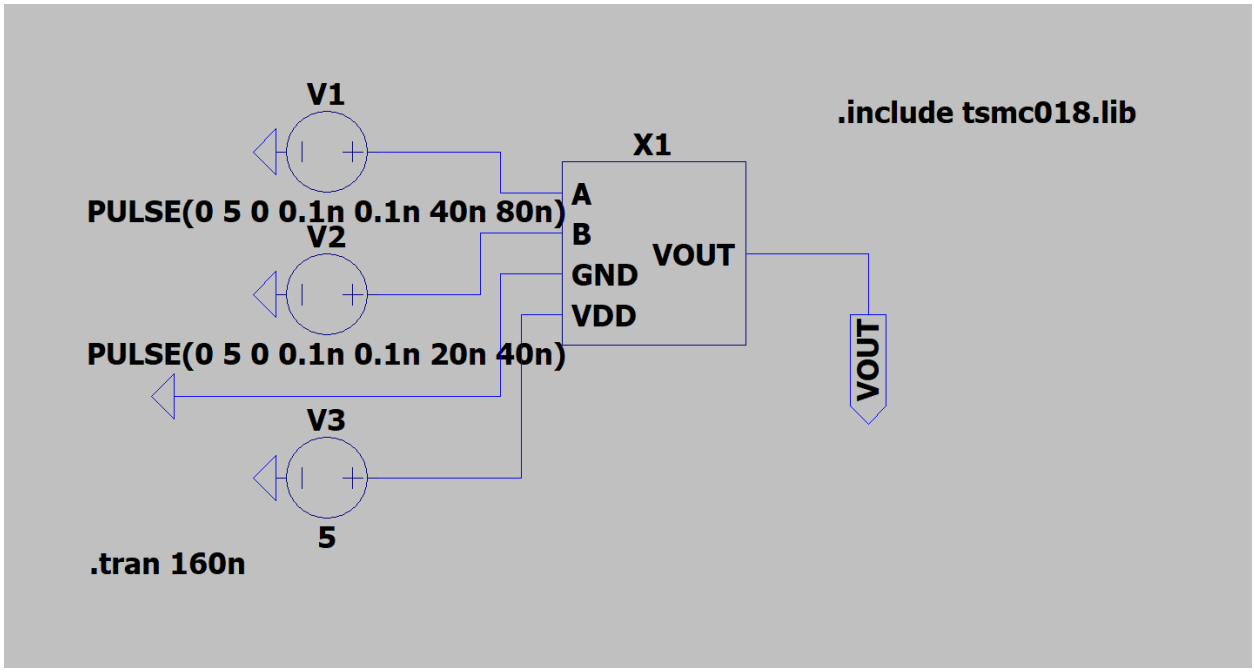

VDD
M2
M4
CMOSP
CMOSP
A
B
vout
M1
CMOSN
M3
CMOSN
GND

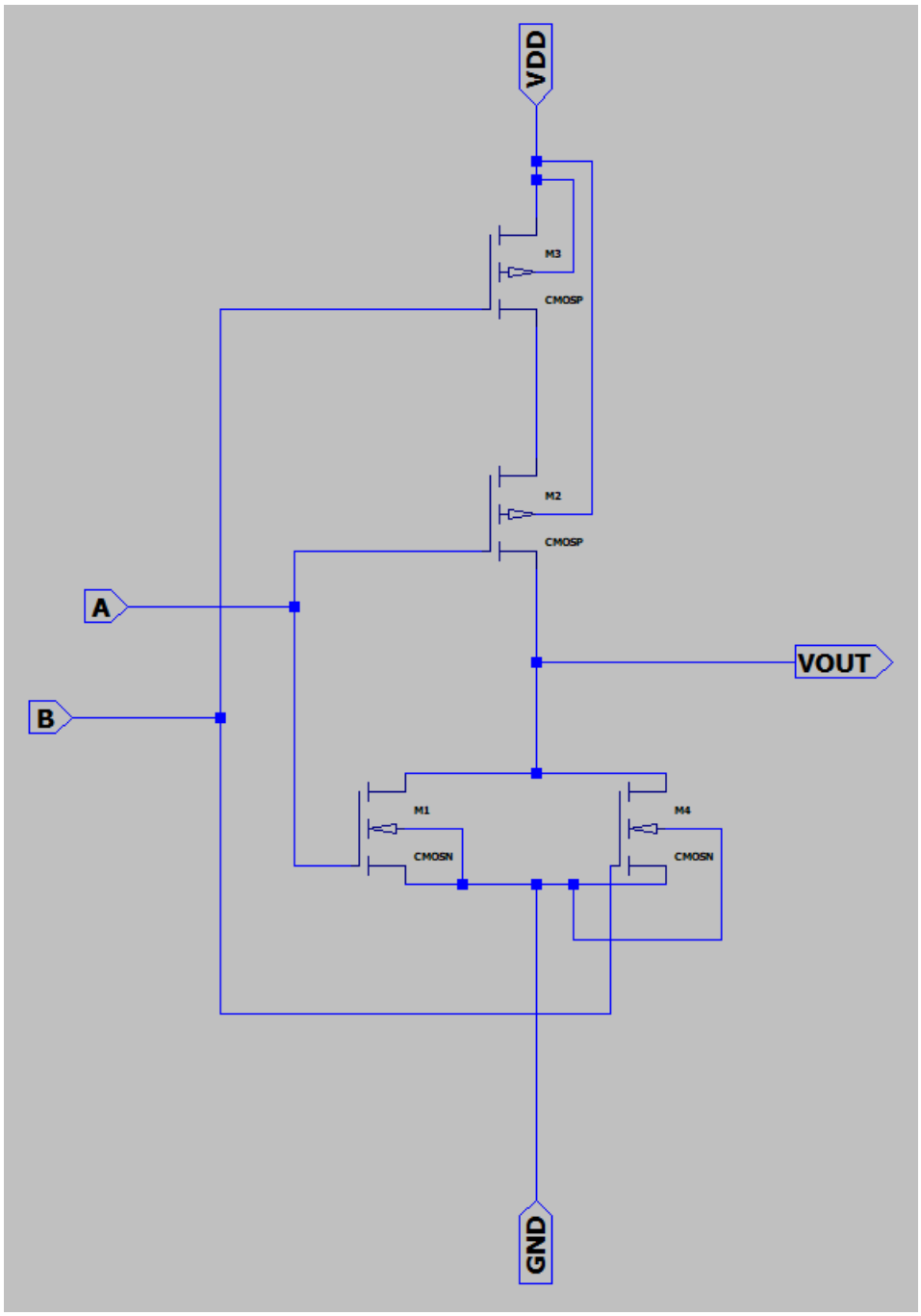

V1
PULSE(0 5 0 0.1n 0.1n 40n 80n)
V2
PULSE(0 5 0 0.1n 0.1n 20n 40n)
V3
5
.tran 160n
X1
A
B
VDD
GND
vout
VOUT
.include tsmc018.lib

Test Bench

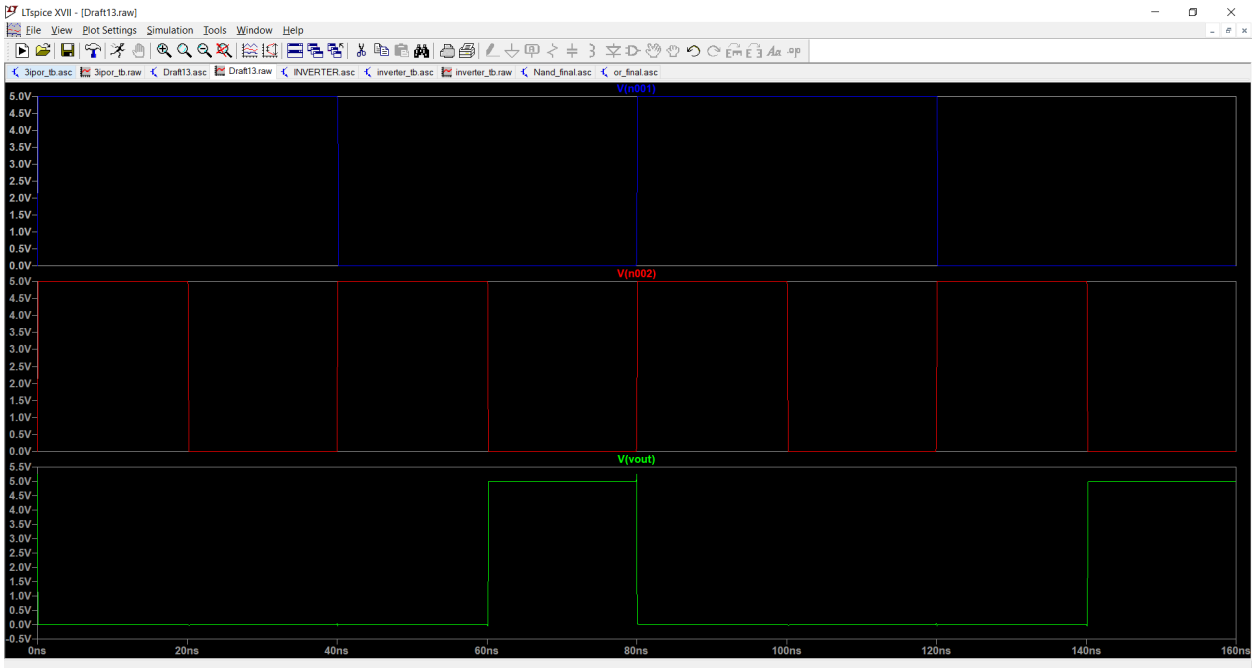


OR Gate

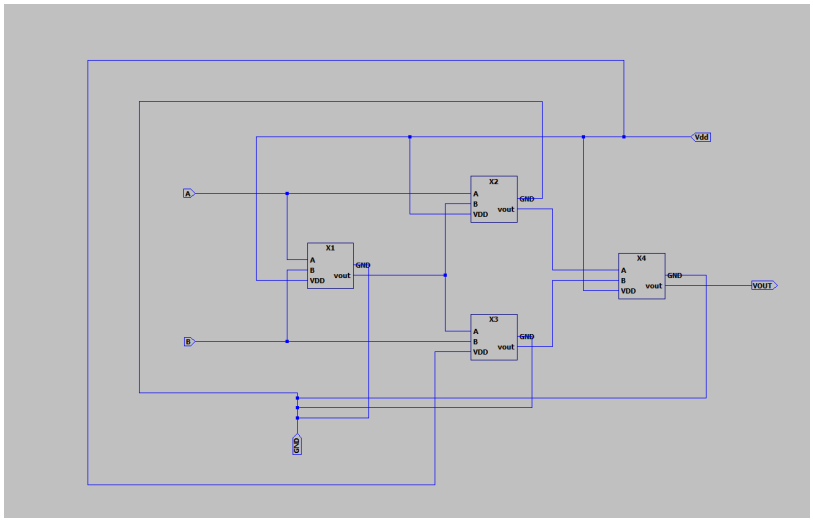


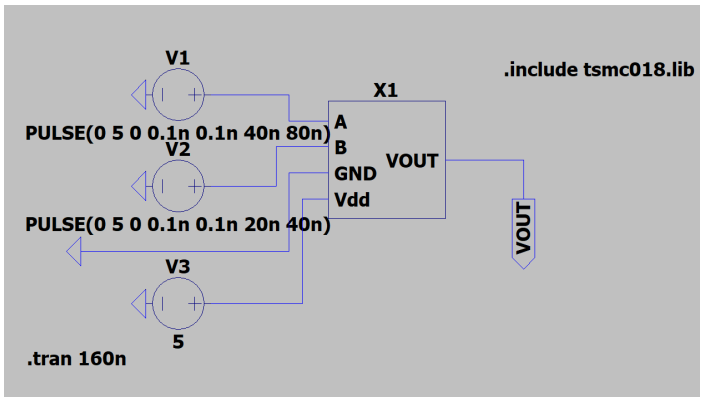

VDD
M3
CMOSP
M2
CMOSP
A
VOUT
B
M1
CMOSN
M4
CMOSN
GND

Testbench

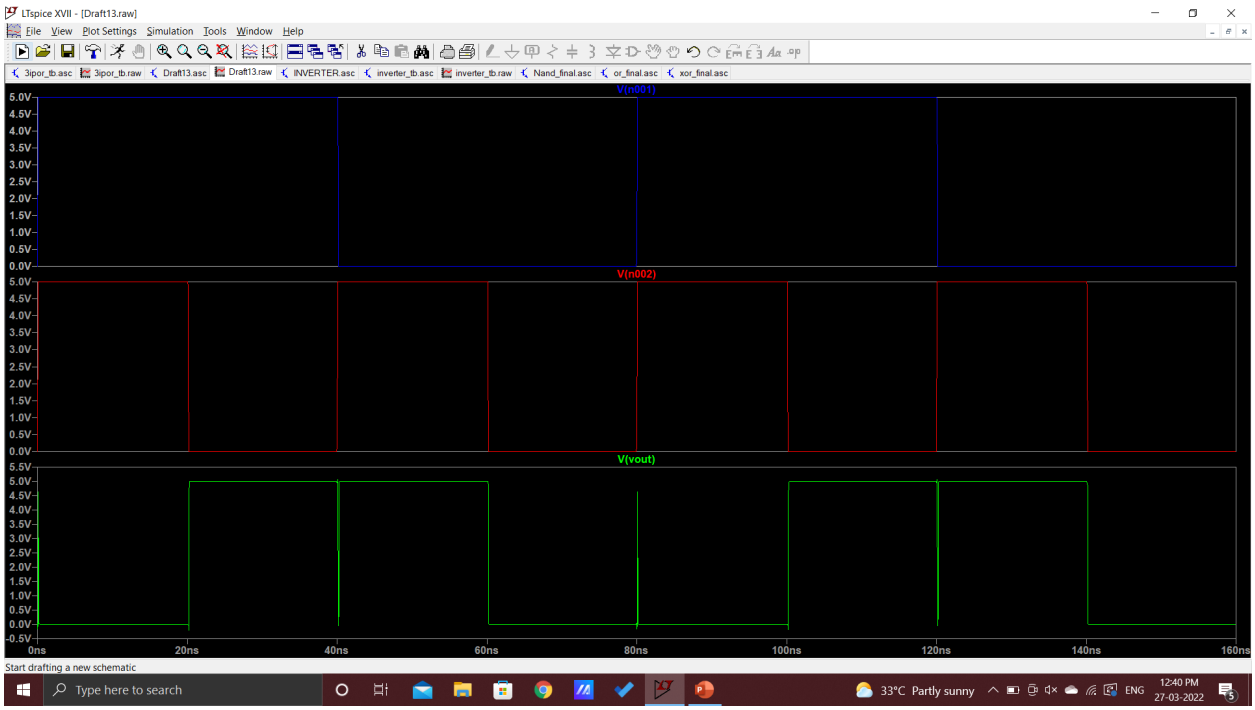


XOR Gate

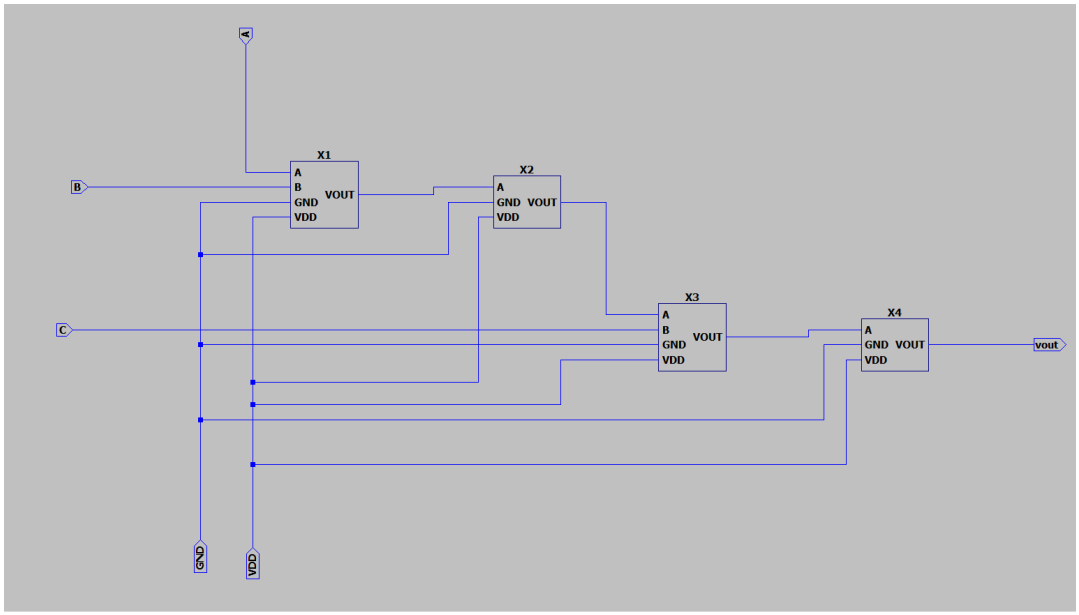


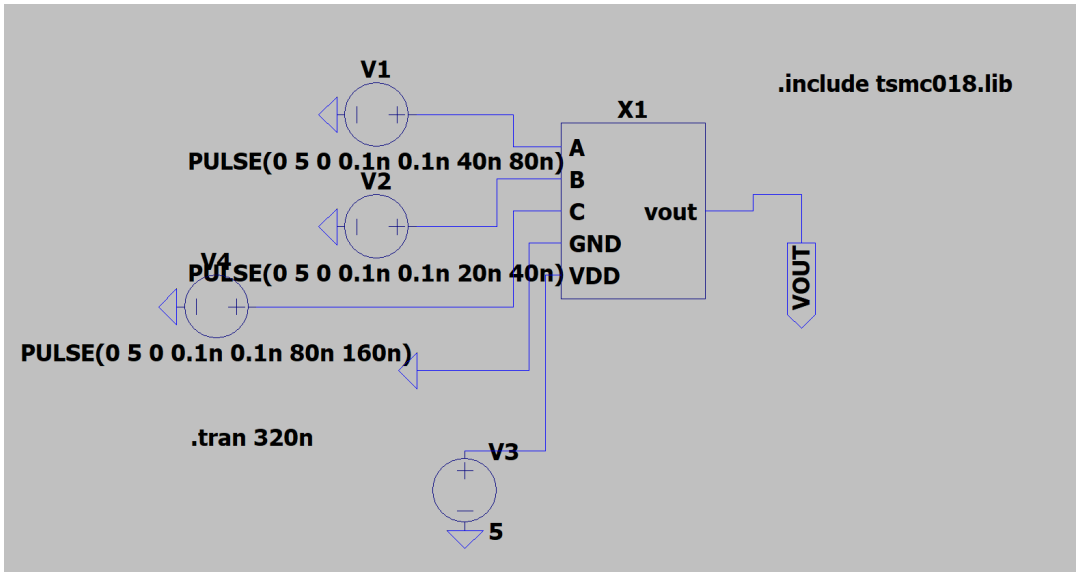

V1
PULSE(0 5 0 0.1n 0.1n 40n 80n)
V2
PULSE(0 5 0 0.1n 0.1n 20n 40n)
V3
5
.tran 160n
X1
A
B
GND
Vdd
VOUT
VOUT
.include tsmc018.lib

Testbench

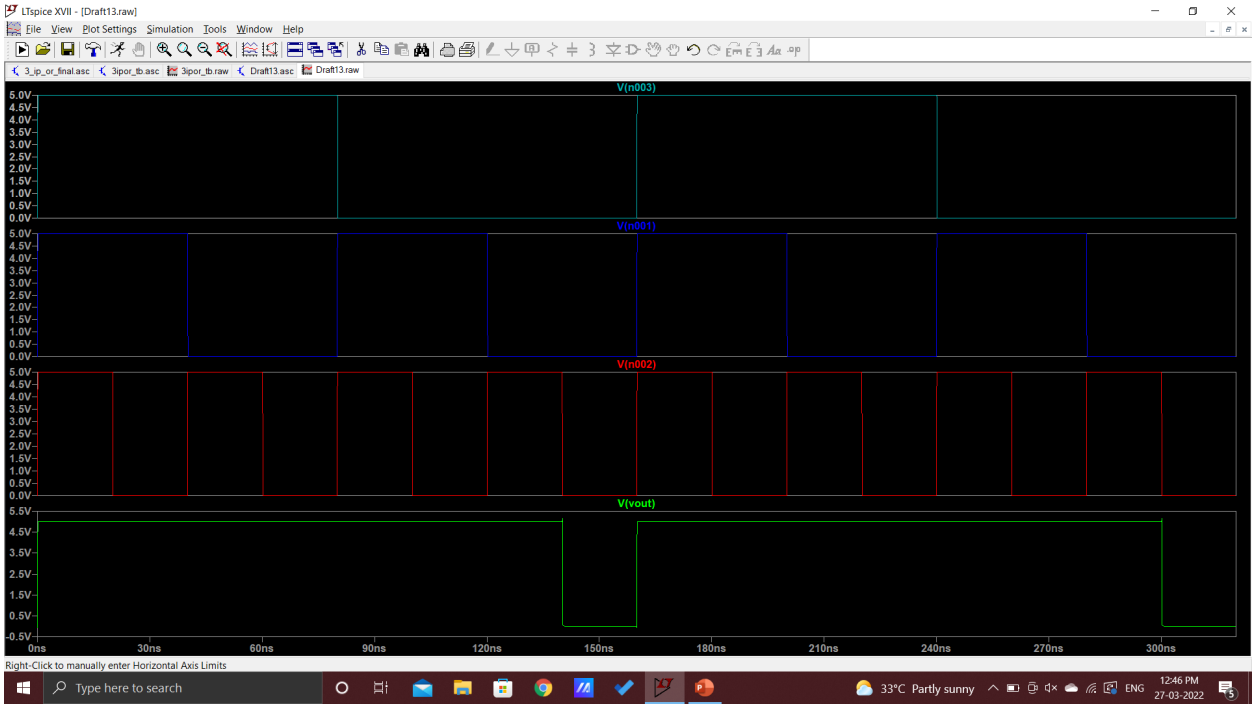

LTspice XVII - [Draft13.raw]
File View Plot Settings Simulation Tools Window Help
V(n001)
V(n002)
V(vout)
0ns 20ns 40ns 60ns 80ns 100ns 120ns 140ns 160ns
Start drafting a new schematic
Type here to search
33°C Partly sunny
ENG
12:40 PM
27-03-2022

3-Input OR Gate

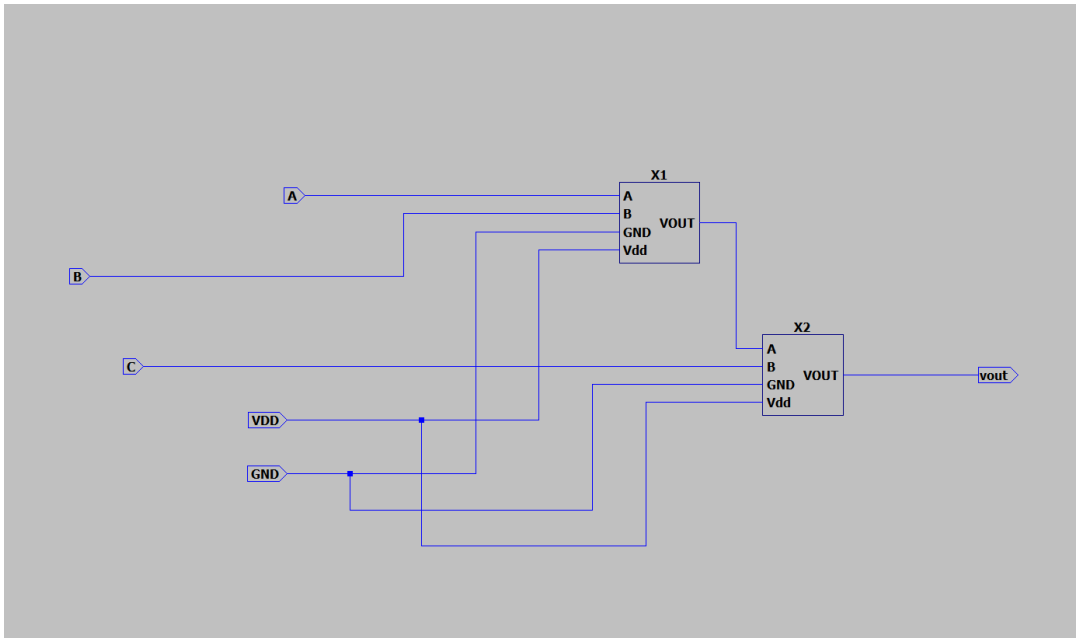


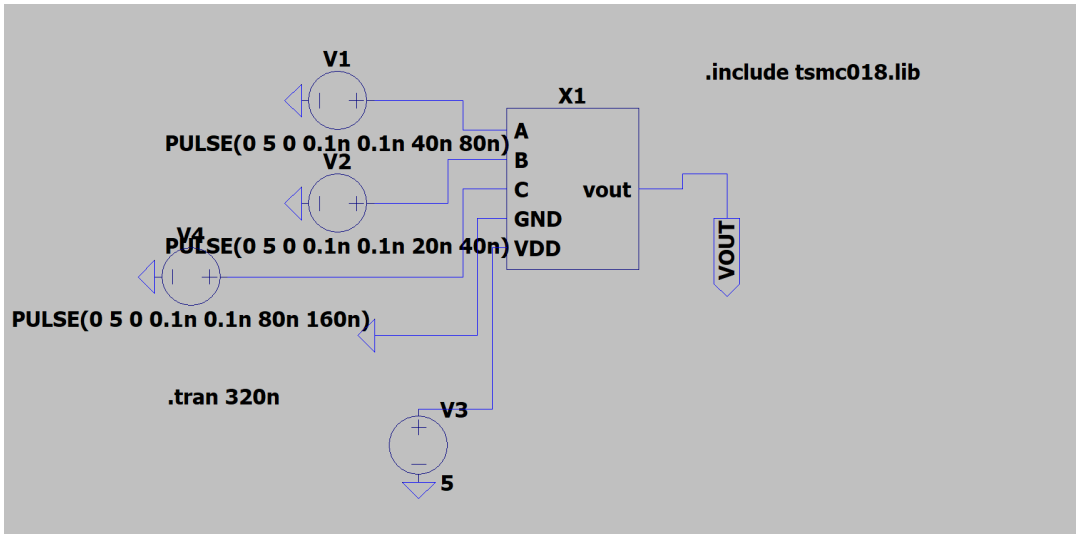


Testbench

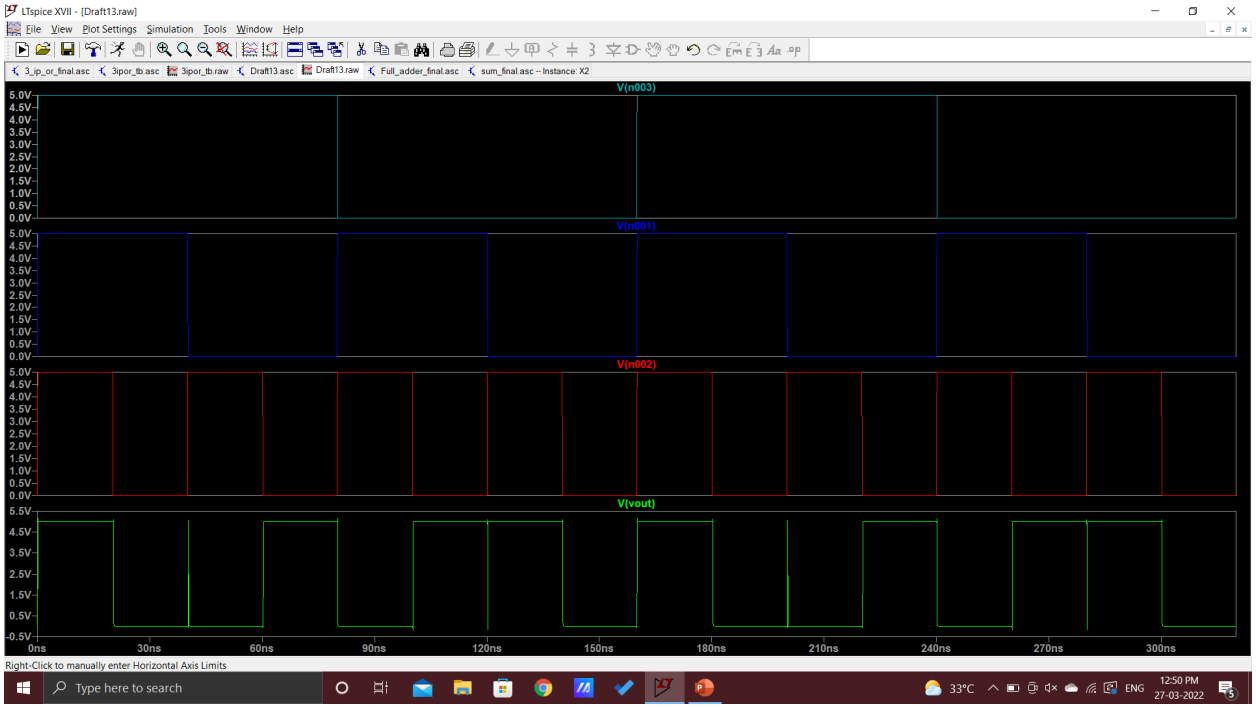

LTspice XVII - [Draft13.raw]
File View Plot Settings Simulation Tools Window Help
3_ip_or_final.asc 3ipor_tb.asc 3ipor_tb.raw Draft13.asc Draft13.raw
V(n003)
V(n001)
V(n002)
V(vout)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
-0.5V
0ns 30ns 60ns 90ns 120ns 150ns 180ns 210ns 240ns 270ns 300ns
Right-Click to manually enter Horizontal Axis Limits
Type here to search
33°C Partly sunny
ENG
12:46 PM
27-03-2022

3-Input XOR Gate

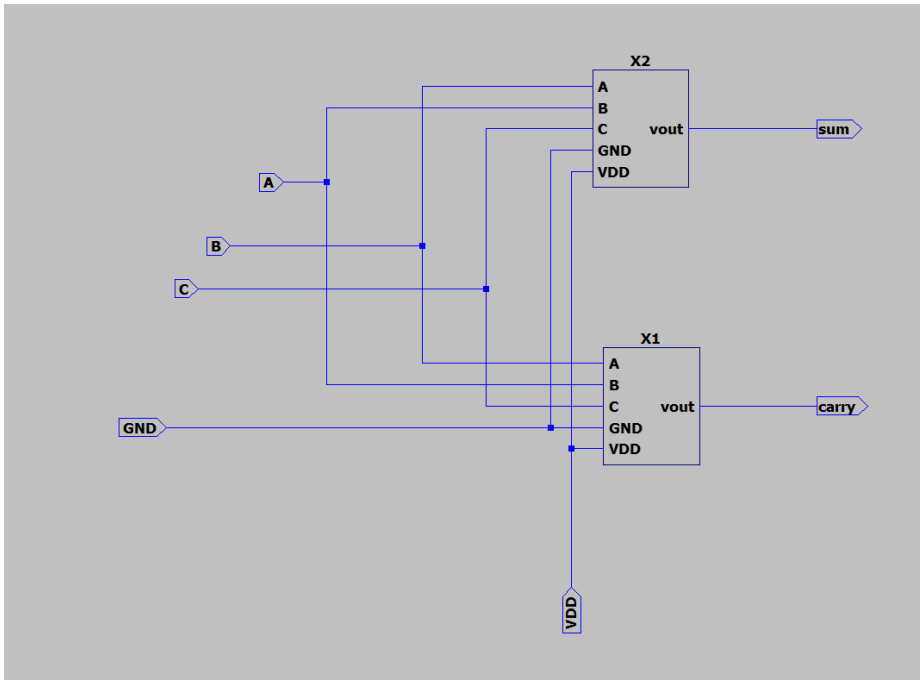


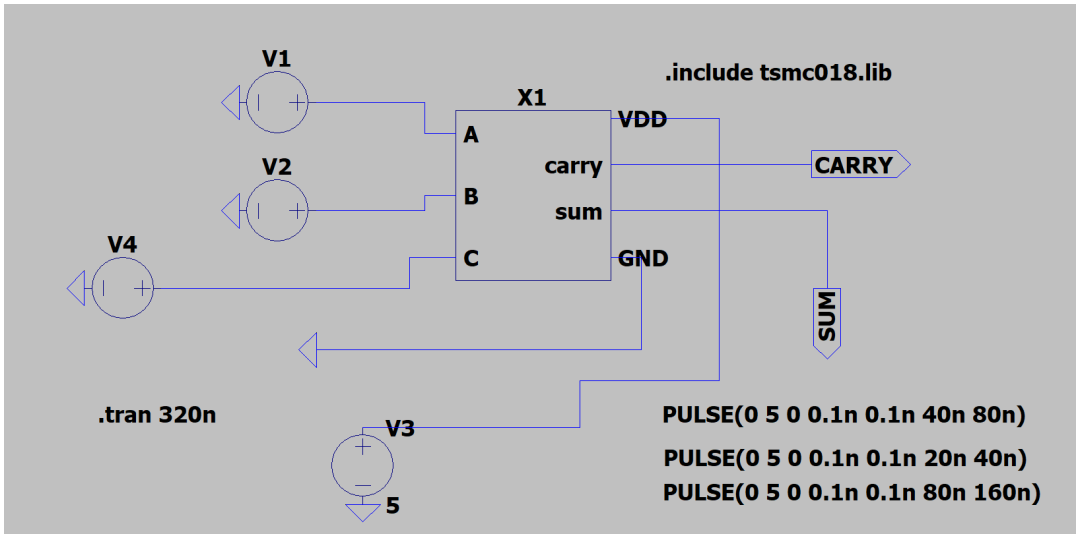


Testbench

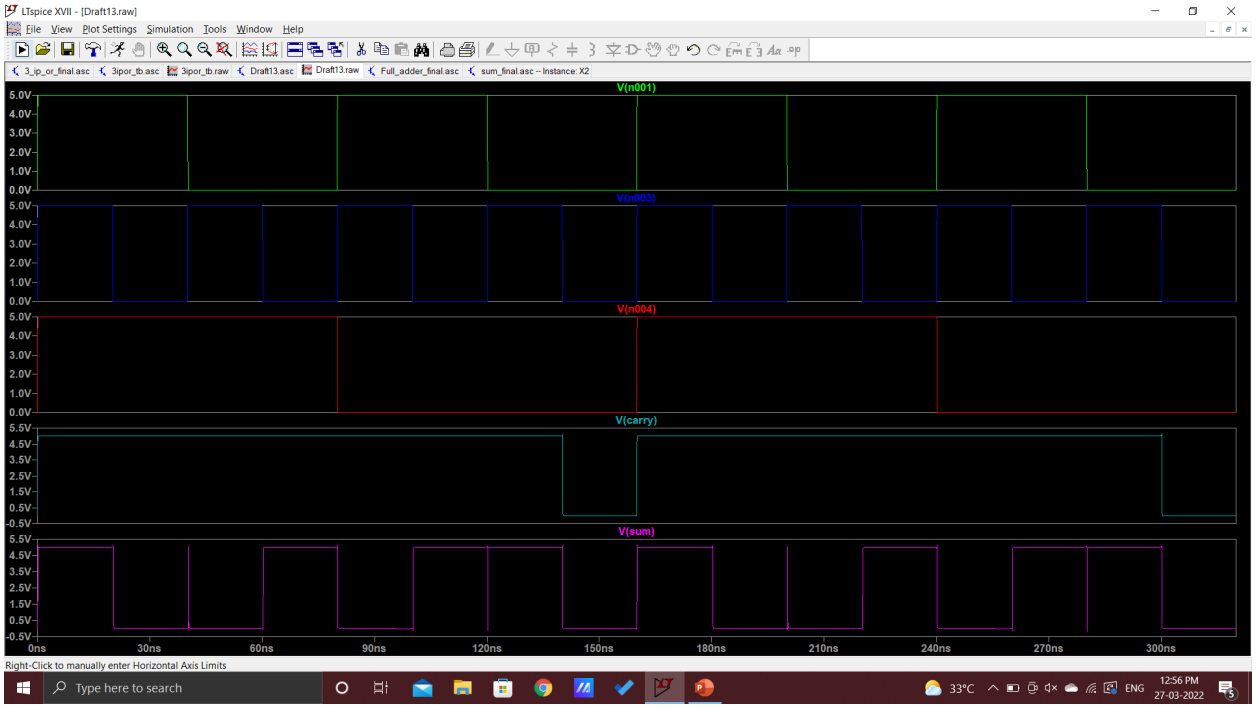

LTspice XVII - [Draft13.raw]
File View Plot Settings Simulation Tools Window Help
3_ip_or_final.asc 3ipor_tb.asc 3ipor_tb.raw Draft13.asc Draft13.raw Full_adder_final.asc sum_final.asc -- Instance: X2
V(n003)
V(n001)
V(n002)
V(vout)
0ns 30ns 60ns 90ns 120ns 150ns 180ns 210ns 240ns 270ns 300ns
Right-Click to manually enter Horizontal Axis Limits
Type here to search
33°C
ENG
12:50 PM
27-03-2022

Full Adder

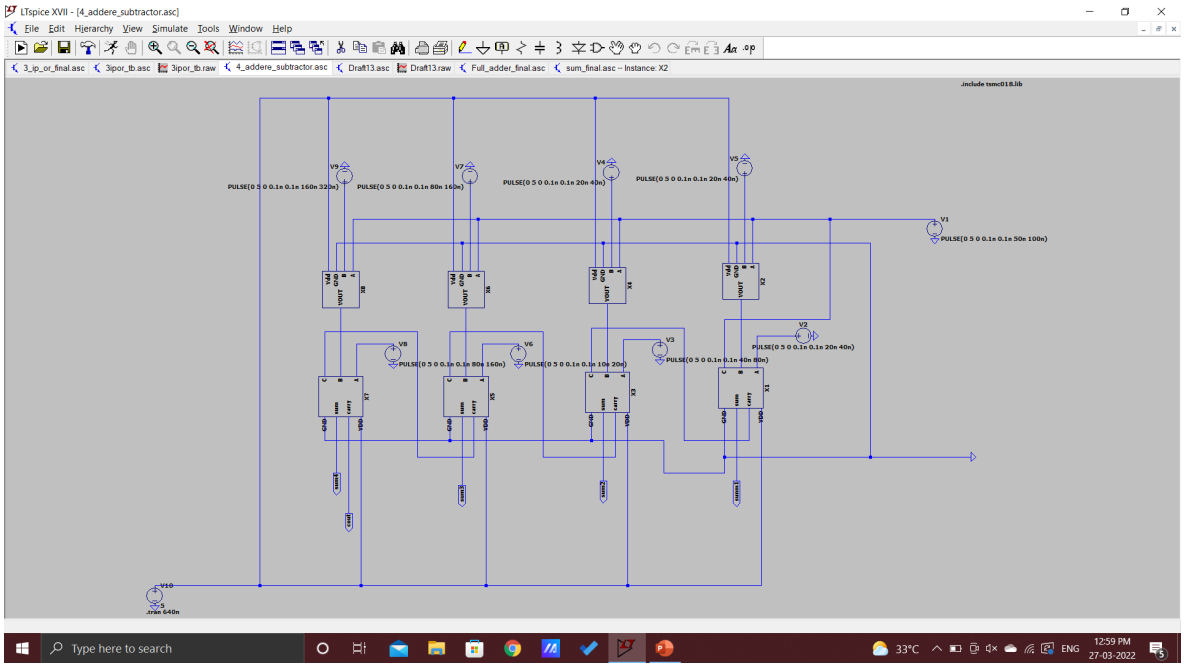

X2
A
B
C
GND
VDD
vout
sum
A
B
C
X1
A
B
C
GND
VDD
vout
carry
GND
VDD


V1
V2
V4
X1
A
B
C
VDD
carry
sum
GND
CARRY
SUM
.include tsmc018.lib
.tran 320n
V3
5
PULSE(0 5 0 0.1n 0.1n 40n 80n)
PULSE(0 5 0 0.1n 0.1n 20n 40n)
PULSE(0 5 0 0.1n 0.1n 80n 160n)

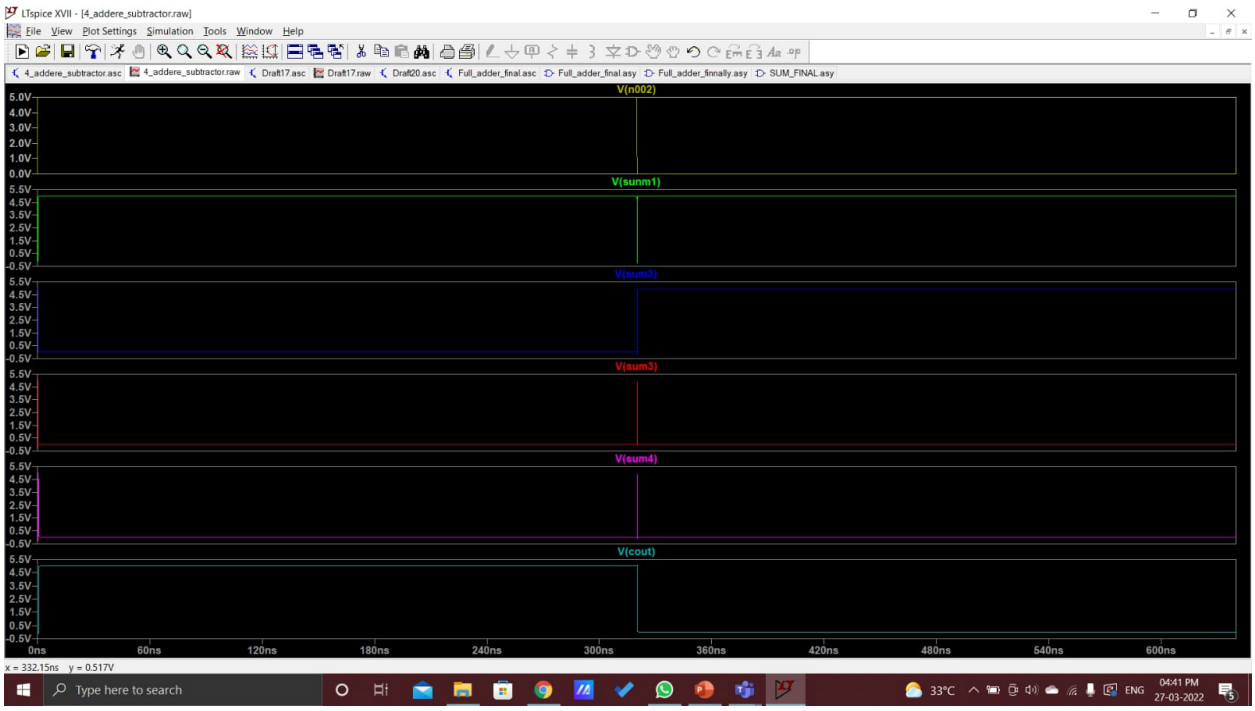
Testbench



4-bit Adder



Testbench


LTspice XVII - [4_addere_subtractor.raw]
File View Plot Settings Simulation Tools Window Help
4_addere_subtractor.asc
4_addere_subtractor.raw
Draft17.asc
Draft17.raw
Draft20.asc
Full_adder_final.asc
Full_adder_final.asy
Full_adder_finnally.asy
SUM_FINAL.asy
V(n002)
V(sunm1)
V(sum2)
V(sum3)
V(sum4)
V(cout)
0ns
60ns
120ns
180ns
240ns
300ns
360ns
420ns
480ns
540ns
600ns
x = 332.15ns y = 0.517V
Type here to search
33°C
ENG
04:41 PM
27-03-2022