

## **RISC V Architecture**

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#### RISC V ARCHITECTURE

# **UNIT 4: Arithmetic for Computers**

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#### **Multiplication:**



Similar to multiplication of decimal numbers in longhand method.

Example: Multiply 1000ten by 1001ten:

Multiplicand  
Multiplier
$$1000_{\text{ten}}$$
  
 $1000_{\text{ten}}$  $1000_{\text{ten}}$  $1000_{\text{ten}}$  $0000_{\text{ten}}$  $1000_{\text{ten}}$ Product $1001000_{\text{ten}}$ 



Ignore the sign bits, the length of the multiplication of an n-bit multiplicand and an m-bit multiplier is a product that is n + m bits long.

n + m bits are required to represent all possible products

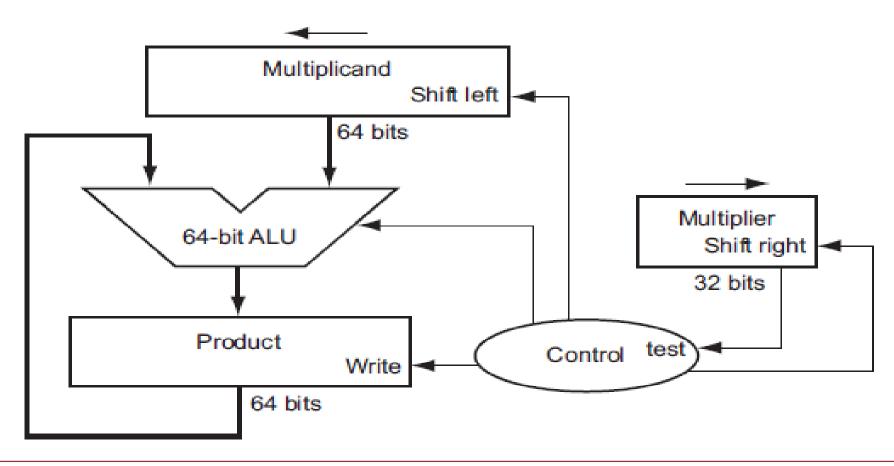
#### Steps:

- 1. Just place a copy of the multiplicand ( $1 \times \text{multiplicand}$ ) in the proper place if the multiplier digit is a 1, or
- 2. Place 0 (0  $\times$  multiplicand) in the proper place if the digit is 0.

**Unit 4: Arithmetic for Computers** 

#### Sequential Version of the Multiplication Algorithm and Hardware







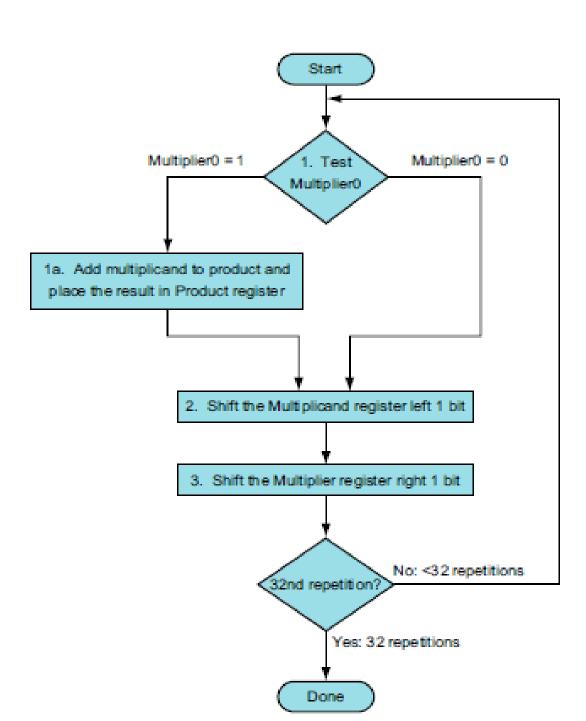
- •The Multiplicand register, ALU, and Product register are all 64 bits wide, with only the Multiplier register containing 32 bits.
- •The 32-bit multiplicand starts in the right half of the Multiplicand register and is shifted left 1 bit on each step.
- •The multiplier is shifted in the opposite direction at each step. The algorithm starts with the product initialized to 0.
- Control decides when to shift the Multiplicand and Multiplier registers and when to write new values into the Product register

# **Unit 4: Arithmetic for Comp The first multiplication algori**

If the least significant bit of the multiplier is 1, add the multiplicand to the product.

If not, go to the next step.
Shift the multiplicand left and the multiplier right in the next two steps.

These three steps are repeated 32 times.





#### Multiply example using algorithm in Figure above

Bit circled in color is the bit to be checked to determine the next step



Iteration	Step	Multiplier	Multiplicand	Product
0	Initial values	0011	0000 0010	0000 0000
1	1a: 1 ⇒ Prod = Prod + Mcand	0011	0000 0010	0000 0010
	2: Shift left Multiplicand	0011	0000 0100	0000 0010
	3: Shift right Multiplier	000①	0000 0100	0000 0010
2	1a: 1 ⇒ Prod = Prod + Mcand	0001	0000 0100	0000 0110
	2: Shift left Multiplicand	0001	0000 1000	0000 0110
	3: Shift right Multiplier	0000	0000 1000	0000 0110
3	1: 0 ⇒ No operation	0000	0000 1000	0000 0110
	2: Shift left Multiplicand	0000	0001 0000	0000 0110
	3: Shift right Multiplier	0000	0001 0000	0000 0110
4	1: 0 ⇒ No operation	0000	0001 0000	0000 0110
	2: Shift left Multiplicand	0000	0010 0000	0000 0110
	3: Shift right Multiplier	0000	0010 0000	0000 0110

Reference: Computer Architecture with RISC V - The Hardware/Software Interface: RISC-V Edition by David A. Patterson and John L. Hennessy





## **THANK YOU**

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