Digital VLSI Design

Mahesh Awati

Department of Electronics and Communication Engineering.

DIGITAL VLSI DESIGN

MOS INVERTERS: SWITCHING CHARACTERISTICS AND INTERCONNECT EFFECTS

Mahesh Awati
Department of Electronics and Communication Engineering

Interconnect Resistance Estimation

- The line, itself a **three-dimensional structure in metal and/or polysilicon**, usually has a **non-negligible resistance** in addition to **its capacitance**. The (length/width) ratio of the wire usually dictates that the parameters are distributed, making the interconnect a true transmission line.

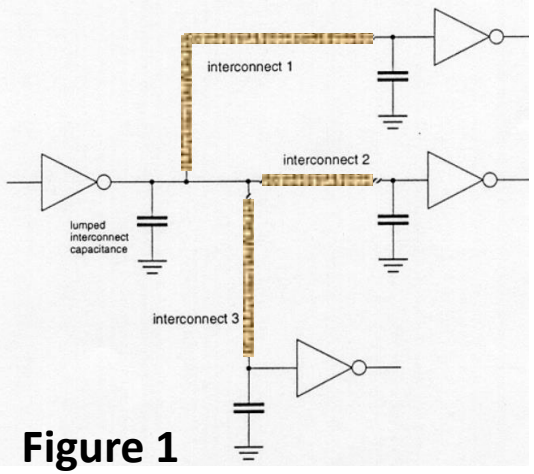
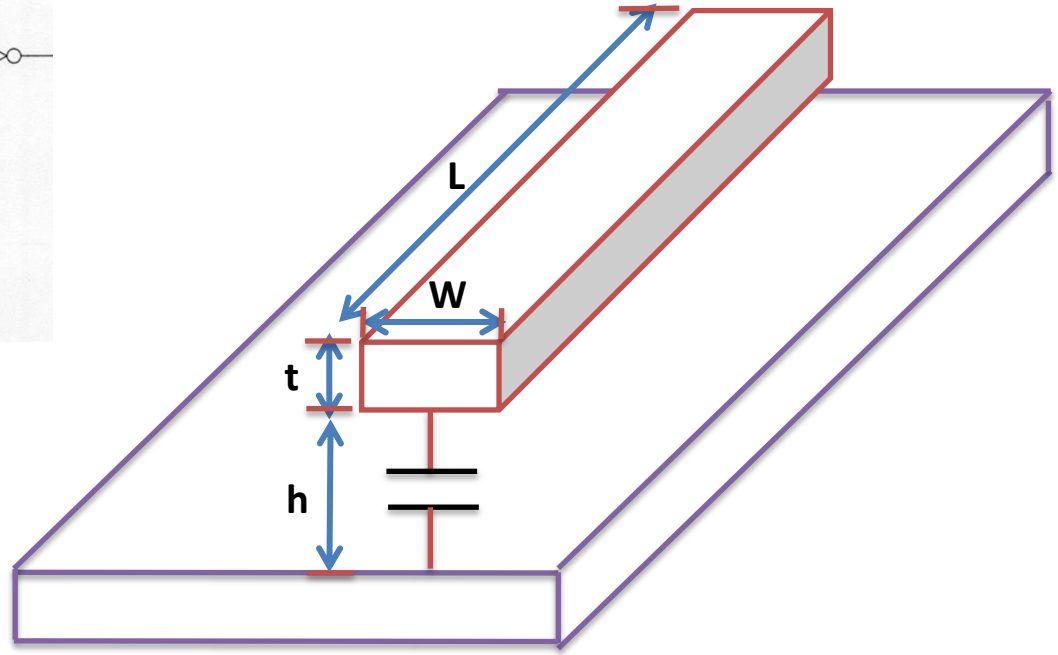


Figure 1

Interconnect Segment running parallel to Surface



$$R_{wire} = \rho \cdot \frac{l}{w \cdot t} = R_{sheet}\left(\frac{l}{w}\right)$$

$$R_{sheet} = \frac{\rho}{t}$$

Interconnect Capacitance Estimation (Cpp)

- The line, itself a **three-dimensional structure in metal and/or polysilicon**, usually has a **non-negligible resistance** in addition to **its capacitance**. The (length/width) ratio of the wire usually dictates that the parameters are distributed, making the interconnect a true transmission line.

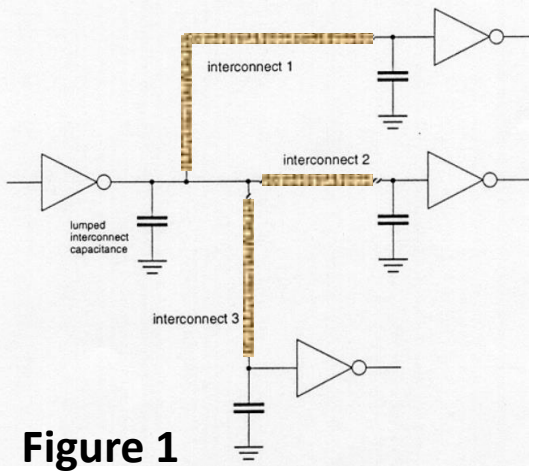
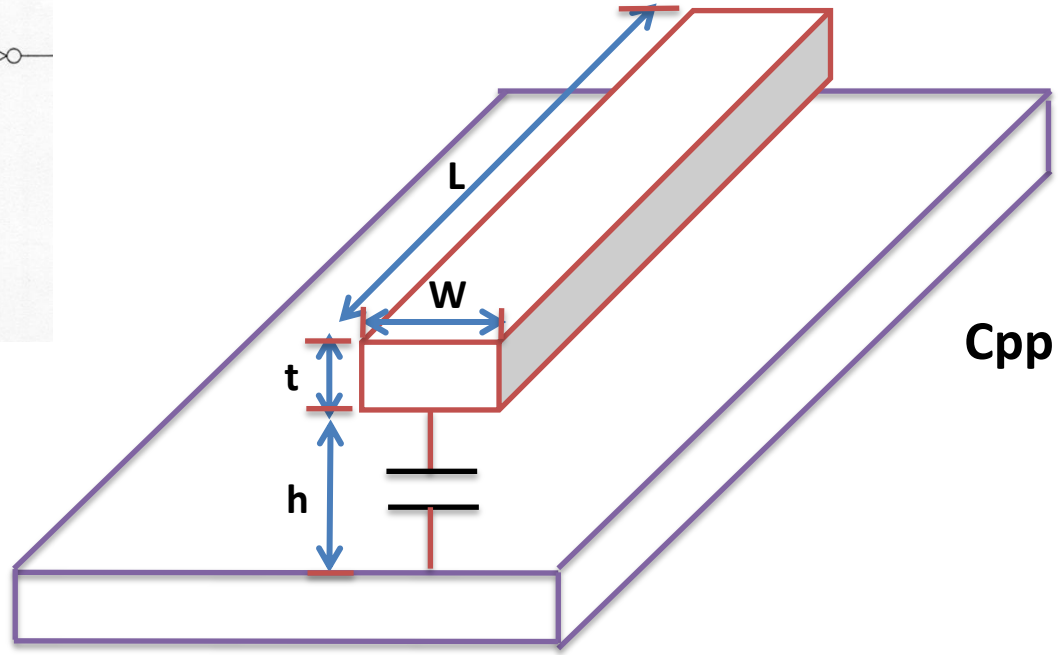


Figure 1

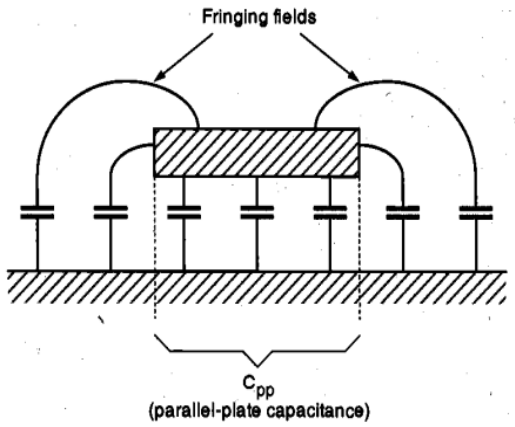
Interconnect Segment running parallel to Surface acts like Parallel Plate Capacitor Cpp



$$Cpp = \varepsilon_{ox}(A/d) = \varepsilon_{ox}(WL/h)$$
$$= \text{Unit Area Capacitance}(WxL)$$

Interconnect Capacitance Estimation(Cfring)

- However, in interconnect lines where the wire thickness (t) is comparable in magnitude to the ground-plane distance (h),fringing electric fields significantly increase the total parasitic capacitance
- Fringing-field factor FF = Ctotal/Cpp, as a function of (t/h), (w/h) and (w/l).
- The influence of fringing fields increases with the decreasing (w/h).
- the submicron fabrication technologies allow the **width of the metal lines to be decreased rather significantly, but the thickness of the line must be preserved in order to ensure structural integrity.** This situation, which involves **narrow metal lines with a considerable vertical thickness, makes these interconnection lines especially vulnerable to fringing field effects**

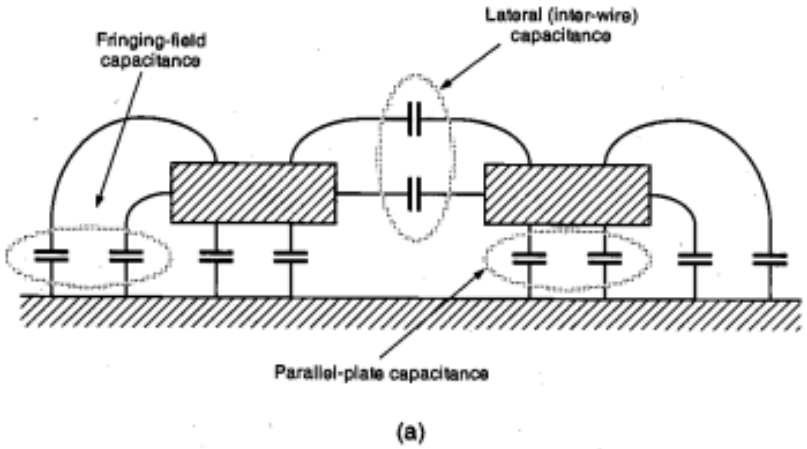


Influence of fringing electric fields upon the parasitic wire capacitance.

MOS INVERTERS: SWITCHING CHARACTERISTICS AND INTERCONNECT EFFECTS

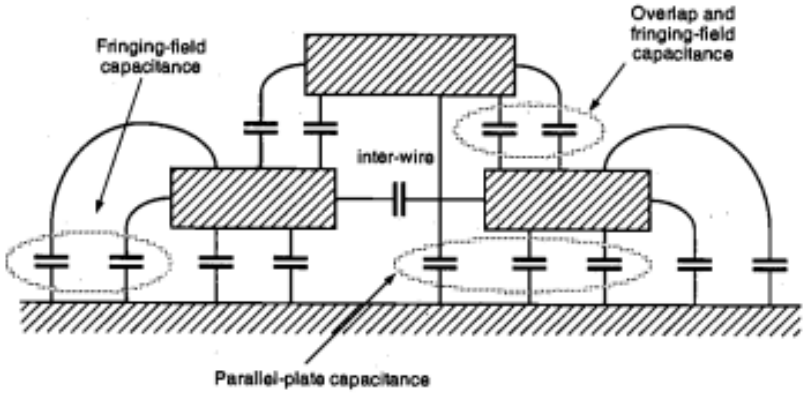
Estimation of Interconnect Parasitics (Inter –wire Capacitance)

Capacitive Coupling components between two parallel lines running on the same level,



In this case, the total parasitic capacitance of the line is not only increased by the fringing-field effects, but also by the capacitive coupling between the lines

Capacitive Coupling components between three parallel lines running on two different levels



The capacitive coupling between neighboring lines is increased when the thickness of the wire is comparable to its width.

This **coupling between the interconnect** lines is mainly responsible for **signal crosstalk**, where transitions in **one line can cause noise in the other lines**

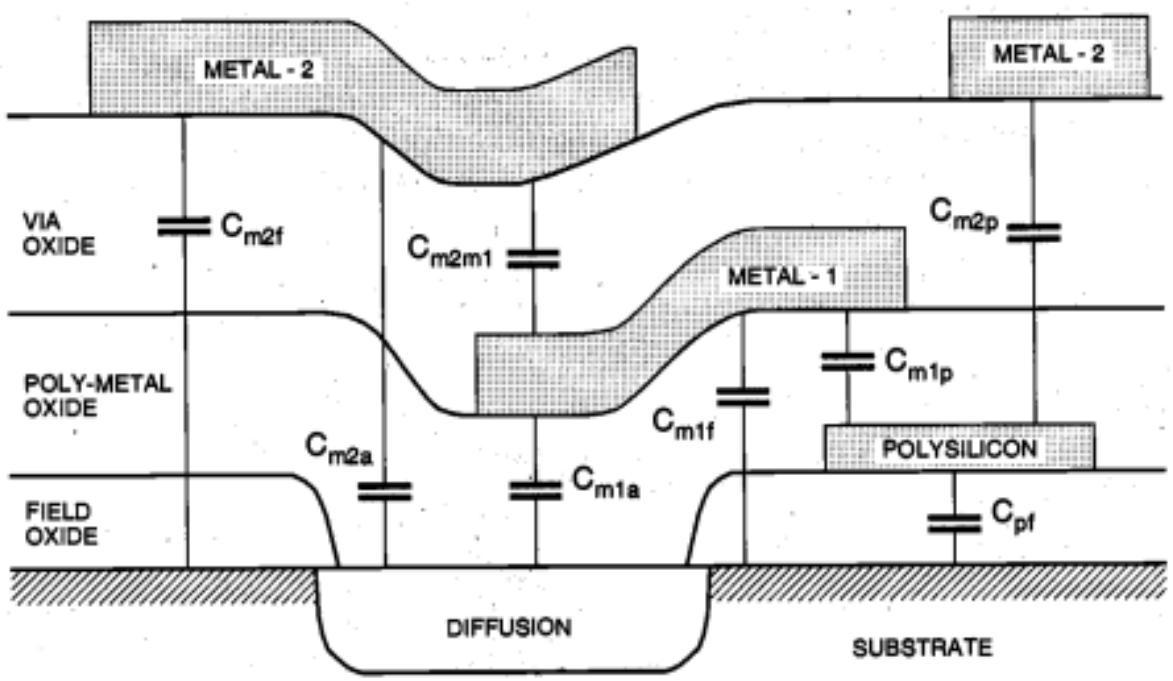
Capacitance of a line which is coupled with two other lines on both sides (at the same level); separated by the minimum design rule.

Especially if both of the neighboring lines are biased at ground, the total parasitic cap of the interconnect in the middle can be more than 20 times as large as the simple parallel-plate capacitance.

MOS INVERTERS: SWITCHING CHARACTERISTICS AND INTERCONNECT EFFECTS

Estimation of Interconnect Parasitics

Cross-section view of a double-metal CMOS structure, where the individual parasitic capacitances between the layers are also indicated.



- The inter-layer capacitances between Metal-2 and Metal-1, Metal-1 and Polysilicon, and Metal-2 and Polysilicon.
- The other parasitic capacitance components are defined with respect to the substrate.
- If the metal line passes over an active region, the oxide thickness underneath is smaller (because of the active area window), and consequently, the capacitance is larger. These special cases are labeled as Cm1a and Cm2a.
- Otherwise, the thick field oxide layer results in a smaller capacitance value.

MOS INVERTERS: SWITCHING CHARACTERISTICS AND INTERCONNECT EFFECTS

Interconnect Capacitance Estimation

Thickness values of different layers in a typical 0.8 micron CMOS process.

Field oxide thickness	0.52	µm	
Gate oxide thickness	16.0	nm	(= 0.016 µm)
Polysilicon thickness	0.35	µm	(minimum width 0.8 µm)
Poly - metal oxide thickness	0.65	µm	
Metal - 1 thickness	0.60	µm	(minimum width 1.4 µm)
Via oxide thickness	1.00	µm	
Metal - 2 thickness	1.00	µm	(minimum width 1.4 µm)
n + junction depth	0.40	µm	
p + junction depth	0.40	µm	
n - well junction depth	3.50	µm	

Table 6.2. Parasitic capacitance values between various layers, for a typical double-metal 0.8 micron CMOS technology.

Poly over field oxide	C_{pf}	Area	0.066	fF / µm^2
		Perimeter	0.046	fF / µm
Metal - 1 over field oxide	C_{m1f}	Area	0.030	fF / µm^2
		Perimeter	0.044	fF / µm
Metal - 2 over field oxide	C_{m2f}	Area	0.016	fF / µm^2
		Perimeter	0.042	fF / µm
Metal - 1 over Poly	C_{m1p}	Area	0.053	fF / µm^2
		Perimeter	0.051	fF / µm
Metal - 2 over Poly	C_{m2p}	Area	0.021	fF / µm^2
		Perimeter	0.045	fF / µm
Metal - 2 over Metal - 1	C_{m2m1}	Area	0.035	fF / µm^2
		Perimeter	0.051	fF / µm

THANK YOU

Mahesh Awati
Department of Electronics and Communication

mahesha@pes.edu

+91 9741172822