DIGITAL VLSI DESIGN

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Unit 2: Fabrication of MOSFETs & Circuit Design Process

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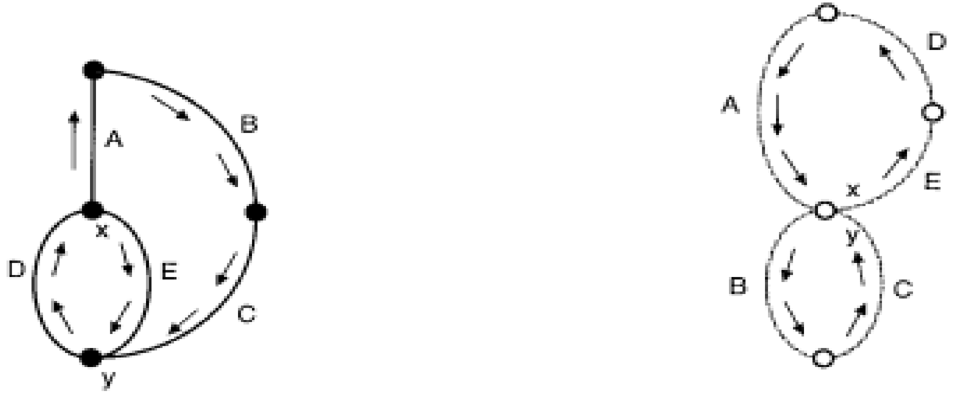
Complex Logic Circuits

Euler path – Uninterrupted path that traverses each edge of the graph EXACTLY ONCE

Optimal Input (POLY) Ordering

- Common Euler path in BOTH PDN graph and PUN graph gives optimal ordering of POLY input I



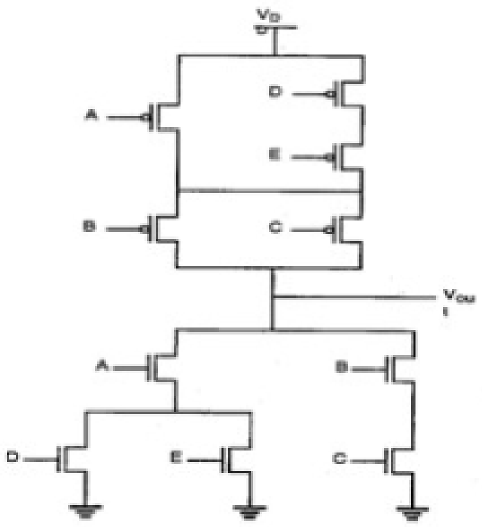
nMOS network

pMOS network

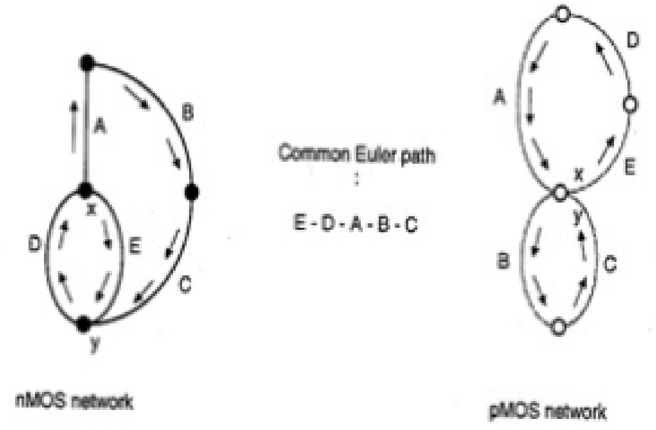
Finding a common Euler path in both graphs for n-net and p-net provides a gate ordering that minimizes the number of diffusion breaks and, thus, minimizes the logic- gate layout area. In both cases, the Euler path starts at (x) and ends at (y).

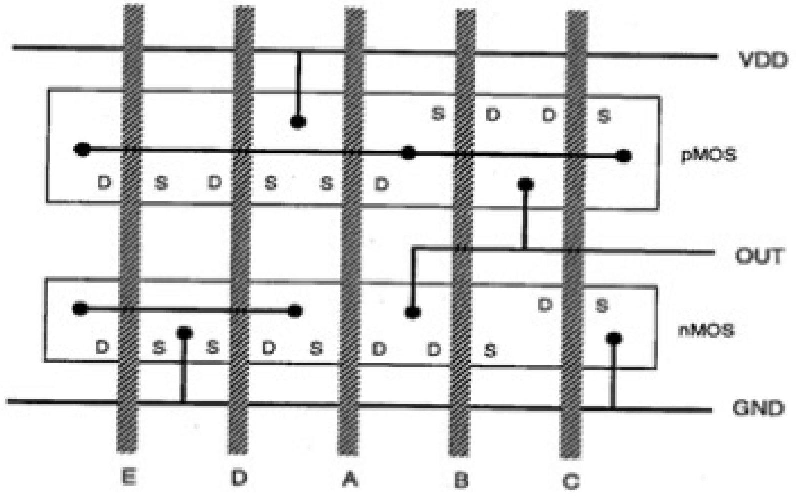
Complex Logic Circuits

Layout with Optimum Gate Ordering



- By using the Euler path approach to re-order the polysilicon lines of the previous chart, we can obtain an optimum layout.
- Find a Euler path in both the pull-down tree graph and the pull-up tree graph with identical ordering of the inputs.
  - –Euler path: traverses each branch of the graph exactly once!
- By reordering the input gates as E-D-A-B-C, we can obtain an optimum layout of the given CMOS gate with single actives for both NMOS and PMOS devices (below).





Complex Logic Circuits

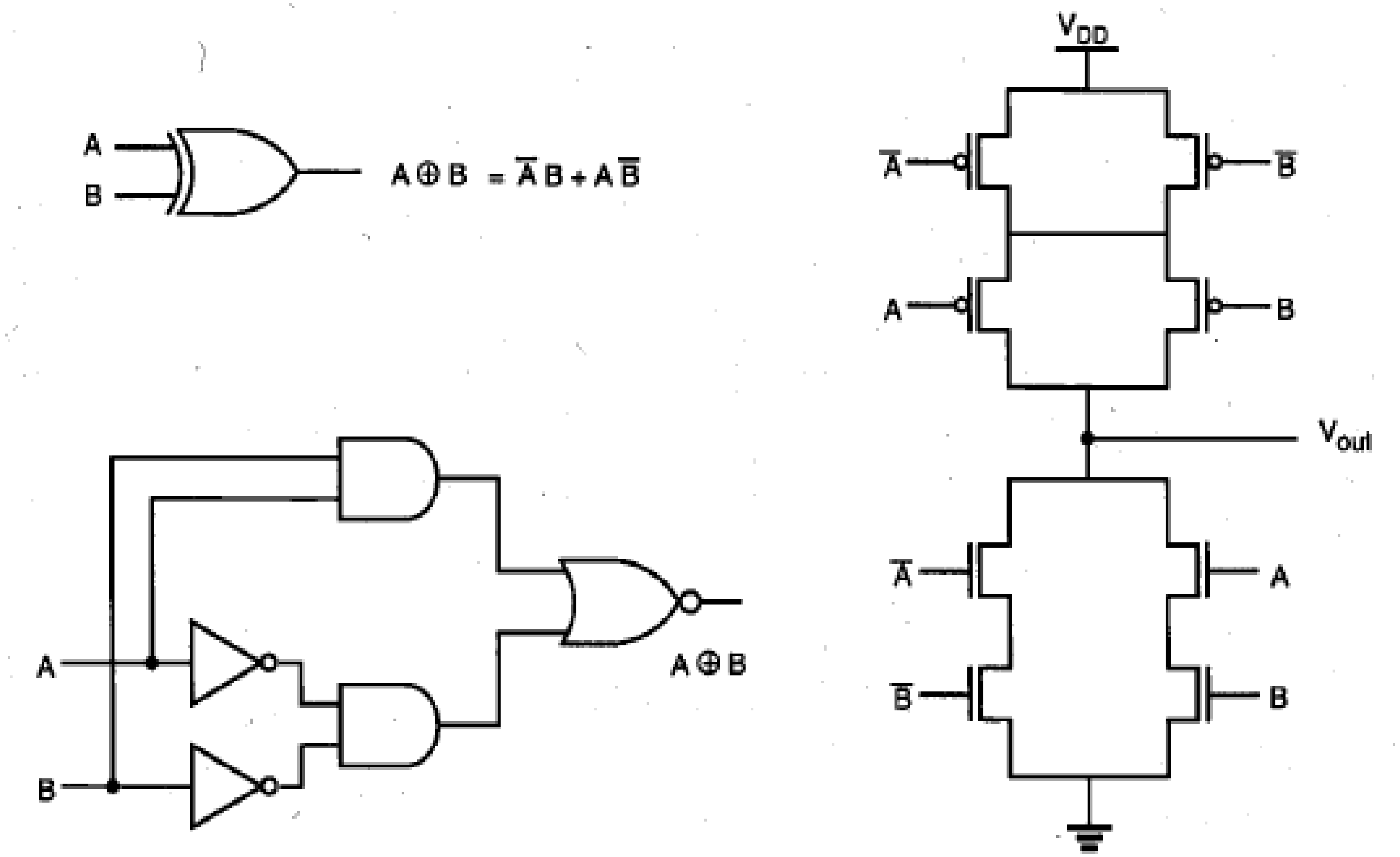
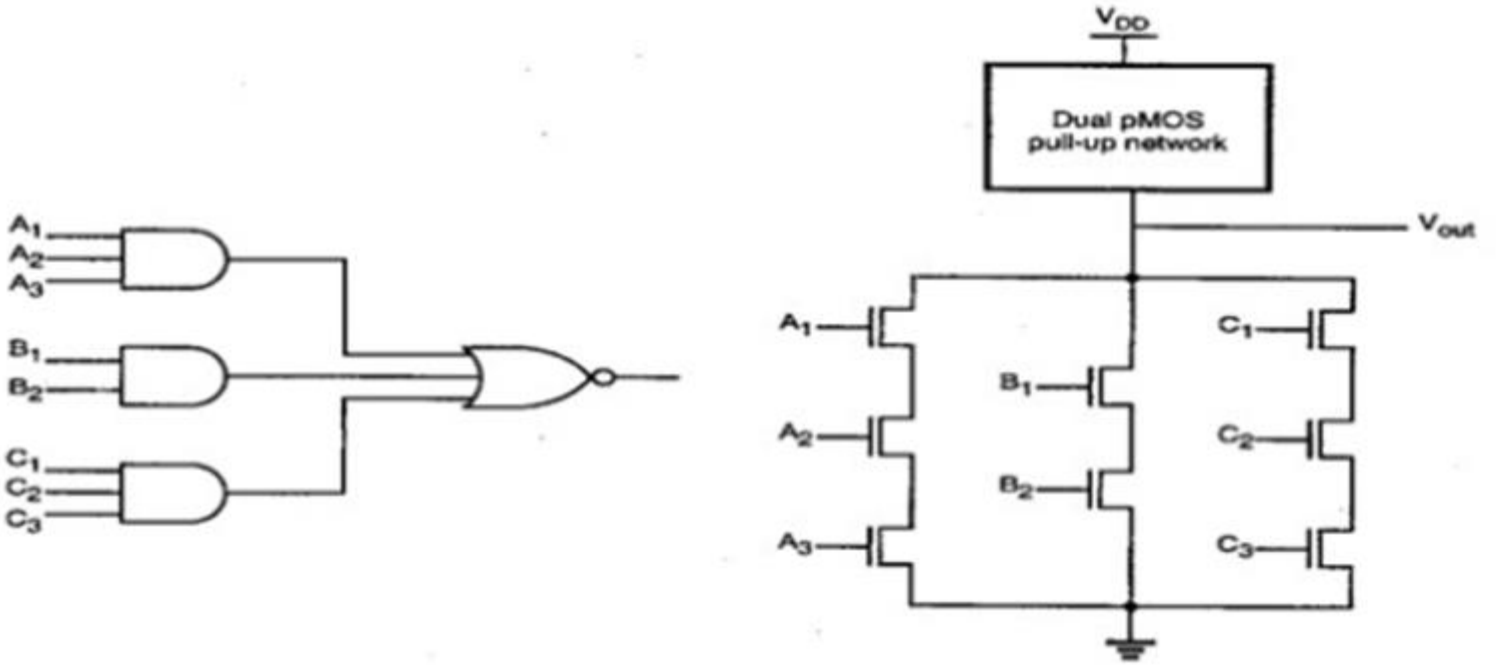


Figure 7.23. Full-CMOS implementation of the XOR function.

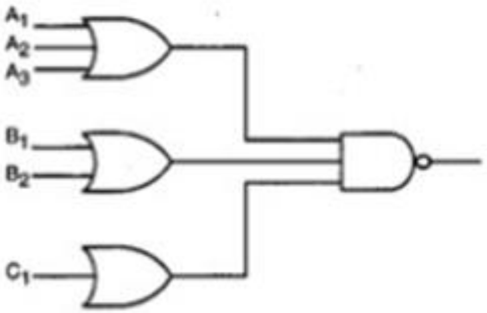
AOI (AND – OR - INVERT) CMOS Gate

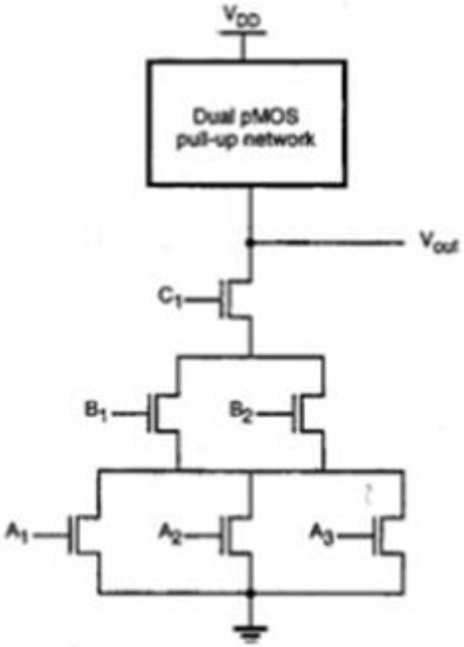


- AOI complex CMOS gate can be used to directly implement a sum-of-products Boolean function
- The pull-down N-tree can be implemented as follows:
  - –Product terms yield series-connected NMOS transistors
  - –Sums are denoted by parallel-connected legs
  - –The complete function must be an inverted representation
- The pull-up P-tree is derived as the dual of the N-tree

OAI (OR – AND - INVERT) CMOS Gate

- An Or-And-Invert (OAI) CMOS gate is similar to the AOI gate except that it is an implementation of product-of-sums realization of a function
- The N-tree is implemented as follows:
  - Each product term is a set of parallel transistors for each input in the term
  - All product terms (parallel groups) are put in series
  - The complete function is again assumed to be an inverted representation
- The P-tree can be implemented as the dual of the N-tree
- Note: AO and OA gates (non-inverted function representation) can be implemented directly on the P-tree if inverted inputs are available





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THANK YOU

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