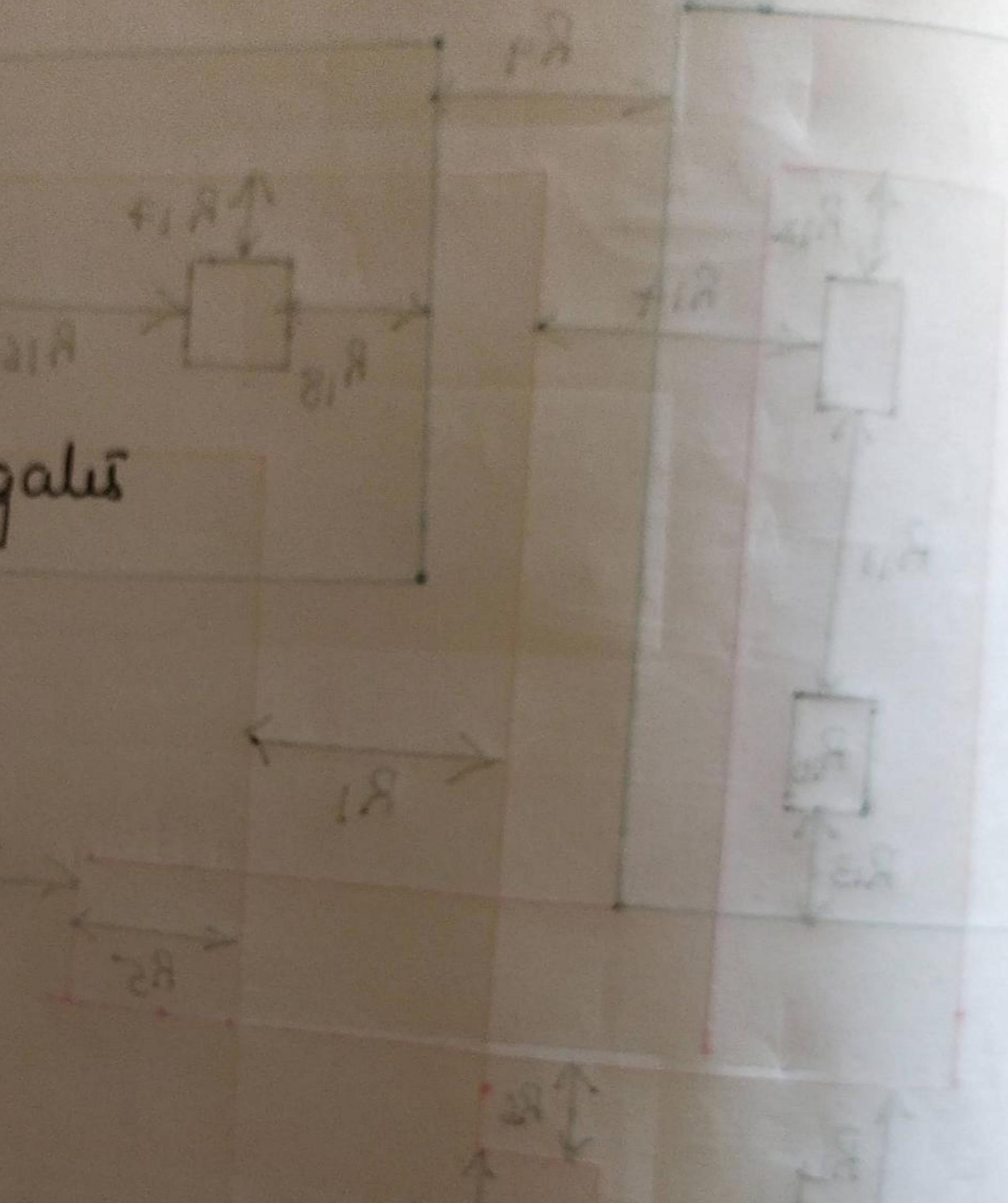


Module 2

contents :

1. Fabrication
2. Layout rules
3. complex MOS gates
4. Euler path
5. Full adder
6. MOS Sizing
7. MOS Scaling



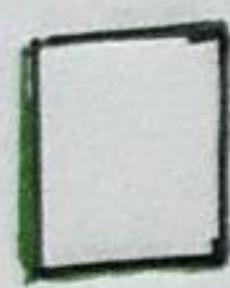
Layout Design Rules

- Physical mask layout of any circuit to be manufactured by particular process must conform to a set of geometric constraints or rules which are generally called layout design rules.
- It specifies the minimum allowable line width for physical objects on chip
- If a metal line width is made too small there is a possibility of line to break during fabrication
- If two lines are placed too close to one another there is a possibility of short circuit
- The main objective of design rules is to achieve high overall yield & reliability while using smallest possible silicon area
- The design rules are usually described in two ways
 1. Micron rules
 2. Lambda rules

Design rules :-

polygate, gate, contact, minimum width, height, overlap, margin

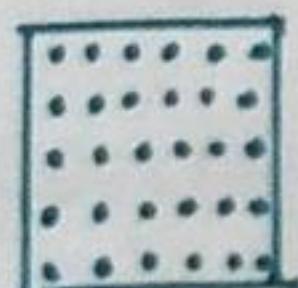
1. Active area rules :-



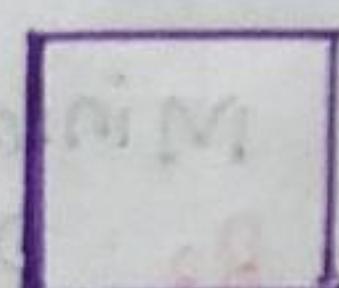
Active area [diffusion]



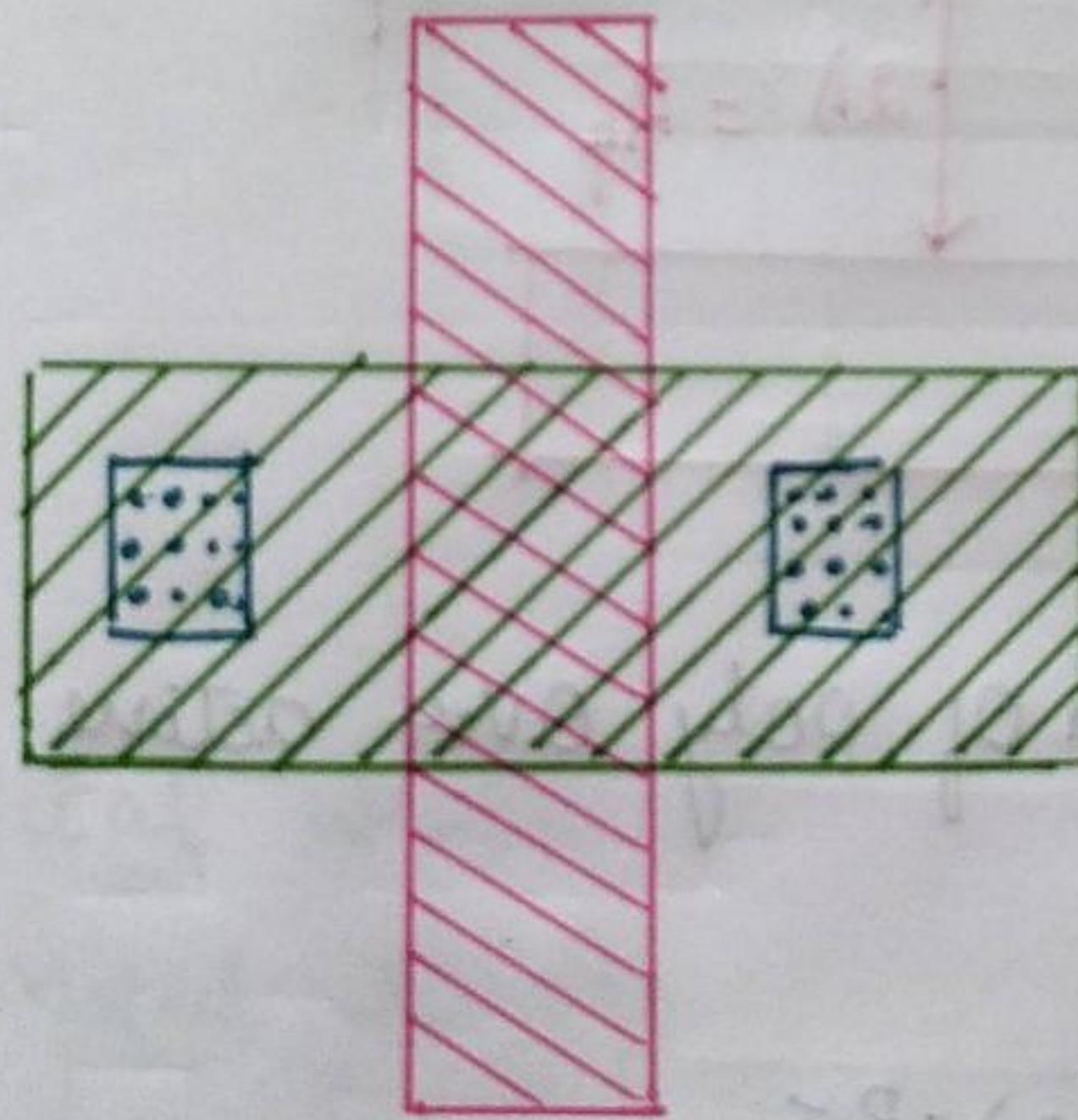
Polysilicon



contact



Metal

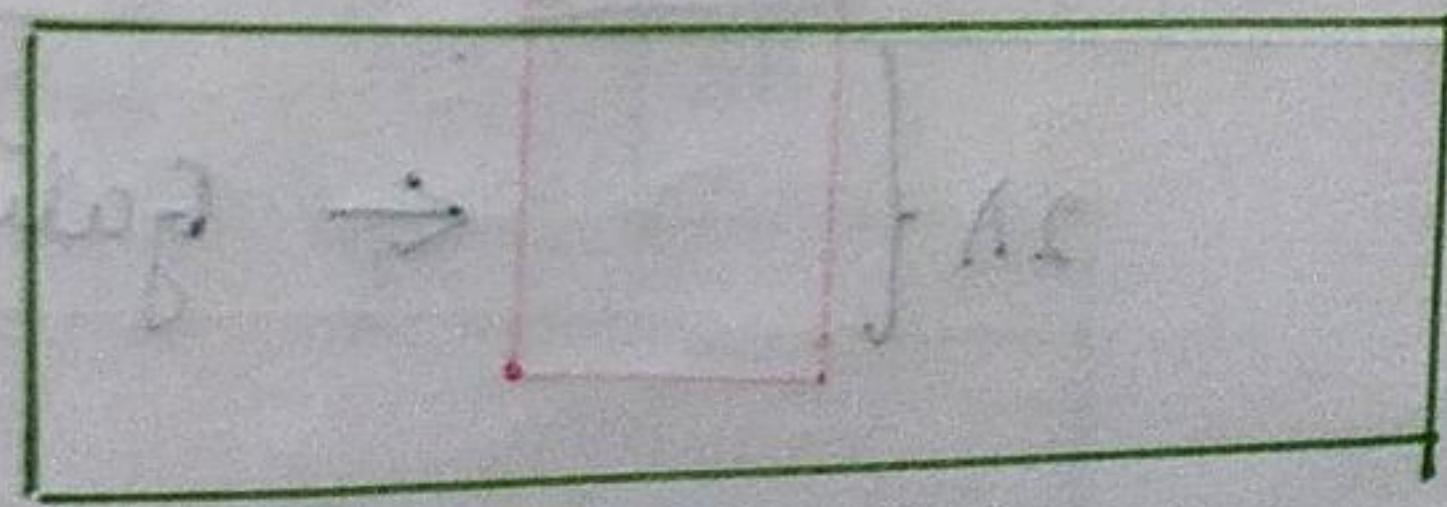


← active area.

i) Minimum active area width.

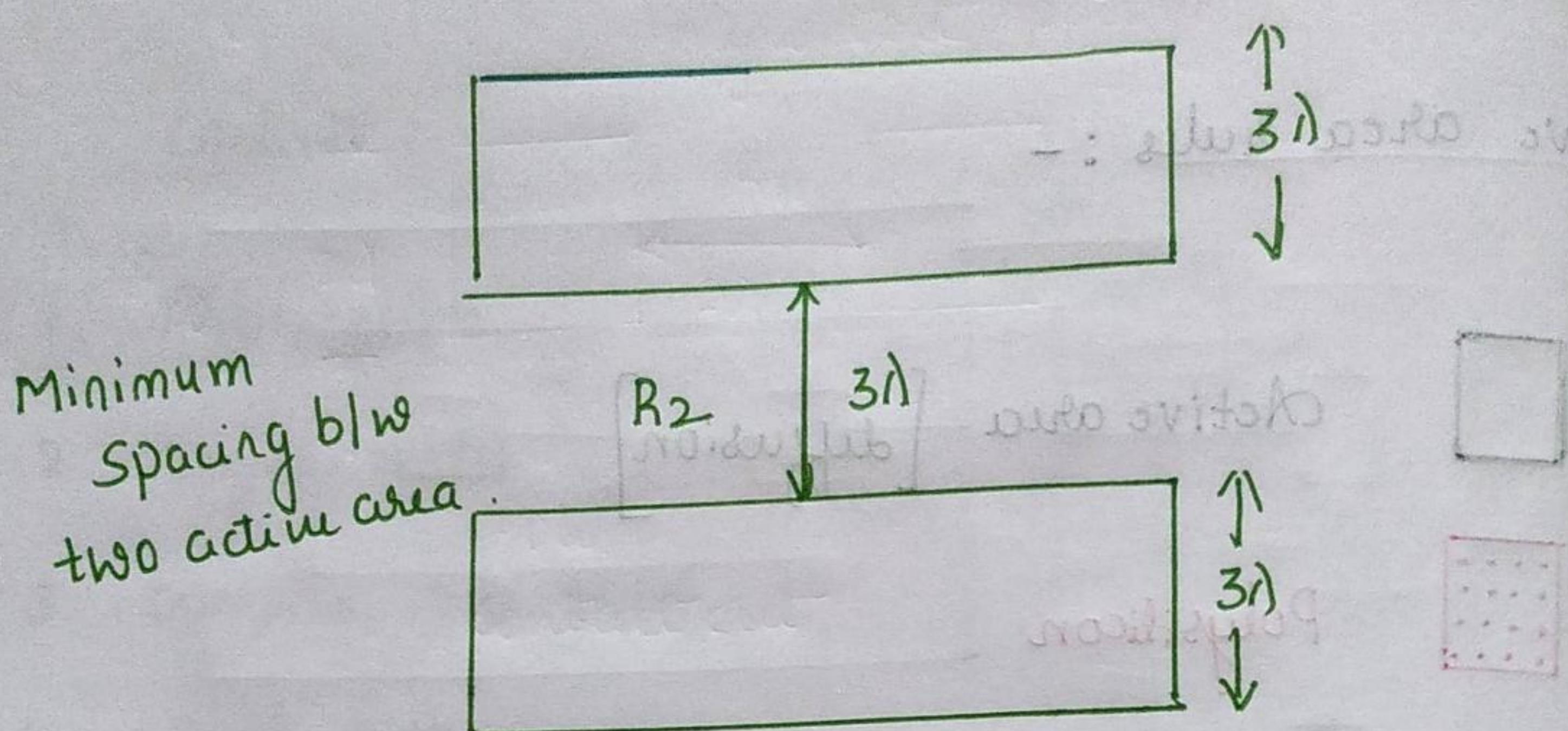
minimum
active
area
width

R_1

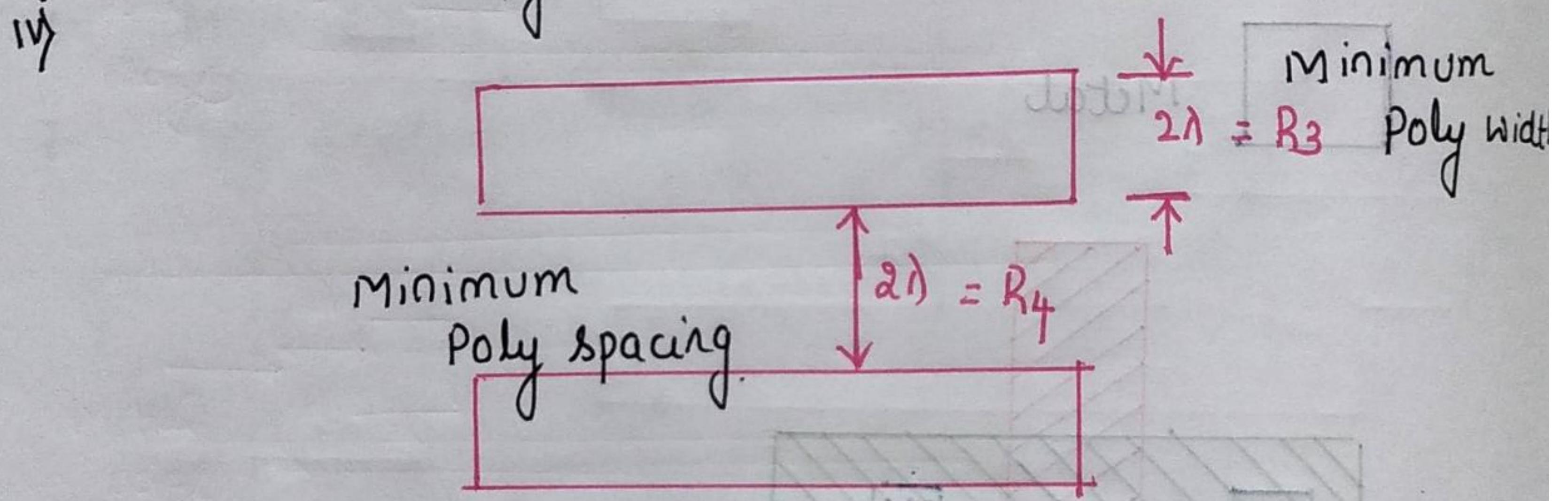


3λ

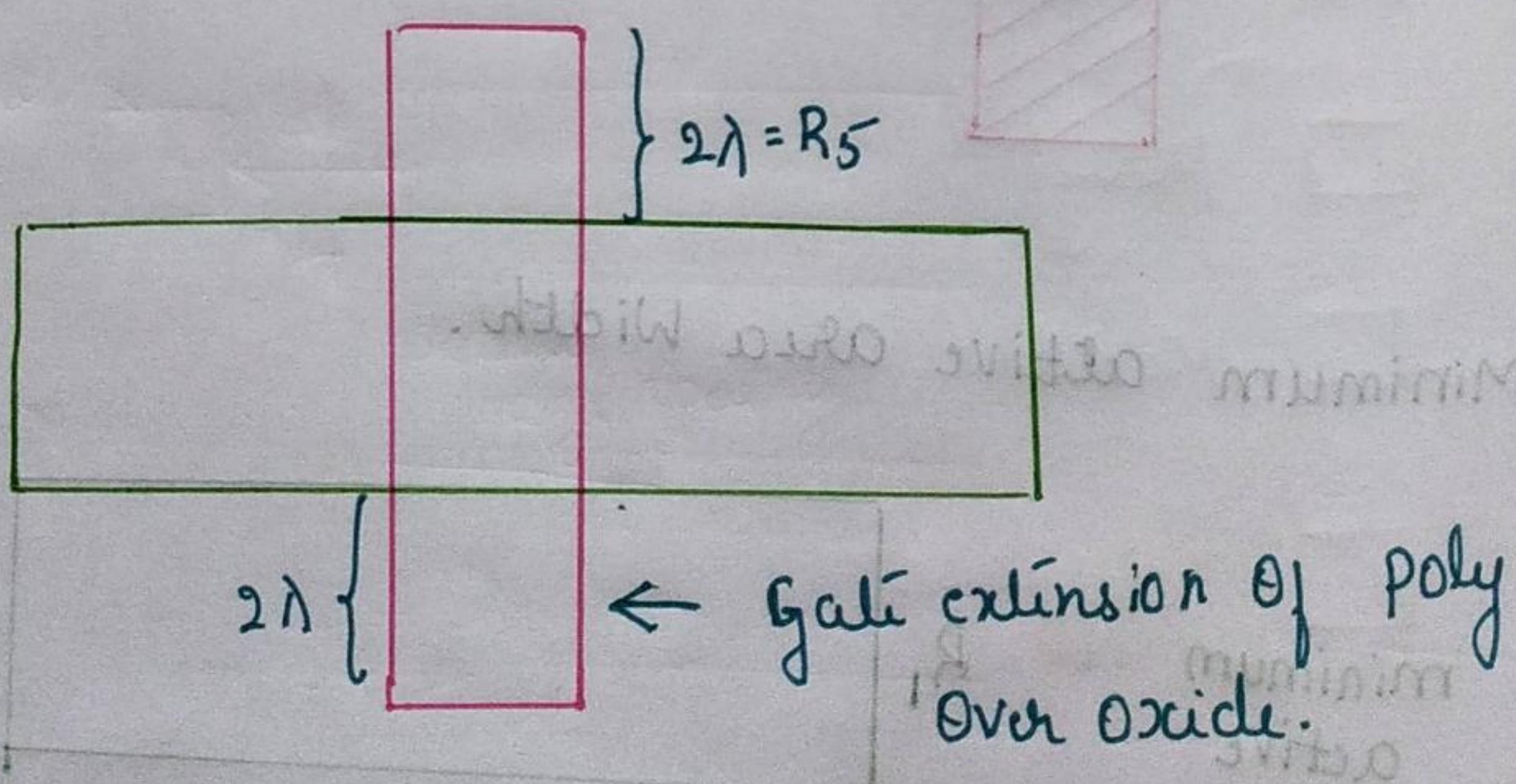
II) Minimum active area spacing



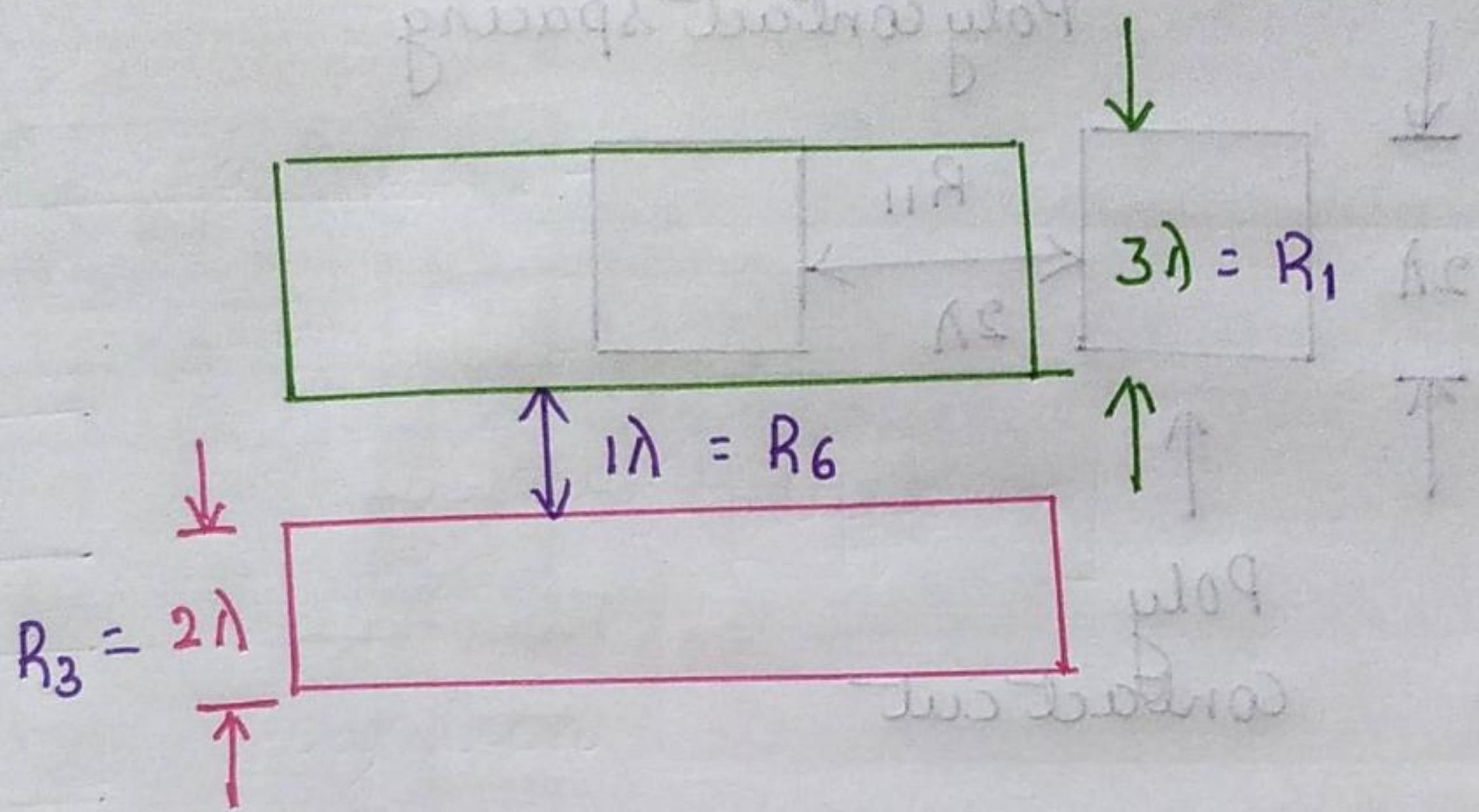
III) Minimum poly width



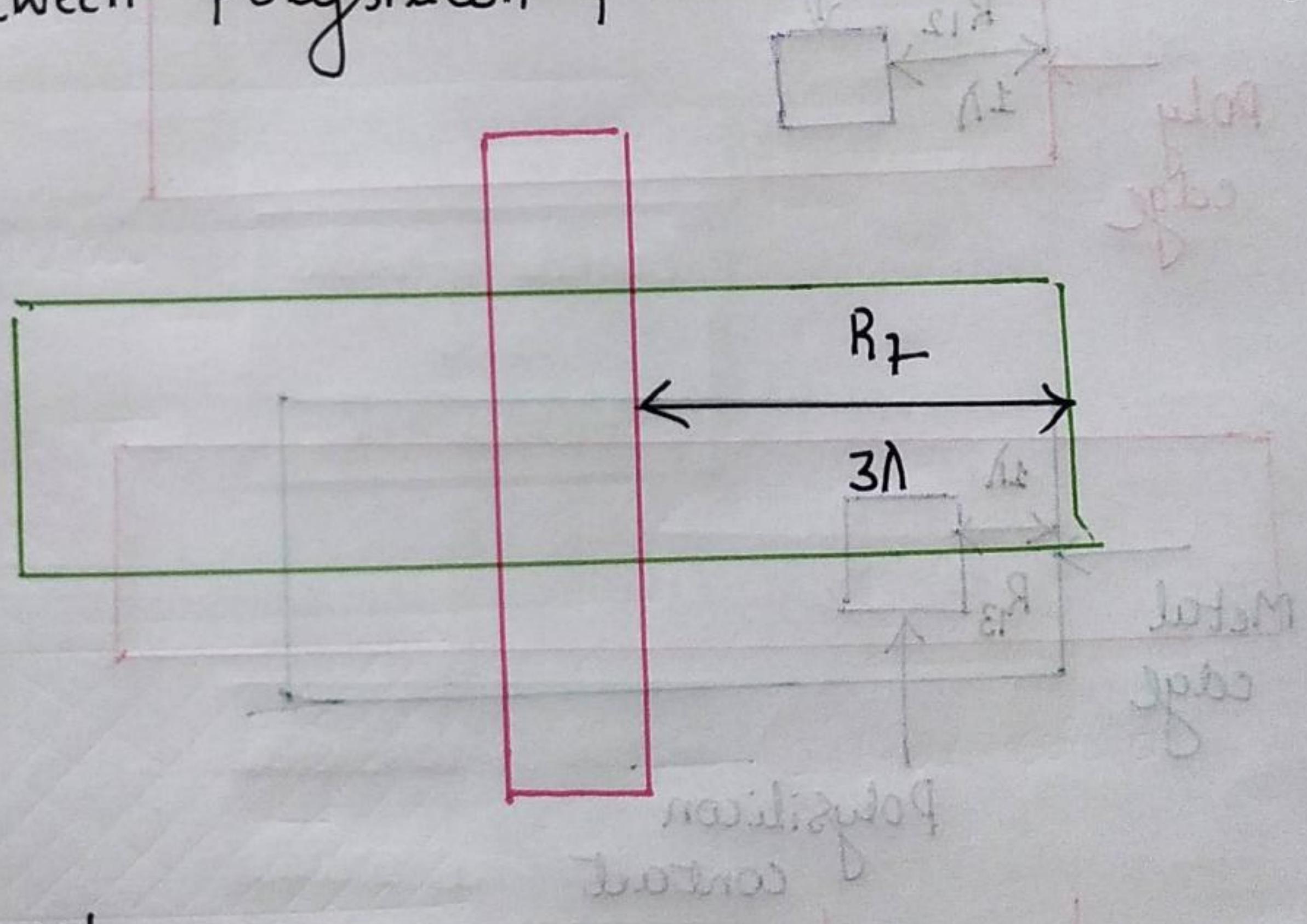
IV) Minimum gali extension of poly over active



vi) Spacing between polysilicon & active [External]

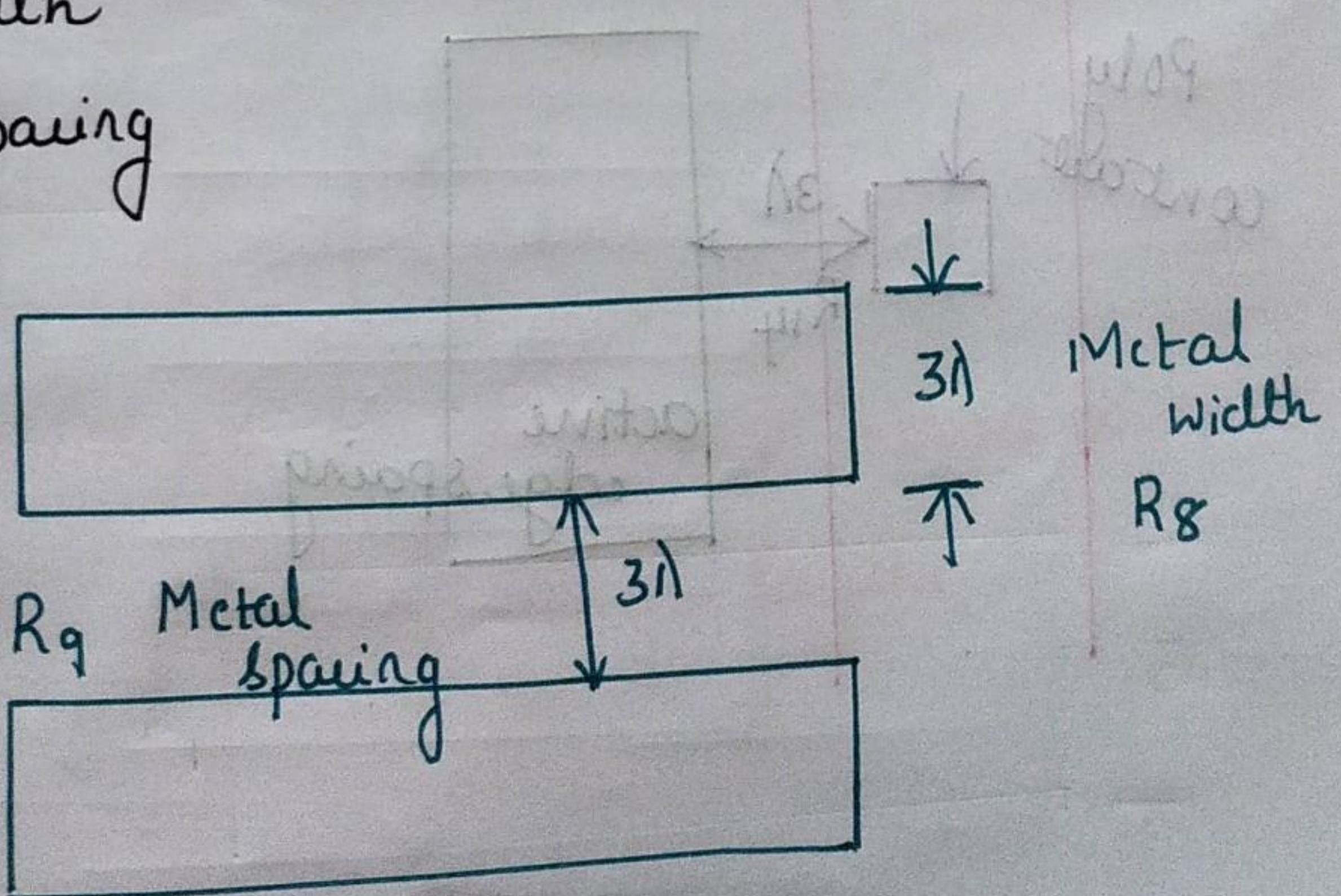


vii) Spacing between polysilicon & active area [internal]



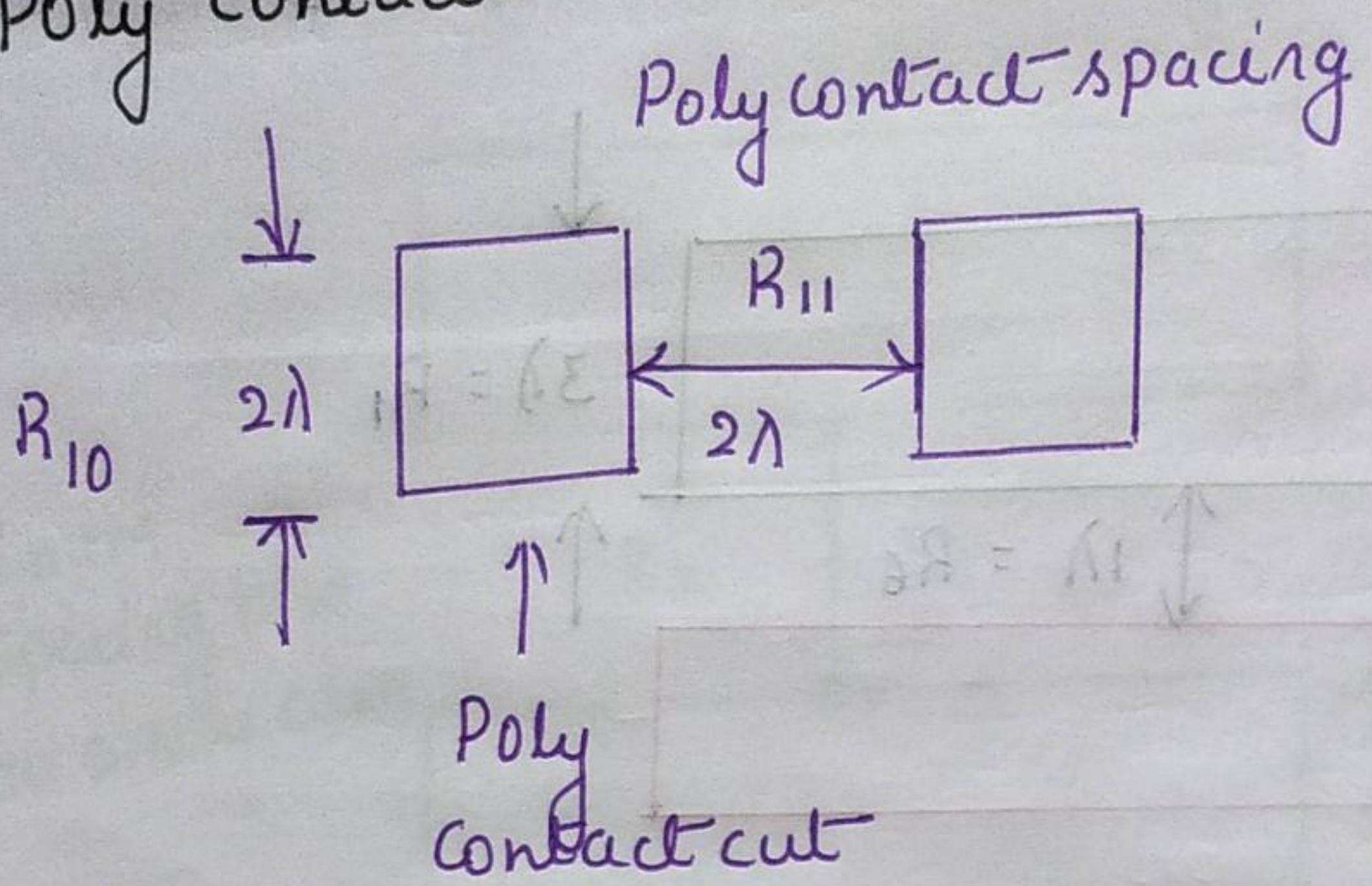
viii) Metal width

ix) Metal Spacing

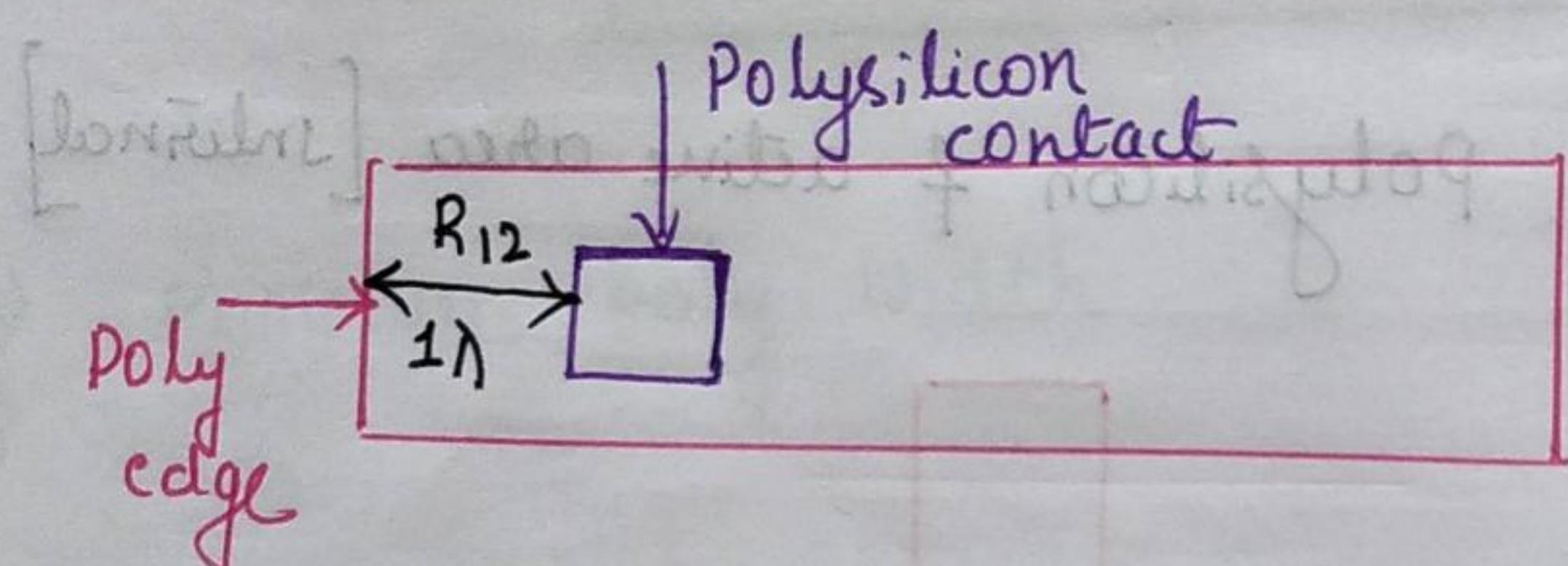


X) Poly contact size

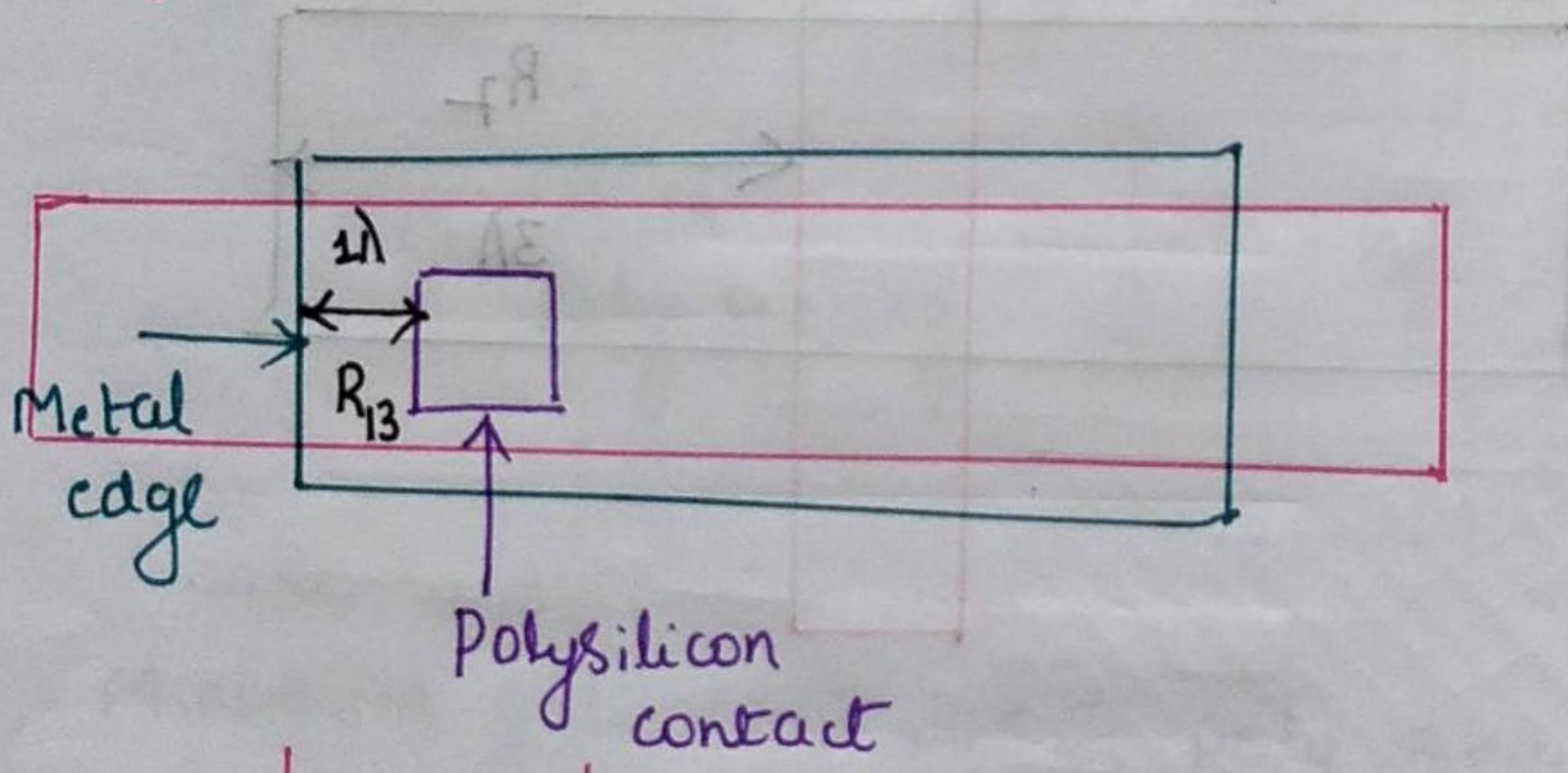
→



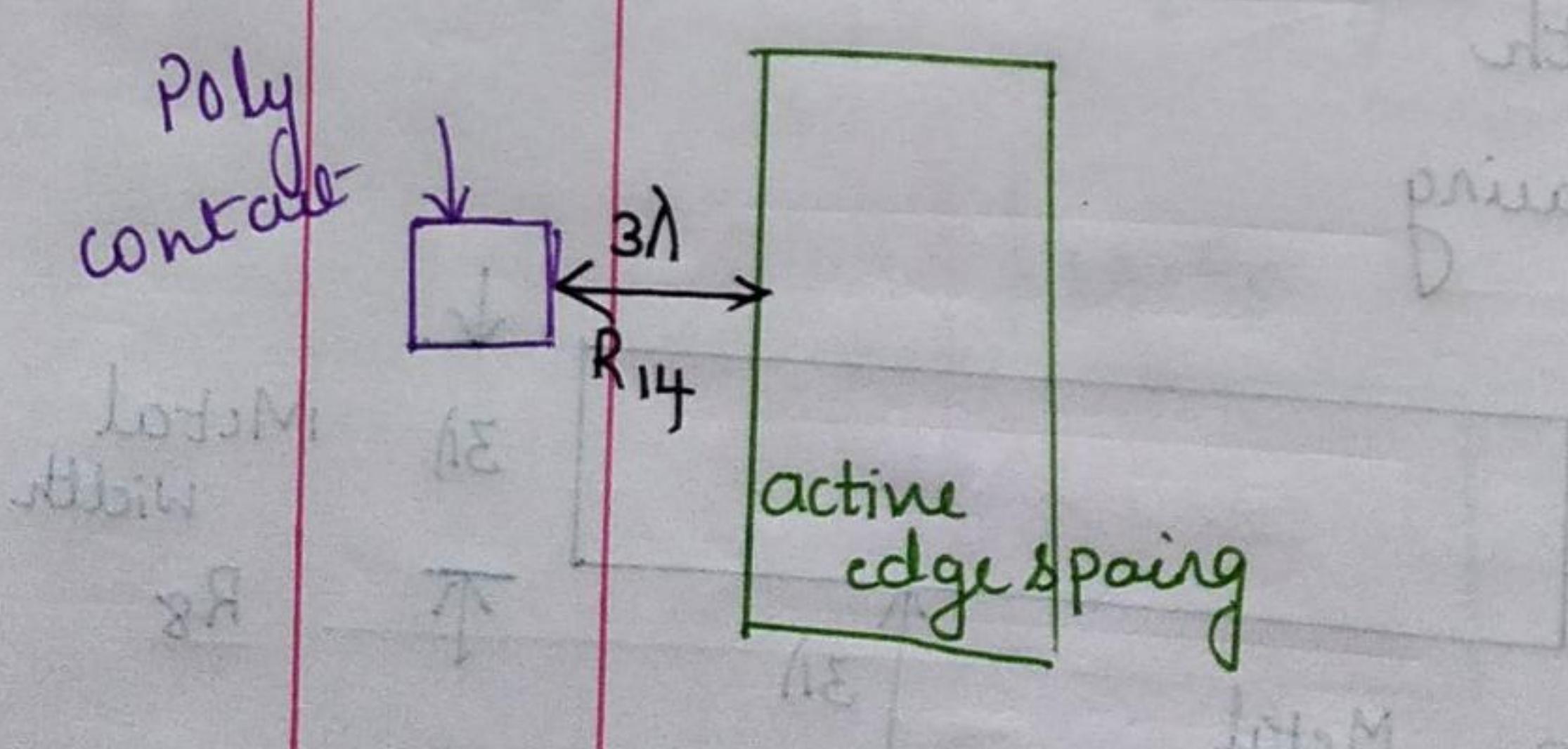
→



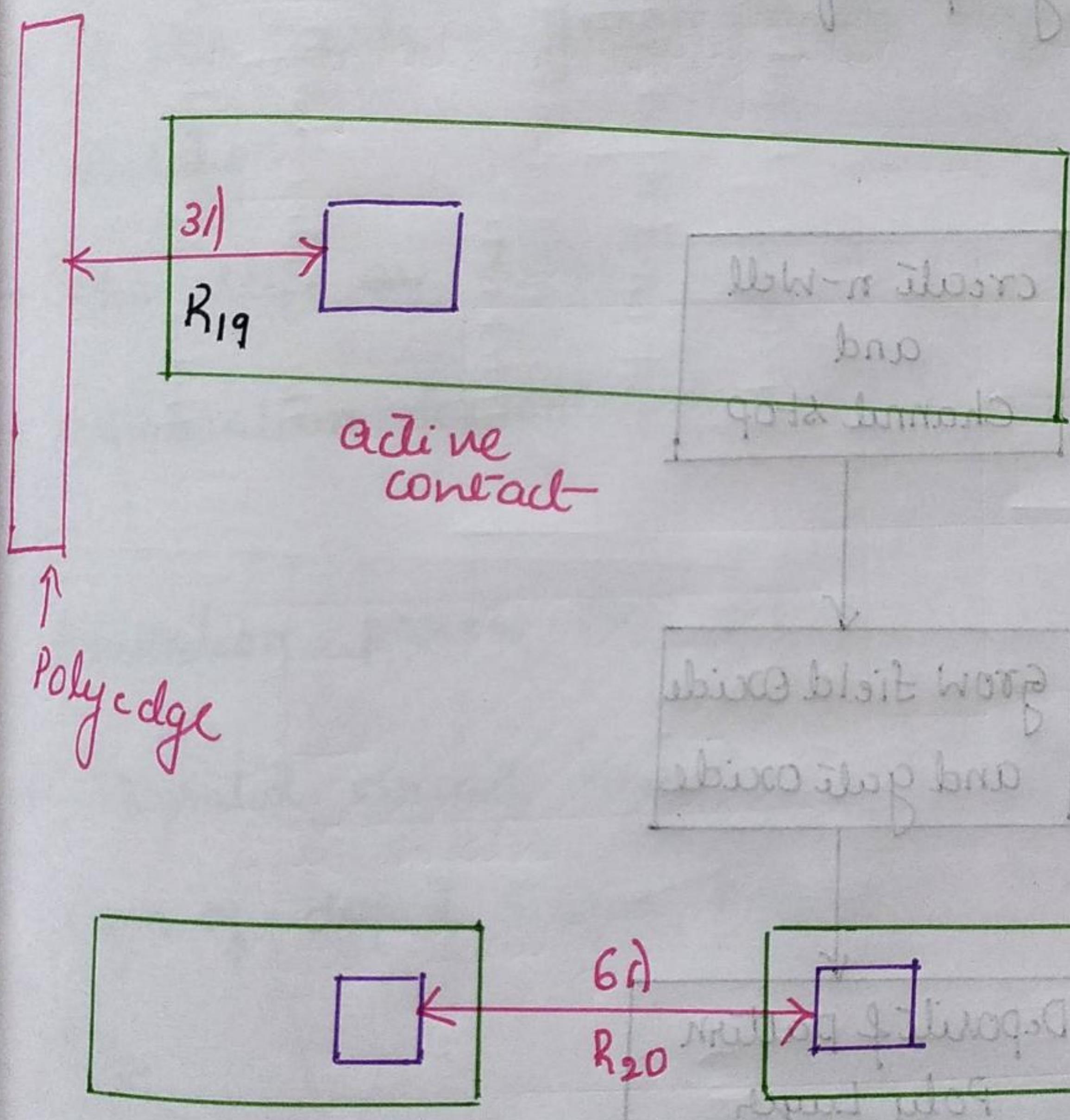
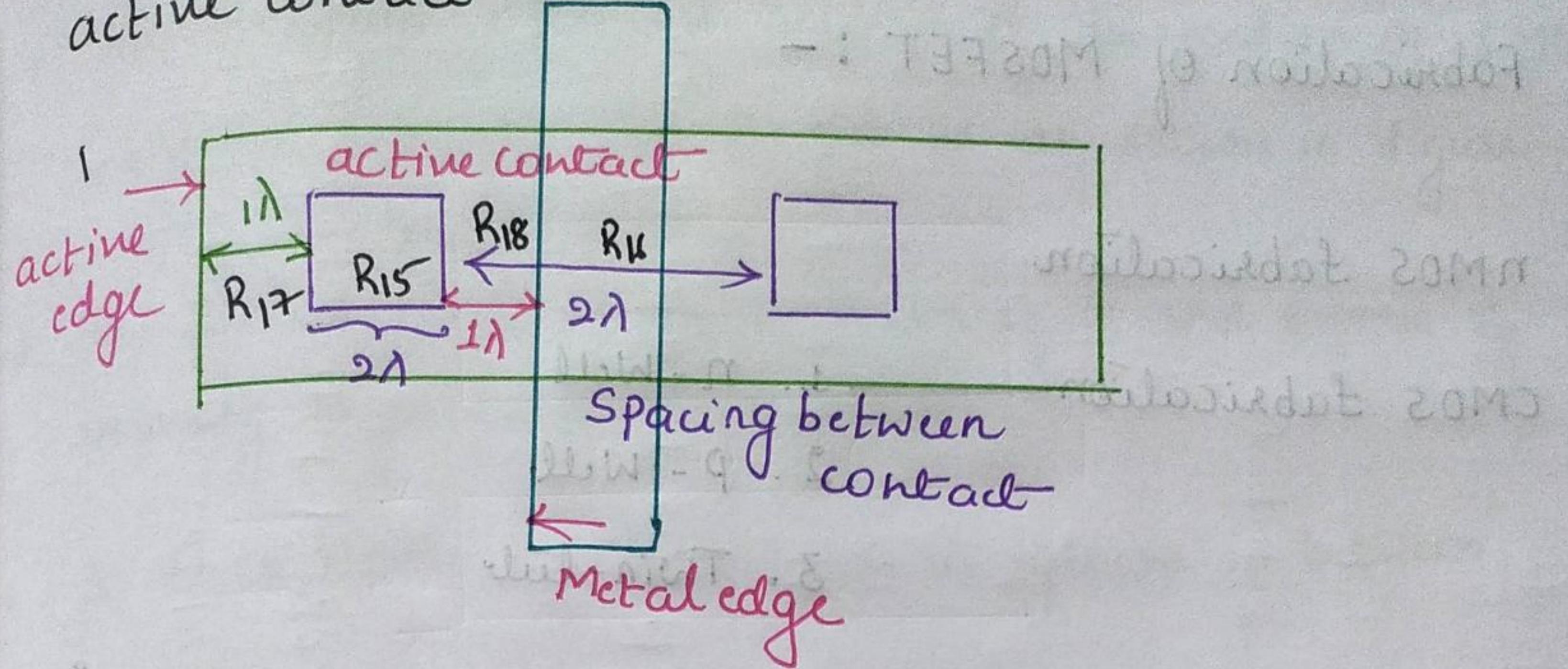
→



→



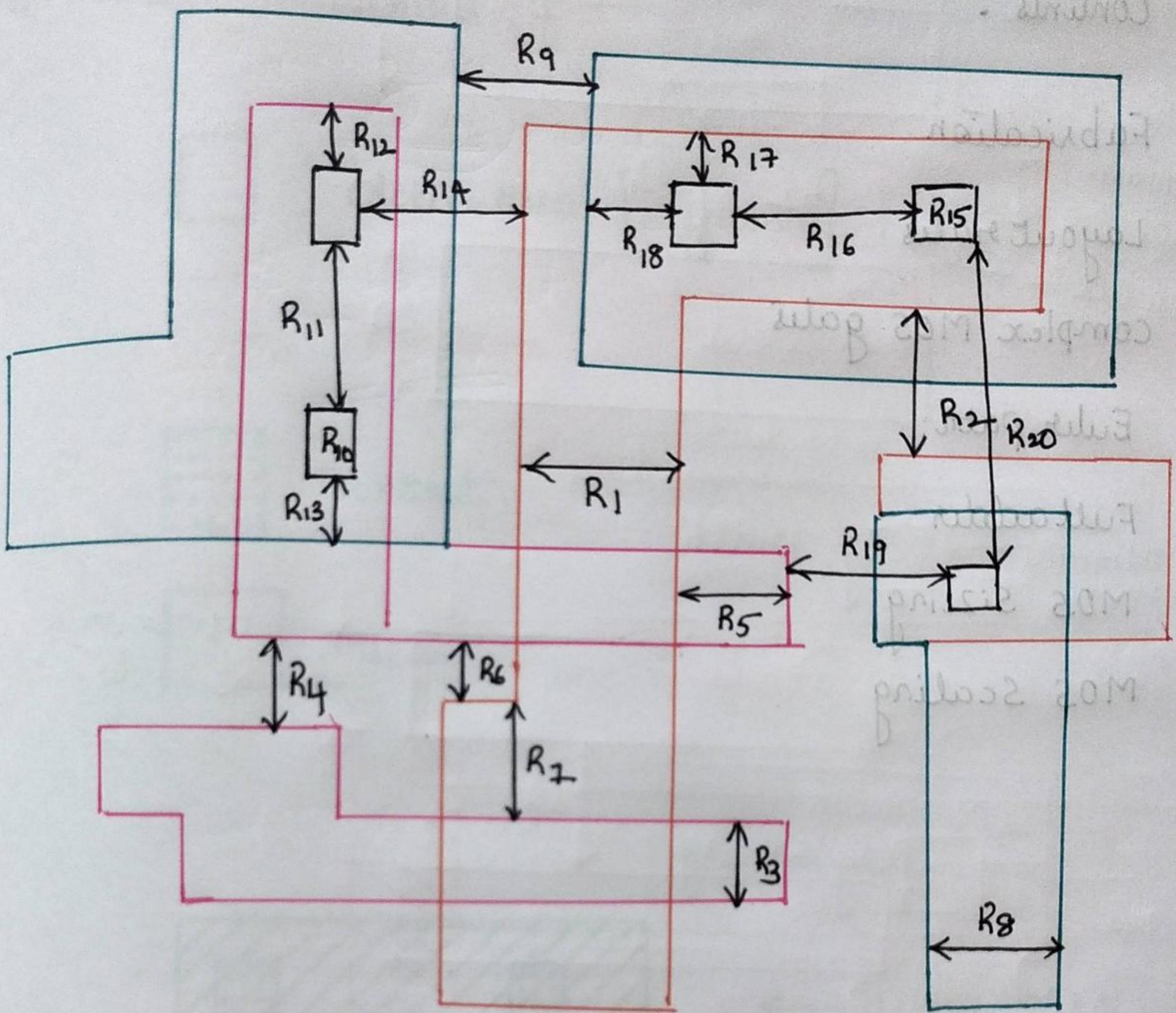
active contact



Minimum spacing b/w two active contact

in different active layers.

Layout Design rules :-



contact

poly

metal

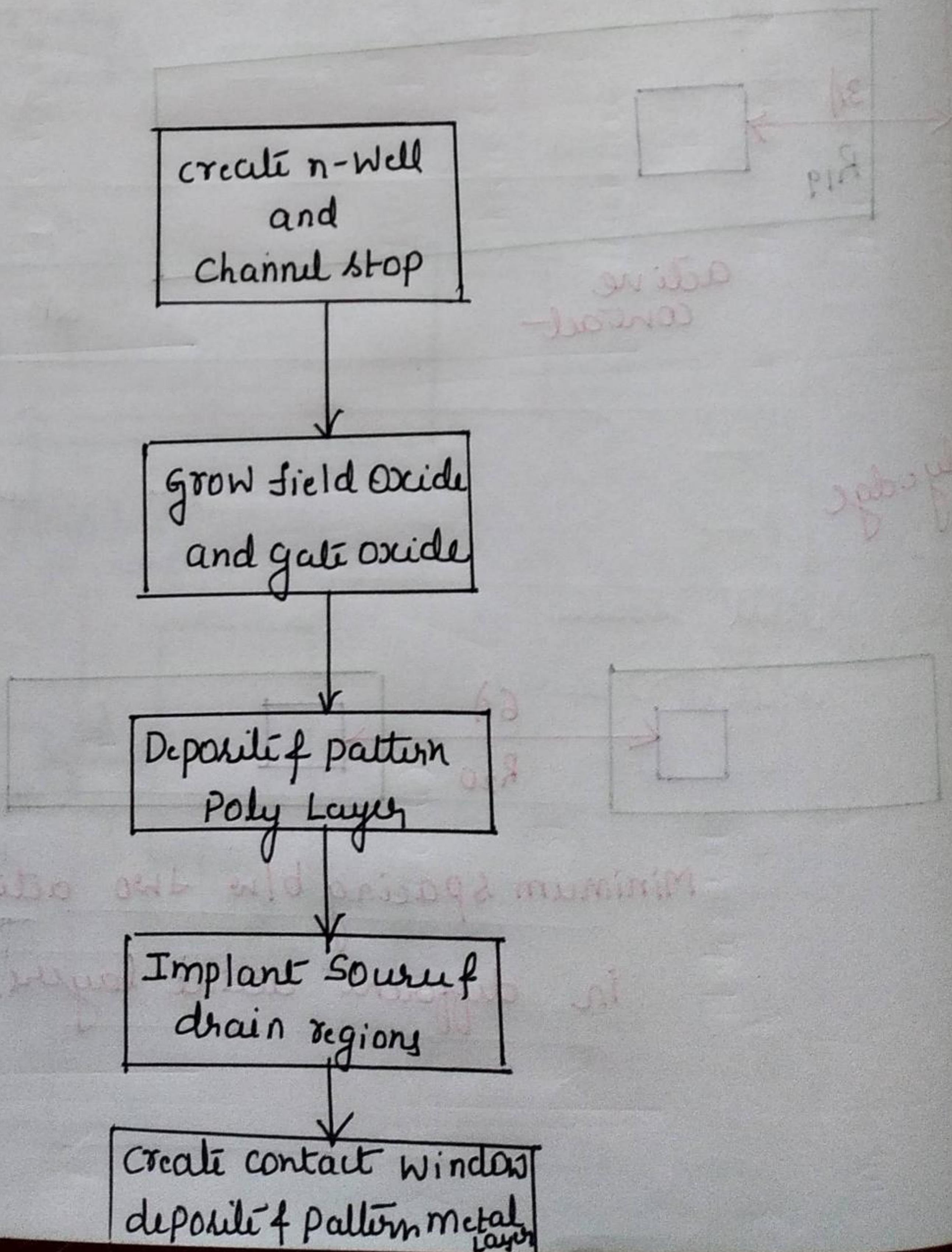
diffusion

Fabrication of MOSFET :-

- i nMOS fabrication
- ii CMOS fabrication
 - 1. n-Well
 - 2. p-Well
 - 3. Twin-tub

Simplified flow graph of n-Well CMOS Subrication

Steps.



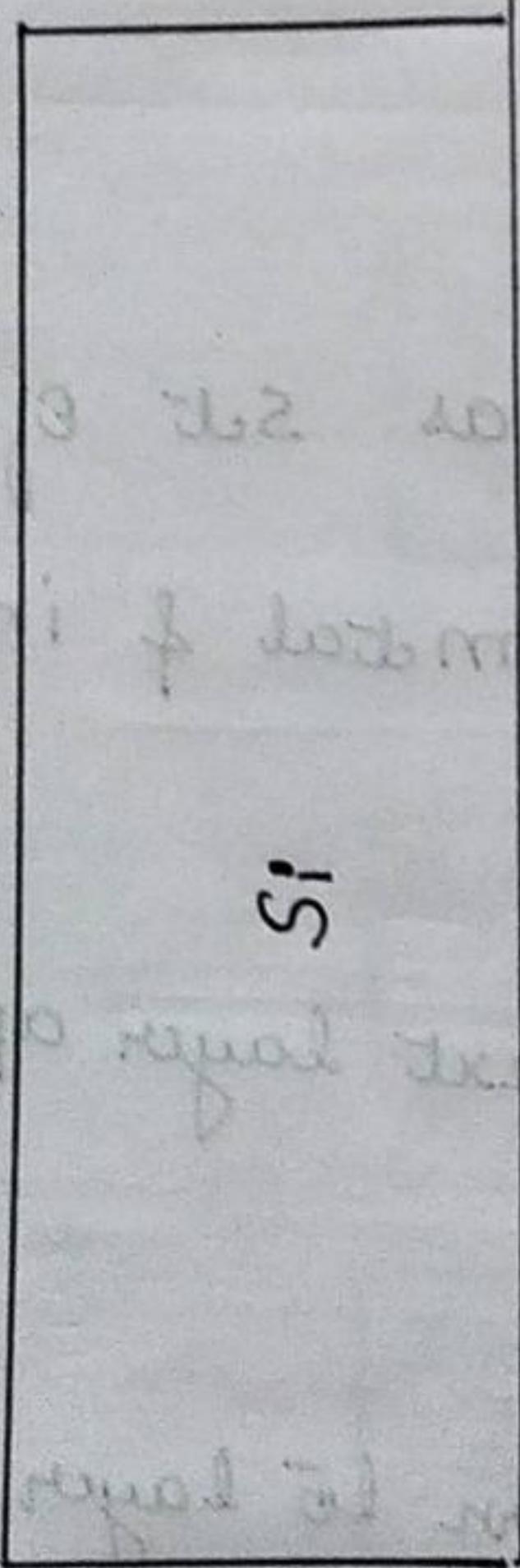
- The simplified process sequence of fabrication of CMOS integrated circuit on P-sub is as shown in figure
- The process starts with creation of n-well region by impurity implantation to substrate.
- A thick Oxide or field Oxide is grown in between MOSFET
- A thin oxide is grown on the surface through thermal oxidation
- These steps are followed by creation of n^+ & p^+ regions
- Metallization for external contacts

Fabrication process flow

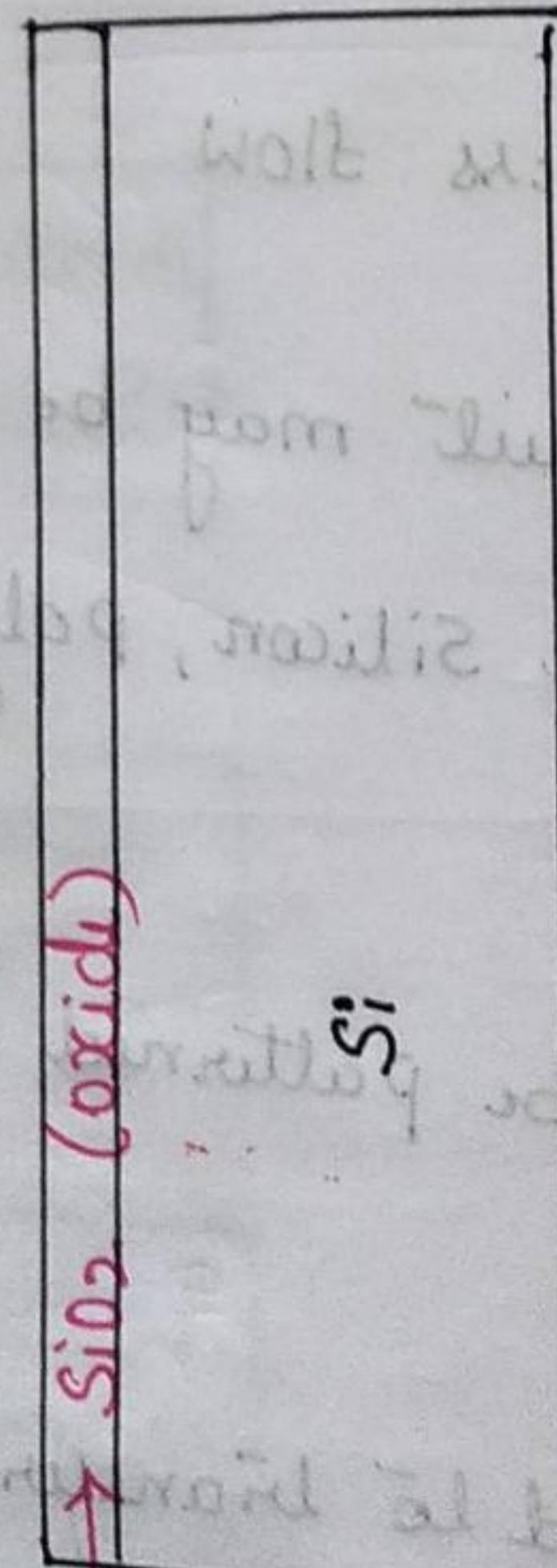
- Integrated circuit may be viewed as set of patterned layer of doped silicon, polysilicon, metal & insulating SiO_2
- A layer must be patterned before next layer applied on chip.
- The process used to transfer a pattern to layer on a chip is called lithography.

Process steps used to patterning of silicon dioxide

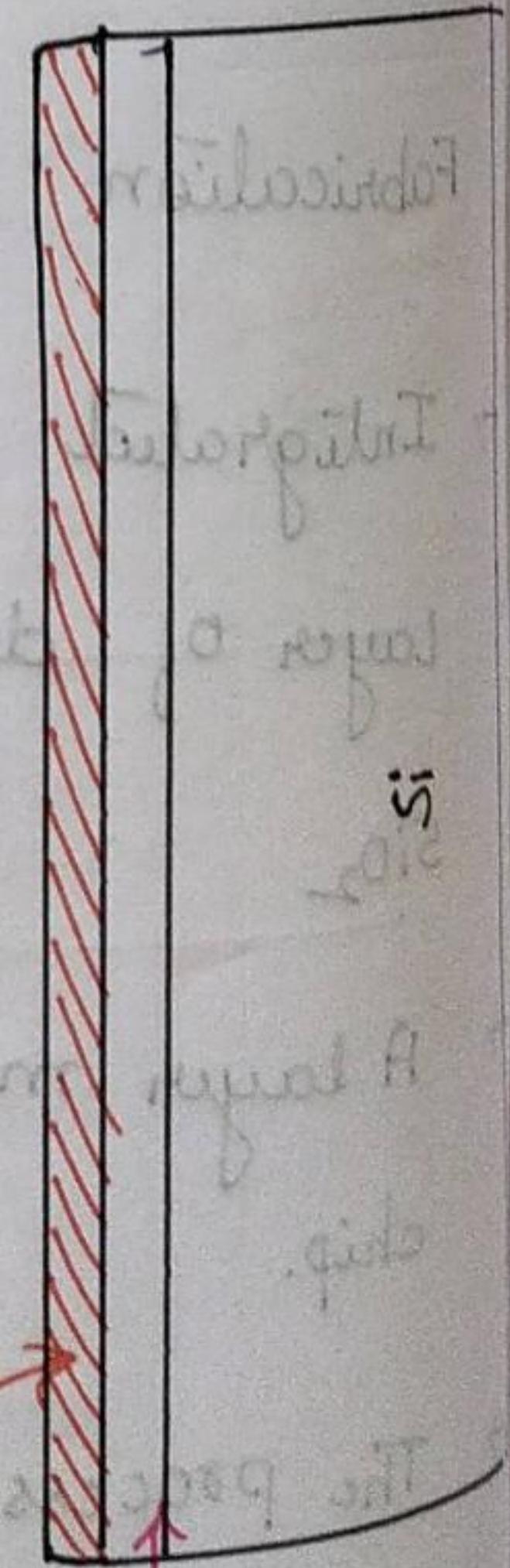
consider a Si substrate



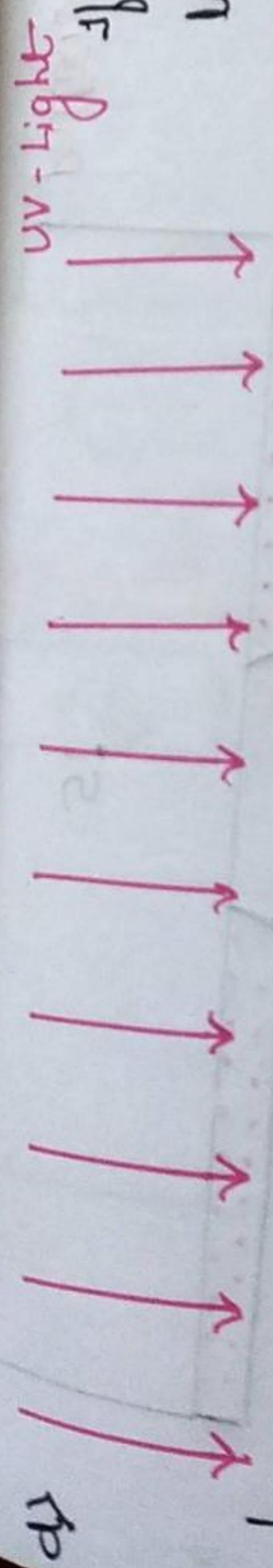
process starts with thermal oxidation of Silicon surface by which Oxide layer of 1mm thickness



Photolith

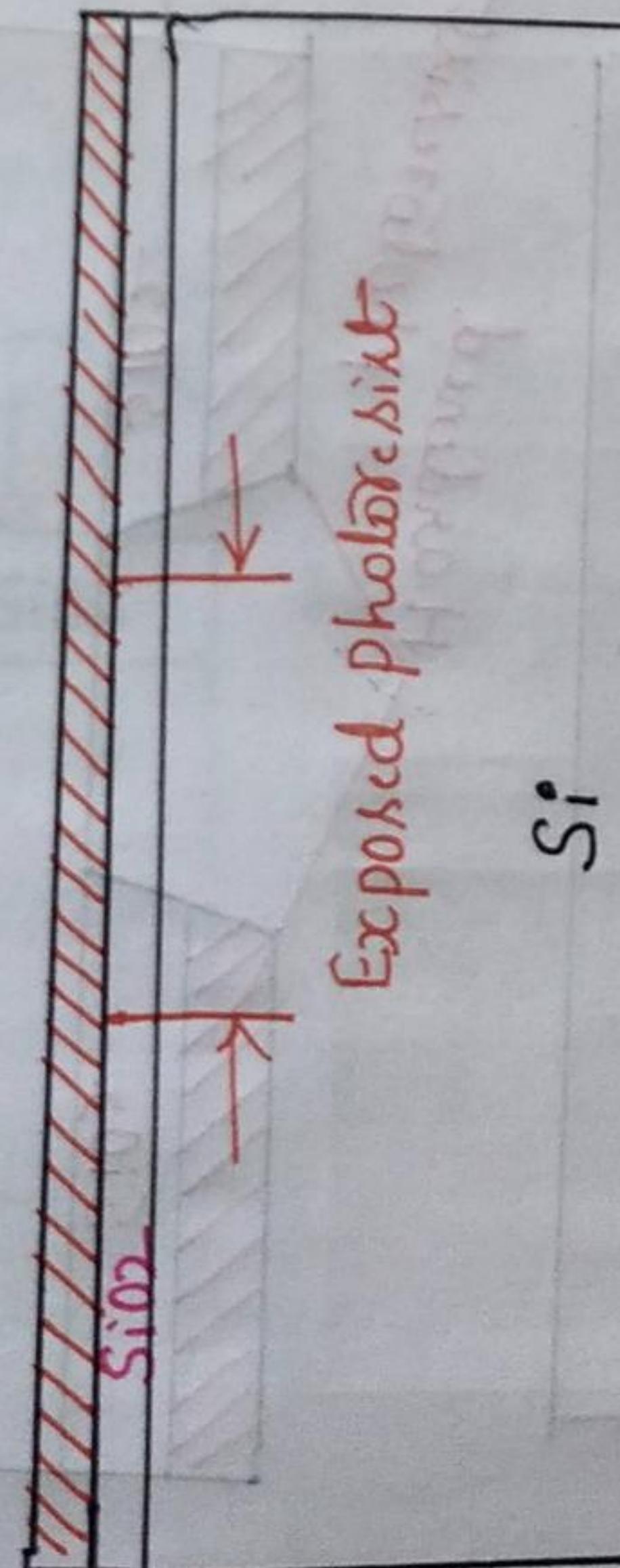


The entire layer is covered with a layer of photoresist material which is essentially light sensitive acid resistant organic polymers



Exposed area becomes soluble to etching solvents.

To selectively expose photoresist material, cover surface with mask.



Type of photoresist which is initially insoluble and becomes soluble after expose it to UV radiation

radical is called +ve photoresist

Type of photoresist which is initially soluble & becomes insoluble after expose it to UV radiation is called -ve photoresist

-ve photoresist are more sensitive but its photolithographic resolution is not high as +ve photoresist

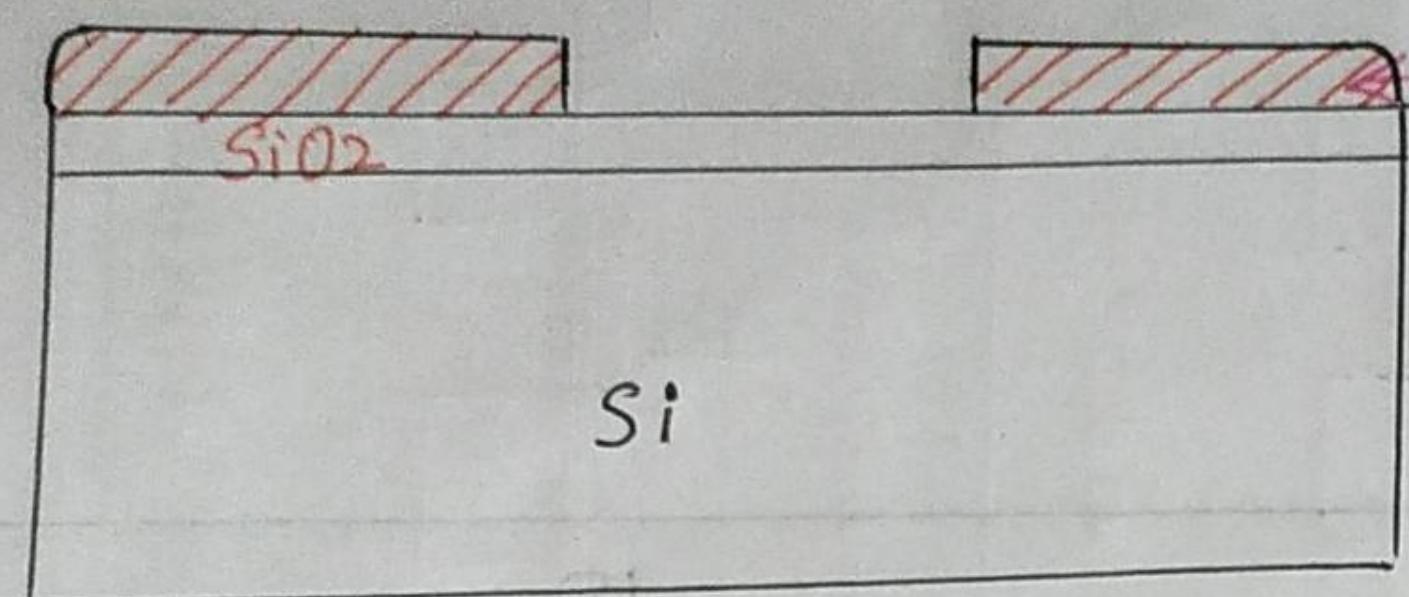
-ve photoresists are less commonly used in IC

↓ ↓ ↓ ↓ ↓ ↓

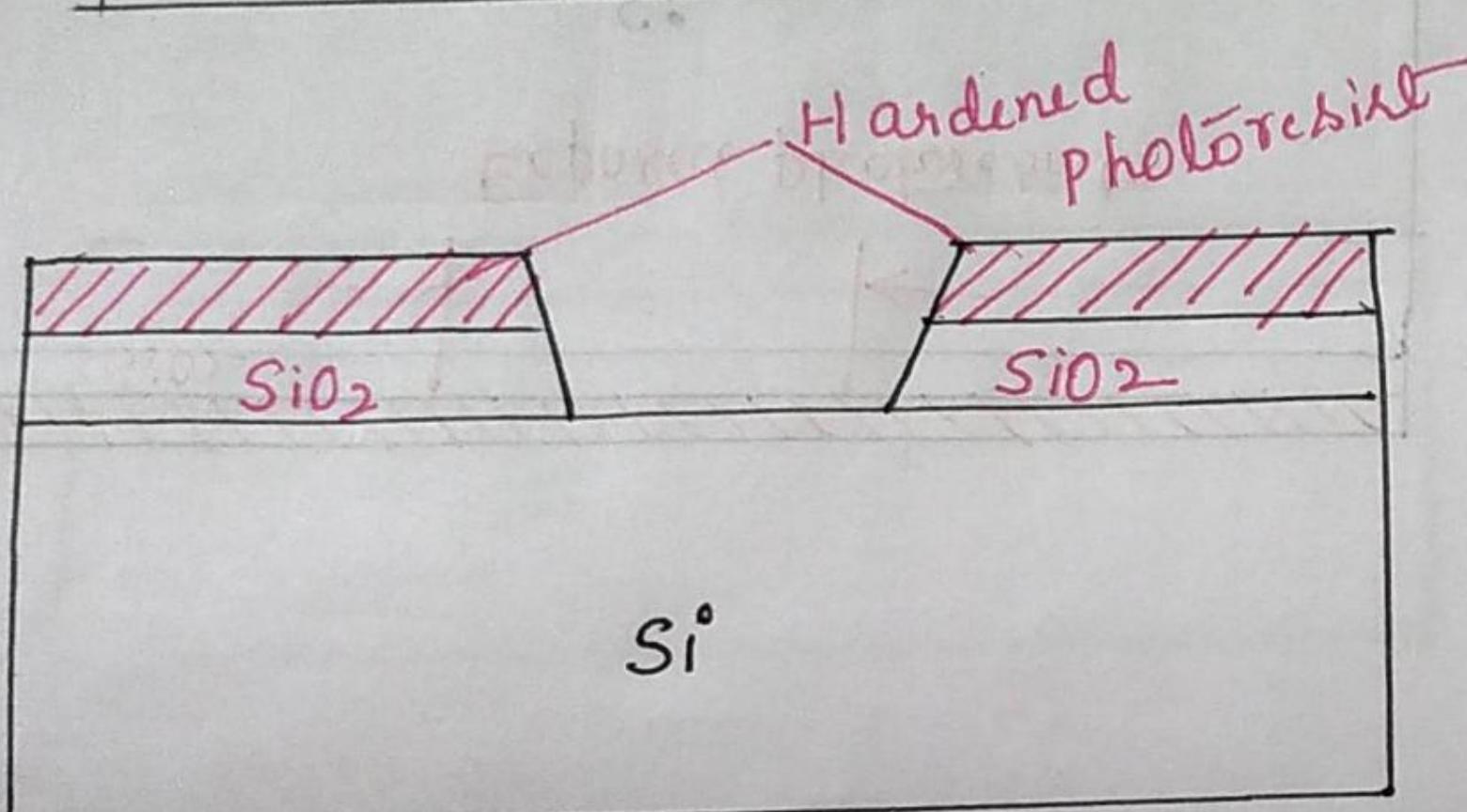
Chemical etch [chemical]

Dry etch [plasma] → Following UV radiation unexposed

portions of photoresist can be removed
by solvent



Hardened photoresist



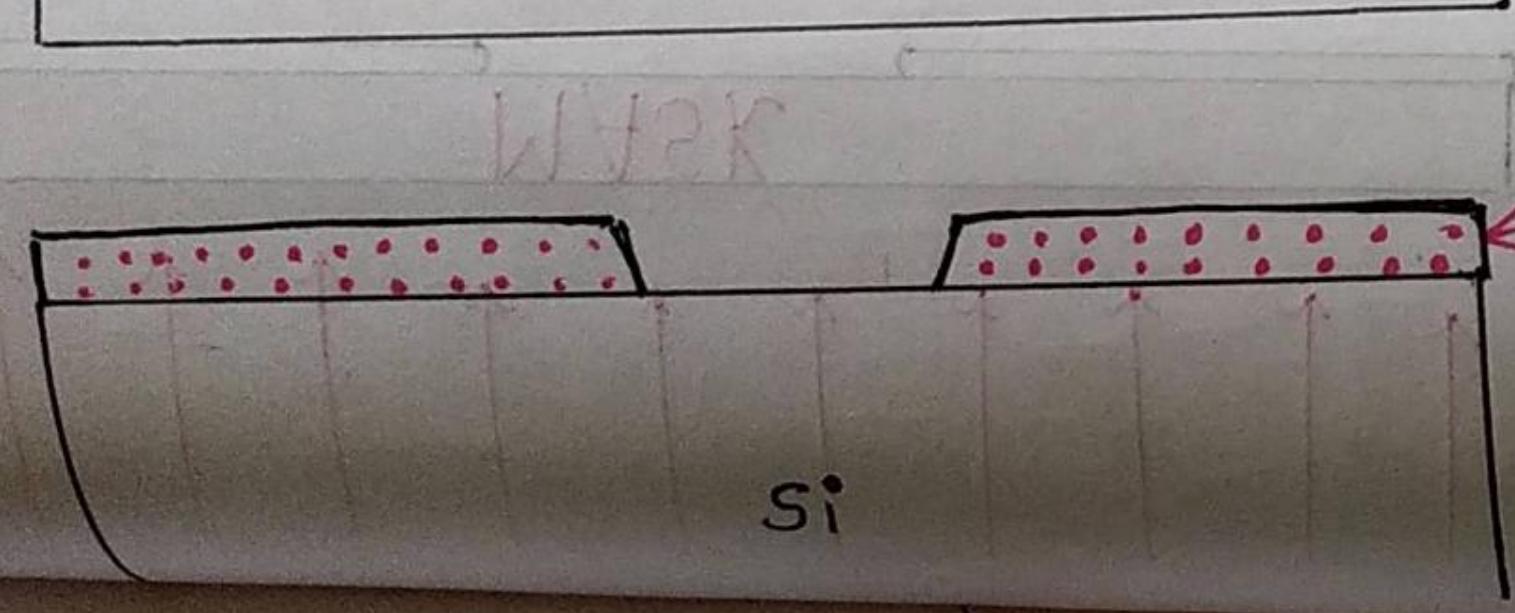
dry etch

→ at the end of this step window is generated that reaches down to silicon surface

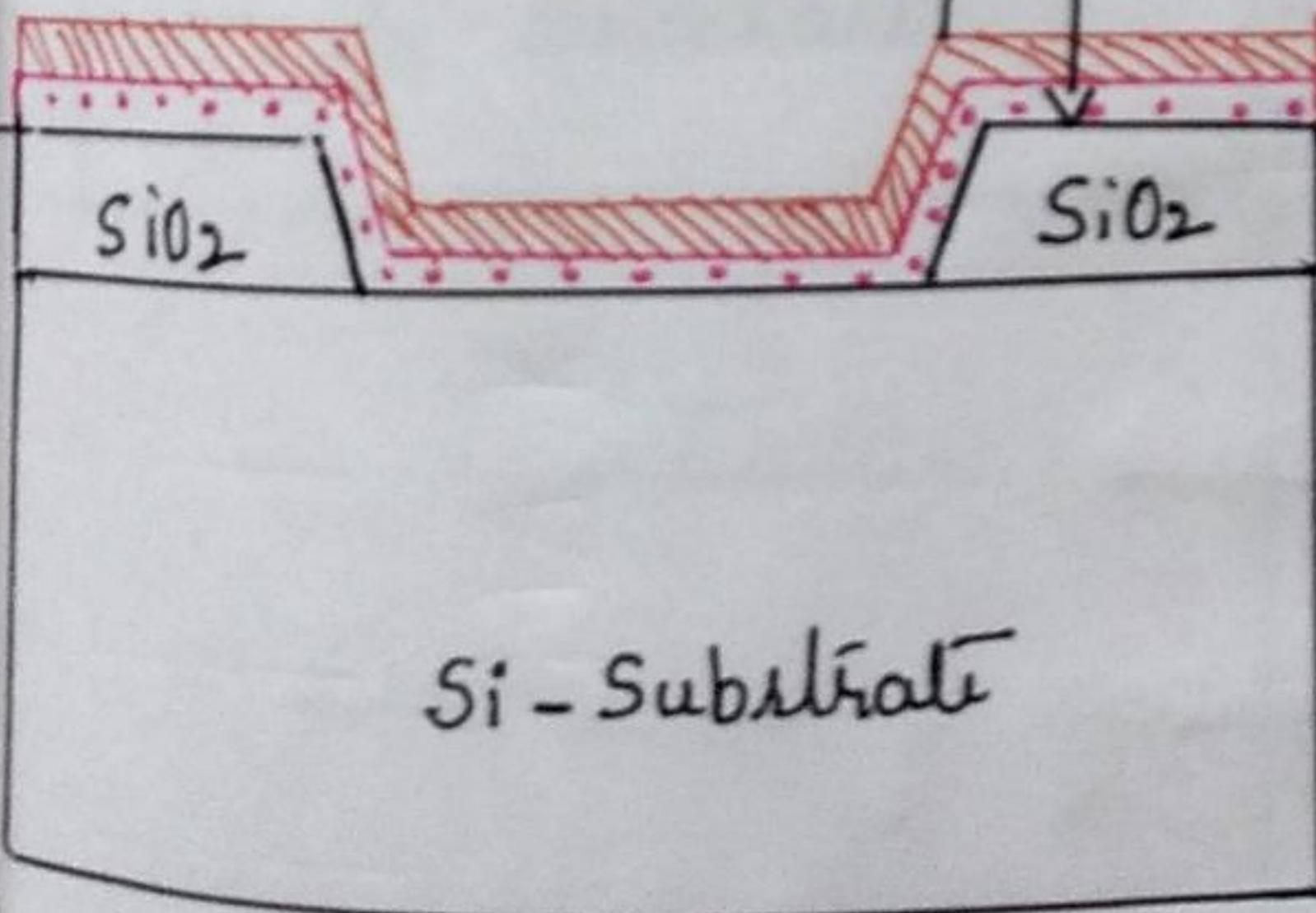
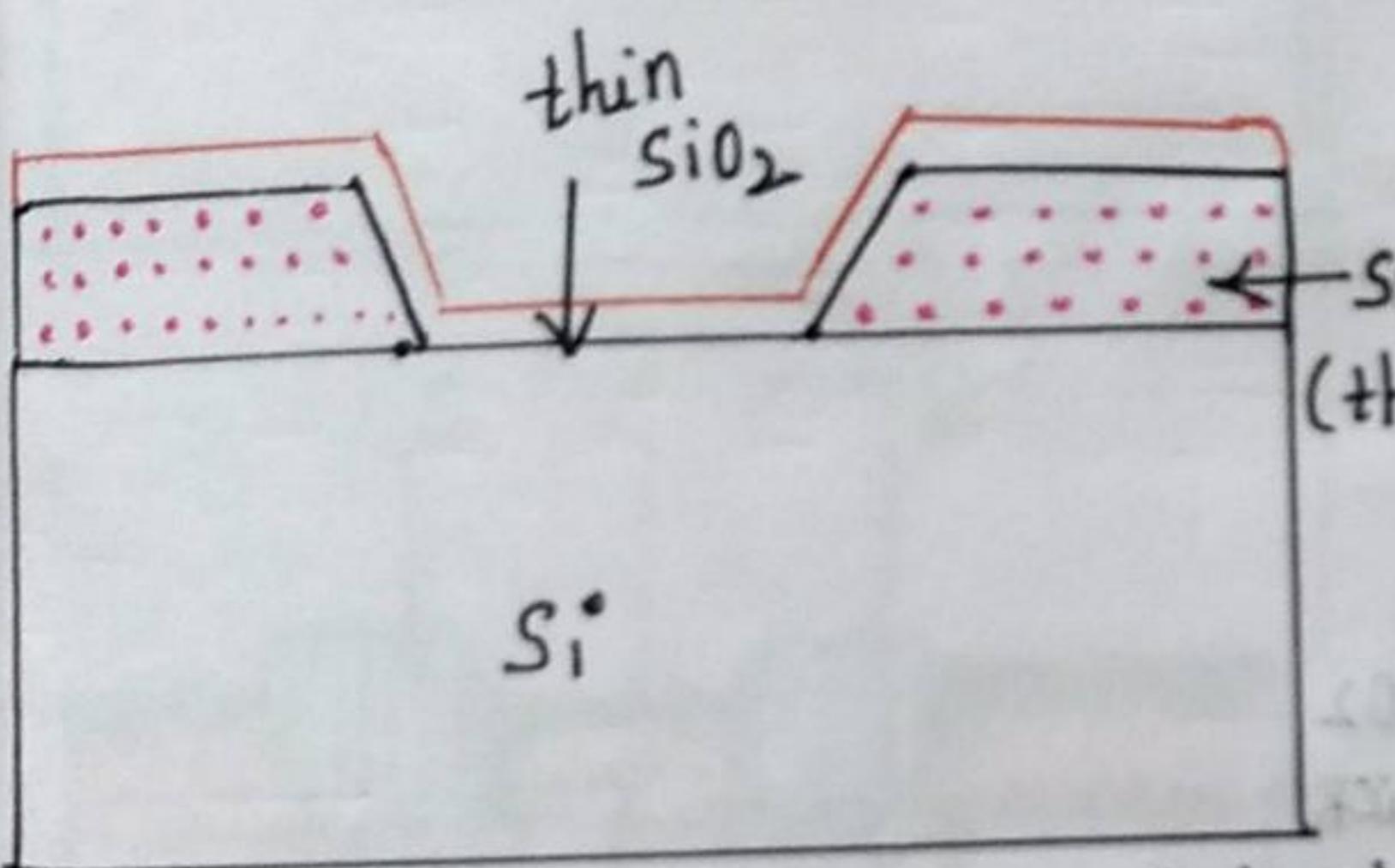
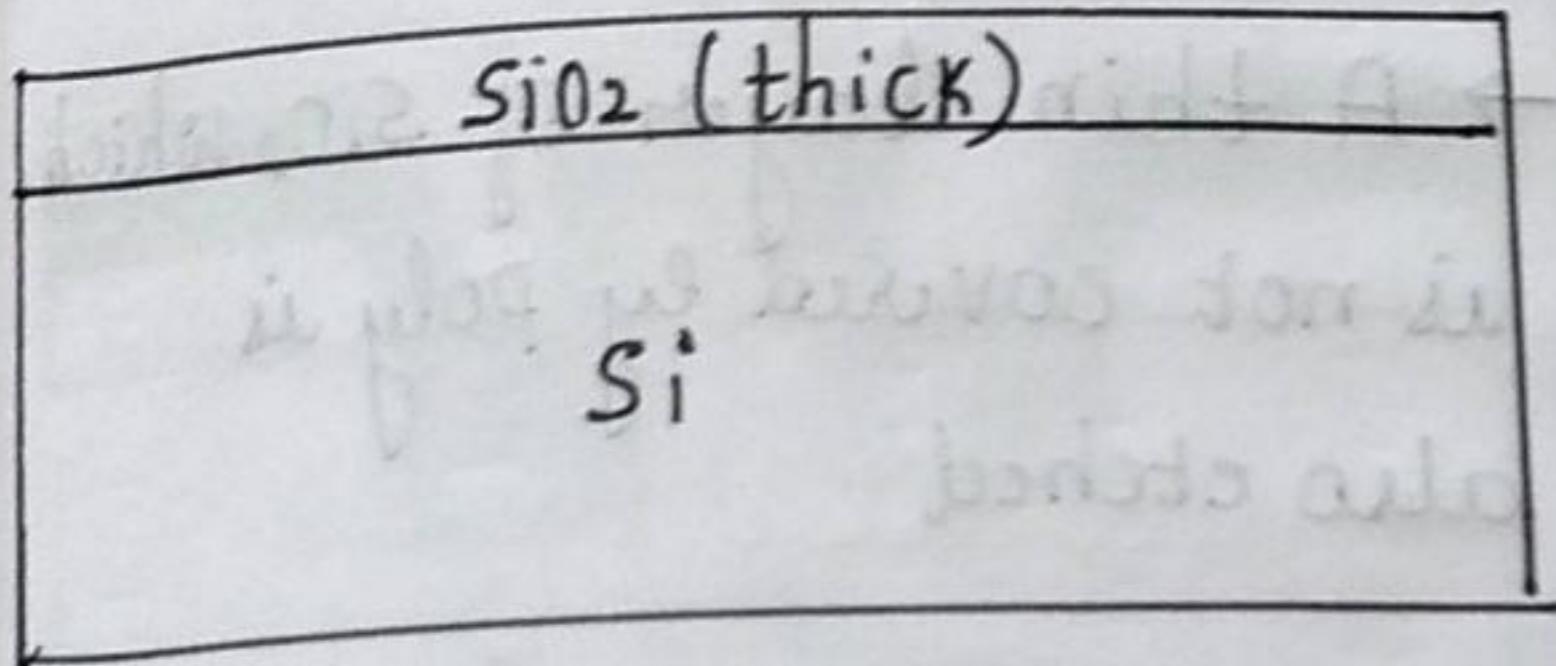
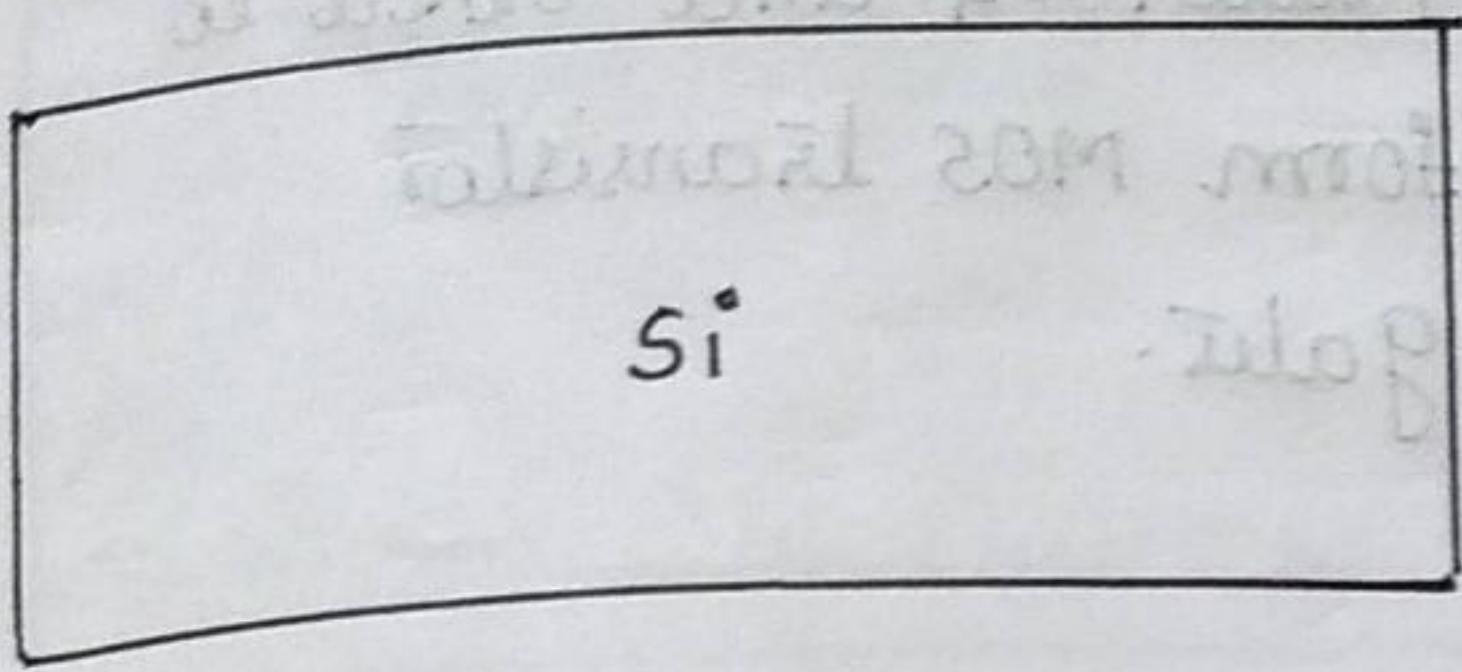
→ The remaining photoresist are removed from SiO₂ from another solvent leaving

Patterned SiO₂ on the surface

Pattern poly



Fabrication of nMOS Transistor



→ Process starts from Oxidation of Silicon substrate

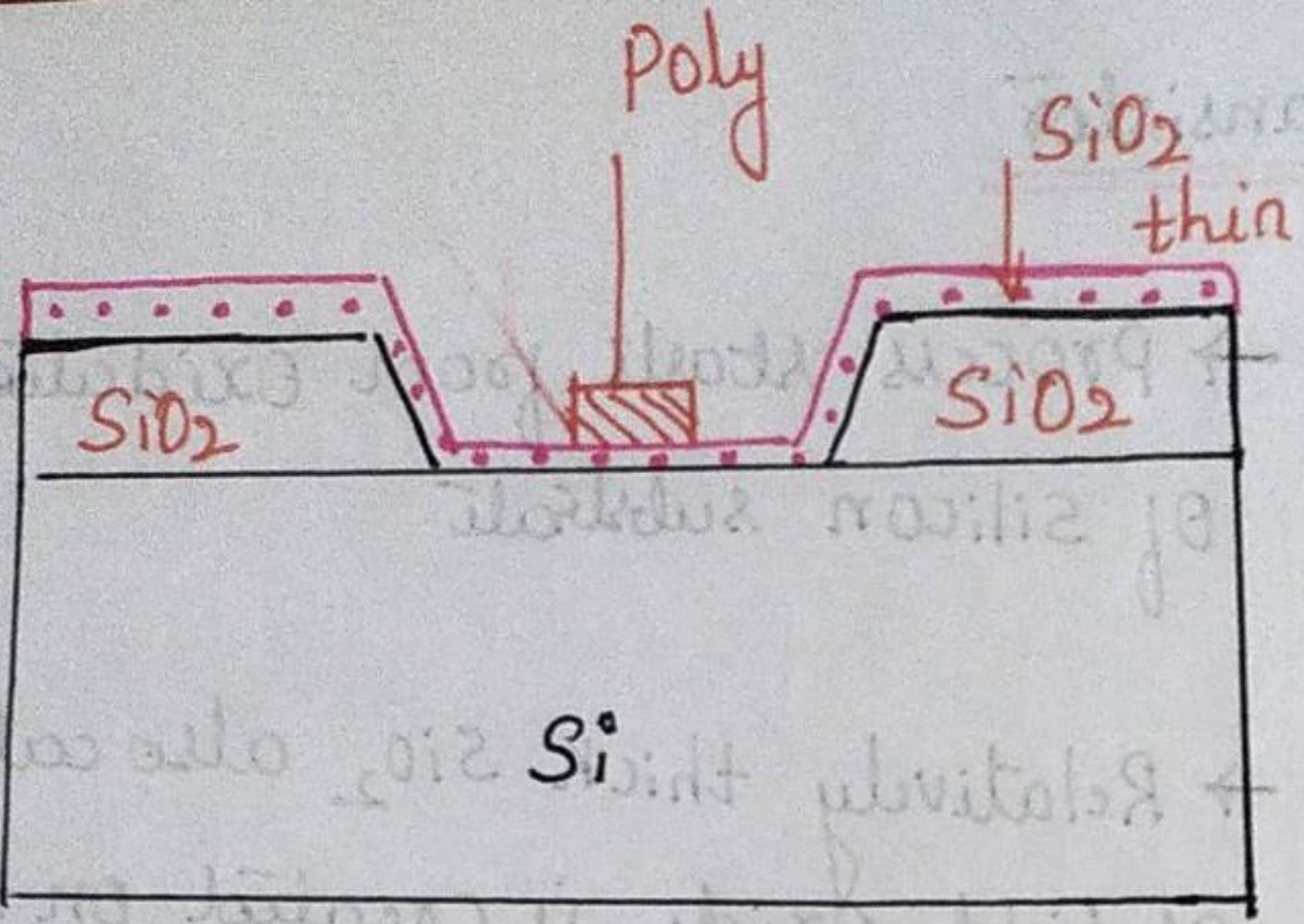
→ Relatively thick SiO₂ also called as field oxide is created on the surface.

→ Field Oxide is selectively etched on which MOS Transistor will be created

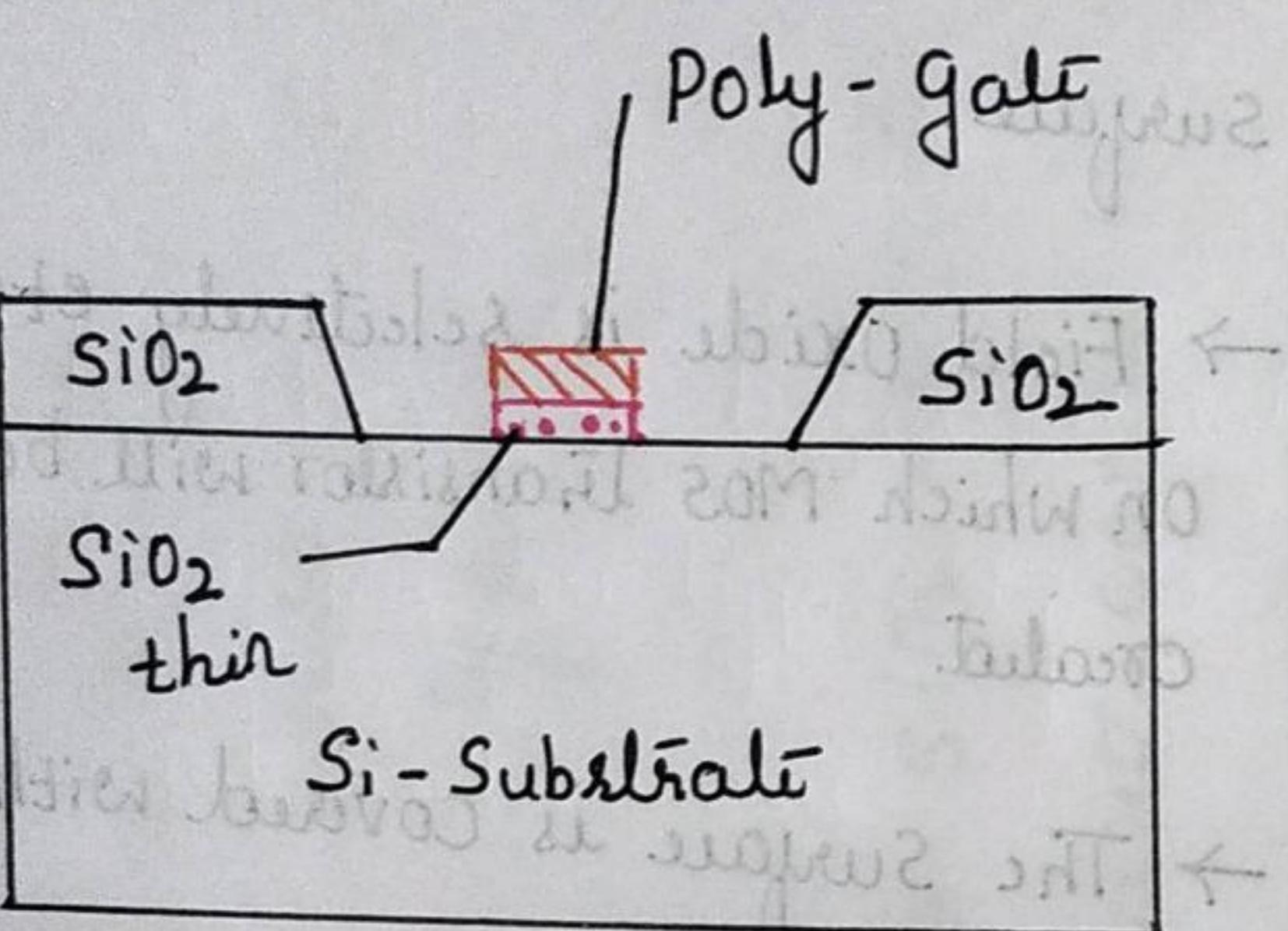
→ The surface is covered with a SiO₂ thin high quality oxide layer (thick) which forms gate oxide of MOS Transistors.

→ on top of thin oxide layer a layer of poly silicon is deposited

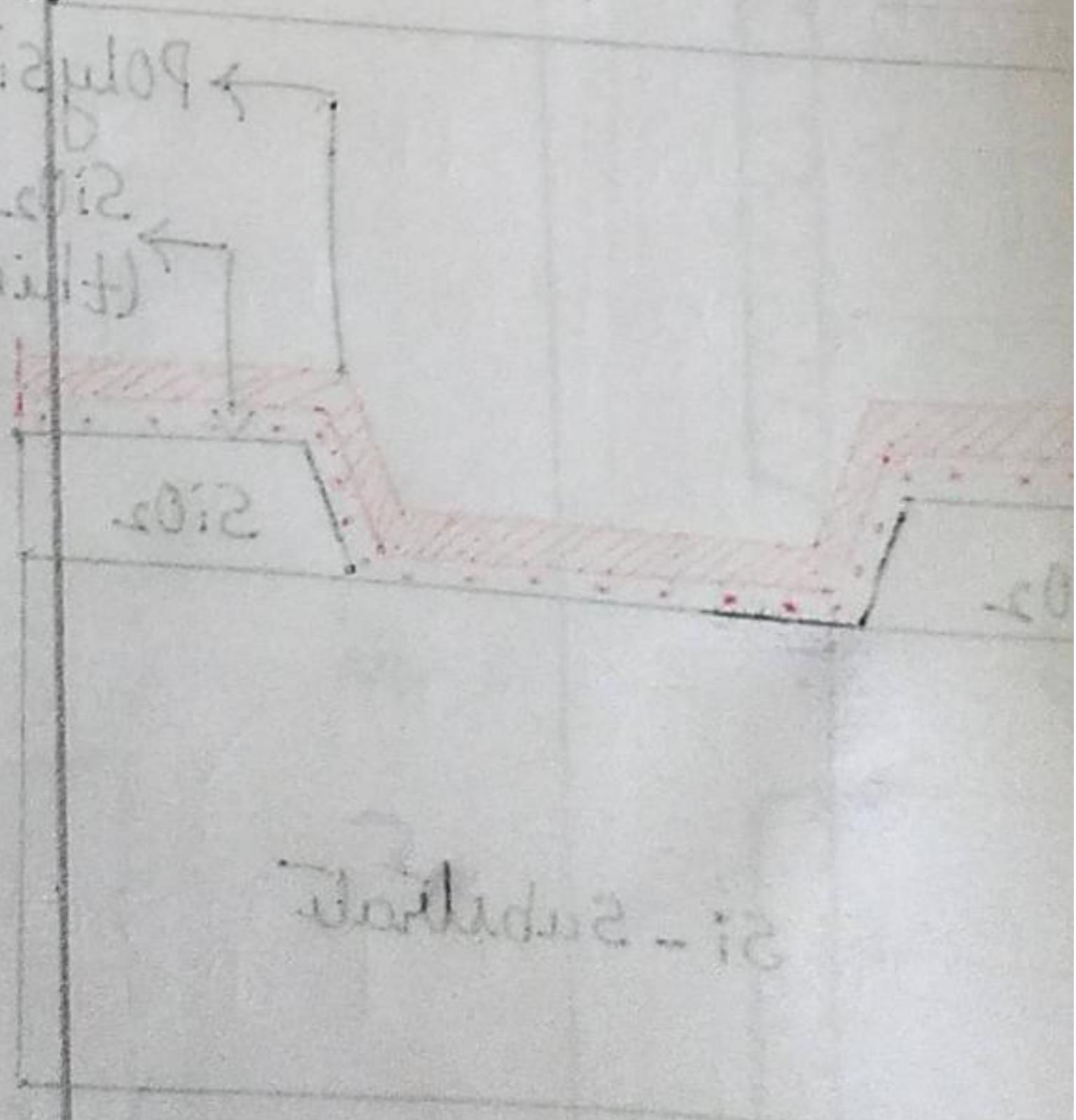
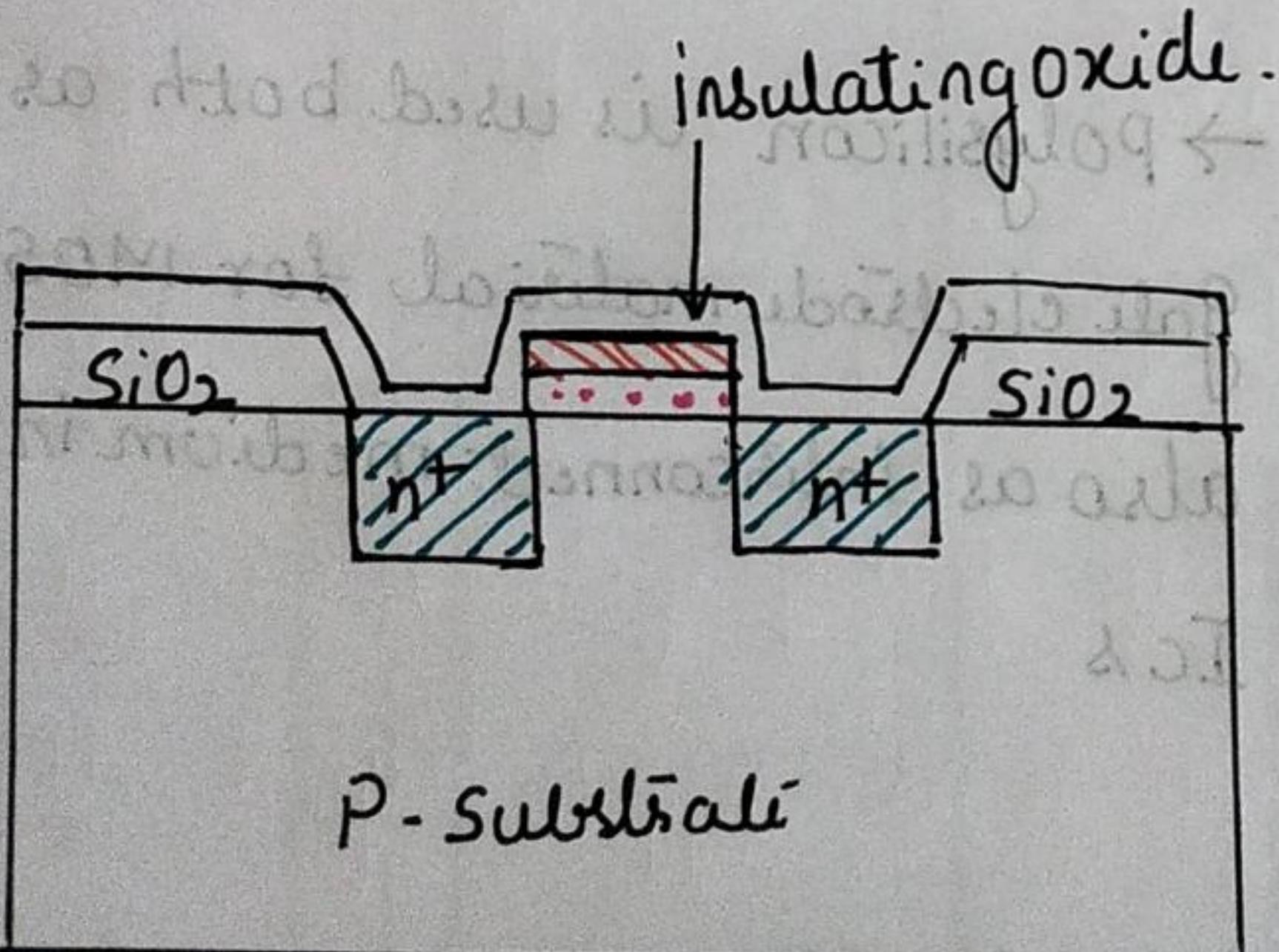
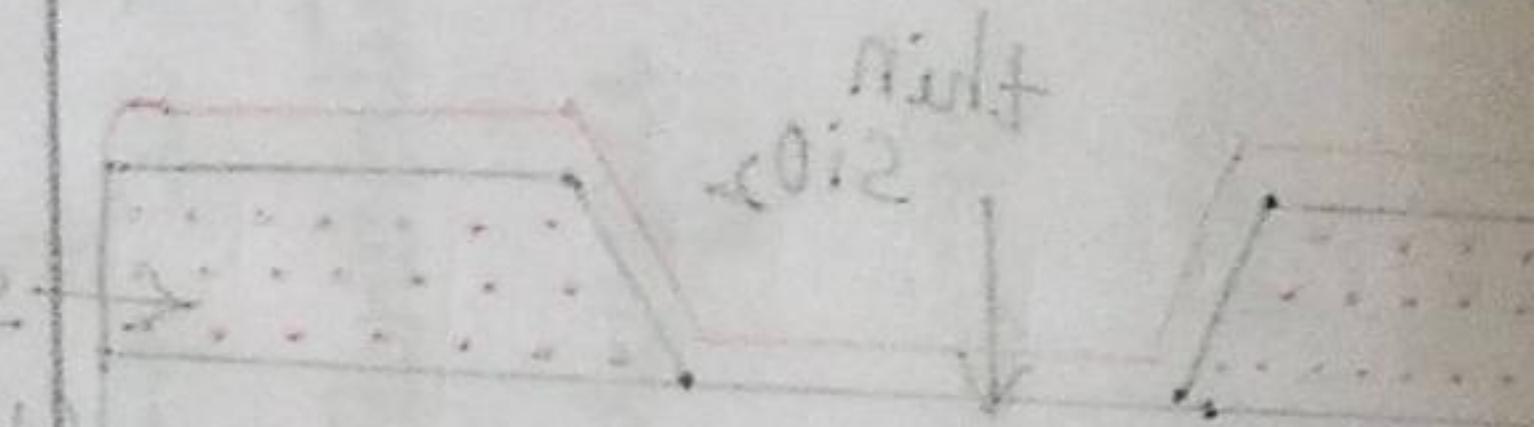
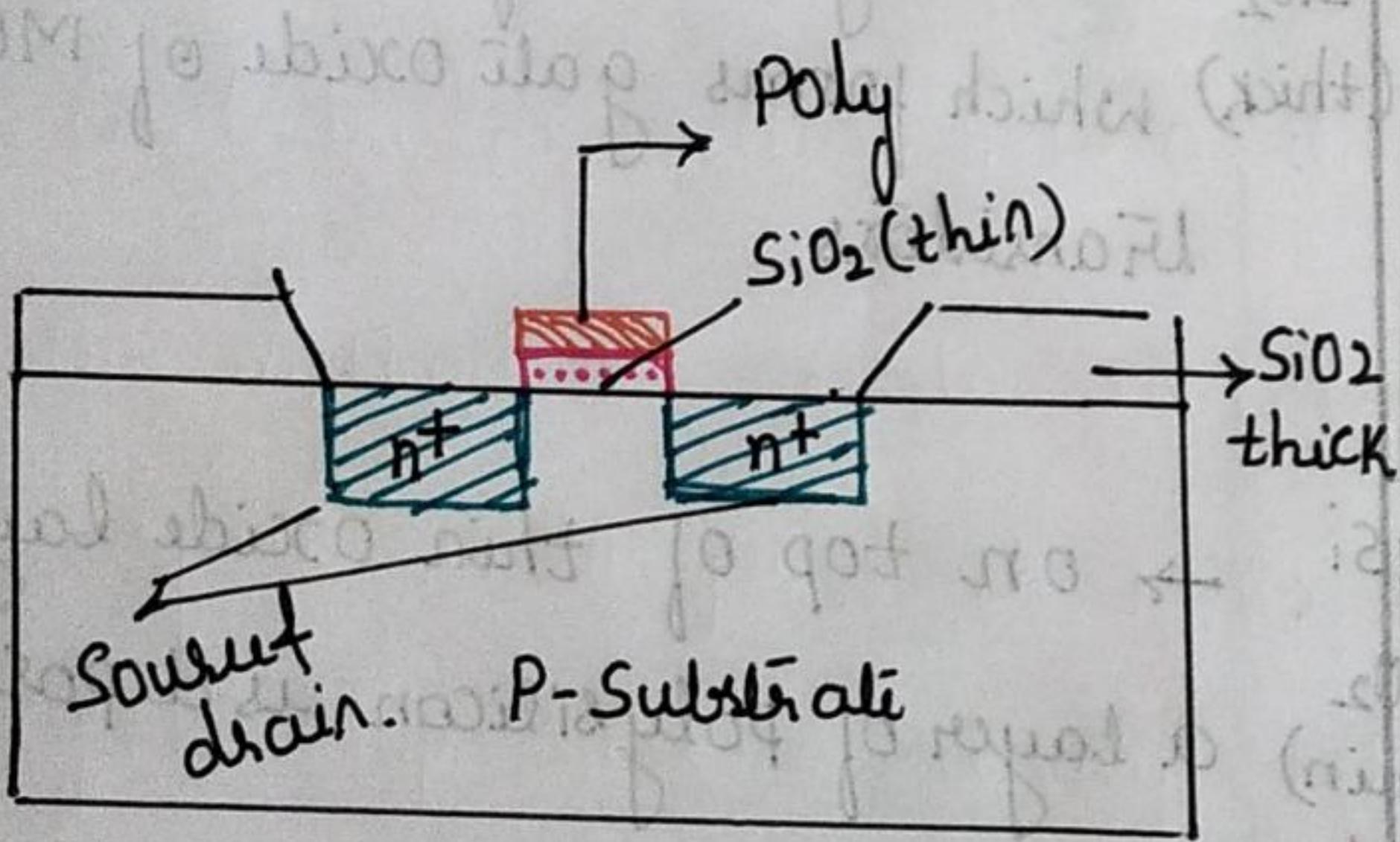
→ polysilicon is used both as gate electrode material for MOSFET also as interconnect medium in ICs

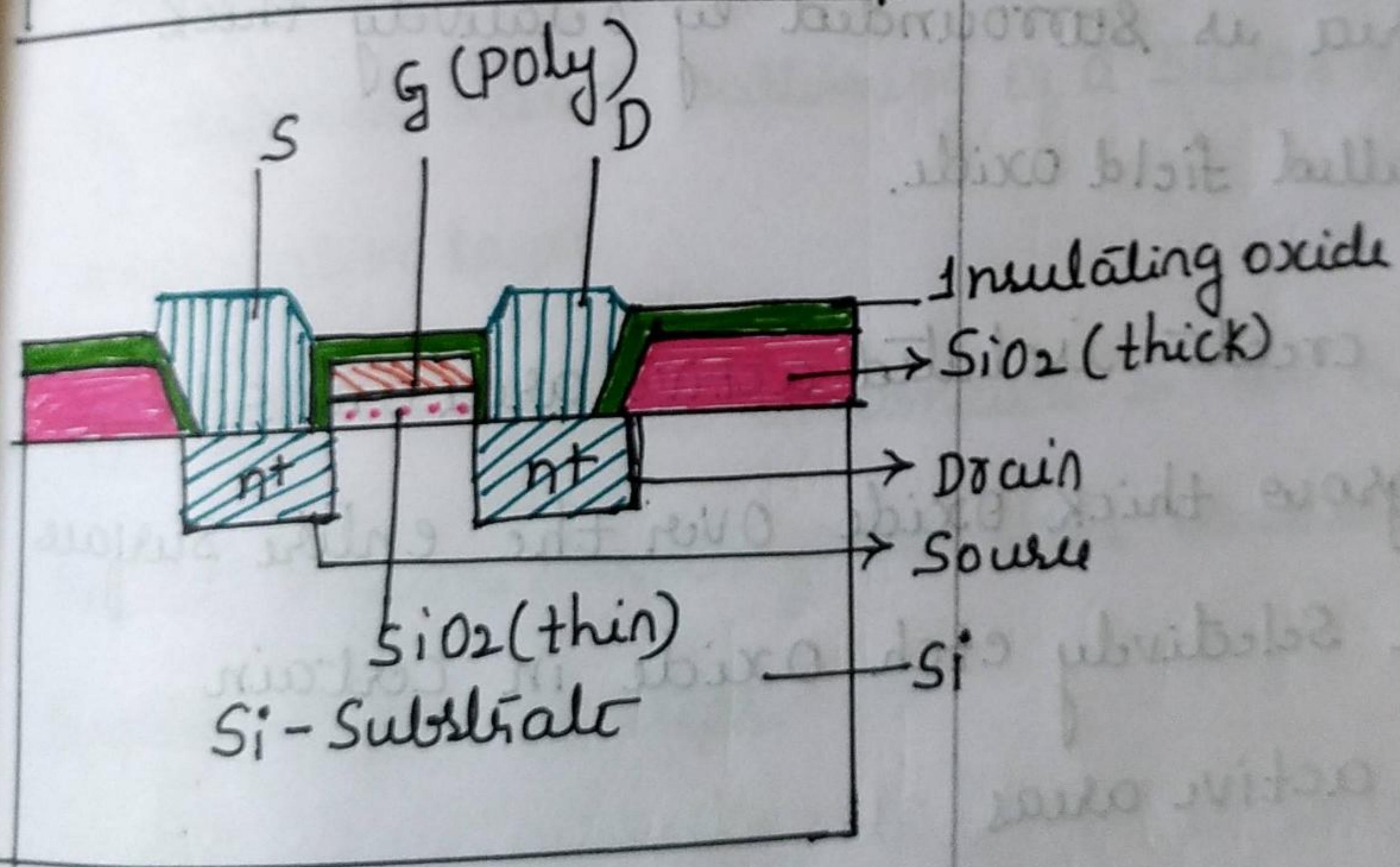
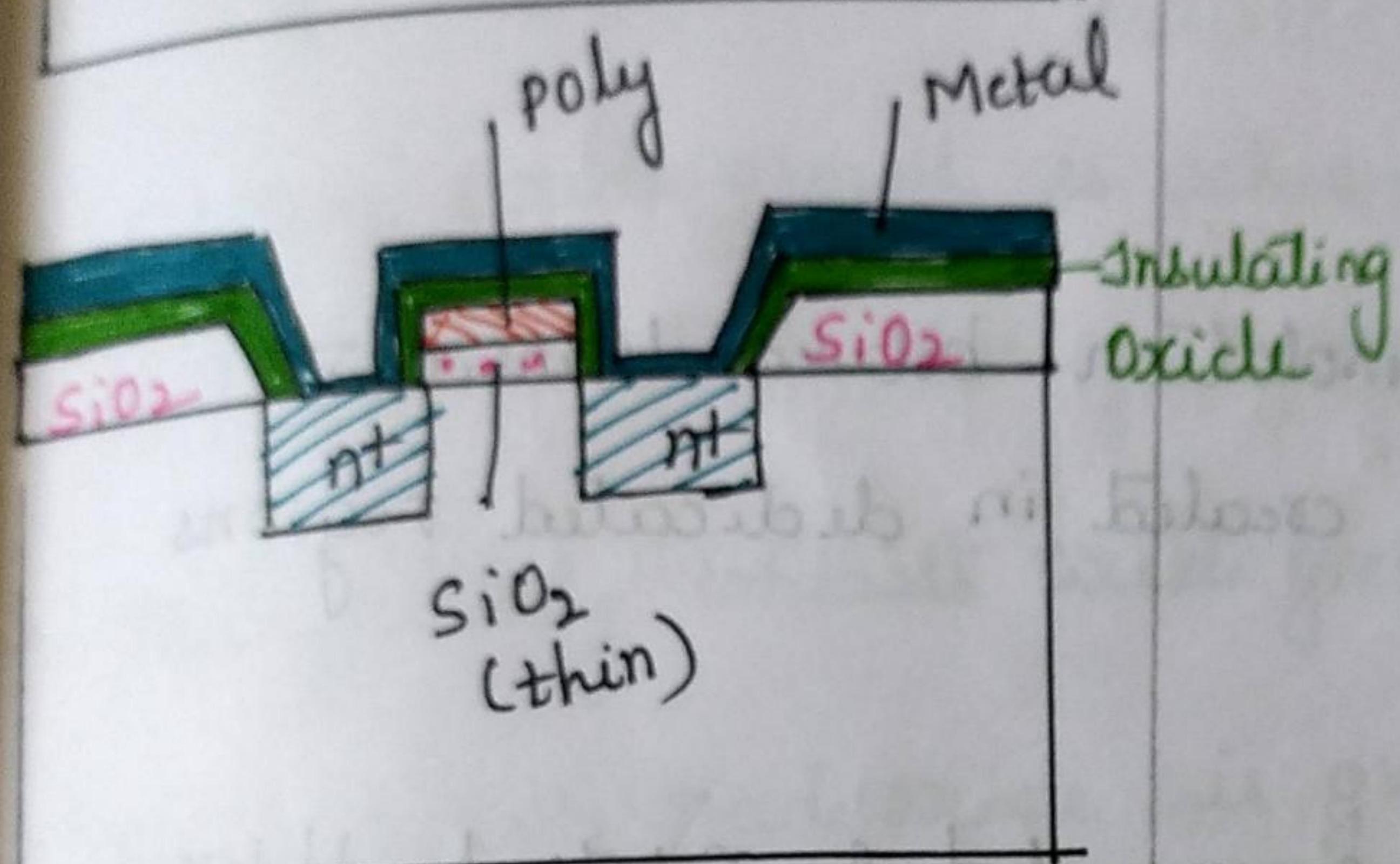
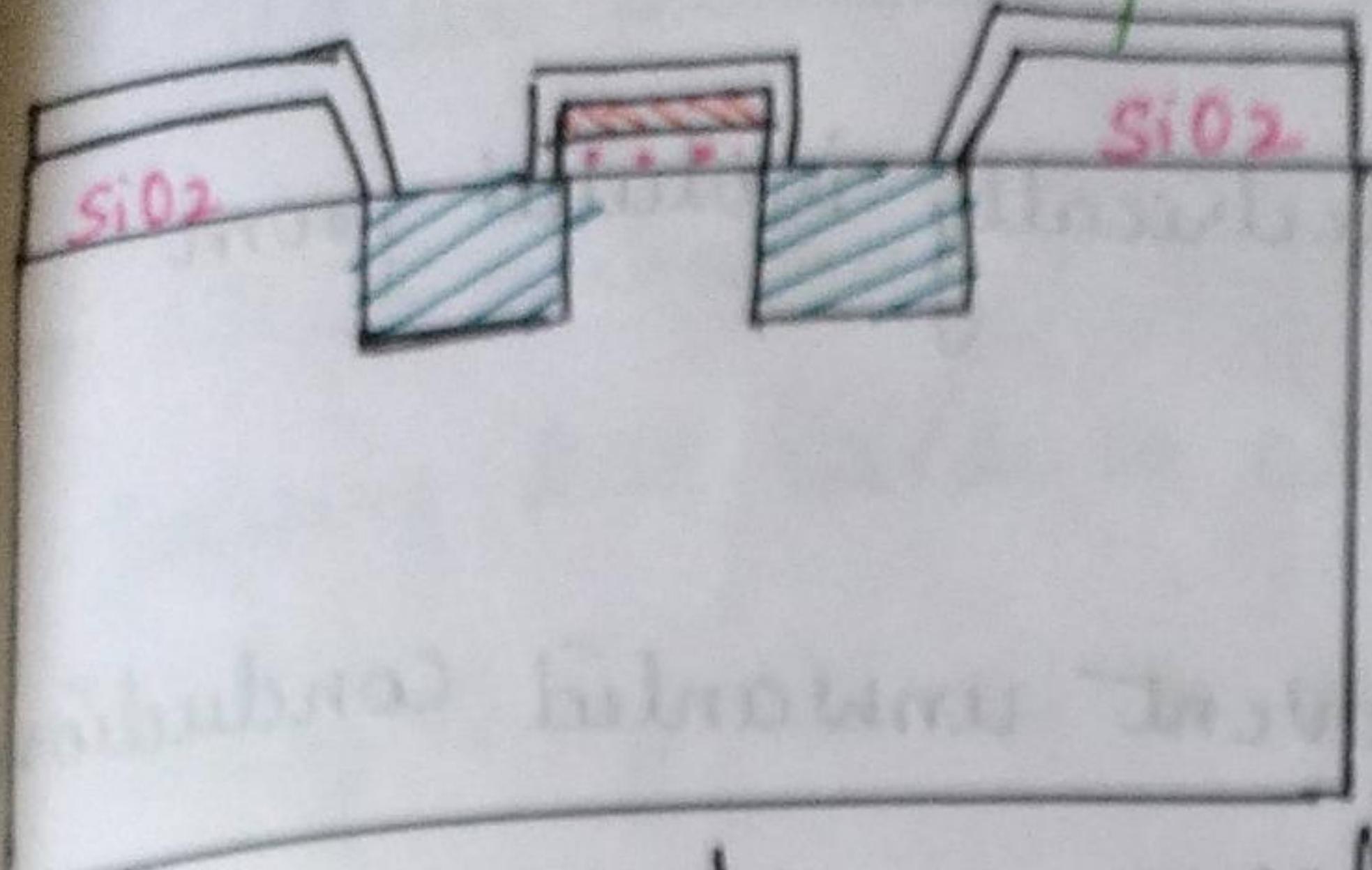


→ Polysilicon layer is patterned and etched to form MOS transistor gates.



→ A thin layer of SiO_2 which is not covered by poly is also etched



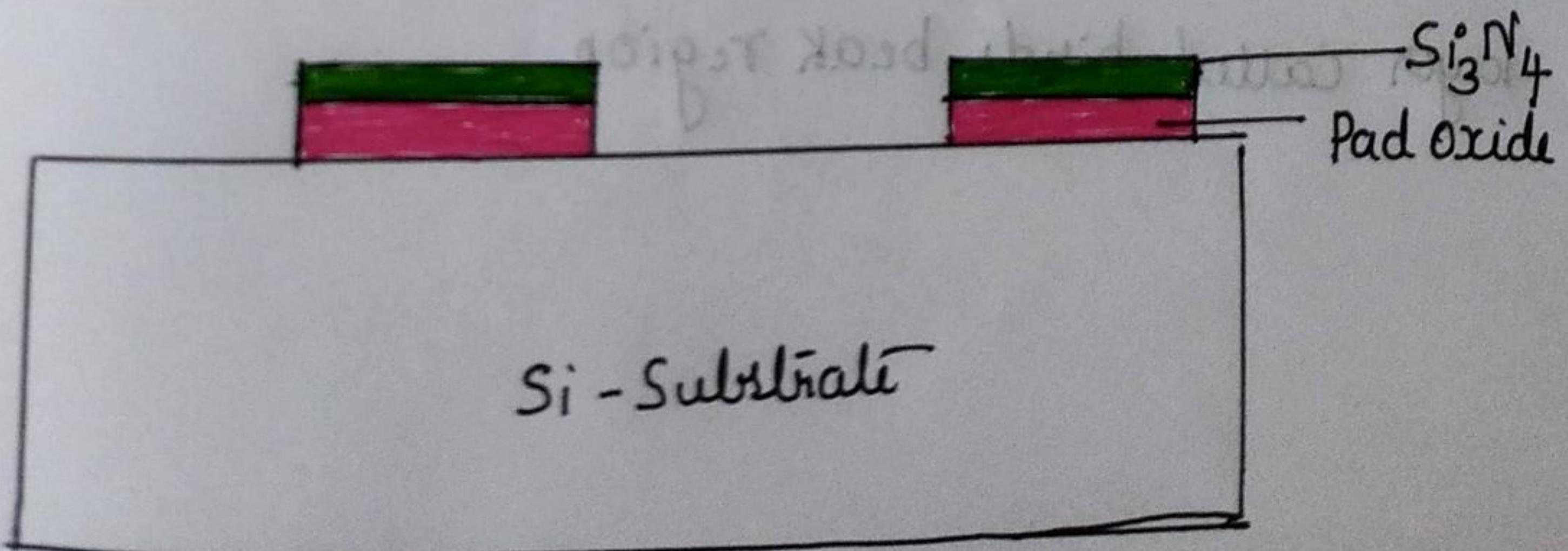


Device isolation techniques

- MOSFET's in IC must be electrically isolated from each other during fabrication.
- Isolations are required to prevent unwanted conductive paths between devices.
- To achieve electrical isolation between transistors the devices are typically created in dedicated regions called active area
- Each active area is surrounded by relatively thick Oxide barrier called field oxide.
- One method to create isolated active area on Silicon surface is to grow thick Oxide over the entire surface of the chip and Selectively etch oxide in certain region to define active areas
- This is called etched field Oxide isolation
- The most significant disadvantage of thick Oxide is the height difference in the boundary of thick oxide if poly can cause crack and leads to chip failure.

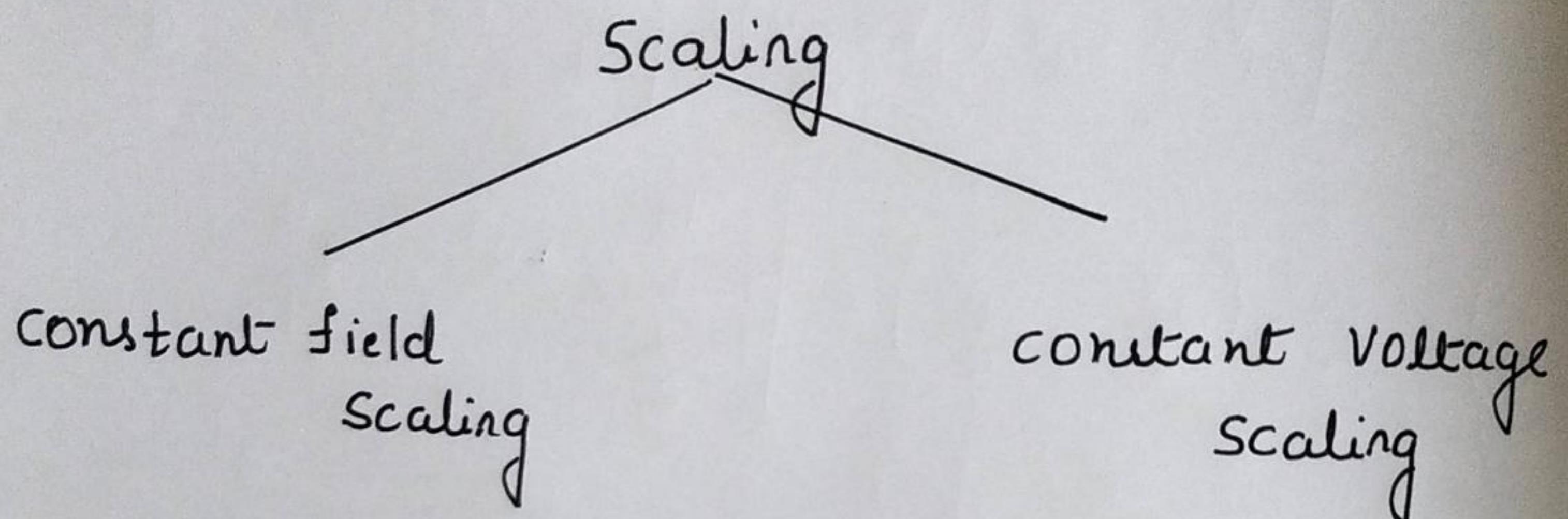
Local Oxidation Of Silicon (LOCOS)

- LOCOS technique is based on the principle of selectively growing field oxide in certain regions instead of selectively etching away the active area after oxide growth
- Selective oxide growth is achieved by shielding active area with Silicon nitride during oxidation.
- This effectively inhibits oxide growth.
- First a thin pad oxide is grown on Si surface followed by deposition and patterning of a Silicon nitride layer to mask active layer.
- The thin pad oxide underneath silicon nitride is used to protect silicon surface from stress caused by nitride during subsequent process steps.



MOSFET Scaling :-

- The reduction of size i.e. dimension of MOSFET.
Commonly referred as scaling



- Symmetric reduction of overall dimension of the device results in reduction of overall silicon area and thereby increasing overall functional density of chip.
- $S > 1$

I constant field scaling :-

- This scaling attempts to preserve magnitude of internal electric field.
- Dimensions are scaled by a factor of S
- To achieve this goal all Potentials are scaled by a factor of S .

1.	channel length	L	$\frac{L}{S}$
2.	channel width	W	$\frac{W}{S}$
3.	Gate Oxide thickness	t_{ox}	$\frac{t_{ox}}{S}$
4.	junction depth	x_j	$\frac{x_j}{S}$
5.	Power Supply voltage	V_{DD}	$\frac{V_{DD}}{S}$
6.	Threshold voltage	V_{TO}	$\frac{V_{TO}}{S}$
7.	Doping density	N_D	$N_D \cdot S.$

→ constant field $E = \frac{V}{L} = \frac{V/S}{L/S} = \frac{V}{L}$

→ charge density must be increased by a factor of 5 in order to maintain constant electric field

I Oxide capacitance

⑨ ~~polysilicon thickness~~
for uniform voltage

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = S \cdot \frac{\epsilon_{ox}}{t_{ox}} = S \cdot C_{ox}$$

$\therefore C_{ox} = S \cdot C_{ox}$

II I_D

$$I_D - \text{Linear} = \frac{\kappa n}{2} \left[2(v_{GS} - v_T) v_{DS} - v_{DS}^2 \right]$$

$$I_D' = \mu_n C_{Ox} \cdot \frac{W}{L} \left[2(v_{GS} - v_T) v_{DS} - v_{DS}^2 \right]$$

$$= \mu_n \cdot S \cdot C_{Ox} \cdot \frac{\frac{W}{S}}{\frac{L}{S}} \left[2 \left(\frac{v_{GS}}{S} - \frac{v_T}{S} \right) \frac{v_{DS}}{S} - \left(\frac{v_{DS}}{S} \right)^2 \right]$$

$$\boxed{I_D' = \frac{I_D}{S}}$$

Linear region

$$I_D - \text{Sat} = \mu_n C_{Ox} \frac{W}{L} \left[v_{GS} - v_T \right]^2$$

$$I_D' = \mu_n S \cdot C_{Ox} \frac{\frac{W}{S}}{\frac{L}{S}} \left(\frac{v_{GS}}{S} - \frac{v_T}{S} \right)^2$$

$$\boxed{I_D' = \frac{I_D}{S}}$$

Saturation region.

III P

$$P = V_{DD} \cdot I_D$$

$$P' = \frac{V_{DD}}{S} \cdot \frac{I_D}{S}$$

$$\boxed{P' = \frac{P}{S^2}}$$

Significant reduction of P
is the attractive feature of
full scaling.

$$\frac{\text{Power}}{\text{Area}} = \frac{\frac{P}{S^2}}{\frac{W}{S} \cdot \frac{L}{S}} = \frac{P}{W \cdot L} = \frac{P}{A}$$

$$\boxed{\frac{P'}{A'} = \frac{P}{A}}$$

II constant voltage scaling.

- In constant voltage scaling all dimensions are reduced by a factor of S
- Power supply voltage and terminal voltages are remain unchanged
- Doping density must be increased by a factor of S^2 in order to preserve charge field relations.

Length	L	$\frac{L}{S}$
Width	W	$\frac{W}{S}$
Oxide thickness	t_{Ox}	$\frac{t_{Ox}}{S}$
Junction depth	x_j	x_j/S
Voltage	V_{DD}, V_T	unchanged
Doping density	N_A, N_D	$S^2 N_A$

$$I_{COX} = \frac{q}{A} = \frac{q}{L \cdot W} = \frac{\frac{q}{t_{OX}}}{\frac{W}{S}} = \frac{C_{Ox}}{S}$$

$$C_{Ox} = \frac{\epsilon_{Ox}}{t_{OX}}$$

$$C_{Ox}' = \frac{\epsilon_{Ox}}{t_{OX}} = S \cdot C_{Ox}$$

$$C_{Ox}' = S \cdot C_{Ox}$$

$$\underline{II} \quad I_D - \text{Linear} = \mu_n C_{Ox} \frac{W}{L} \left[2(V_{GS} - V_T) V_{DS} - V_{DS}^2 \right]$$

$$I_D' = \mu_n S C_{Ox} \frac{\frac{W}{S}}{\frac{L}{S}} \left[2(V_{GS} - V_T) V_{DS} - V_{DS}^2 \right]$$

$$I_D' = S I_D$$

$$I_D - \text{Sat} = \mu_n C_{Ox} \frac{W}{L} \left[V_{GS} - V_T \right]^2$$

$$= \mu_n C_{Ox} S \frac{\frac{W}{S}}{\frac{L}{S}} \left(V_{GS} - V_T \right)^2$$

$$I_D' = S I_D$$

$$\underline{III} \quad P = V_{DD} I_D$$

$$P' = V_{DD} \cdot S I_D$$

$$P' = S P$$

$$\underline{IV} \quad \frac{P'}{A'} = \frac{S P}{\frac{W}{S} \cdot \frac{L}{S}}$$

$$\frac{P'}{A'} = S^3 \frac{P}{A}$$

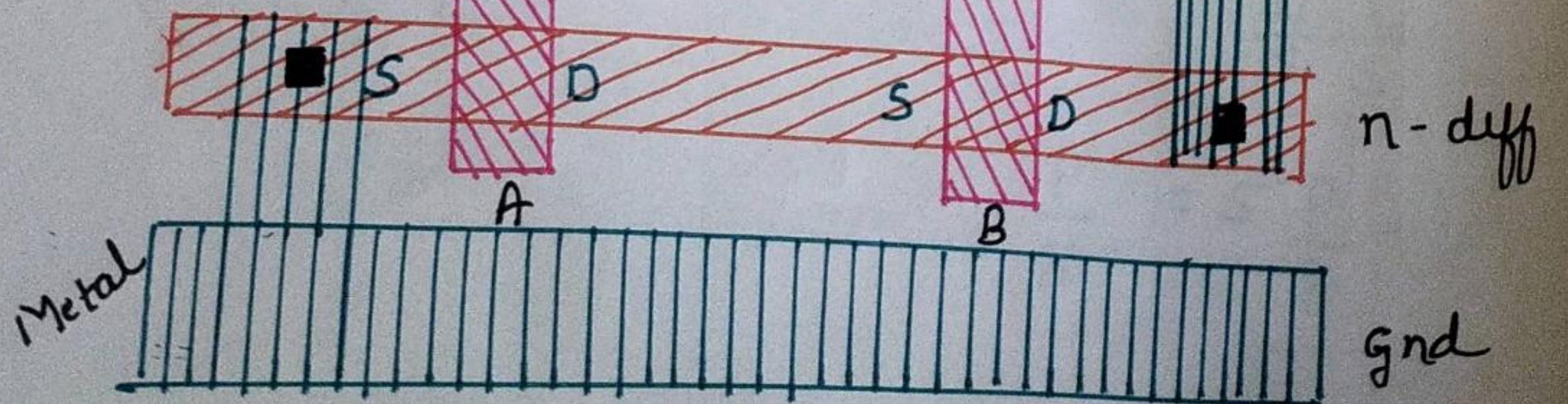
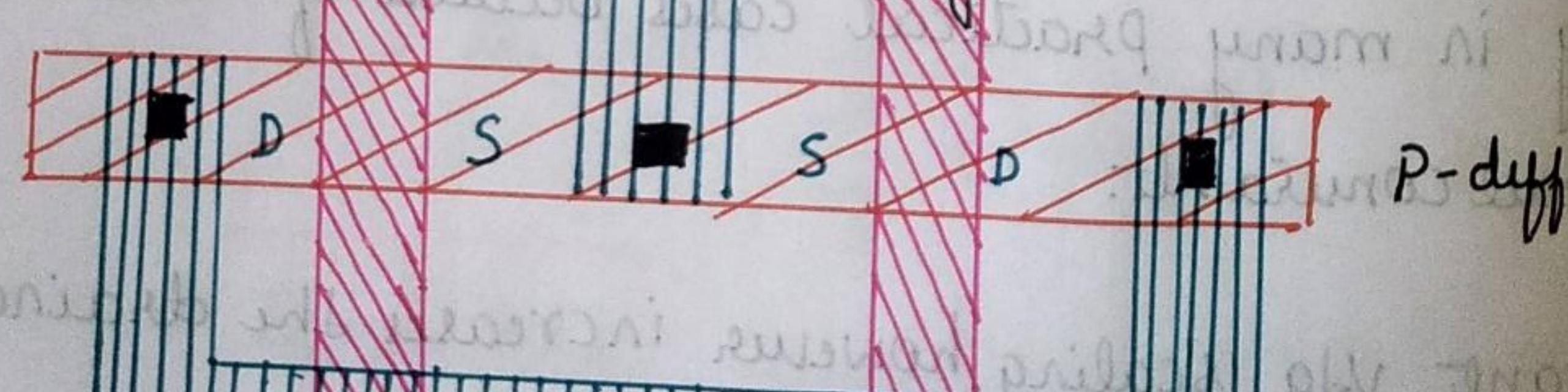
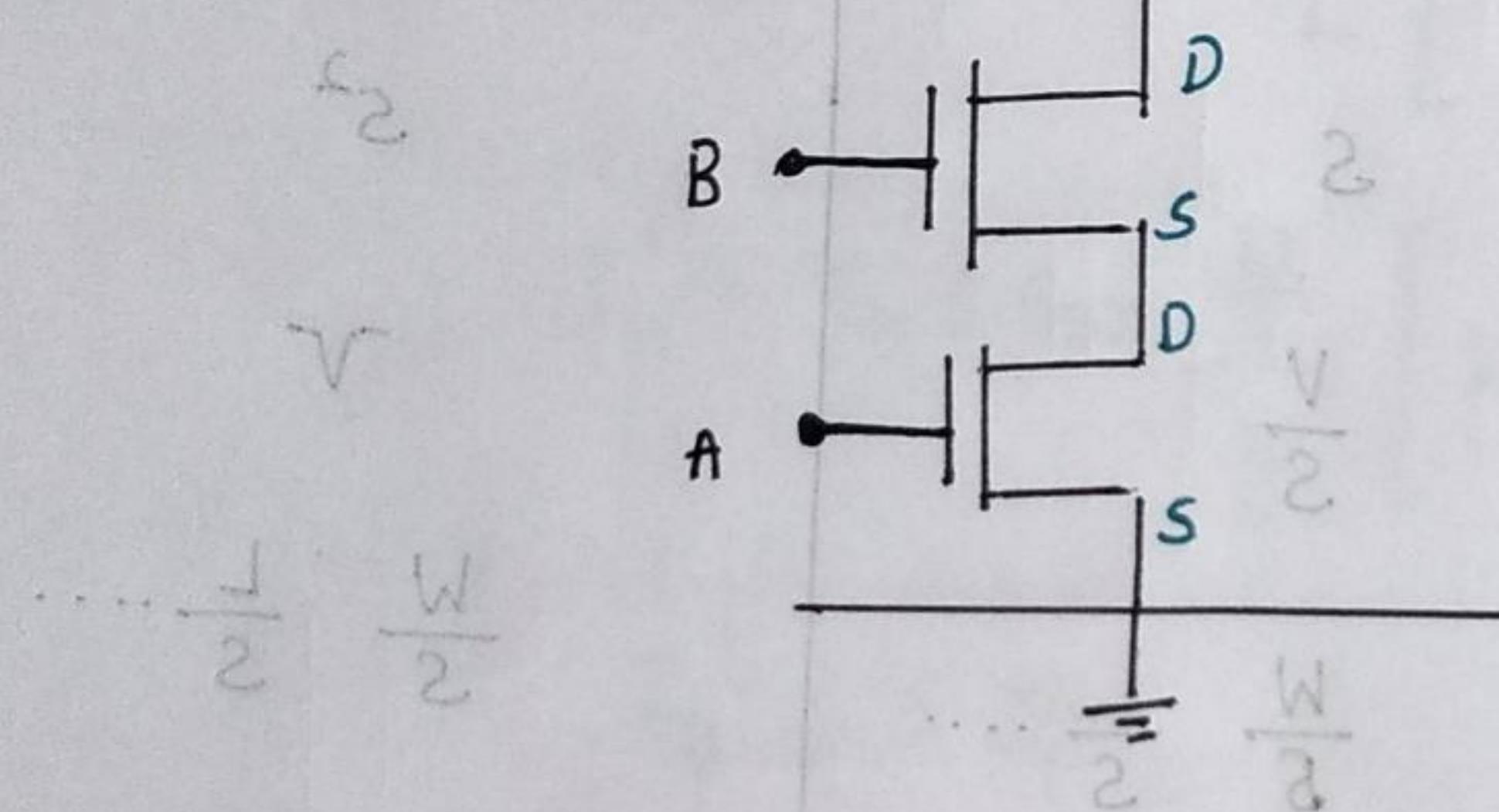
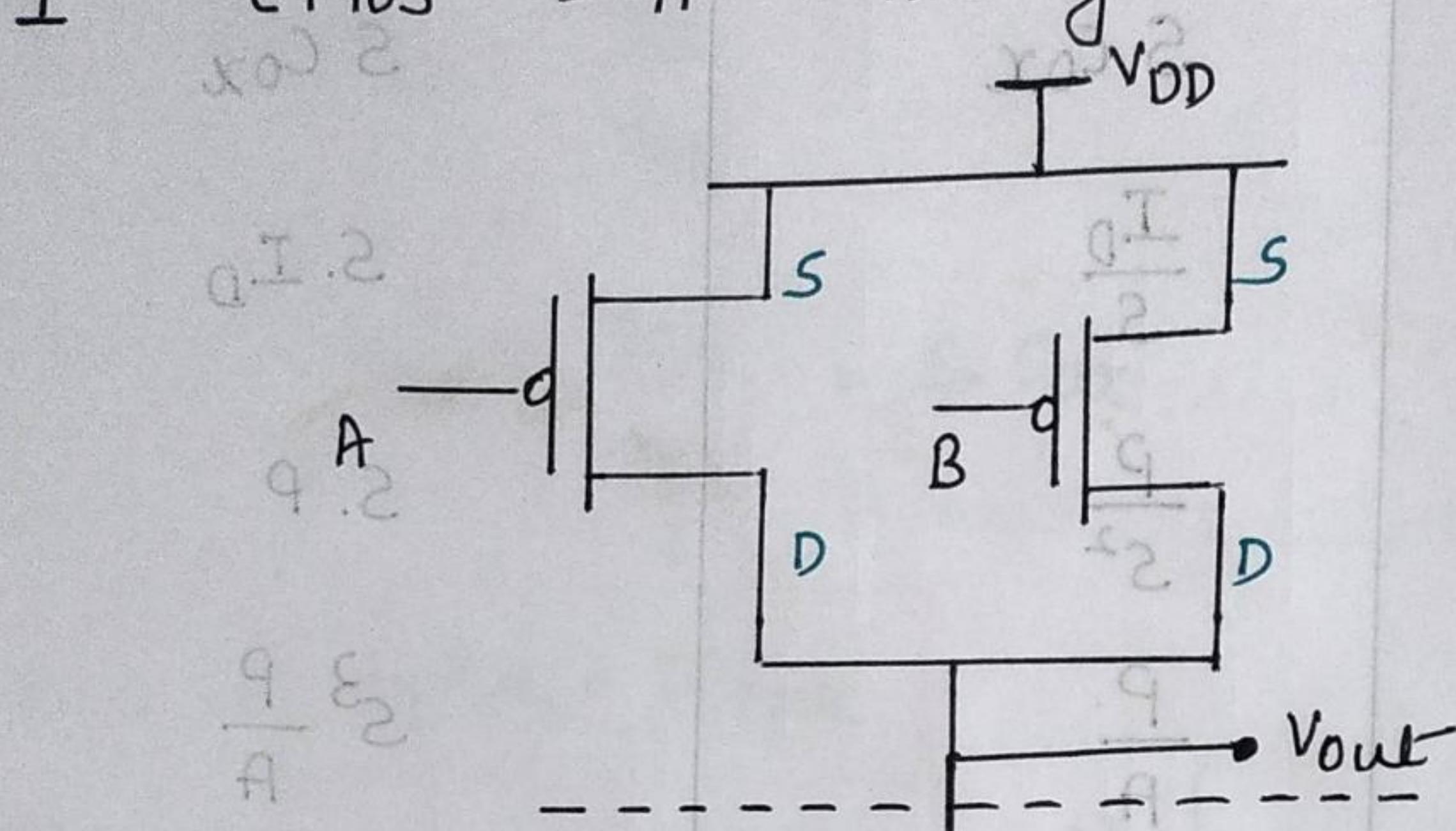
Parameters	Constant field Scaling	constant voltage Scaling
C_{ox}	$S C_{ox}$	$S C_{ox}$
I_D	$\frac{I_D}{S}$	$S \cdot I_D$
P	$\frac{P}{S^2}$	$S \cdot P$
$\frac{P}{A}$	$\frac{P}{A}$	$S^3 \frac{P}{A}$
N_A, N_D	S	S^2
Voltage	$\frac{V}{S}$	V
all remaining dimensions	$\frac{W}{S} \quad \frac{L}{S} \dots$	$\frac{W}{S} \quad \frac{L}{S} \dots$

→ constant voltage scaling is preferred over constant field scaling in many practical cases because of external Vtg. level constraints.

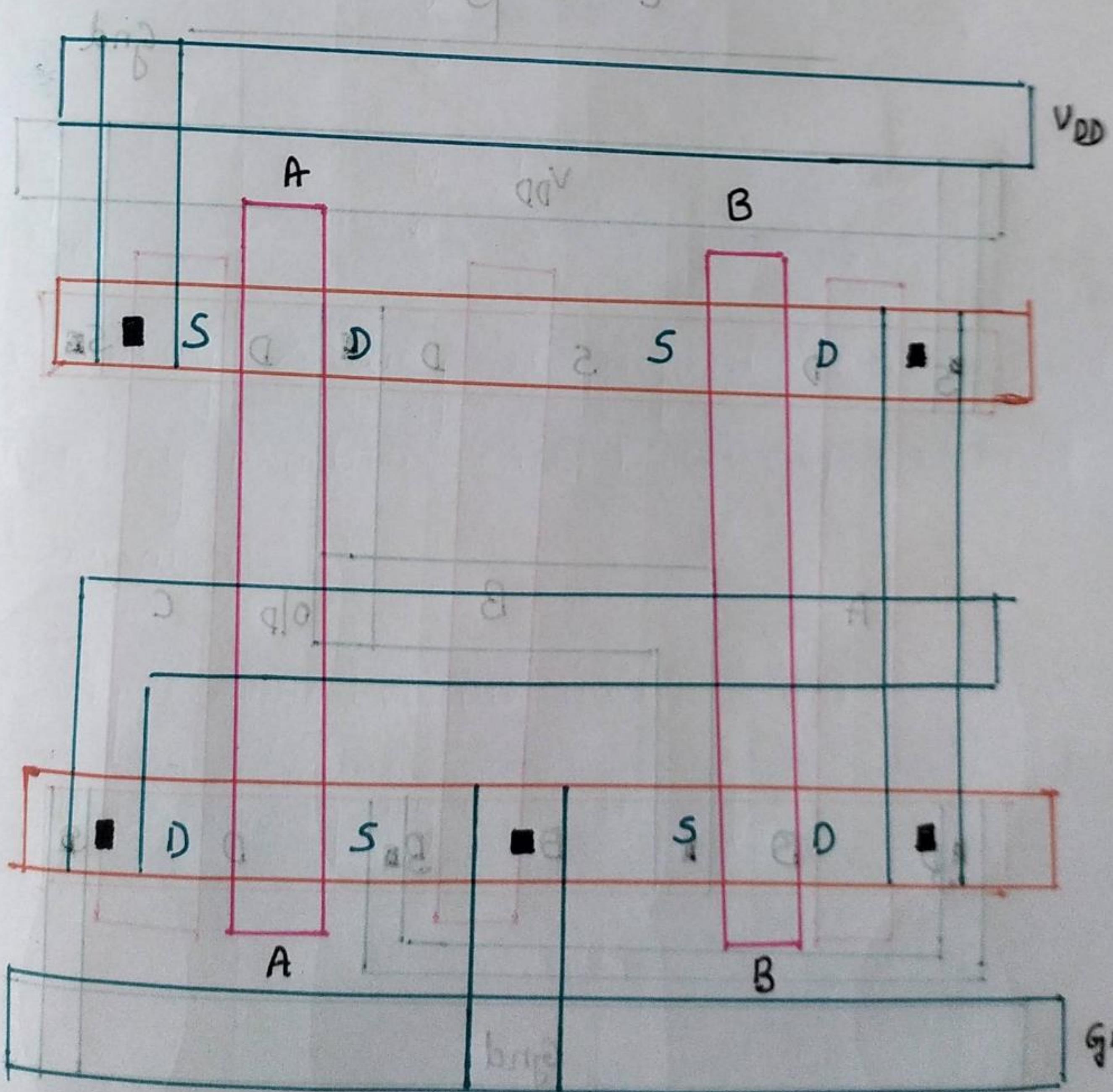
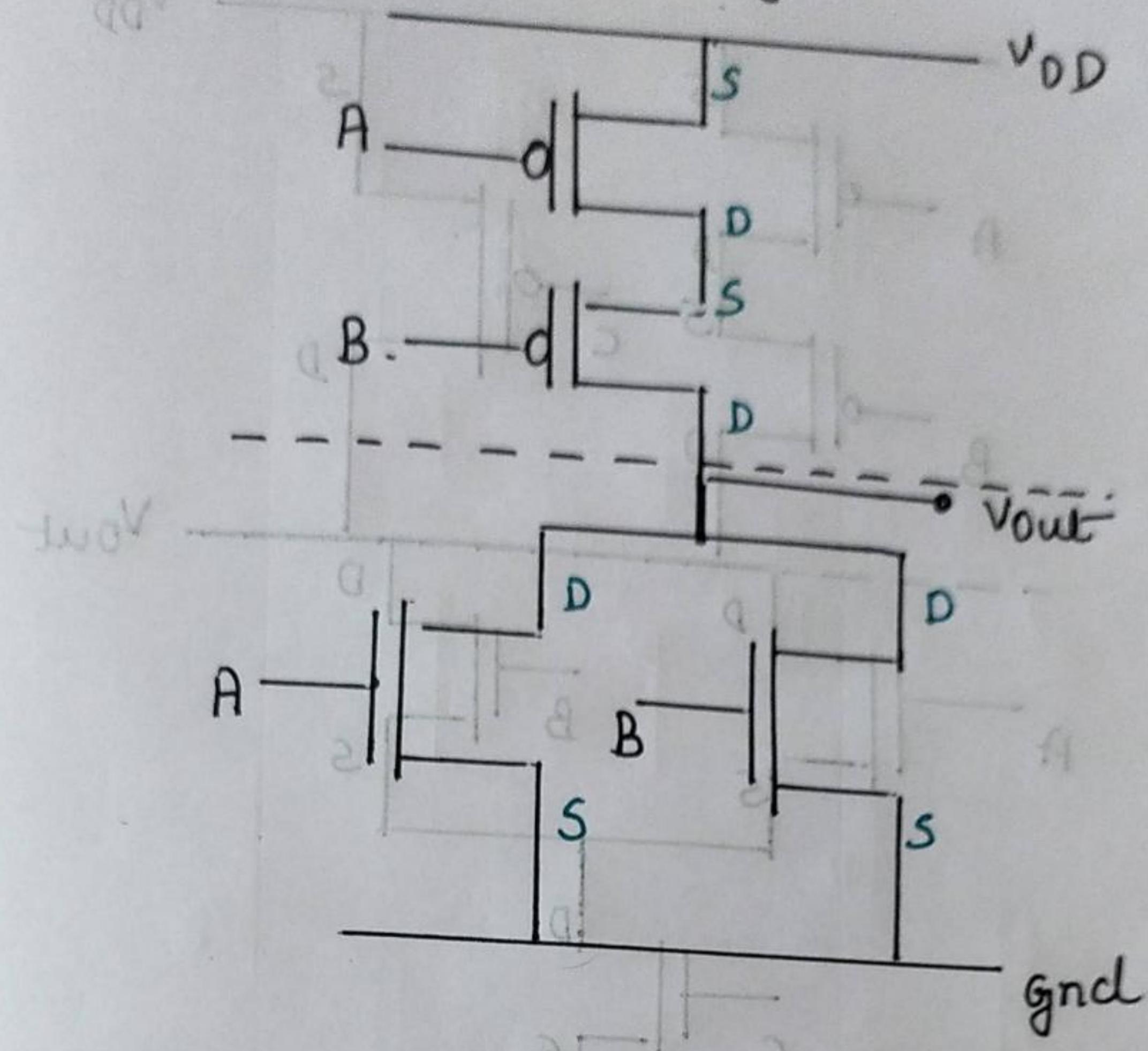
→ constant Vdg scaling however increases the drain current density + power density by a factor of S^3 .

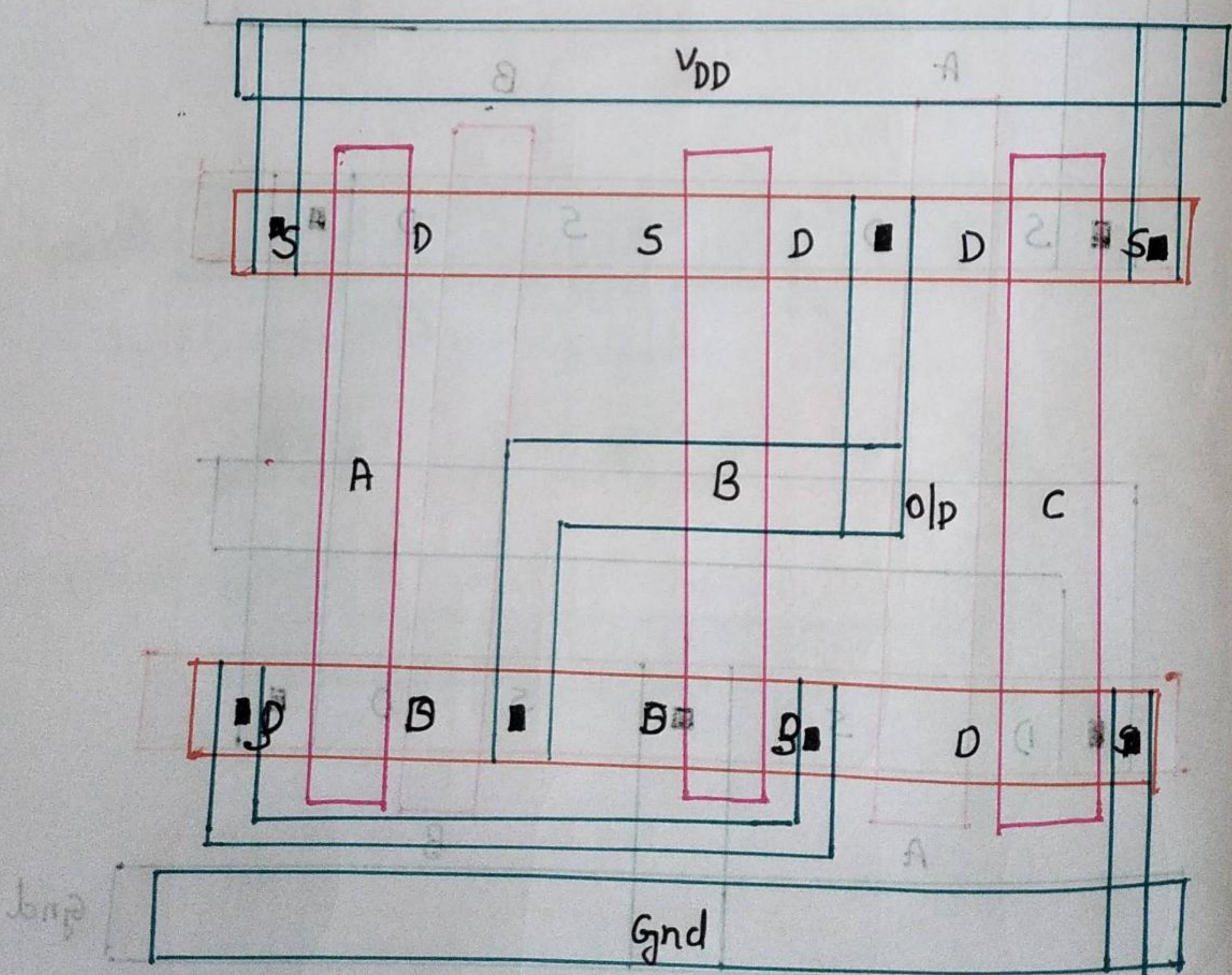
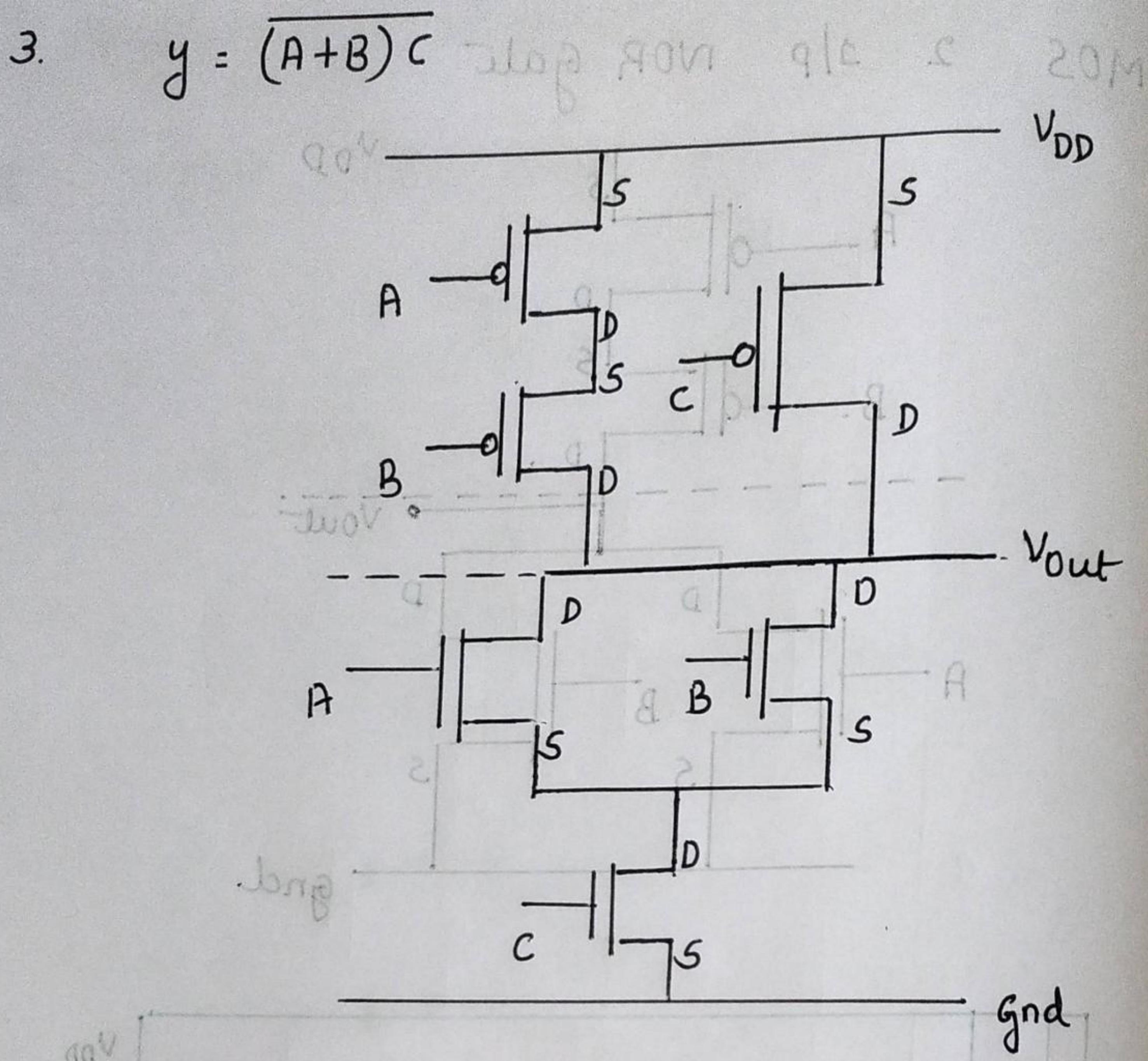
complex Logic circuits :-

I CMOS 2 s/p NAND gate

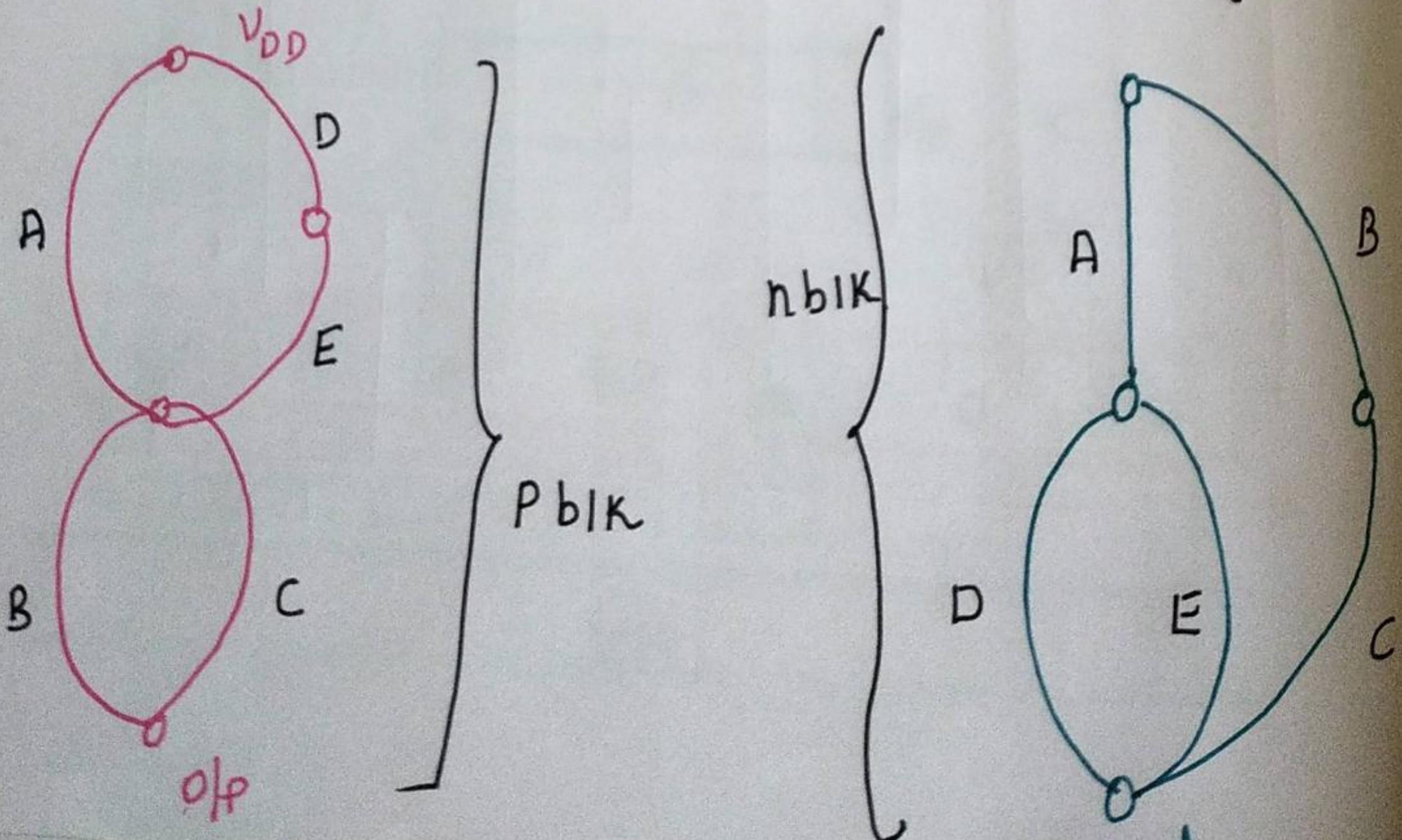
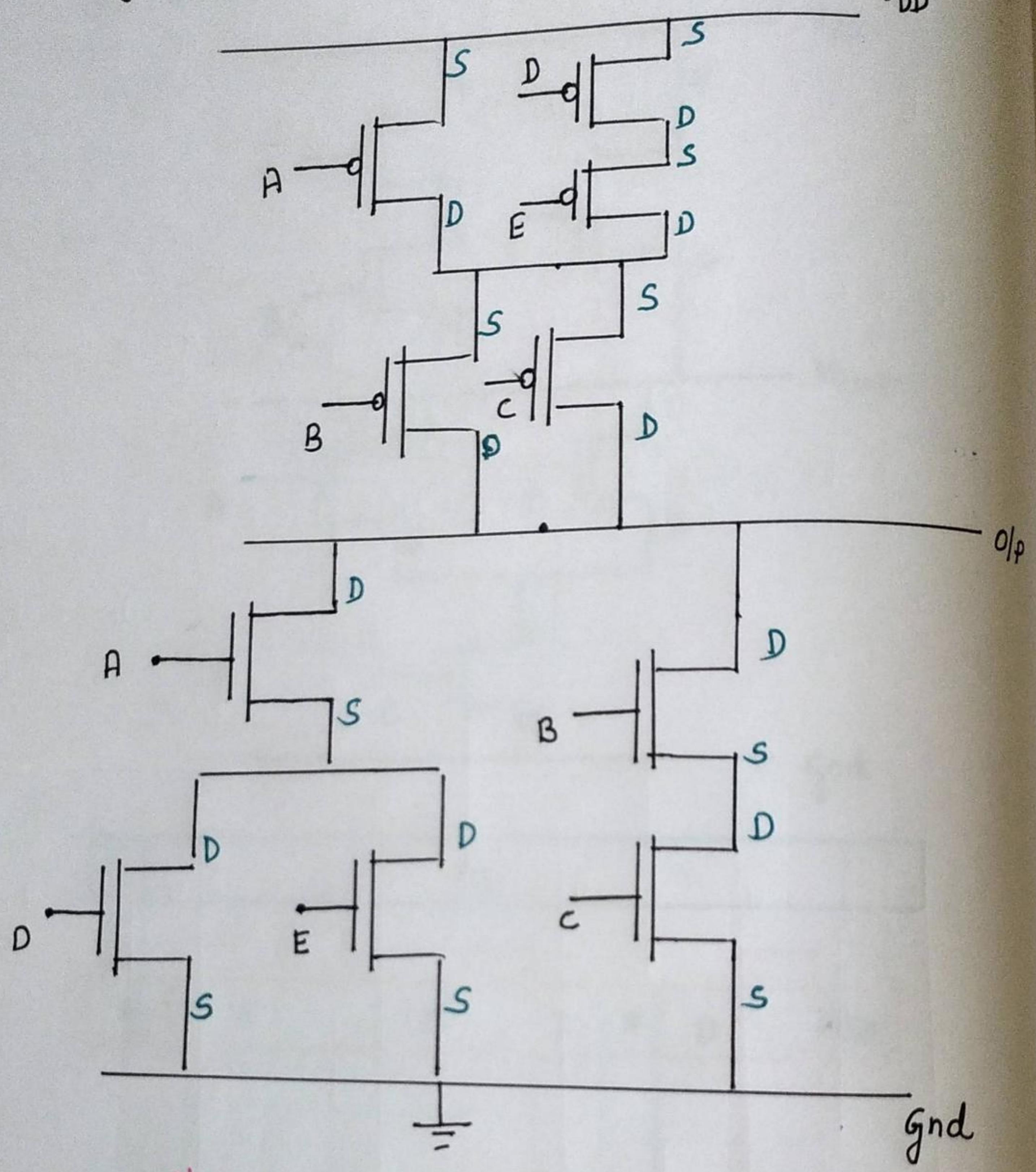


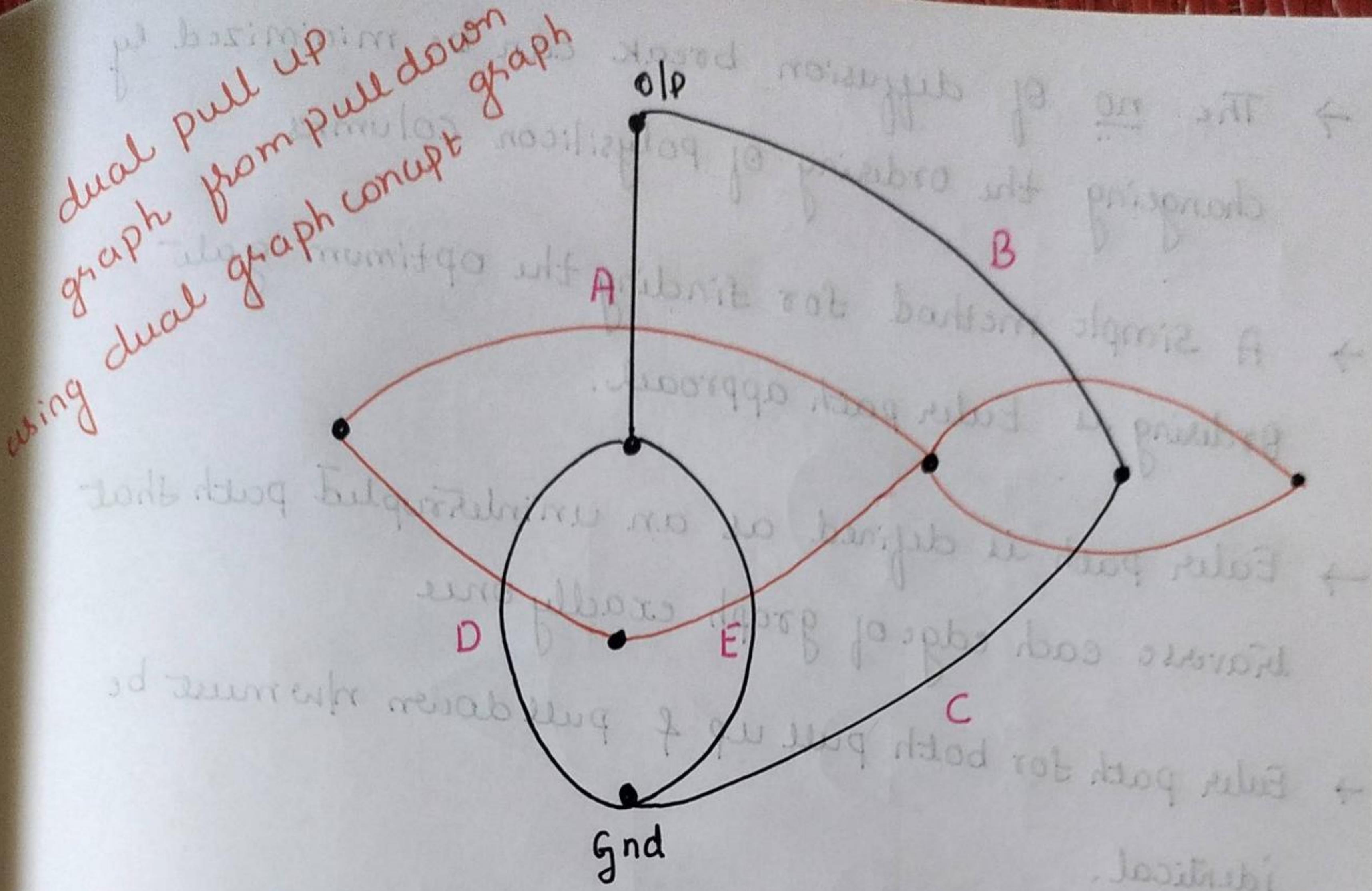
II

CMOS 2 s/p NOR gate $\Sigma(8+A) = B$ 

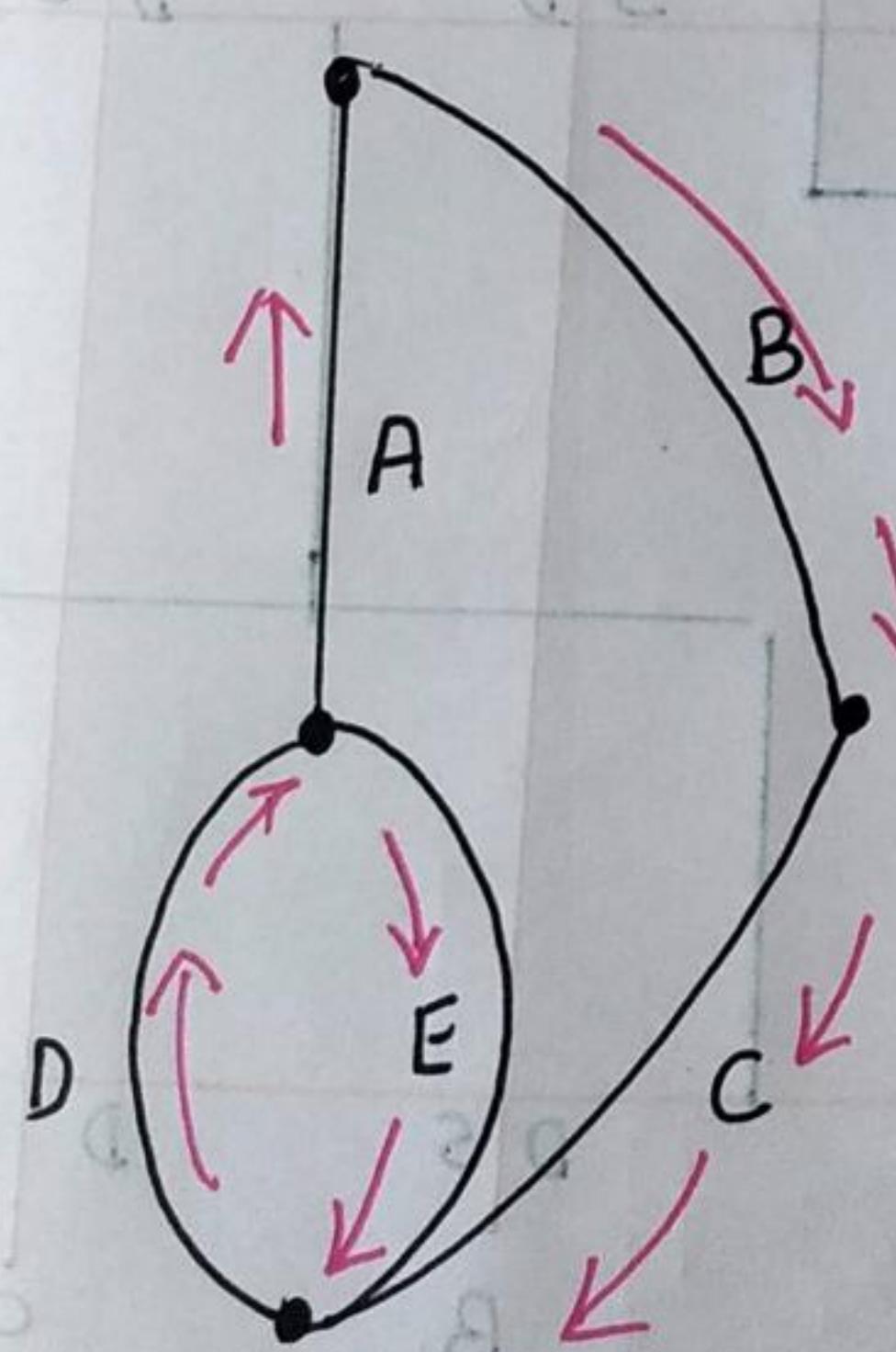


$$5) \quad y = A(D+E) + BC$$

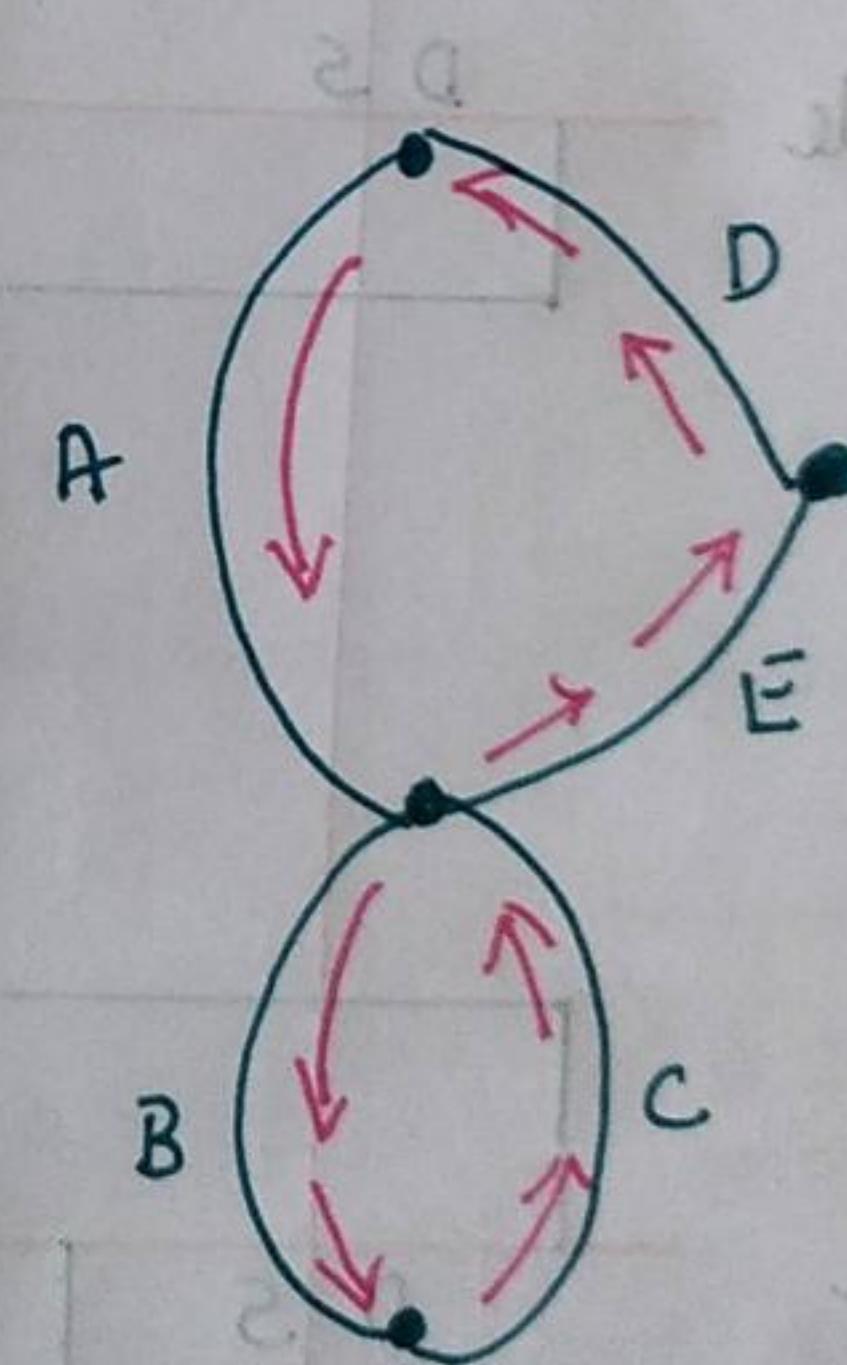




Euler's path :-



EDABC

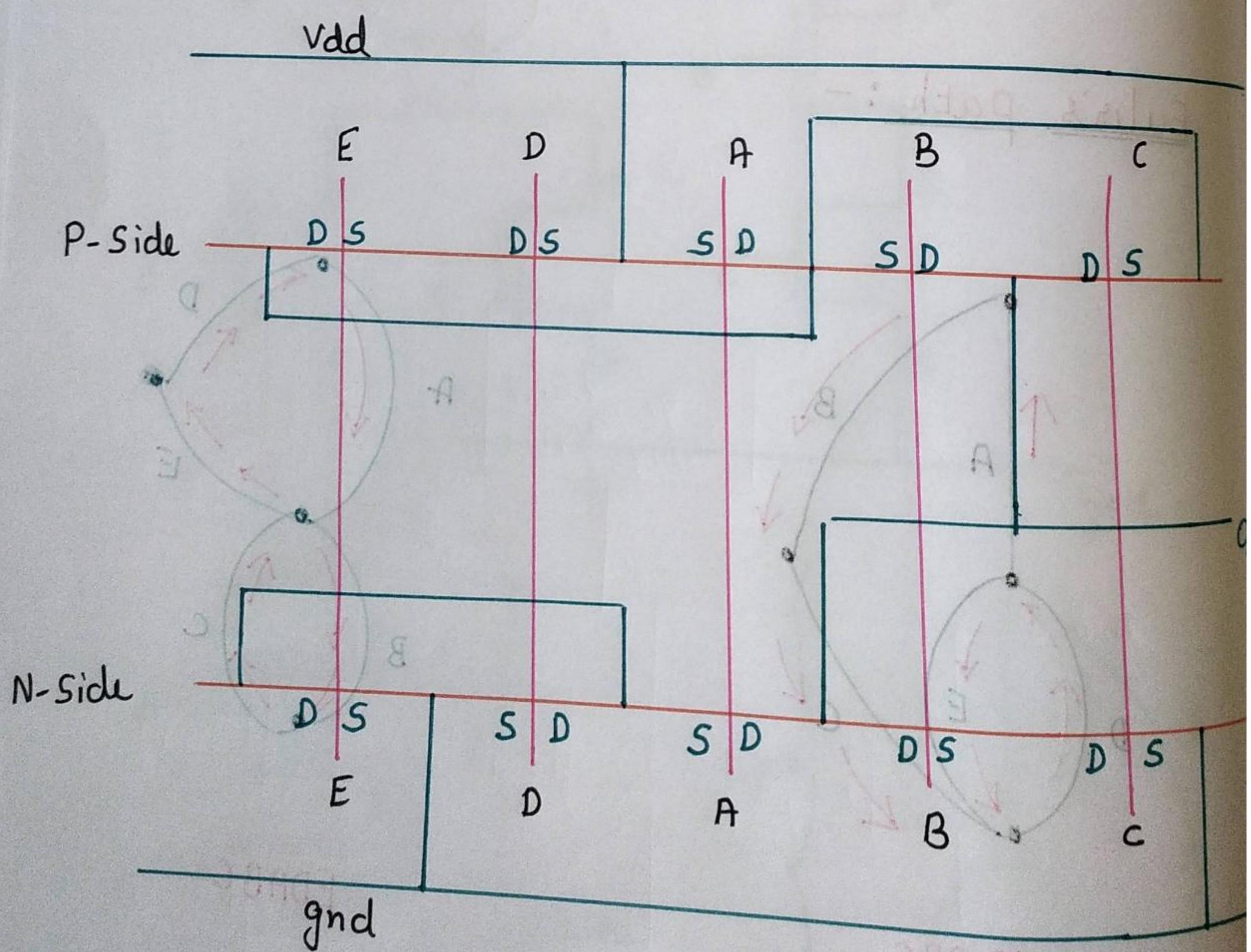


EDABC

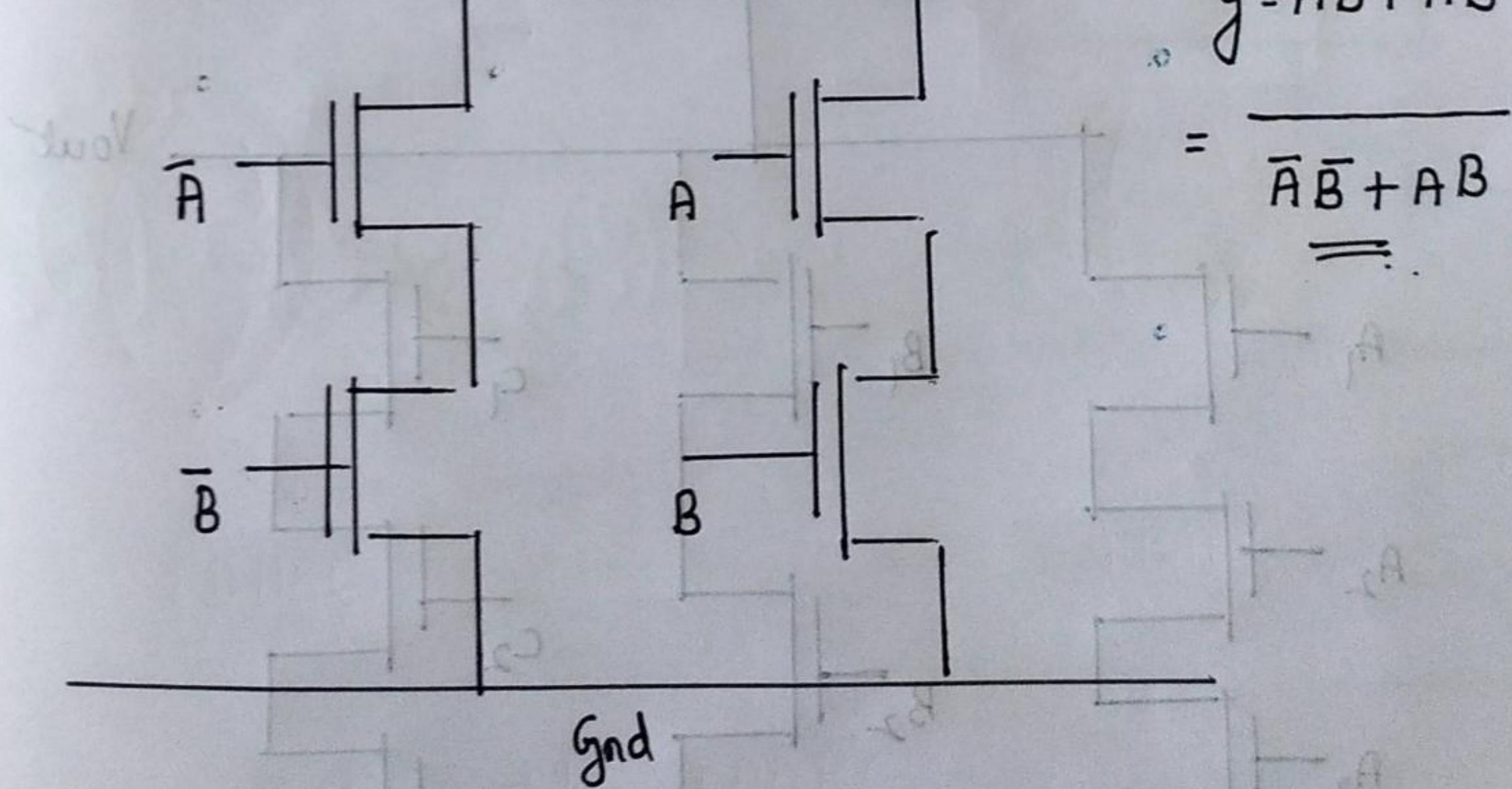
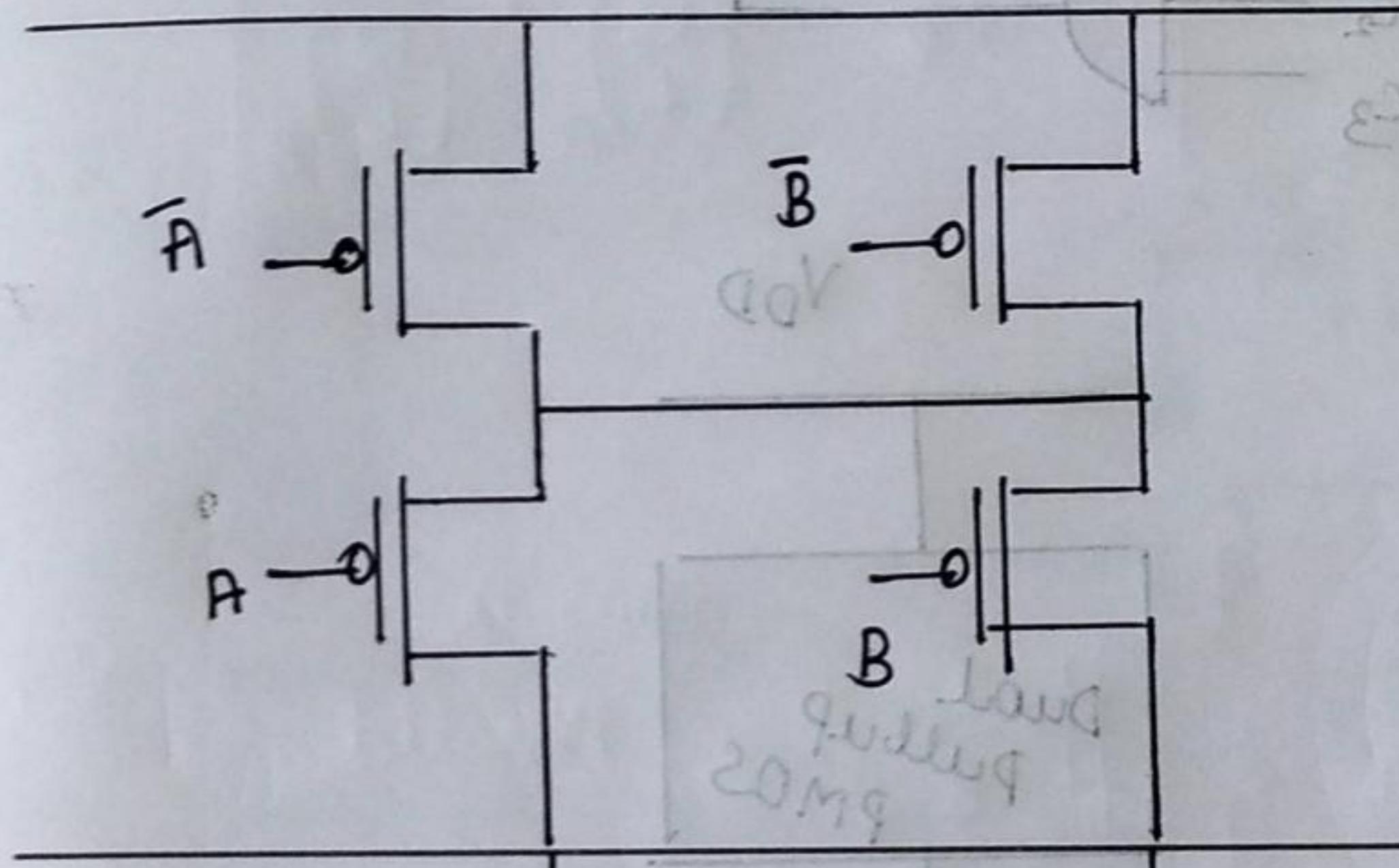
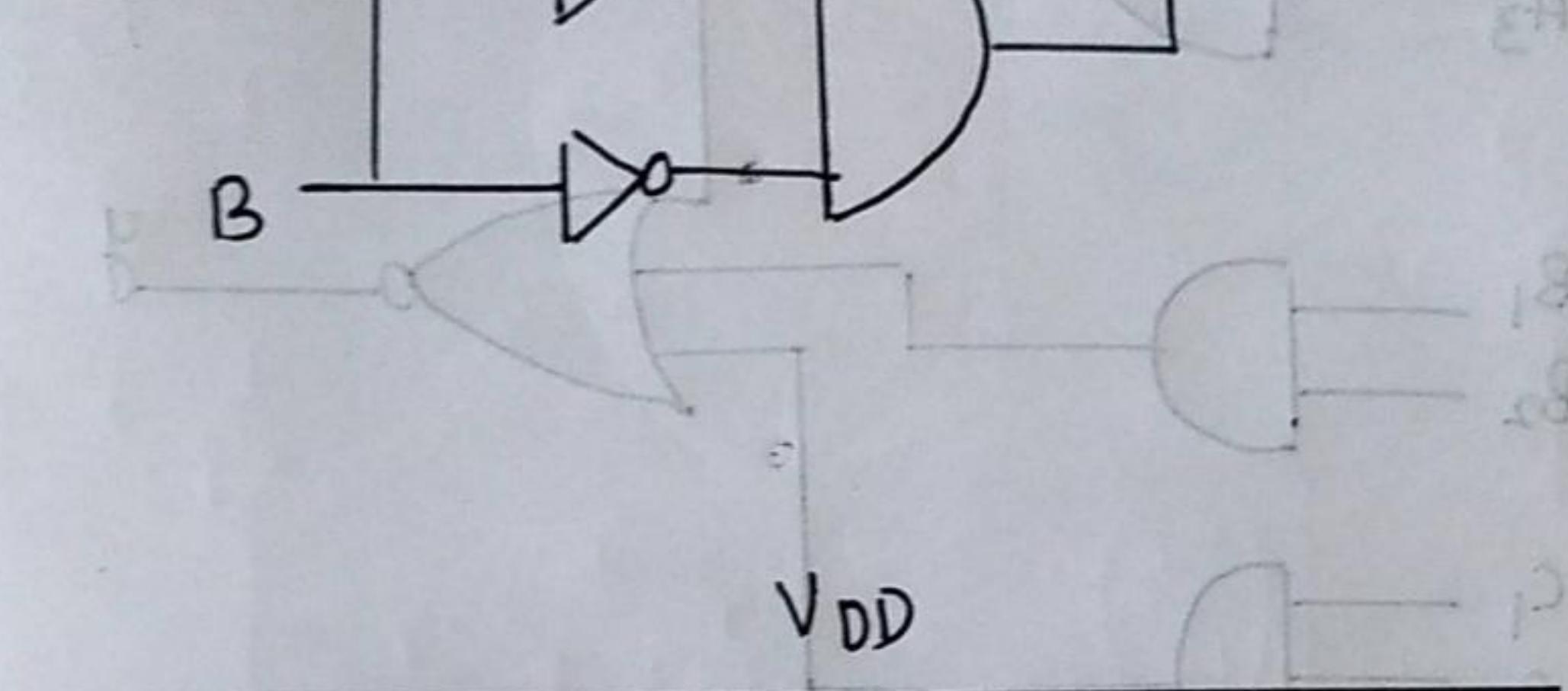
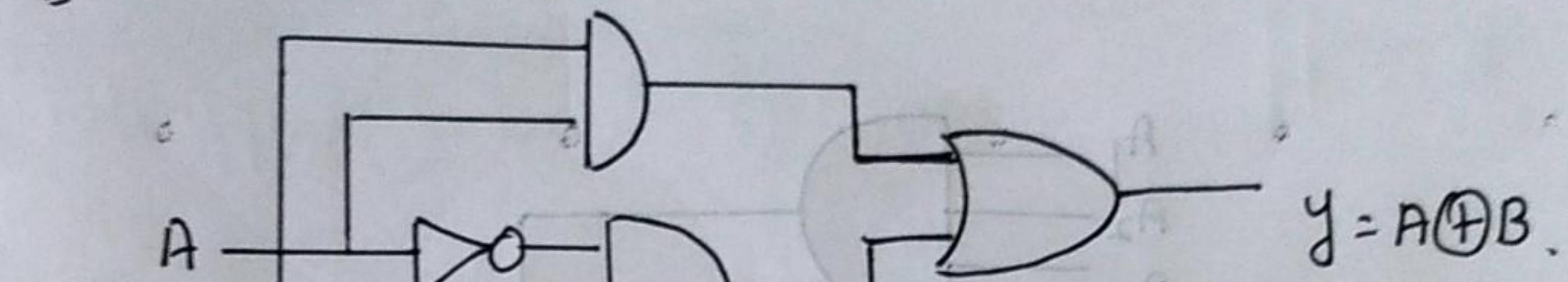
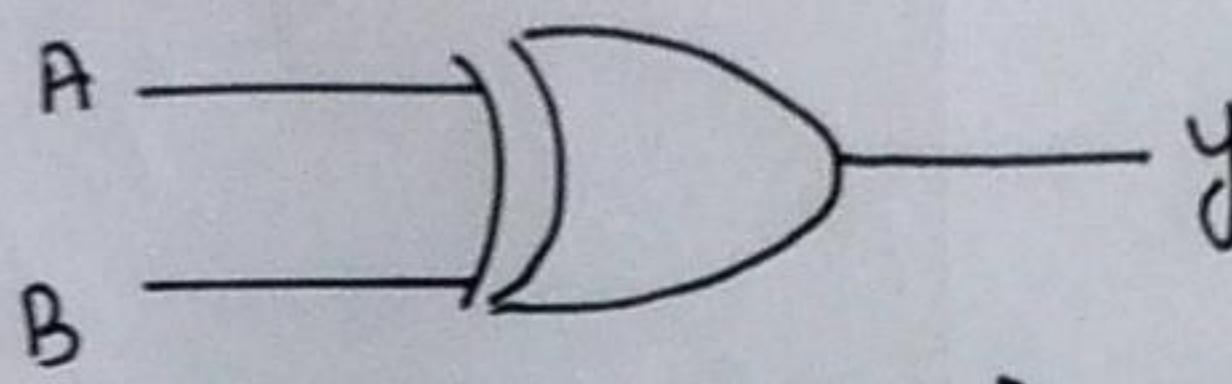
∴ Euler's path

EDABC

- The no of diffusion break can be minimized by changing the ordering of polysilicon columns
- → A simple method for finding the optimum gate Ordering is Euler path approach.
- Euler path is defined as an uninterrupted path that traverse each edge of graph exactly once
- Euler path for both pull up & pull down must be identical.

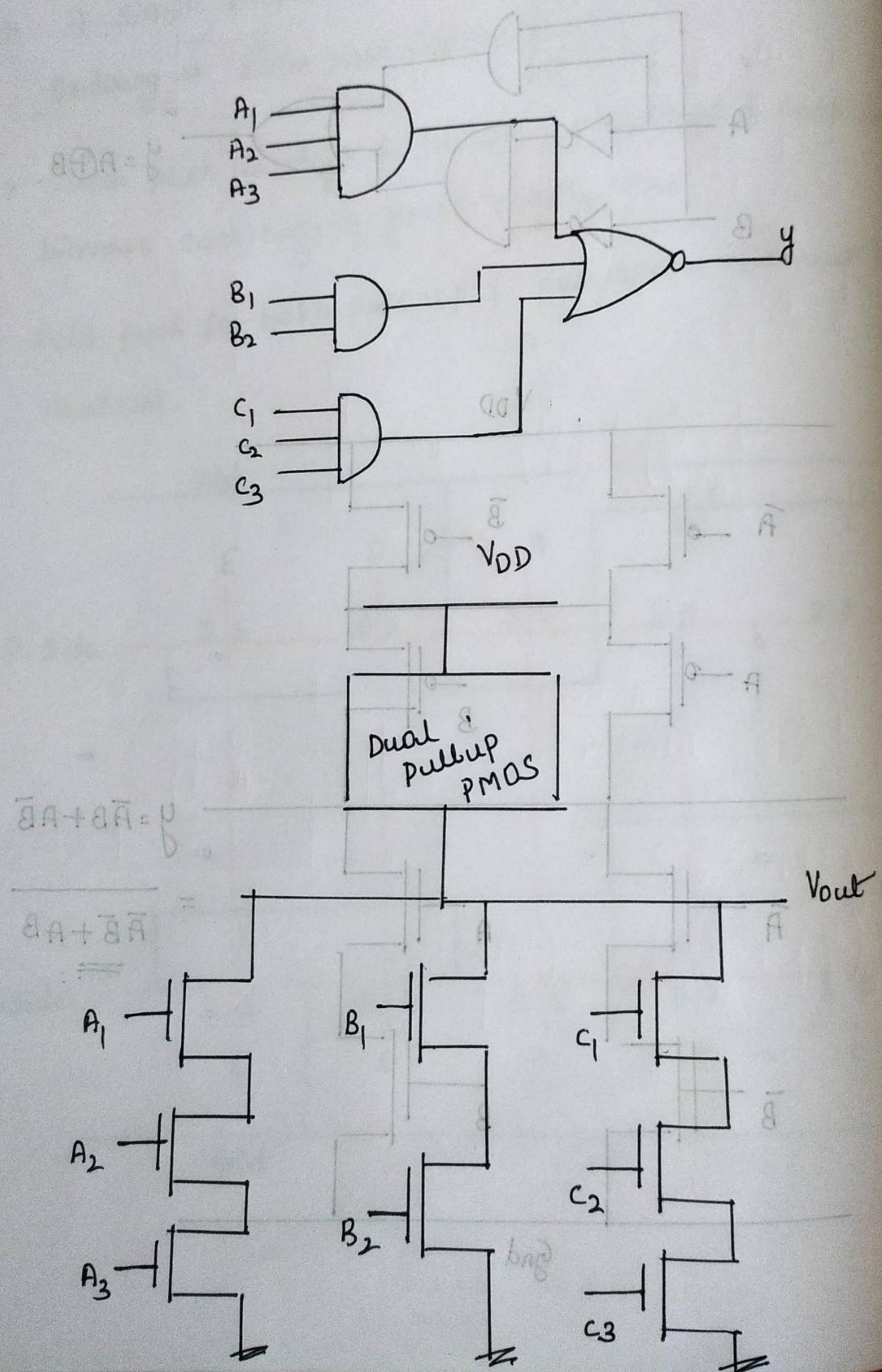


$$y = A \oplus B$$

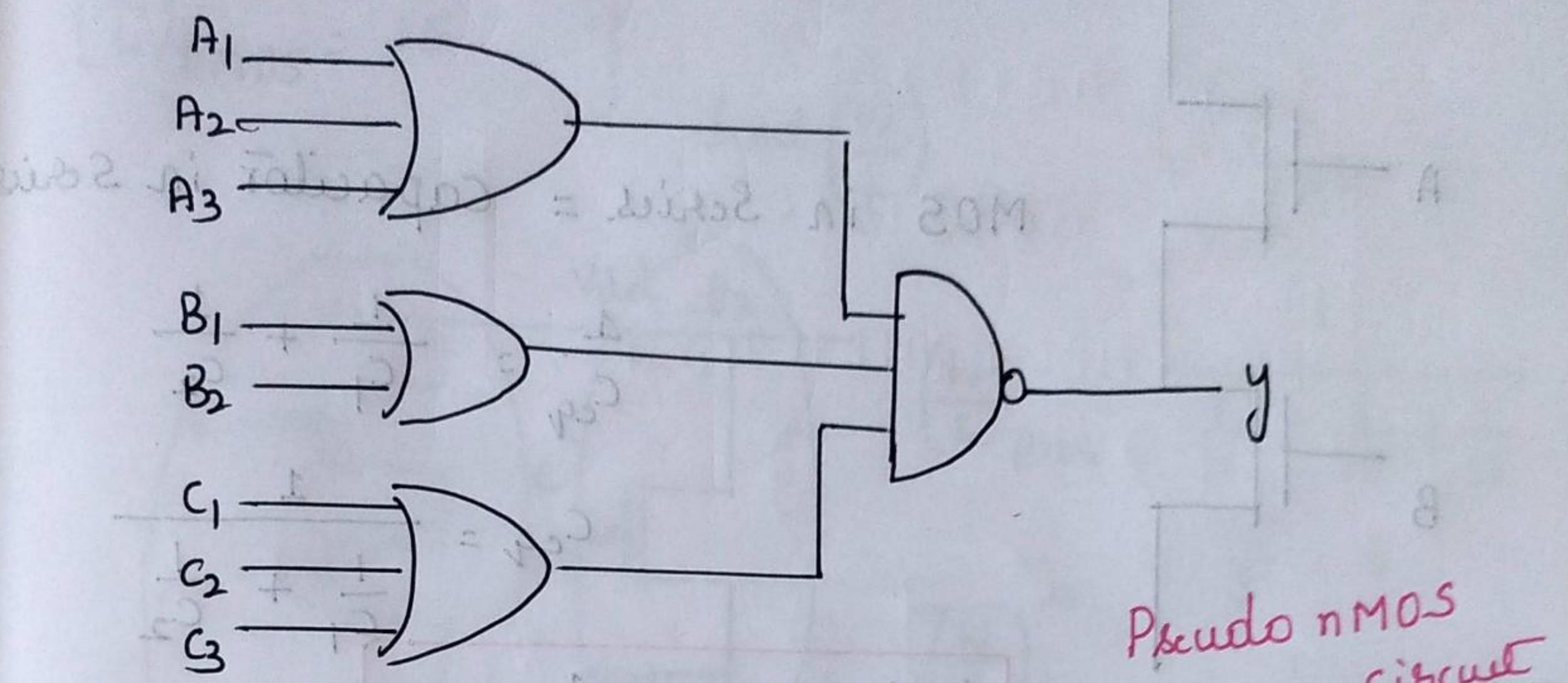


AOI and OAI gates

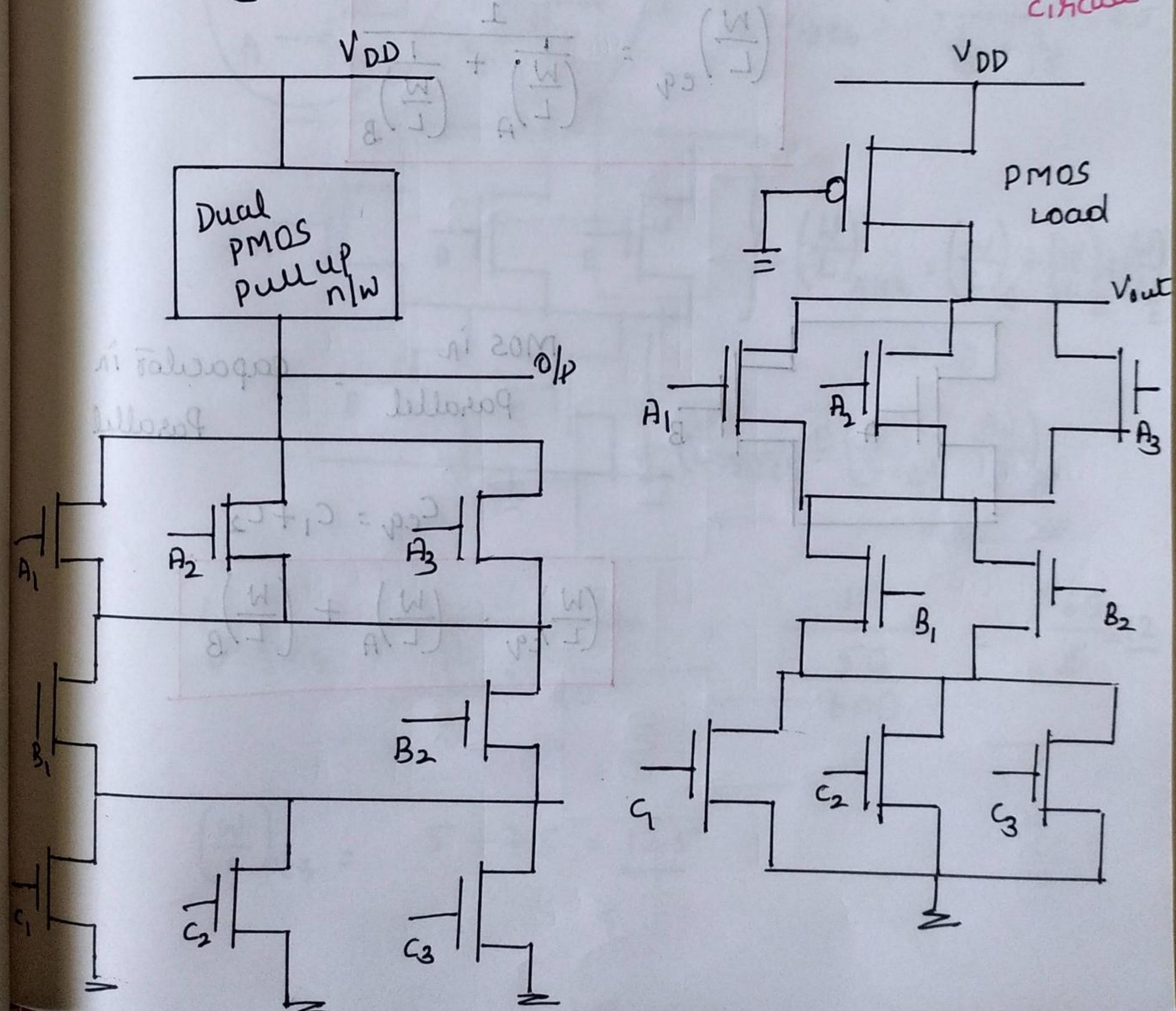
$$y = \overline{A_1 A_2 A_3 + B_1 B_2 + C_1 C_2 C_3}$$



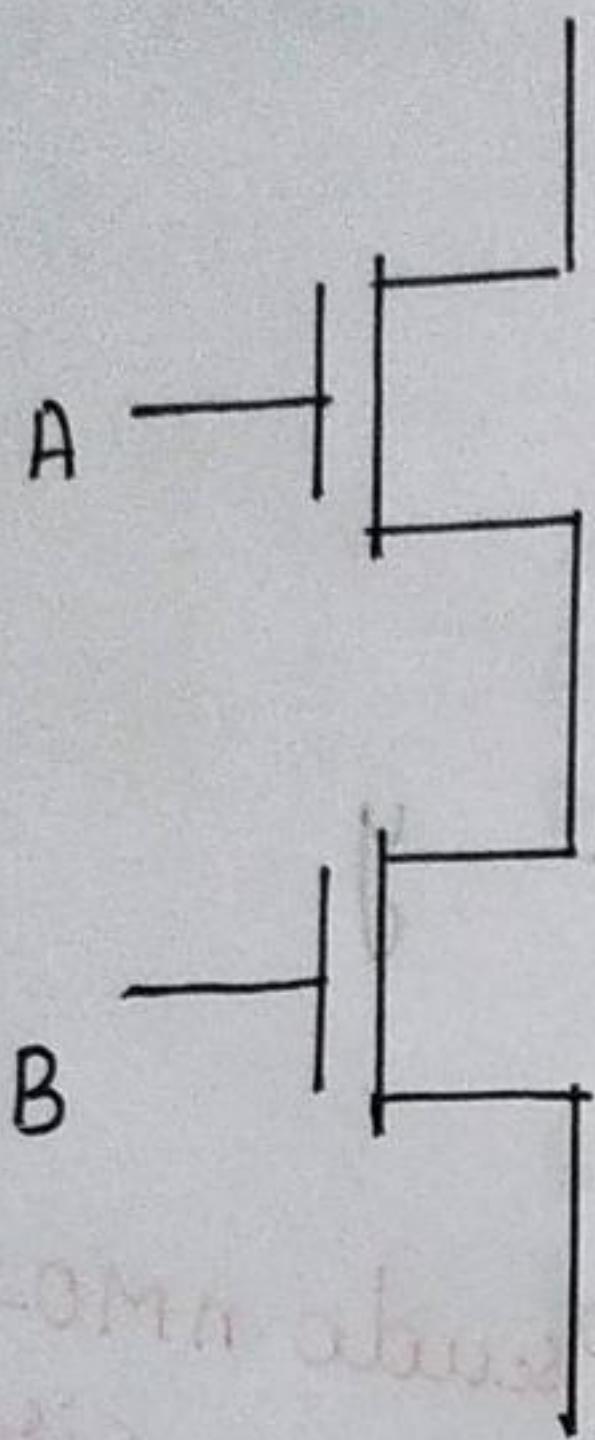
$$y = \overline{(A_1 + A_2 + A_3)(B_1 + B_2)(C_1 + C_2 + C_3)}$$



Pseudo nMOS circuit



Transistor Sizing :-

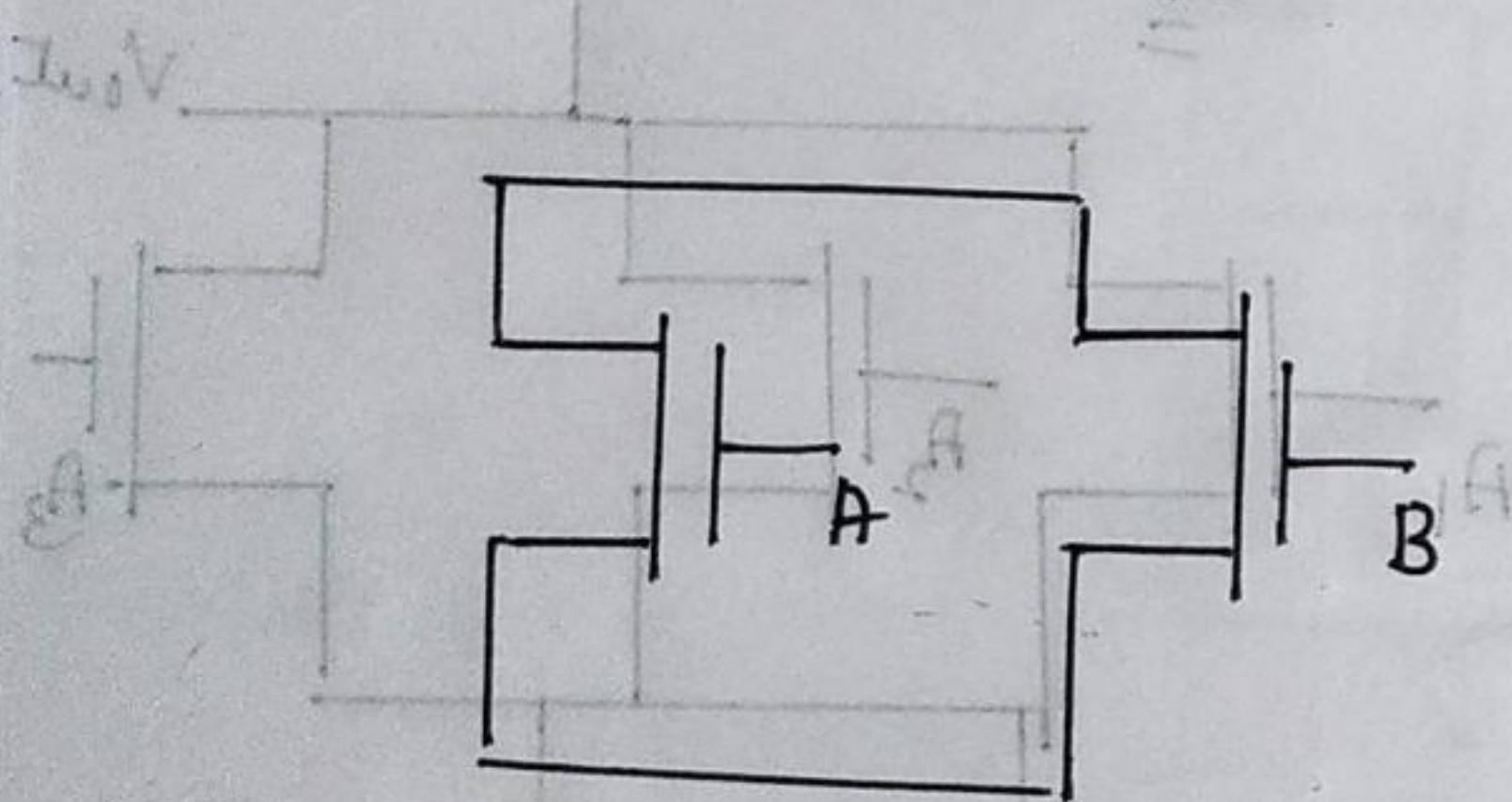
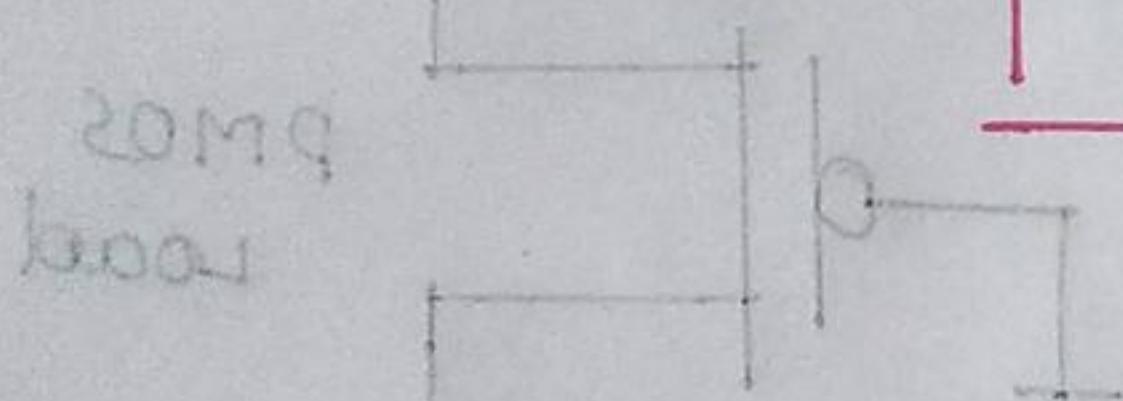


MOS in Series = Capacitor in Series

$$\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2}$$

$$C_{eq} = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2}}$$

$$\left(\frac{W}{L}\right)_{eq} = \frac{1}{\left(\frac{W}{L}\right)_A + \left(\frac{W}{L}\right)_B}$$



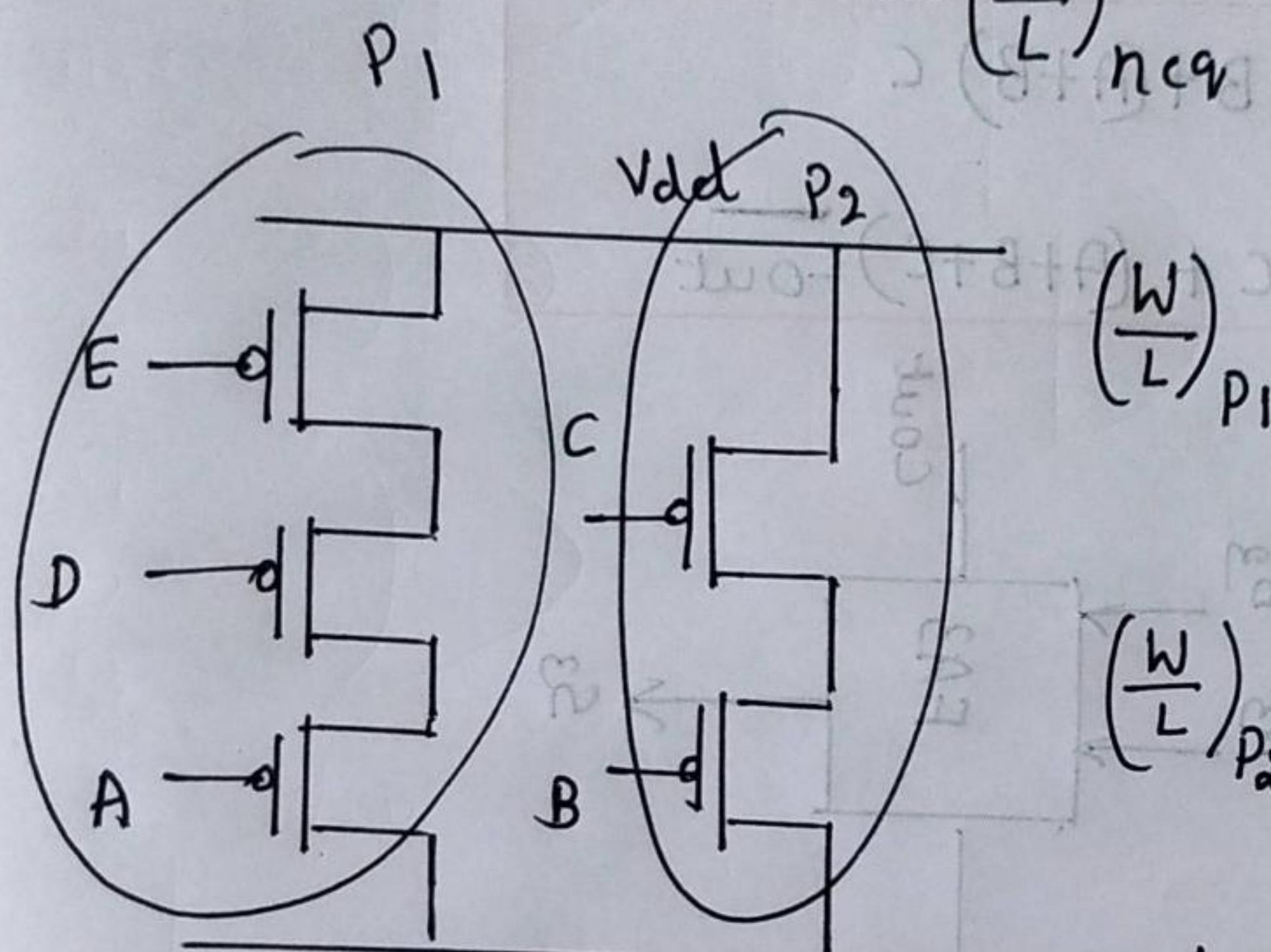
MOS in Parallel = Capacitor in Parallel

$$C_{eq} = C_1 + C_2$$

$$\left(\frac{W}{L}\right)_{eq} = \left(\frac{W}{L}\right)_A + \left(\frac{W}{L}\right)_B$$

$$1. \left(\frac{W}{L} \right)_{nMOS} = 10$$

$$\left(\frac{W}{L} \right)_{pMOS} = 15$$

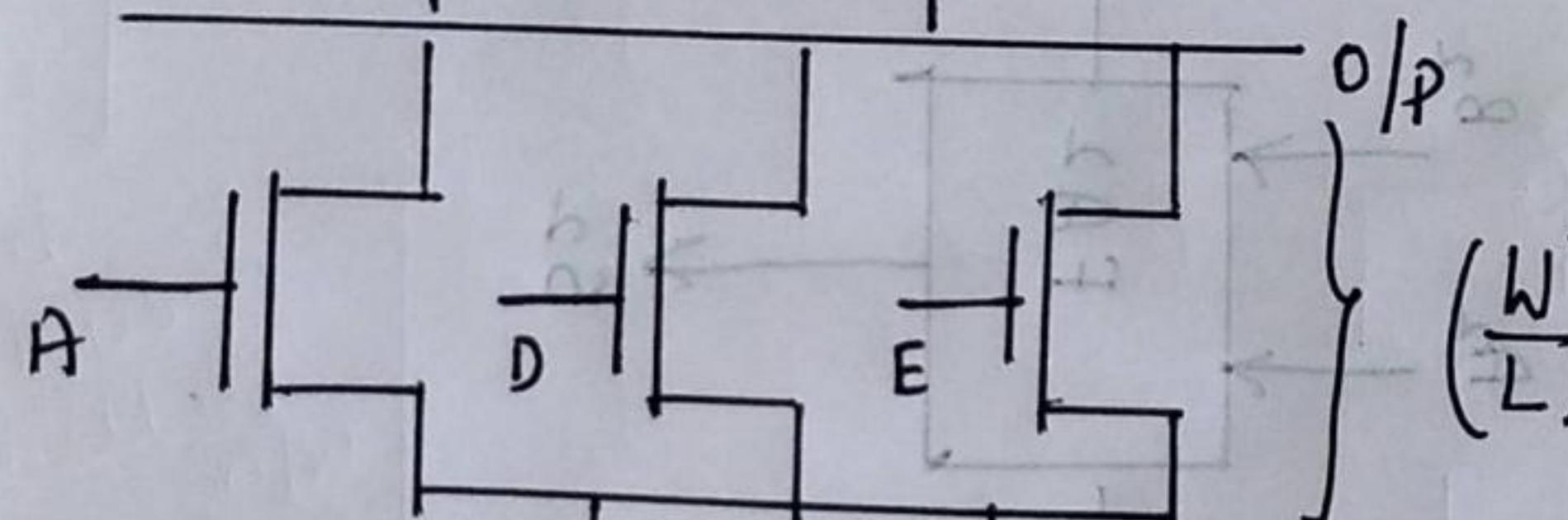


$$Y = \overline{(A+D+E)(B+C)}$$

find $\left(\frac{W}{L} \right)_{nCG}$ $\left(\frac{W}{L} \right)_{pCG}$

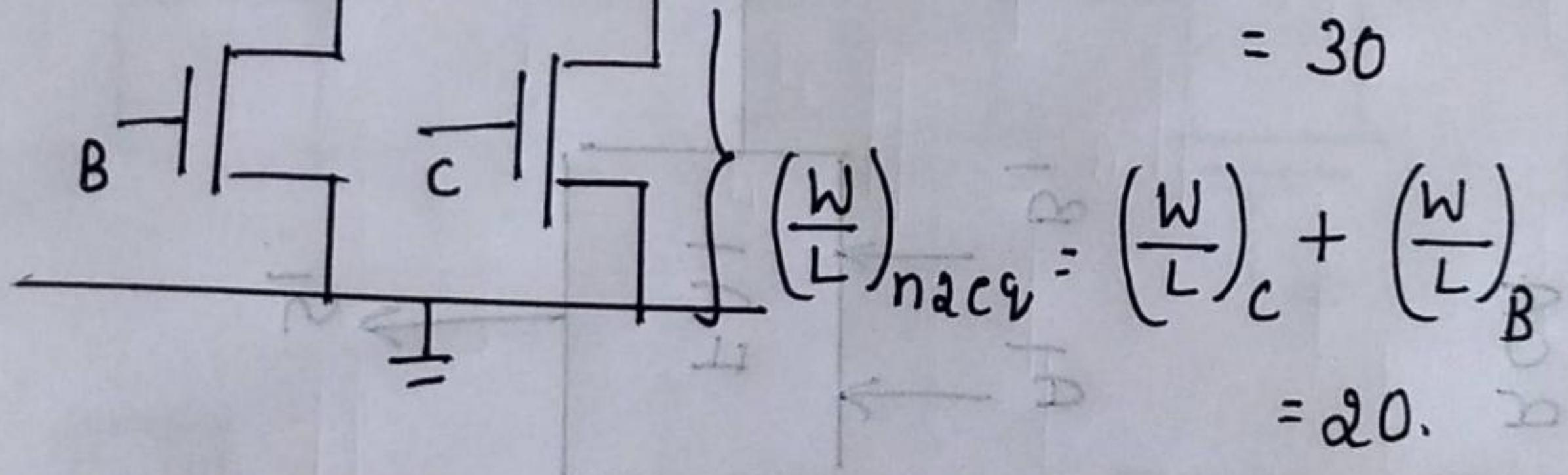
$$\left(\frac{W}{L} \right)_{pCG} = \frac{1}{\frac{1}{15} + \frac{1}{15} + \frac{1}{15}} = \frac{15}{3} = 5$$

$$\left(\frac{W}{L} \right)_{nCG} = \frac{1}{\frac{1}{30} + \frac{1}{20}} = 12$$



$$\left(\frac{W}{L} \right)_{nCG} = \left(\frac{W}{L} \right)_A + \left(\frac{W}{L} \right)_B + \left(\frac{W}{L} \right)_E$$

$$= 30$$



$$\left(\frac{W}{L} \right)_{pCG} = \left(\frac{W}{L} \right)_C + \left(\frac{W}{L} \right)_B$$

$$= 20.$$

$$\left(\frac{W}{L} \right)_{nCG} = \frac{1}{\frac{1}{30} + \frac{1}{20}} = \frac{1}{\frac{50}{600}} = \frac{60}{5} = 12$$

$$\left(\frac{W}{L} \right)_{pCG} = 5 + 7.5 = \underline{\underline{12.5}}$$

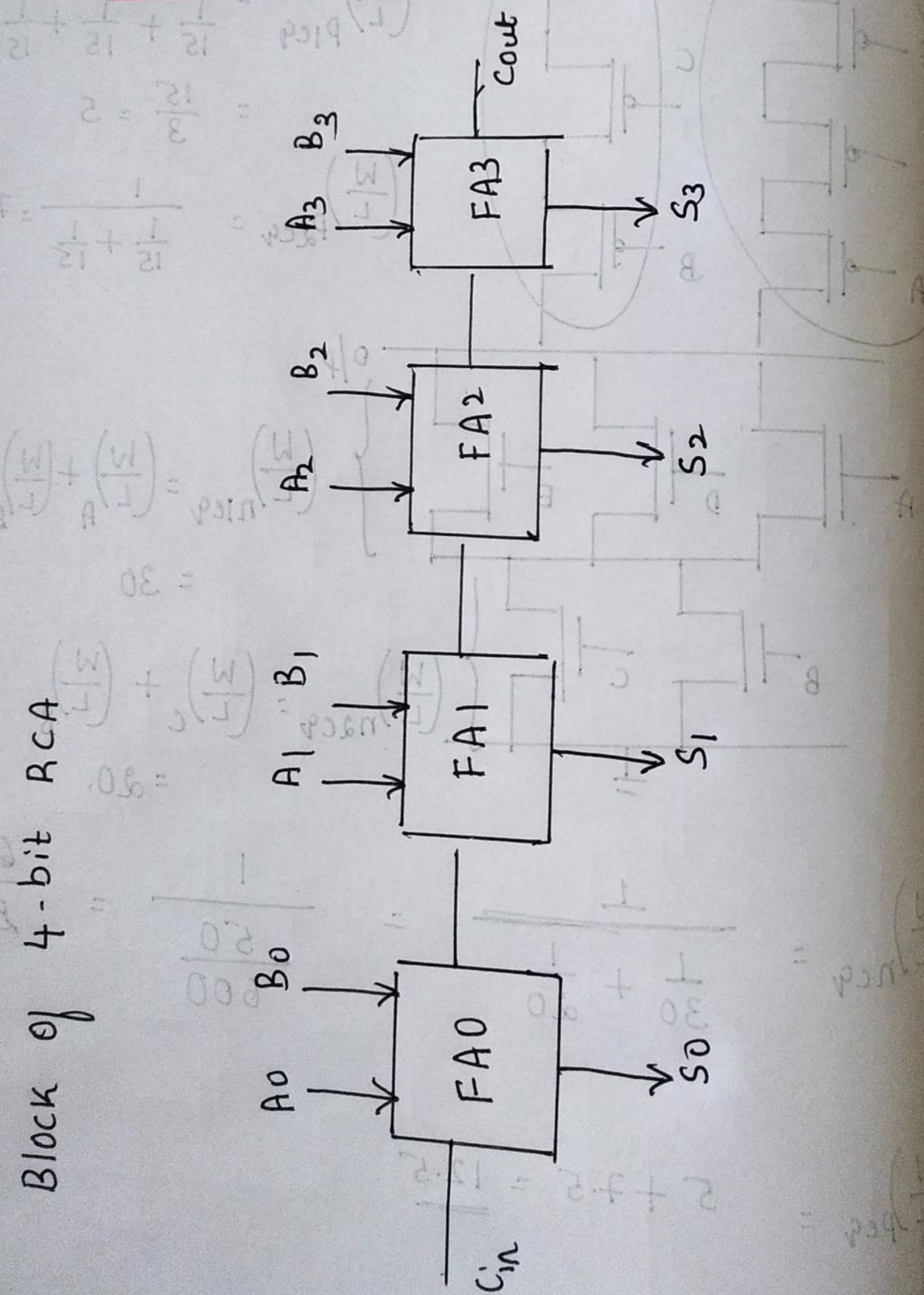
CMOS Full Adder circuit

$$\text{sum} = A \oplus B \oplus C$$

$$C_{\text{out}} = AB + BC + AC$$

$$C_{\text{out}} = AB + (A+B)C$$

$$\text{Sum} = ABC + (A+B+C)\overline{C_{\text{out}}}$$



Transistor Level Schematic of 1-bit full adder

