DIGITAL VLSI DESIGN

Unit 2: Fabrication of MOSFETs & Circuit Design Process

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CMOS Full-Adder Circuit

The one-bit full adder circuit is one of the most widely used building blocks in all data processing (arithmetic) and digital signal processing architectures.

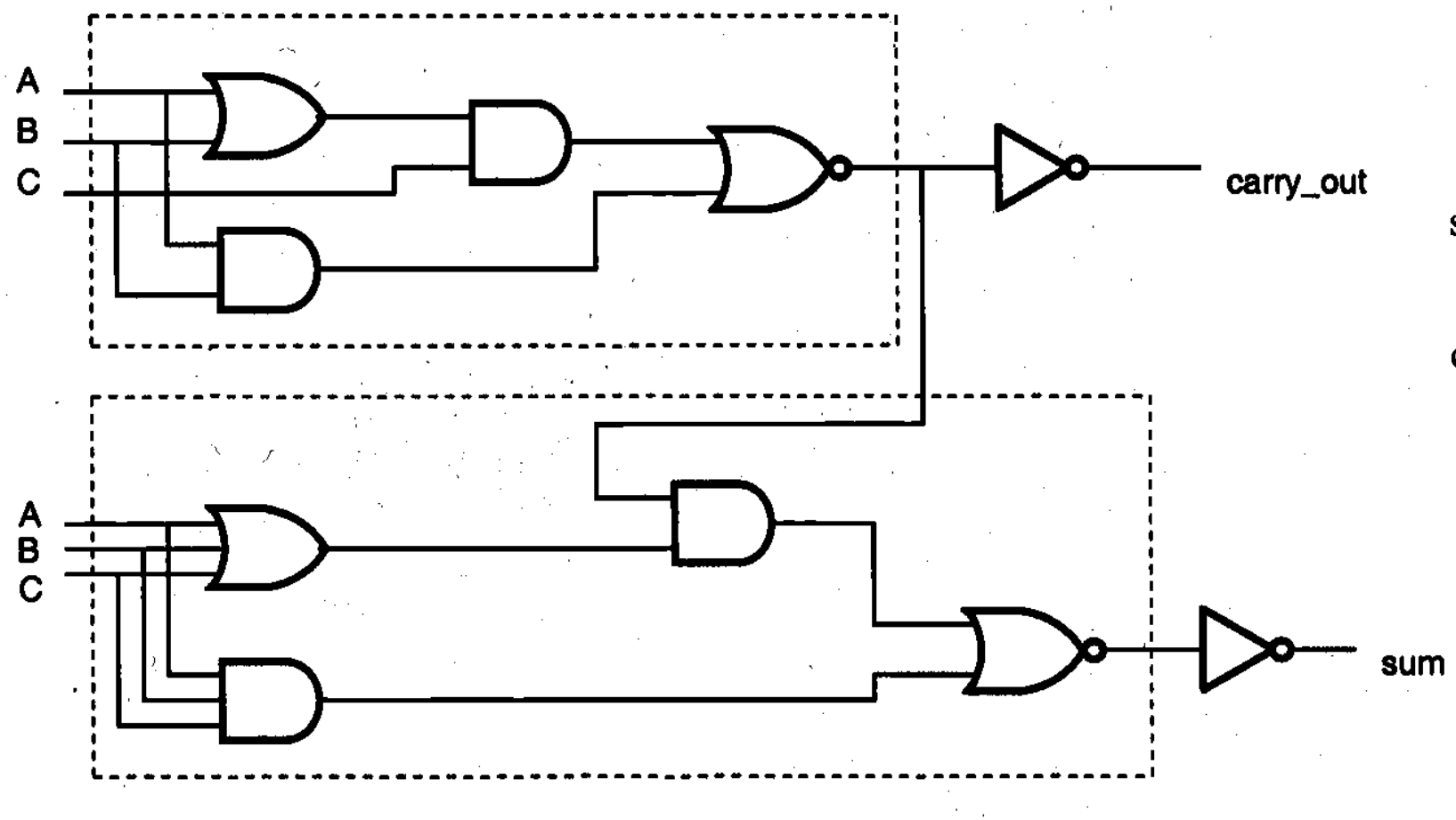
In the following, we will examine the circuit structure and the realization of the full adder using the conventional CMOS design style.

The sumout and carry-out signals of the full adder are defined as the following two combinational Boolean functions of the three input variables, A, *B,* and C.

$$\begin{aligned} \text{sum\_out} &= A \oplus B \oplus C \\ &= ABC + A\overline{B}\,\overline{C} + \overline{A}\,\overline{B}C + \overline{A}\,\overline{C}B \\ \text{carry\_out} &= AB + AC + BC \end{aligned}$$

CMOS Full-Adder Circuit

Gate-level schematic of the one-bit full-adder circuit



$$\text{sum\_out} = A \oplus B \oplus C$$

$$= A\,B\,C + A\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C + \overline{A}\,\overline{C}\,B$$

$$\text{carry\_out} = AB + AC + BC$$

$$C_{i+1} = a_i b_i + c_i(a_i + b_i)$$

$$S_i = (a_i + b_i + c_i).C'_{i+1} + (a_i b_i c_i)$$

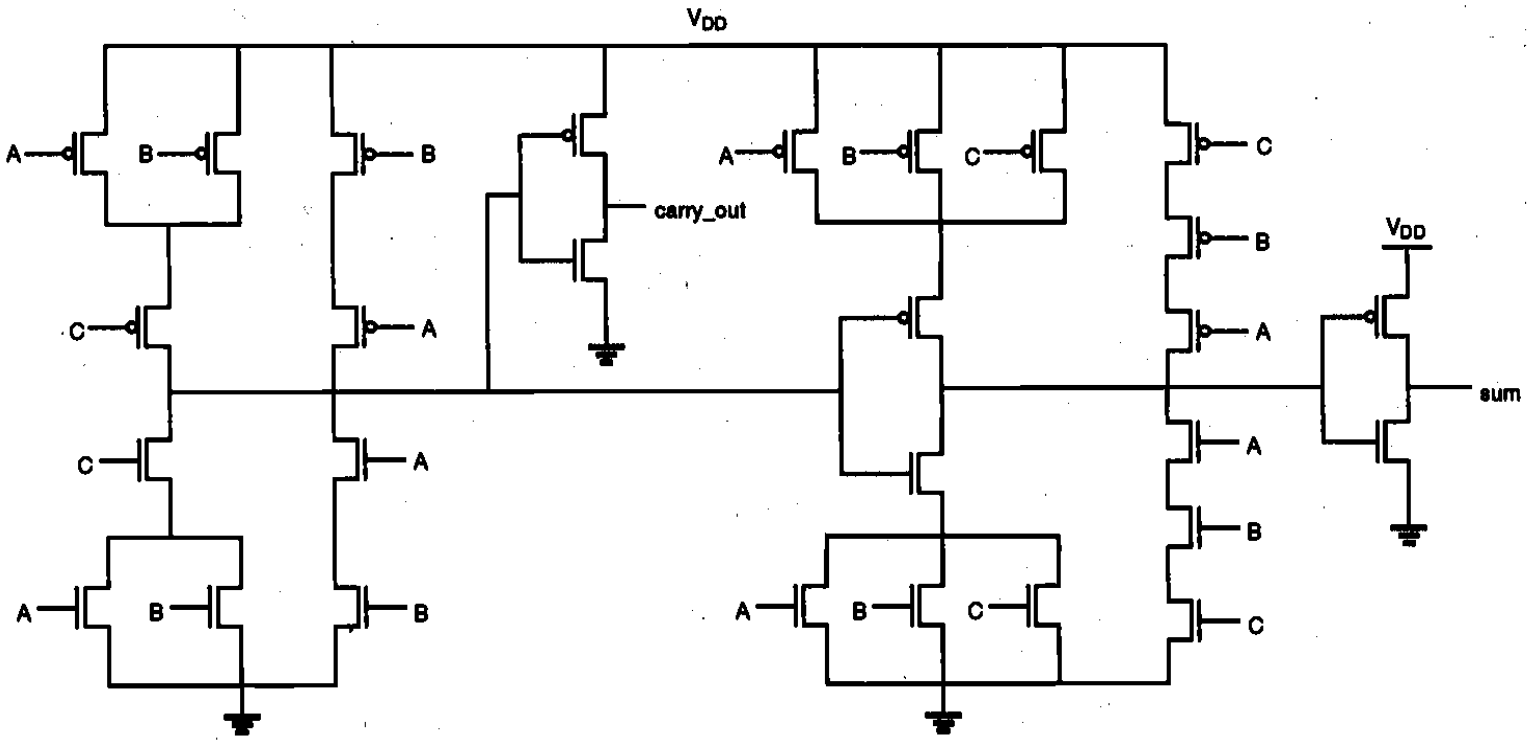
CMOS Full-Adder Circuit

Transistor-level schematic of the one-bit full-adder circuit

$$\begin{aligned} \text{sum\_out} &= A \oplus B \oplus C \\ &= ABC + A\overline{B}\,\overline{C} + \overline{A}\,\overline{B}C + \overline{A}\,\overline{C}B \\ \text{carry\_out} &= AB + AC + BC \end{aligned}$$

$$C_{i+1} = a_i b_i + c_i(a_i + b_i)$$

$$S_i = (a_i + b_i + c_i).C'_{i+1} + (a_i b_i c_i)$$



The transistor-level design of the CMOS full-adder circuit is shown in figure.

Note that the circuit contains a total of 14 nMOS and 14 pMOS transistors, together with the two CMOS inverters which are used to generate the outputs.

Transistor Sizing

When transistors are connected in series, their individual resistances get added up while the net W/L ratio is equal to 1/n times that of the individual device. In parallel connection, the equivalent W/L ratio is equal to 'n' times that of the individual device (n= no. of transistors connected).

- Expression for $(W/L)_{eq}$ for transistors connected in series:

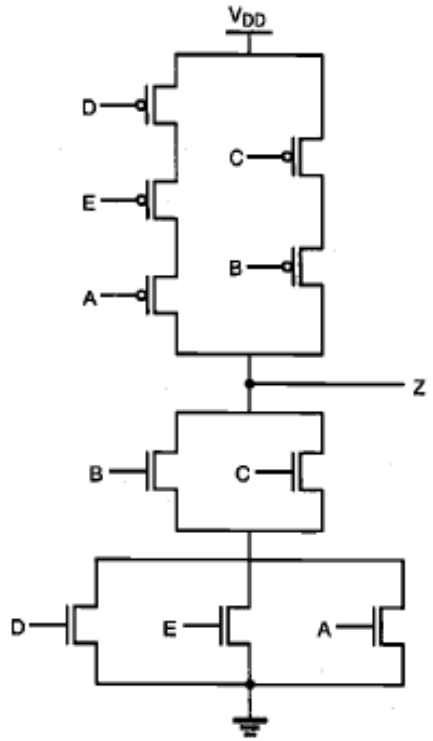
$$(W/L)_{eq} = \frac{1}{\frac{1}{(W/L)_1} + \frac{1}{(W/L)_2} + \ldots}$$

- The parallel connection of transistors with W/L ratios of $(W/L)_1, (W/L)_2, \ldots$, results in an equivalent W/L of

$$(W/L)_{eq} = (W/L)_1 + (W/L)_2 + \ldots$$

Transistor Sizing

Q. For the circuit diagram shown find an equivalent CMOS inverter circuit for simultaneous switching of all inputs, assuming that *(W/L)p = 15 for all pMOS transistors* and *(W/L)n = 10 for all nMOS transistors.*



The Boolean function realized by this circuit is

$$Z = \overline{(D+E+A)(B+C)}$$

The equivalent *(WIL) ratios of the nMOS network and the pMOS network are determined* by using the series-parallel equivalency rules

$$\left(\frac{W}{L}\right)_{n,eq} = \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_D + \left(\frac{W}{L}\right)_E + \left(\frac{W}{L}\right)_A} + \frac{1}{\left(\frac{W}{L}\right)_B + \left(\frac{W}{L}\right)_C}}$$

$$= \frac{1}{\frac{1}{30} + \frac{1}{20}} = 12$$

$$\left(\frac{W}{L}\right)_{p,eq} = \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_D} + \frac{1}{\left(\frac{W}{L}\right)_E} + \frac{1}{\left(\frac{W}{L}\right)_A}} + \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_B} + \frac{1}{\left(\frac{W}{L}\right)_C}}$$

$$= \frac{1}{\frac{1}{15} + \frac{1}{15} + \frac{1}{15}} + \frac{1}{\frac{1}{15} + \frac{1}{15}} = 12.5$$

THANK YOU

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