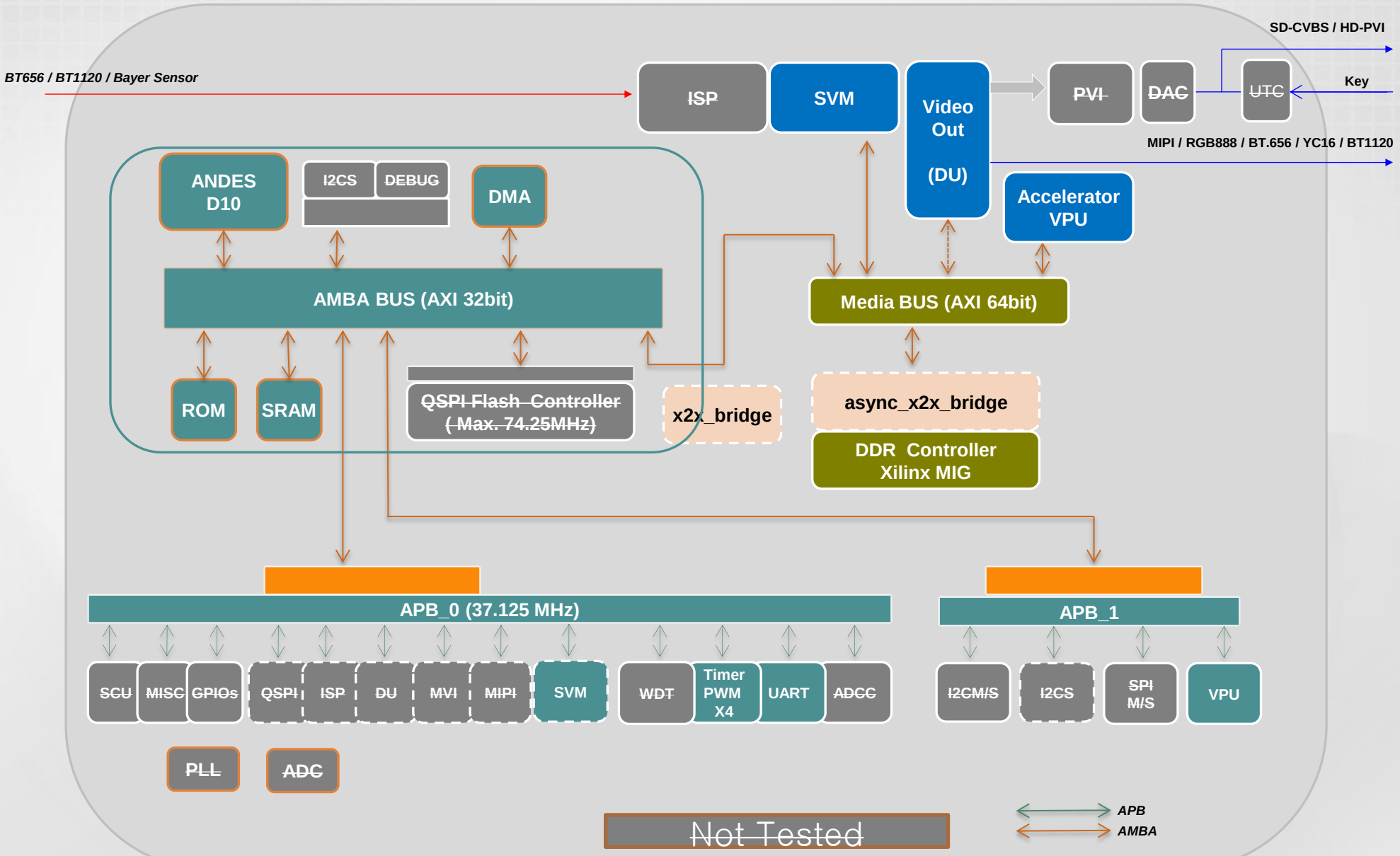
PI5008 FPGA Release 1차

PIXELPLUS

2017.02.22

Block Diagram



CPU Sub-system

❖ **ANDES D10**
N10 + DSP + SPU logic
D10 Datasheet - AndesCore_D1088-S_DS099_V1.2.pdf
DSP Datasheet - AndeStar_DSP_ISA_EXT_UM128_V1.0.pdf
SPU Datasheet - AndeStar_FPU_ISA_UM029_V1.3.pdf

❖ **PERIs**
- ✓ WDT
  Datasheet – AndeShape_ATCWDT200_DS088_V1.0.pdf
- ✓ UART
  Datasheet – AndeShape_ATCUART100_DS093_V1.0.pdf
- ✓ SPI
  Datasheet – AndeShape_ATCSPI200_DS087_V1.0.pdf
- ✓ Timer/PWM
  Datasheet – AndeShape_ATCPIT100_DS086_V1.0.pdf
- ✓ I2C
  Datasheet – AndeShape_ATCIIC100_DS091_V1.0.pdf
- ✓ GPIO
  Datasheet – AndeShape_ATCGPIO100_DS080_V1.0.pdf
- ✓ DMA
  Datasheet – AndeShape_ATCDMAC100_DS079_V1.0.pdf

Memory Map

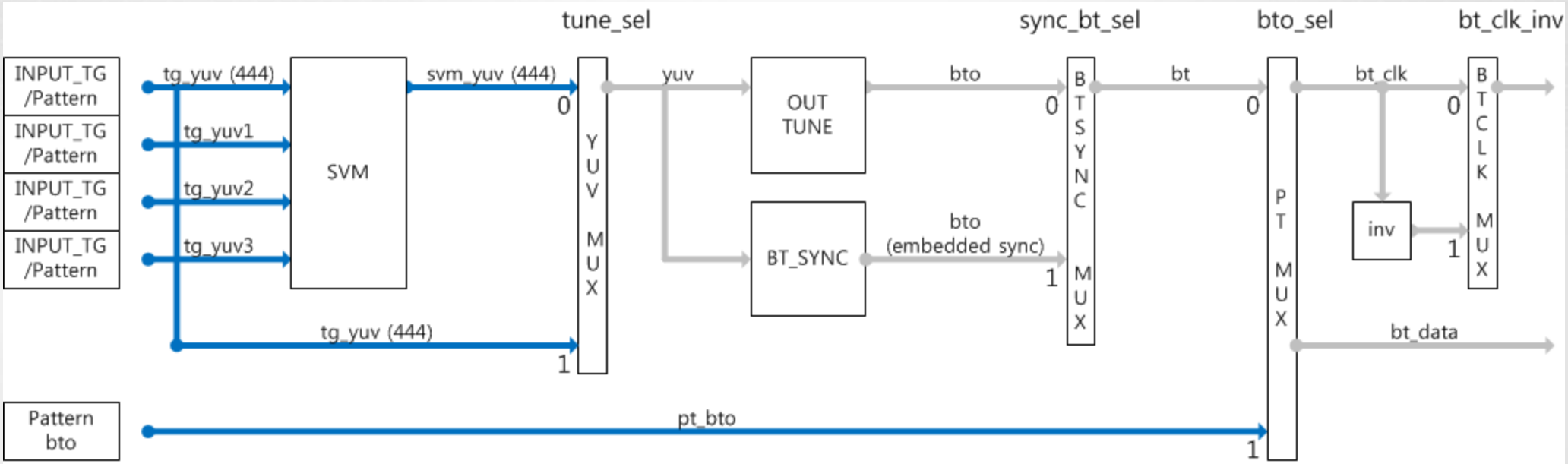
Address	Destination	추가 예정	Size
32'h0000_0000 ~ 32'h0000_3FFF	On-chip Boot Memory		16 KByte
32'h0001_0000 ~ 32'h0001_3FFF	On-chip SRAM Memory		16 KByte
32'h1000_0000 ~ 32'h1FFF_FFFF	SPI Flash Memory		256 MByte
32'h2000_0000 ~ 32'h2FFF_FFFF	DRAM Memory		256 MByte
32'hF000_0000 ~ 32'hF0FF_FFFF	Sync domain Peripherals		16 MByte
32'hF100_0000 ~ 32'hF1FF_FFFF	Sync domain peripherals		16 MByte
Pi5008 APB Register Map			
32'hF000_0000	SCU		1 Mbyte
32'hF010_0000	MISC		1 Mbyte
32'hF020_0000 32'h_____1000	GPIO0	GPIO0 GPIO1	1 Mbyte
32'hF030_0000	Reserved		1 Mbyte
32'hF040_0000	WDT		1 Mbyte
32'hF050_0000	DDRC		1 Mbyte
32'hF060_0000	ISP		1 Mbyte
32'hF070_0000	ISP SRAM		1 MByte
32'hF080_0000	SVM		1 Mbyte
32'hF090_0000	DU		1 Mbyte
32'hF0A0_0000	ADCC		1 Mbyte
32'hF0B0_0000 32'h_____1000	QSPI Memory Controller (Read only) SPI serial IF (for erase, program)		1 Mbyte
32'hF0C0_0000	TIMER (4 ch)	TIMER (8ch)	1 Mbyte
32'hF0D0_0000 32'h_____1000	UART 0	UART 0 UART 1	1 Mbyte
32'hF0E0_0000	MIPI		1 Mbyte
32'hF0F0_0000	Reserved		1 Mbyte
32'hF100_0000	I2CS (for picaso)		1 Mbyte
32'hF110_0000 32'h_____1000	I2CMS 0	I2CMS 0 I2CMS 1	1 Mbyte
32'hF120_0000 32'h_____1000	SPI 0	SPI 0 SPI 1	1 Mbyte
32'hF130_0000	Reserved		1 Mbyte
32'hF140_0000	VPU (Vaccel)		1 Mbyte
32'hF150_0000	Reserved	I2S	1 Mbyte
32'hF1E0_0000	Main BUS Matrix		1 Mbyte
32'hF1F0_0000	Media BUS Matrix		1 Mbyte
32'hF200_0000	DMA register		1 Mbyte

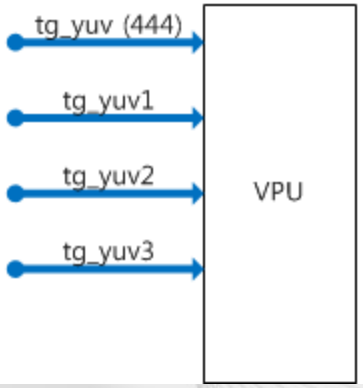
Not Tested

Interrupt Table

IRQ number	Name	Descriptioon
31	output bto_vsync	최종 출력의 vsync
30	svm vsync	SVM 출력의 vsync
29	cam3 vsync	입력 CAM3 의 vsync
28	cam2 vsync	입력 CAM2 의 vsync
27	cam1 vsync	입력 CAM1 의 vsync
26	cam0 vsync	입력 CAM0 의 vsync
25	VPU 1	VPU DMA done
24	VPU 0	VPU OTF done
23 : 19	–	
18	SPI	
17	i2c master	
16	UART	
15 : 10	–	
9	TIMER 0 (system)	
8	WDT	
7	DMA	
6 : 0	–	

Debug path - Image





0xf01000ec – Mux Selcet
[7] : bto_sel
[6] : tune_sel
[5] : bto_clk_inv
[4] : sync_bt_sel
[3:0] : VCLK_inv[3:0] (input vedio clock inversion)

Test Pattern

Pattern Gen (0xf010_00e8)		
[7]	Pattern enable	0 : Normal Input 1 : Test Pattern Enable
[6:4]	Mode	When Clock = 37.125M (현재 동작 Mode 임) 0 : 1280x720@30 1 : 1280x720@25 2 : 1280x720@15 3 : 1280x720@12.5 4 : 1920x1080@15 5 : 1920x1080@12.5 When Clock = 74.25M 0 : 1280x720@60 1 : 1280x720@50 2 : 1280x720@30 3 : 1280x720@25 4 : 1920x1080@30 5 : 1920x1080@25
[3:0]	Pattern	0 : Black 1 : Blue 2 : Red 3 : Magenta 4 : Green 5 : Cyan 6 : Yellow 7 : White 8 : Color Bar 9 : Ramp A : Hatch B : Square Box C : Mixed Pattern with Moving Bar

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감사합니다