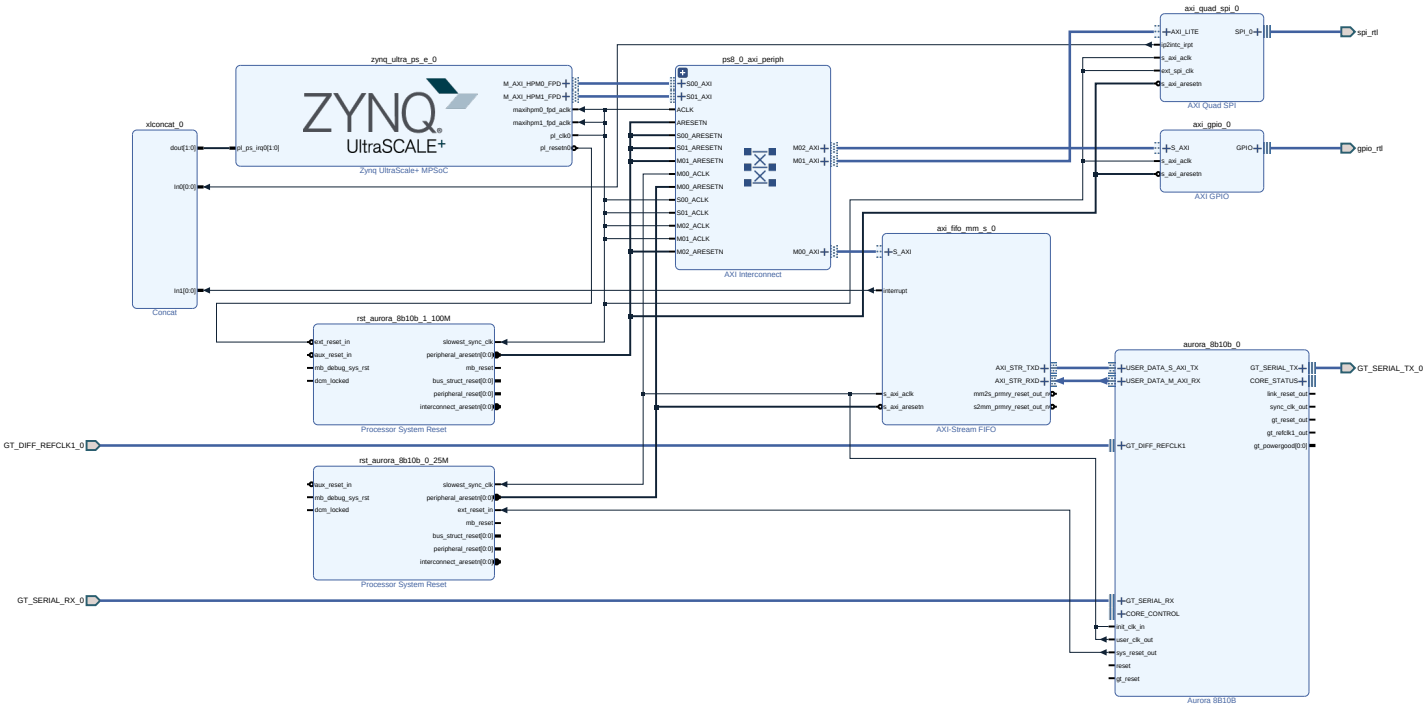
axi_quad_spi_0
AXI_LITE
ip2intc_irpt
s_axi_aclk
ext_spi_clk
s_axi_aresetn
SPI_0
AXI Quad SPI
spi_rtl
axi_gpio_0
S_AXI
s_axi_aclk
s_axi_aresetn
GPIO
AXI GPIO
gpio_rtl
zynq_ultra_ps_e_0
ZYNQ
UltraSCALE+
pl_ps_irq0[1:0]
M_AXI_HPM0_FPD
M_AXI_HPM1_FPD
maxihpm0_fpd_aclk
maxihpm1_fpd_aclk
pl_clk0
pl_resetn0
Zynq UltraScale+ MPSoC
xlconcat_0
dout[1:0]
in0[0:0]
in1[0:0]
Concat
ps8_0_axi_periph
S00_AXI
S01_AXI
ACLK
ARESETN
S00_ARESETN
S01_ARESETN
M01_ARESETN
M00_ACLK
M00_ARESETN
S00_ACLK
S01_ACLK
M02_ACLK
M01_ACLK
M02_ARESETN
M02_AXI
M01_AXI
M00_AXI
AXI Interconnect
axi_fifo_mm_s_0
S_AXI
interrupt
s_axi_aclk
s_axi_aresetn
AXI_STR_TXD
AXI_STR_RXD
mm2s_prmry_reset_out_n
s2mm_prmry_reset_out_n
AXI-Stream FIFO
rst_aurora_8b10b_1_100M
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
slowest_sync_clk
peripheral_aresetn(0:0)
mb_reset
bus_struct_reset(0:0)
peripheral_reset(0:0)
interconnect_aresetn(0:0)
Processor System Reset
aurora_8b10b_0
USER_DATA_S_AXI_TX
USER_DATA_M_AXI_RX
GT_SERIAL_TX
CORE_STATUS
link_reset_out
sync_clk_out
gt_reset_out
gt_refclk1_out
gt_powergood[0:0]
GT_DIFF_REFCLK1
GT_SERIAL_RX
CORE_CONTROL
init_clk_in
user_clk_out
sys_reset_out
reset
gt_reset
Aurora 8B10B
GT_SERIAL_TX_0
GT_DIFF_REFCLK1_0
rst_aurora_8b10b_0_25M
aux_reset_in
mb_debug_sys_rst
dcm_locked
slowest_sync_clk
peripheral_aresetn(0:0)
ext_reset_in
mb_reset
bus_struct_reset(0:0)
peripheral_reset(0:0)
interconnect_aresetn(0:0)
Processor System Reset
GT_SERIAL_RX_0