UNIVERSITY OF ALASKA FAIRBANKS

COLLEGE OF ENGINEERING AND MINES

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

COURSE CODE	EE F102 F01 (CRN: 34544)
COURSE NAME	INTRODUCTION TO ELECTRICAL AND COMPUTER ENGINEERING
SEMESTER	SPRING
YEAR	2022
LABORATORY LOCATION	ELIF 331 (ELECTRONICS LAB)
LAB SESSION DATE AND TIME	MONDAY 21 FEB 2022
TYPE OF SUBMISSION	LABORATORY REPORT
NUMBER OF SUBMISSION	5
TITLE OF SUBMISSION	BOARD LAYOUT
METHOD OF SUBMISSION	ONLINE TO: maher.albadri@alaska.edu
DUE DATE OF SUBMISSION	MONDAY 28 FEB 2022
DUE TIME OF SUBMISSION	23:59
STUDENT NAME	

MAKE THIS FORM A "COVER PAGE" FOR YOUR REPORT SUBMISSION.

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REMARKS:

BOARD LAYOUT

Objective

In this lab we will gain experience creating a circuit board layout. We will investigate footprints and other physical constraints of a board layout. This lab will create a voltage regulator board to use with your Arduino when it is not connected to the computer. J1 will connect to a battery connector, and J2 and J3 will connect to a 4-pin SIP that can be plugged directly into your protoboard.

Requirements

- Turn in alongside your Lab 5 report three design files: Bottom_*yourname*.art, Outline_*yourname*.art, and *yourname*.drl
- Turn in Lab 5 report which includes a schematic of what we are building, a figure showing your final layout, a short discussion of the layout and any constraints that exist on the layout design.

1. Open Design Entry CIS and build the circuit shown in Figure 1 using the parts contained in the EE102_LIBRARY that you downloaded in lab 2.

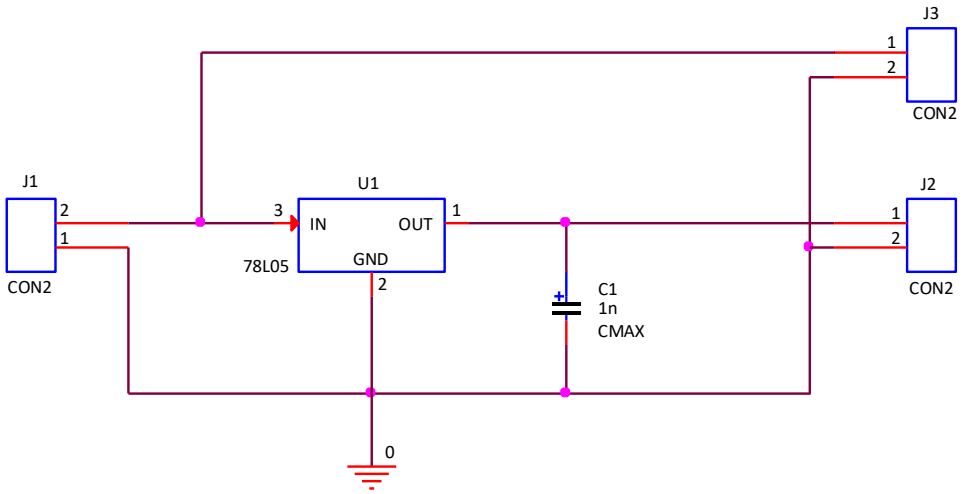

Figure 1. Complete schematic for voltage regulator board.

2. Select the 78L05 voltage regulator. Right click and select **Show Footprint**. Your footprint should display in the Footprint Viewer window. The pins for this are too close together. We need to change the footprint that the part points to.
3. Right click on the 78L05 and select **Edit Properties**. The **Property Editor** dialog box may display data for this part in a row or in a column. Scroll over to the right or down until you find the heading **PCB Footprint**. The field contains the code TO92. This code means that the package for this part is Transistor Outline Package, Case Style 92. A footprint is a physical description of the device. Most of the footprints needed are already be available in the standard Cadence library. We want to use a slightly modified package where the leads are slightly further apart. Change this to TO92_100. Close the **Property Editor** dialog box.
4. Right click on the 78L05 voltage regulator and select **Show Footprint** again. If a footprint doesn't show up, download the to92_100.dra and to92_100.psm from CANVAS to yourfolder *your_project_folder*\allegro\symbols. If the allegro\symbols folders do not exist, create them. After you have downloaded the files to your allegro\symbols folder check and see if you can see the footprint. IF YOU STILL CANNOT SEE THE FOOTPRINT ASK

FOR HELP!!

5. Select other components. You should see that all components have their PCB footprints pre-defined for you. If you do not see footprints for all the parts then Cadence cannot find the footprints and you should contact me for help.
6. At this point the schematic has been drawn and the part footprints defined. We now need to export this information into a layout tool. Click the **Project Manager** tab at the top of the window. Select your ***.dsn** project name and then select the **Create Netlist** icon at the top of

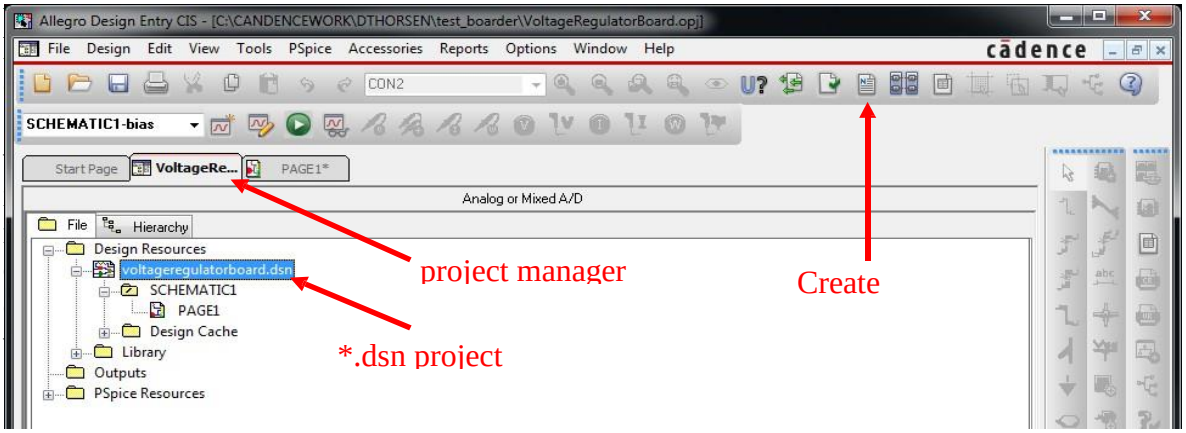

Figure 2. Create netlist icon.

7. The **Create Netlist** dialog box appears. Select the **PCB Editor** tab. Make sure that *PCB Footprint* is in the **PCB Footprint** field and that the box next to **Create PCB Editor Netlist** is selected. Click **OK** and exit **Design Entry CIS**. (see Figure 3.)

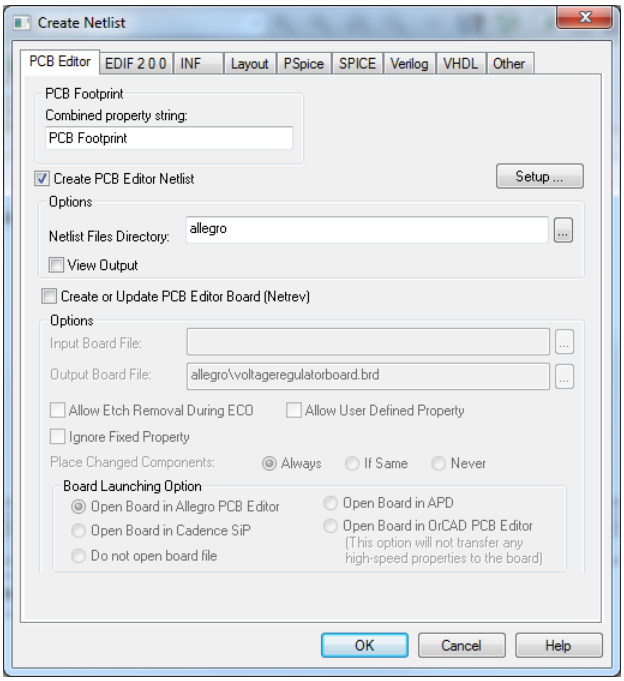

Figure 3. Create Netlist dialog box.

8. Start PCB Editor: *Start->Programs->Cadence->Release 16.5->PCB Editor*. In Juneau the program is called OrCAD PCB Editor Lite. In the **Cadence Product Choices** pop-up window select *Allegro PCB Designer*.

9. Create a new design: *File->New*. When the **New Drawing** dialog window appears **Browse** to select the allegro folder in your design folder and name your board design. Scroll through the various **Drawing Types** and select **Board (Wizard)**. Select OK.

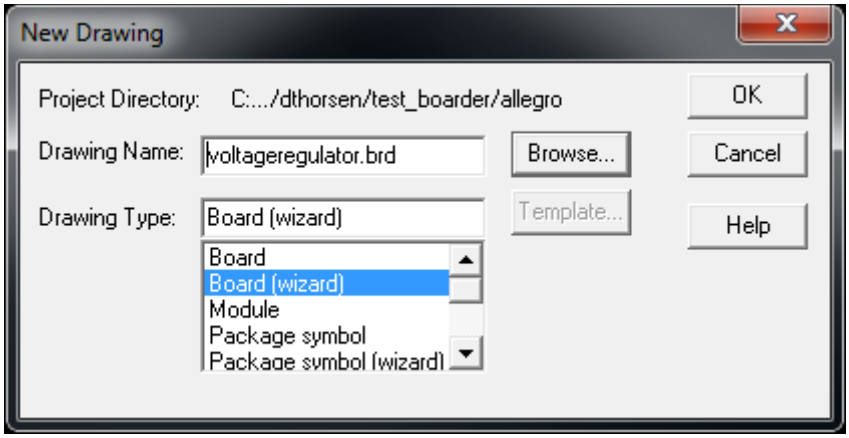

Figure 4. New Drawing dialog box.

10. The **Board Wizard** will help us define various parameters used in creating our board. These include Drawing units, size, and origin; Board outline; Grid spacing; Board cross-section; and Initial Constraints.
    a. Select Next four times. We do not have a board template, tech or parameter files, or board symbol.
    b. When you reach the **Parameters** section you should select the following:
        i. Units: Mils
        ii. Size: A
        iii. Location of Origin: At the center of the drawing
        iv. Grid spacing: 1 mils
        v. Etch layer count: 2
        vi. Default definitions: Don't generate artwork films.
    c. Under Custom Data select:
        i. Etch layer: Layer Name – Top, Layer Type – Routing Layer.
        ii. Etch layer: Layer Name – Bottom, Layer Type – Routing Layer
        iii. Unselect: Generate negative layers for Power planes
        iv. Minimum Line Width: 50 mils
        v. Minimum Line to Line spacing: 20 mils
        vi. Minimum Line to Pad spacing: 20 mils
        vii. Minimum Pad to Pad spacing: 20 mils
        viii. Default via padstack: via
        ix. Board Outline: Rectangular board
        x. Width: 1000 mils
        xi. Height: 1000 mils
        xii. Corner cutoff: unselect

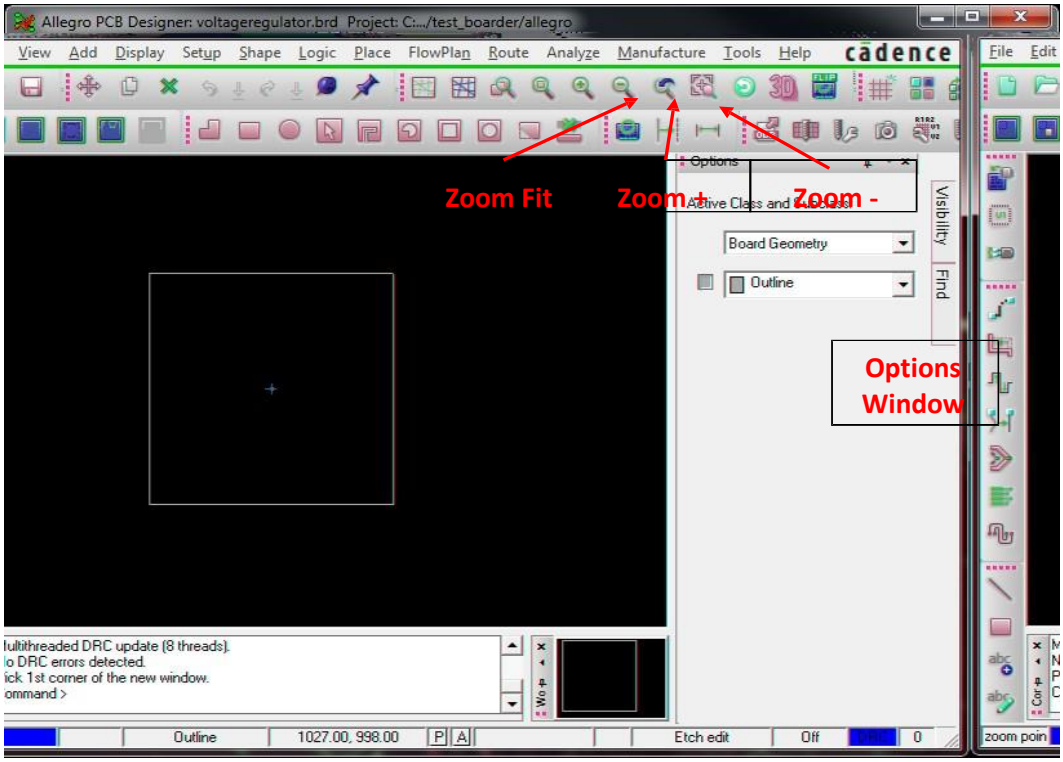

Figure 5. Design showing board outline.

d. Select Next and Finish. Select the Zoom Fit button and the Zoom + or Zoom – button to see your board. You should see something similar to Figure 5. You can open the Options window by selecting the tab to the right of the design and then clicking on the "push pin" icon.

e. Now it's time to import your design into PCB Editor. Select *File->Import->Logic*. Under the Cadence tab select "Design entry CIS (Capture)" and browse to select the *allegro* folder under your project folder as the "Import Directory". Select **Import Cadence**.

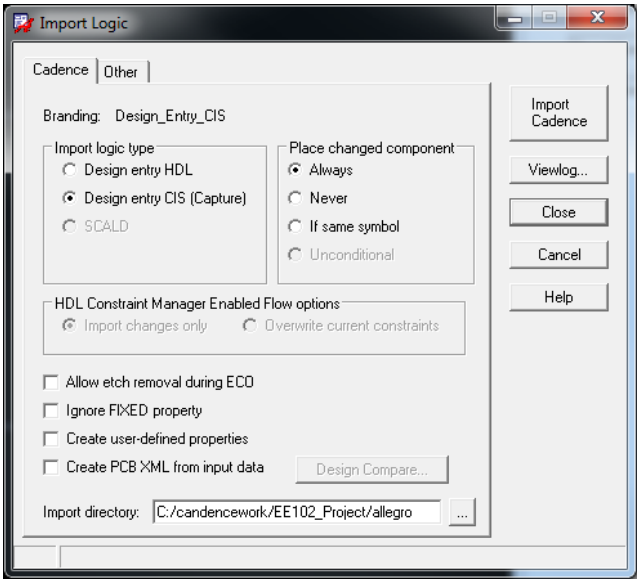

Figure 6. Import Logic pop-up window.

f. Now that we have imported the logic, we have to place the parts on our design. Select *Place->Quickplace*. The **Quickplace** pop-up window should appear. You want to "Place all components", place them "Around package keepin" at the "right" edge, on the "top" board layer. After you verify that the appropriate selections are made, select **Place**, then select **OK**. Your window should now look something like Figure 7. Right now this looks like a jumble of stuff. What you are seeing is the board outline. The footprints of each of your parts and the logical connections between the parts. The logical connection lines between the parts are called the "rats nest" for obvious reasons. Our board only has 15 parts. Can you imagine what the "rats nest" would look like if we had 100 parts on the board. You can turn on and off the "rats nest" by selecting the "Unrats all" and "Rats all" icons.

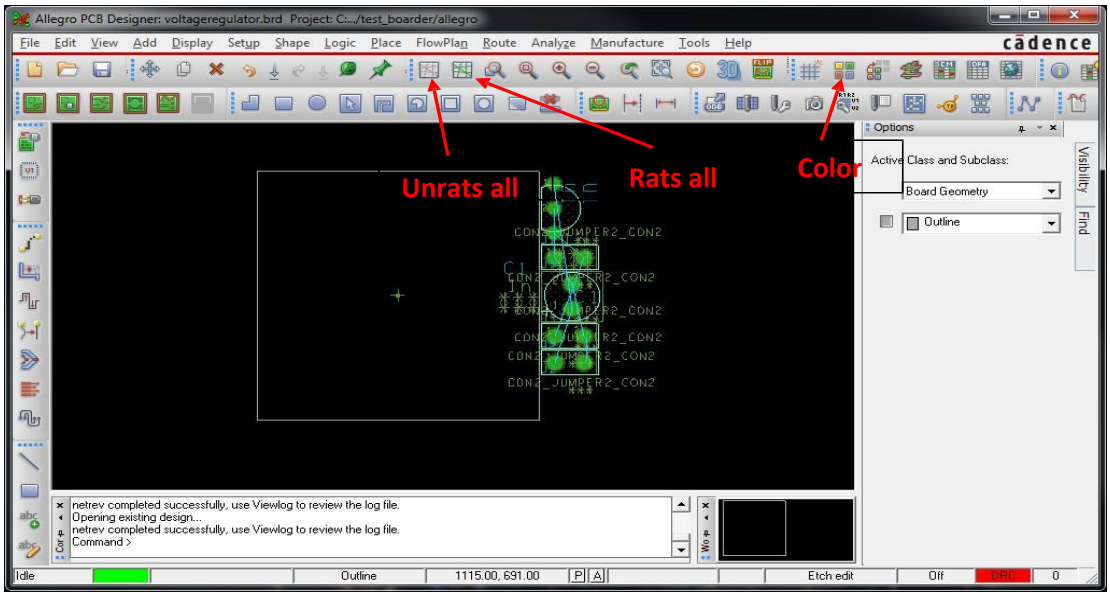

Figure 7. Design window after Quickplace.

11. Now we need to adjust some colors to make it easier to see what we are doing. Select the **Color** icon to access the **Color Dialog** box. Select Global Visibility -> OFF. If you select the Apply button you will see your design disappear. Turn back on the following by selecting the appropriate boxes:
    a. Stack-up – Bottom (select Pin, Etch, DRC), Soldermask_Bottom (select Pin)
    b. Board Geometry – Outline,
    c. Package Geometry – Assembly_Top;
    d. Components – Assembly_Top (select RefDes).

    Now your design should look like Figure 8 when the "rats nest" has been turned off.

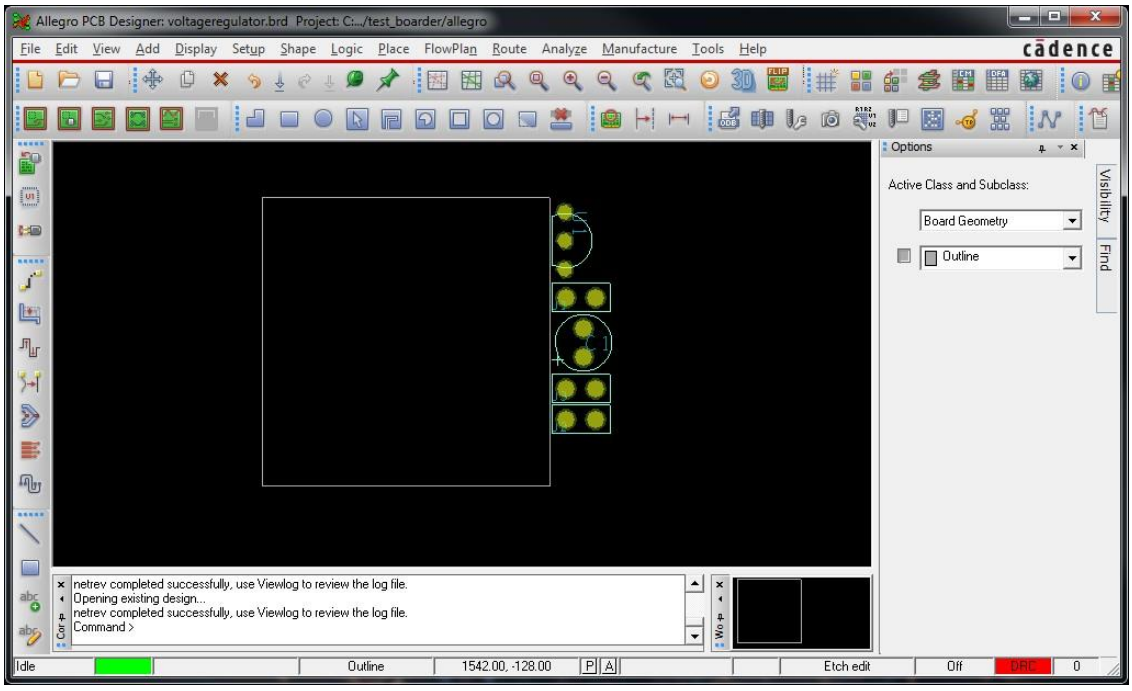

Figure 8. Design window after Color adjustments with Unrats all selected.

12. Now your job is to place each of your parts inside your board outline as efficiently as possible so that the board will route. This is often a difficult task. Try to find the optimum placement yourself. If you are having difficulty, you can use the final layout of this lab (Figure 9). Optimal placement of the parts can be obtained by making sure that the minimum number of "rats" (i.e. the logical connection between parts) cross one another. You can move parts around by selecting the Move icon then the part you wish to move. If the part is not in the orientation you want then after you select it, right click and select rotate. Move your mouse around until the orientation you want is achieved. Left click to exit Rotate, left click again to place the part where you want it. You might want to have your schematic open while you place your parts. It sometimes helps to visualize which parts should be placed next to each other.
13. Two of the connectors should be lined up next to each other so that all four pins are in a row and that all the pins are 100 mils apart. You can check the placement of the pins by using the ruler icon and then selecting the pins of the connectors. The measure dialog box will appear and show you the Dx and Dy measurements.
14. In addition to placing all of our components we need to place two "mechanical" parts that we will use as strain relief holes. You want to place two holes around the connector to the battery (J1). To place the "mechanical" part, select *Place->Manually*. Select the **Advanced Settings** tab and make sure the box next to **Library** is selected. Switch back to the **Placement List** tab. Select Mechanical symbols in the pull down menu and expand the Mechanical symbols folder. Select MTG125 as the mechanical hole to place.
15. Once you believe that everything is placed where you want it you can then route your board. This year we will manually route the board (don't use the Auto-router!). Select *Route->Connect* or the *Add Connect* icon. We will only route on the bottom of the board. Look at the Options tab and make sure that the Active Class and Subclass are Etch and Bottom. Select a pin to start the route and pull your cursor to connect the next pin. Continue until all nets are routed.

16. If after all your nets are routed you see any little red hourglass symbols, that means you have design rule errors. These should be corrected before the final artwork is created. Most of the time these errors are because you routed a trace too close to another trace or pad. If this is the case you can select the *Slide* icon and move the offending trace. When all is done select *Tools -> Update DRC* and verify that there are no additional design rule errors.
17. Final step is to generate your artwork that represents your design. You will need to create three files: a drill file that describes the location and size of all holes that need to be drilled, the artwork that defines the traces on the bottom layer, and the artwork that defines your board outline.
    a. Drill File: Select *Manufacture->NC->NC Drill*. Verify the Root file name and select **Drill**.
    b. Bottom Layer: Select *Manufacture->Artwork*. Select the Bottom box. Make sure that "Film Mirrored" is selected, then click on the **Create Artwork** box.
    c. Board Outline: Select *Manufacture->Artwork*. Notice that the defined folders are only for the top and bottom layers. We need to create another folder that will define the outline. First you need to turn OFF all layers expect the board outline in the COLORS (do you remember how?) Select the **COLOR** icon. Click on **Global Visibility OFF**. Select **Board Geometry -> Outline**. Select **Apply**. You should now see only your board outline. Go back to your Artwork Control Form pop-up window. Right click on one of the folders shown and select **Add**. Enter new film name **OUTLINE**. Under Film Options set the **Undefined line width to 10**. Finally click on **Create Artwork** box.
    d. You need to submit three design files: **BOTTOM.art**, **OUTLINE.art** and ***.drl**. Rename each of these files to ***yourname*_Bottom.art**, ***yourname*_Outline.art** and ***yourname*.drl** and submit them with your lab report.
18. To capture an image of your layout choose *File->Capture Canvas Image*. This will create a jpeg of your layout.

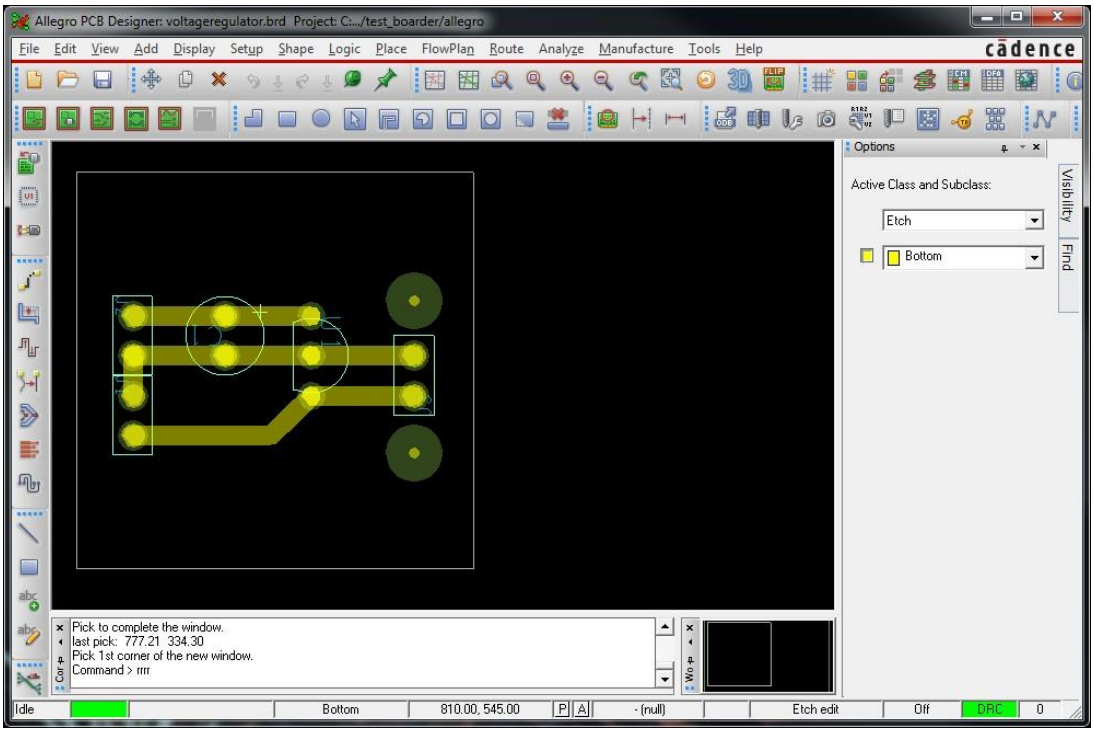

Figure 9. Final layout.