Processor Usage by Motor Control Interrupts

One approach to running the stepper is having an interrupt which pulses the step pin. My concern is that this interrupt will consume too many processor cycles. As shown by the calculations below, this concern is unfounded, as running the motor will take worst case 1.33% of CPU cycles.

Clock cycles required for single step pulse initiated by an interrupt:

Operation	**Worst Case (# cycles)**
Interrupt Entry	15
Direct port set	1
Hold on high	7
Direct port clear	1
Increment position counter	1
Interrupt Return	15
Total	**40**

Number of Interrupts per second:

My simulations showed the motor speed was below 600RPM. 600RPM is 10 rot/sec which, at 1600 microstepping, is 16000 steps per sec. With 40 cycles per step, this is 640,000 cycles. The processor is 48MHz, so that's a mere 1.33% of clock cycles.

References

Interrupt Entry

To reduce interrupt latency and jitter, the Cortex-M0+ processor implements both interrupt late-arrival and interrupt tail-chaining mechanisms, as defined by the ARMv6-M architecture. The worst case interrupt latency, for the highest priority active interrupt in a zero wait-state system not using jitter suppression, is 15 cycles.

(Cortex M0 Technical Reference Manual, 3.6.1 Exception Handling)

Direct Port Set High

Operation	**Description**	**Assembler**	**Cycles**
Store	Word, immediate offset	`STR Rd, [Rn, #<imm>]`	2 or 1[b]

(Cortex M0 Technical Reference Manual, 3.3 Instruction Set Summary)

1 clock cycle if word is written to single-cycle I/O port, which is what I'm doing

Hold on High

STEP and DIR interface timing	**AC-Characteristics** clock period is t_{CLK}					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
step frequency (at maximum microstep resolution)	f_{STEP}				½ f_{CLK}	
fullstep frequency	f_{FS}				f_{CLK}/512	
STEP input minimum low time	t_{SL}		max(t_{FILTSD}, t_{CLK}+20)	100		ns
STEP input minimum high time	t_{SH}		max(t_{FILTSD}, t_{CLK}+20)	100		ns
DIR to STEP setup time	t_{DSU}		20			ns
DIR after STEP hold time	t_{DSH}		20			ns
STEP and DIR spike filtering time *)	t_{FILTSD}	rising and falling edge	13	20	30	ns
STEP and DIR sampling relative to rising CLK input	$t_{SDCLKHI}$	before rising edge of CLK input		t_{FILTSD}		ns

(TMC2209 Stepper Motor Driver Datasheet, 13.1 STEP/DIR Interface Timing)

48Mhz is 20 ns per cycle. 100 ns STEP input minimum high time typical means the processor should hold the output high for at least 5 clock cycles (let's say 7 to be safe)

Direct Port Set High

Same as direct port set

Increment Position Counter

Add	3-bit immediate	ADDS Rd, Rn, #<imm>	1

(Cortex M0 Technical Reference Manual, 3.3 Instruction Set Summary)

Interrupt Return

I could not find in the datasheets a number for the clock cycles required on interrupt return, but I certainly would not expect it to be more than the number required for interrupt entry, so I'm using that as my worst case bound.