3T-APS CMOS Imager

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***Abstract*—This paper presents the circuit schematic, layout, and simulation of a 3T-APS (3-Transistor Active Pixel Sensor) CMOS (Complementary Metal Oxide Semiconductor) Imager. We implement the TSMC 18 nm technology node in Cadence Virtuoso for all designs and simulations while utilizing many key components such as photodiode, shift register, and APS.**

Keywords—CMOS imager, APS, shift register, photodiode

I. Introduction

CMOS image sensors are widely used in numerous modern digital applications due to their advantages such as low power consumption, low cost, high frame rates, and compact size. To gain a deeper understanding of their functionality and the complexities of their design, we undertook the development of a CMOS image sensor from the analog front-end to the digital output. A typical CMOS imager is composed of three primary components: Active Pixel Sensors (APS), a readout system, and shift registers. The APS captures light through a photodiode. It does this by converting accumulated photons into electrical current using the photodiodes. Each pixel includes three transistors that control timing and determine when photocurrent is generated. The readout system collects the photocurrent from each pixel and converts it into a readable output. In our design, we used a faster scanning technique to read the pixels sequentially. The shift registers control which rows and columns are accessed, as well as manage the reset functionality. We implemented this using two shift registers to coordinate the row and column selection.

II. APS

A. APS Schematic

The APS schematic consists of three CMOS transistors arranged such that the photodiode limits the current flow.

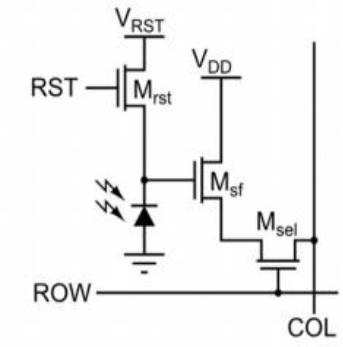

Fig 1. 3T APS schematic

Fig. 1 shows the structure of each pixel, which includes a photodiode and three transistors: Mrst, Msf, and Msel. The photodiode is reverse-biased, meaning it blocks current flow unless photons are present. When light strikes the photodiode, it generates electron-hole pairs, causing electrons to accumulate in the depletion region. These charges are later converted into a drift current. Since Cadence software does not support a true photodiode model, we devised an alternative method for simulation.

We created a current mirror using two CMOS transistors to mimic a constant photocurrent. The Mrst transistor functions as a reset switch. When the RST signal is high, Mrst turns on and charges the photodiode's capacitance to approximately VDD − Vth. In our design, we set VRST = VDD. When RST goes low, the photodiode begins integrating the light-generated charge, which is then converted into a voltage signal. The Msf transistor acts as a source follower, offering high input impedance and low output impedance to buffer and preserve the voltage level. This signal then flows to Msel, the select transistor. When the ROW line is high, Msel turns on, allowing the pixel's output to pass onto the COL line for readout.

B. APS Pixel Layout

When designing an APS pixel, maximizing the surface area of the photodiode is essential, as it directly impacts the pixel's ability to capture incident light. A larger photodiode area results in improved light sensitivity and overall image quality. Working within a pixel size constraint of 10 µm × 10 µm, we optimized the layout to achieve a fill factor of 84.63%, meaning that the photodiode occupies the majority of the pixel area, enhancing light collection efficiency without compromising the functionality of the supporting transistors.

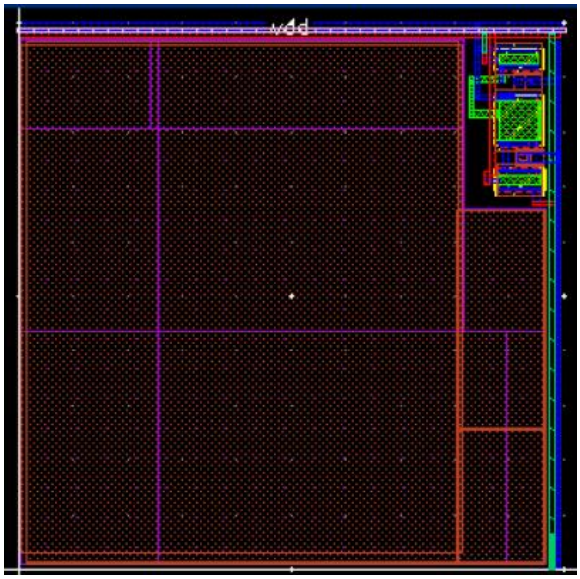

Fig 2. APS Pixel Layout with 84.63% Fill Factor

An important aspect of the pixel layout was ensuring easy connectivity to neighboring pixels. We assigned distinct metal layers to each pin, which improved routing, contributed to the 84.63% fill factor, and allowed the design to pass both DRC and LVS in Cadence. VDD was routed using vertical and horizontal metal1 rails for consistent distribution across the array. COL and RST were routed vertically using metal2 and metal3, while ROW used a horizontal metal5 rail for row-wise access. The photodiode and CMOS transistors were built in a p+/n-well/p-substrate structure, with interconnections made using metal1 and vias. The final layout, shown in Fig. 2, met all design and verification requirements.

III. Readout Infrastructure

To properly obtain the value of the photocurrent, each column needed their own readout infrastructure. Thus, at the bottom of each column, a current mirror was added to permanently drag down the value floating on the line at all times. This makes it possible to always read the induvial APS value when that value is sent to the readout line.

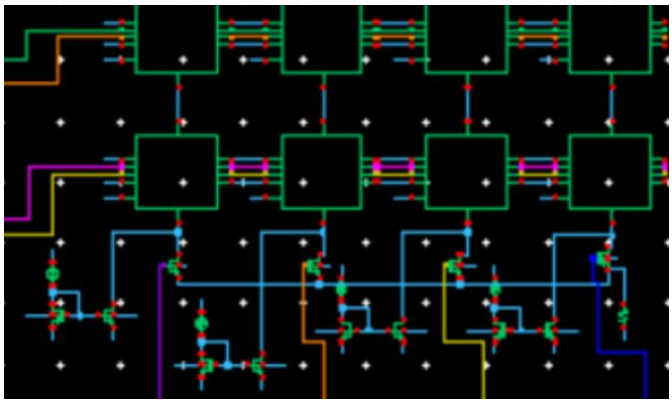

Figure 3. Readout current mirrors present on bottom of each column

IV. Shift Registers

Shift registers were used to control the timing of the rail values such that the APS was being read out at the correct time. Thus, ROW, RST, and Output each were connected to their own shift register circuits.

A. APS Schematic

Multiple C2MOS D-latches were chained together, each q connected to the next d, in series to from the basic shift register.

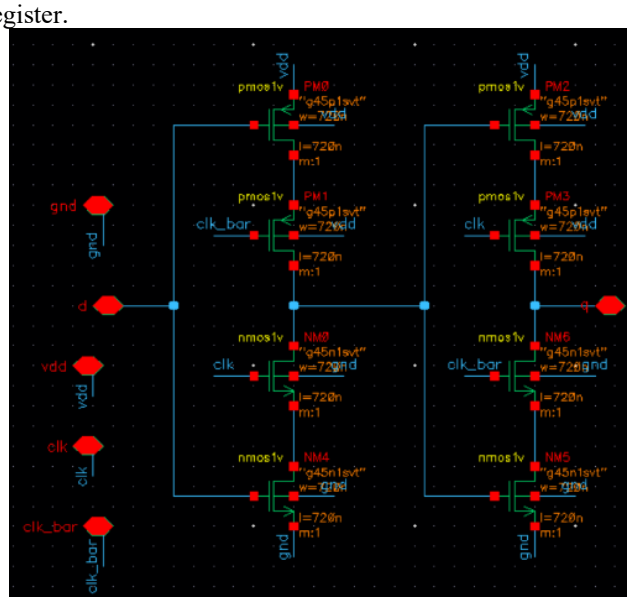

Fig 4. C2MOS D-Latch Schematic

As shown in Fig. 4, the D-latch is controlled by a clock and its inverted counterpart, with D as the input and Q as the output. This configuration enables precise delay of pulse signals, making it well-suited for controlling APS pixel selection. When multiple D-latches are connected in series, they form a shift register, advancing the pulse to the next Q output on each falling edge of the clock.

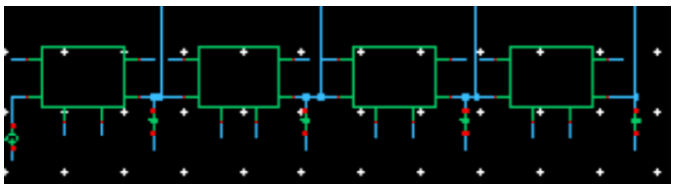

Fig 5. 4-Bit Shift Register using chained C2MOS D-Latches Schematic

As shown in Fig. 5, the D-latches are connected in series, forming a 4-bit shift register with accessible outputs at each stage. This setup allows us to tap the output of every D-latch individually.

B. Shift Register Layout

To begin the shift register layout, we first designed and verified the layout of a single D-latch, ensuring it passed both DRC and LVS checks. Once validated, we chained the D-latches together, aligning their pitch with that of the APS array

to ensure seamless integration and proper alignment with the pixel inputs.

Fig. 6 Chained C2MOS D-Latch Layout

V. 4X4 APS ARRAY

Using the APS, readout circuitry, and shift registers, we implemented a 4×4 APS array schematic to simulate and verify proper readout timing. Additionally, we created a complete layout of the 4×4 APS array excluding the readout circuitry.

C. *APS Timing*

To achieve accurate and stable readout from the 4×4 APS array, precise timing of all control signals was essential. Starting with the shift registers, we ensured that all columns of a given row were read before advancing to the next row. To accomplish this, each active row period consisted of four column pulses, aligning one pulse per column. We also minimized timing gaps between row and column select signals for smooth operation. To synchronize both shift registers using a single clock, the output of the final column shift register was used as the clock input for the row shift register, triggering the next row after every four column cycles.

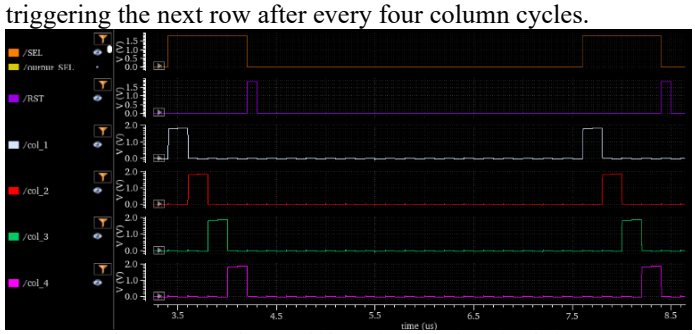

Fig. 7 ROW and COL Shift Register Timing Simulation

As shown in Figure 8, each row consists of exactly four column pulses, with the row triggered immediately after the last column pulse. Once the shift register timing was established, the next step was to define the timing for the RST and readout control signals. Since each pixel needed to be reset after being read, we reused the column select signal as the RST pulse

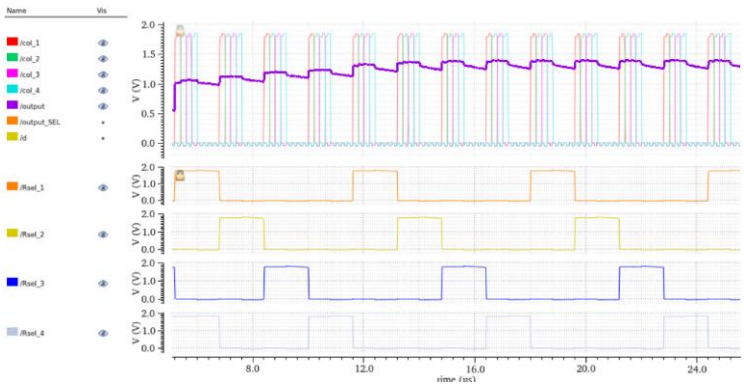

Fig. 8 4x4 APS Array Functionality

D. *APS Simulation*

As mentioned previously and now demonstrated in Figure 8, when the corresponding column and row value are high, the output is read as measure of the photocurrent from the APS cell. Thus, measurements of amount of light (simulated in Fig 8. with unique current mirror representations) falling on the photodiode area can be recorded and read neatly into memory.

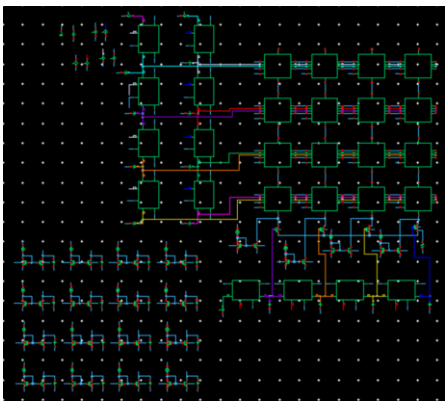

Fig. 9 4x4 Pixel Array Simulation Schematic

VI. FULL 248X249 IMPLIMENTATION

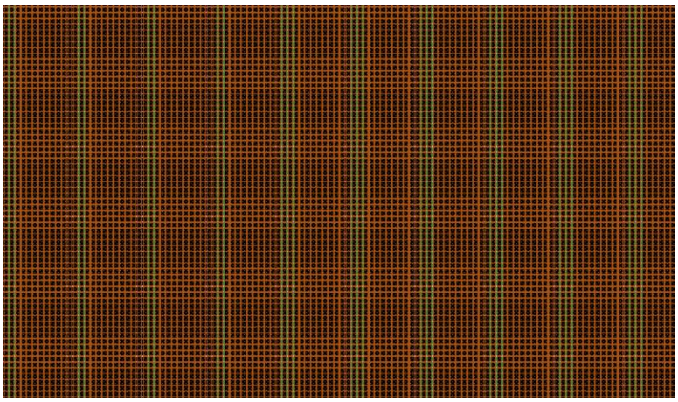

Fig. 10 Full 248x249 Layout

As seen in Figure 10, by tiling the APS as well as their corresponding shift register infrastructure, a fuller implementation of the technology can be achieved. All the prior designs are strictly tileable, such that we can use Mosaic to implement complete imagers with no limitations very quickly. To do this, we use 2 main building blocks:

1. The D-flip flop: this has three custom variations for the R-sel, C-sel, and /Rst shift registers as seen in figure 10
2. The APS Pixel

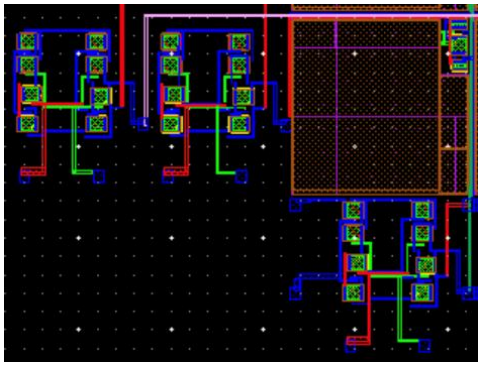

Fig. 11 4x4 All Individual Building Blocks

With a 10x10 micron clearance in between, all tiles fit together perfectly, such that no wiring or positioning is required.

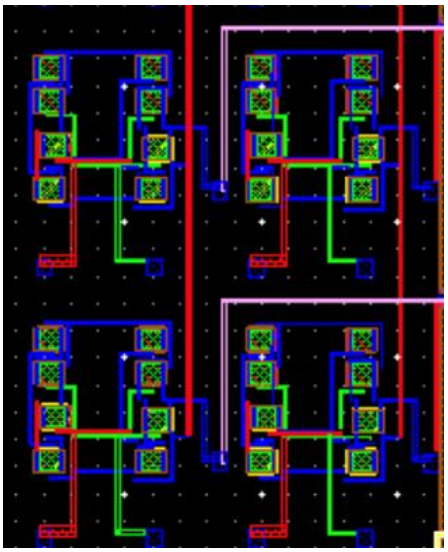

Fig. 12 All Connections Valid

Thus, with DRC and LVS passing, the 3T-APS CMOS Imager is complete.

VII. Global Impacts of IC Design

The development of integrated circuits (ICs) has progressed swiftly in accordance with Moore's Law, with engineers pushing to pack more transistors onto each chip. However, alongside these advancements, the environmental footprint of manufacturing these devices must be carefully considered. The semiconductor production process includes several stages—wafer fabrication, wafer creation, chemical processing for fabrication, and assembly or packaging—each producing various types of waste. For instance, producing a silicon wafer roughly 1 cm^2 can generate as much as 17 kg of wastewater, 7.8 kg of solid residues, and requires a significant amount of energy (Williams 2002). During chemical processing, hazardous substances are emitted from wet chemical baths used for wafer cleaning, coating steps for photolithography, and doping operations. These emissions occur via evaporation or atomization and, if not managed properly, can pollute water sources and release greenhouse gases that contribute to climate change. Consequently, as semiconductor technologies advance, it is essential for companies to innovate and implement effective waste reduction and management solutions.

VIII. Engineering Ethics

While developing our CMOS Imager, we adhered closely to the IEEE Code of Ethics. In particular, we focused on Rule I.5, which encourages seeking, accepting, and providing honest critique of technical work, acknowledging and correcting mistakes, presenting claims and estimates truthfully based on available data, and properly crediting the contributions of others. Throughout the project, we consistently sought feedback from our professor and teaching assistant, which enhanced our understanding of CMOS Imager design and supported our development process. We maintained transparency by asking for help when needed and ensured proper recognition of those who provided guidance. Additionally, we followed Rule I.7 of the IEEE Code of Ethics by treating everyone fairly and respectfully, valuing our peers both inside and outside the classroom.

Acknowledgments

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