CMOS IMAGER

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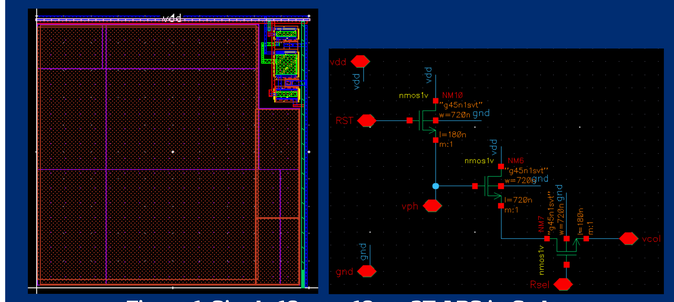

Figure 1: Single 10µm x 10µm 3T APS in Cadence layout (left) and schematic (right) with FF = 84.63%

Overview

The 2.5mm x 2.5mm CMOS photodiode lattice forms the basis of a rudimentary camera device. Built using Cadence Virtuoso, the design and schematic of our CMOS imager are standardized to the TSMC 0.18µm library. Each 10µm by 10µm active pixel sensor (APS), consisting of an nwell-psubstraight light sensitive photodiode with its corresponding integration infrastructure, is scanned using shift registers composed themselves of falling edge d-flipflops. With each of the three register circuits controlling reset, row select, and column select lines, the image is captured and prepared to be stored in memory.

Parameters

The imager should maximize the photodiode within the 2.5mm x 2.5mm area. This 'fill factor' will be obtained through the optimization of the integration infrastructure within the 10µm by 10µm individual pixel and spanning shift register circuits.

Implementation

The full 23x24 imager was designed iteratively with first the construction of the 1x1 APS, followed by the implementation of the 4x4 APS array with scanning technology, and finally the full 23x24 imager with its full complement of shift registers.

Further Optimization

To improve the fill factor, a redesign of the shift register arrays to occupy only 5µm x 10µm would allow for an extra column of APS thus resulting in a 24x24 imager. To reach a maximum fill factor, the individual nmos transistors within each APS's readout infrastructure should be resigned such that all three share as many components as possible. Essentially, they should go from three individual circuit elements to one hyper optimized component with the exact desired functionality.

Product

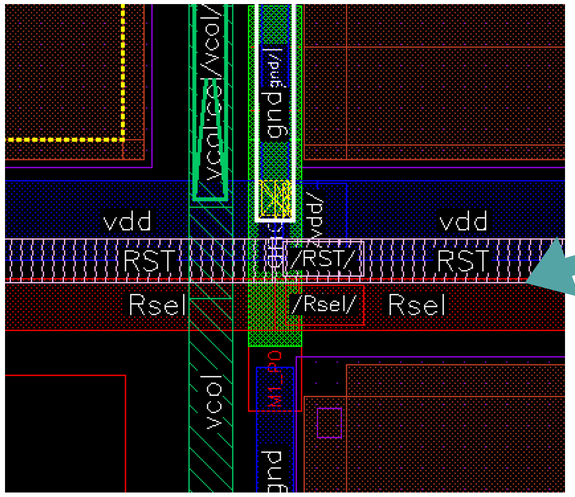

Figure 5a: 4 APS junction highlighting component modularity

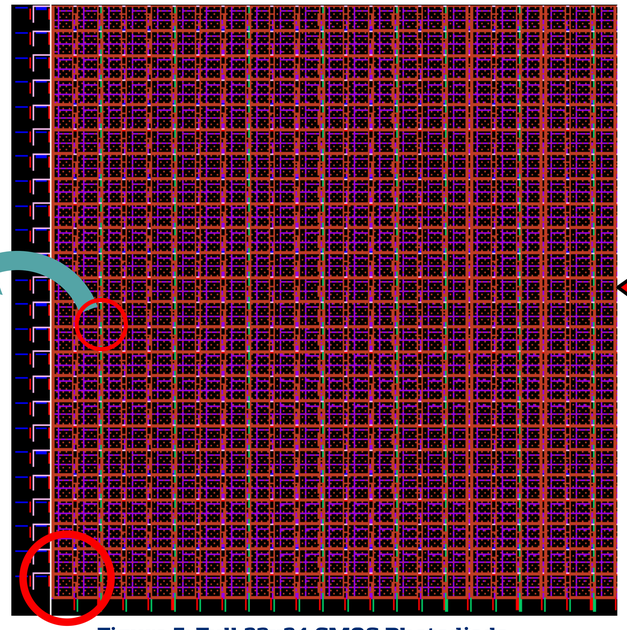

Figure 5: Full 23x24 CMOS Photodiode lattice complete with shift registers

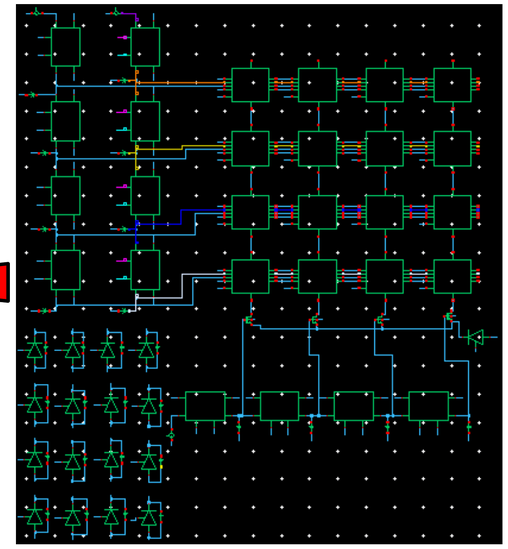

Figure 3: 4x4 3T APS Array Schematic

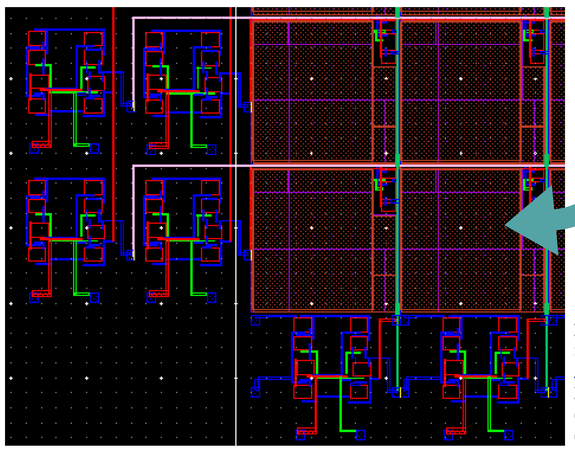

Figure 5b: Shift register APS junction highlighting component compatibility

Fill Factor: 74.75%

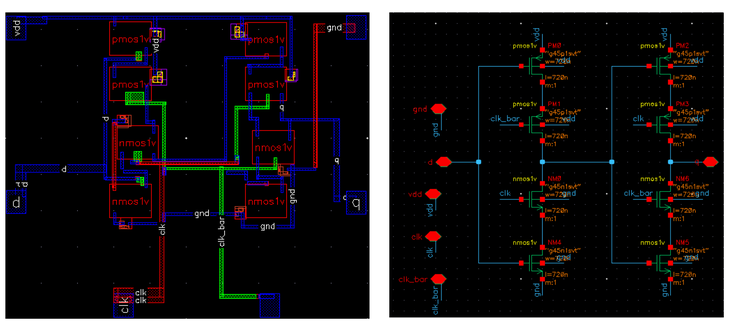

Figure 2: C2MOS D-Latch layout (left) and circuit (right)

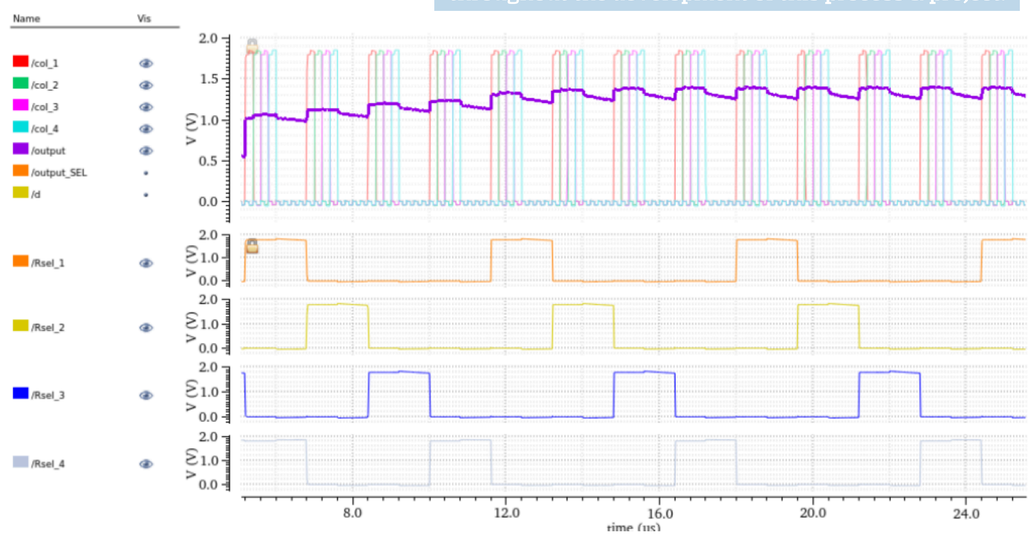

Figure 4: 4x4 APS array simulation with each APS reading a unique test photocurrent

References & Acknowledgements

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