

Design Project 2: Op-Amp Performance Report

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Abstract—Op-Amps are a fundamental building block of many analog and even some digital circuits. In this report we describe the design of a wide-bandwidth op-amp for a $500fF$ captive load in a $45nm$ process with a power supply of $\pm 750mV$. For proper operation it should us an $I_{ref} = 10\mu A$.

I. INTRODUCTION

An op-amp is a very general purpose type of voltage amplifier. They are characterized by having differential inputs, single ended outputs, with wide bandwidth and a very large open loop gain. Their most defining feature, however, is unity gain feedback stability. The ability to use feedback enables these devices to have easily adjustable voltage or transimpedance gain, or even perform non-linear signal processing. Here we describe the design of such a circuit with moderate gain and bandwidth to fill in the symbol in Fig 1. The specifications

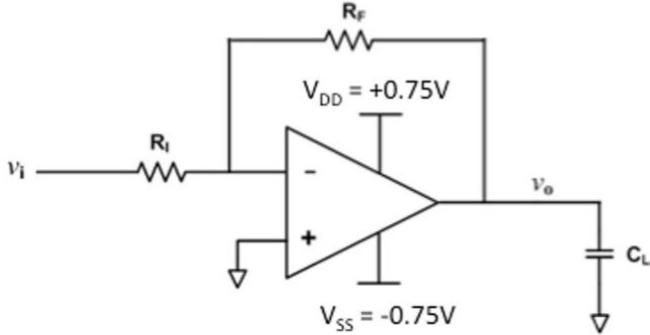


Fig. 1. Typical Op-Amp in an inverting configuration. R_i and R_f are $10K\Omega$ and C_L is $500fF$.

which we are trying to meet are: an open loop gain $> 600V/V$, the magnitude of input-referred offset voltage $< 1mV$, a unity loop gain frequency $> 100MHz$, with a phase margin $> 70^\circ$, an output swing $> 1V_{pkpk}$ centered at the common mode voltage, a slew rate $> 100V/\mu s$, power consumption $< 550\mu W$ and minimum area. These specs will be measured at $27^\circ C$ and three common mode voltages: $-100mV$, $0V$, and $100mV$. We will be using the $1V$ logic level devices in a $45nm$ process. This will require the design to also be mindful of the low breakdown voltage of the thin gate oxide of $1V$.

The rest of the report is as follows. Sections II-A though II-C describe the performance of the circuit based on simplified small signal analysis to provide an intuitive understanding of the circuit. Next in section, III, the nominal performance of the circuit is demonstrated. The simulation performance is also tested against device/process variation in section IV. To

better appreciate these findings we provide a brief discussion, V, before concluding in section VI. For more details we refer the reader to the appendix, that is section IX-B.

II. HAND ANALYSIS

The overall topology we used (neglecting biasing) is shown in Fig. 2. The signal carrying transistors are sized according

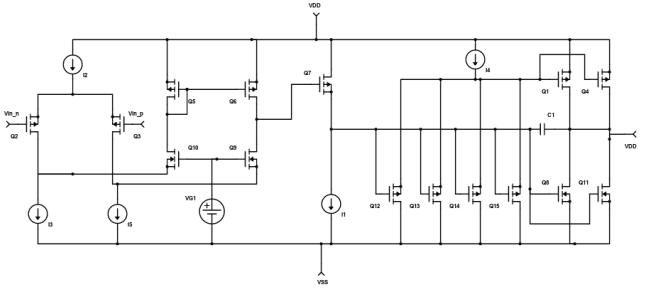


Fig. 2. Our Proposed Topology. Signal transistor sizes are included in Table I. Complete sizing information is included in Table IV

to Table I. The circuit has three distinct stages. It starts with

TABLE I
TABLE OF TRANSISTOR SIZES

Transistor	$W/L(\mu m)$
$Q_{2/3}$	$1/0.2$
$Q_{9/10}$	$0.4/0.15$
$Q_{5/6}$	$0.15/0.15$
Q_7	$0.12/0.12$
Q_{12-15}	$3/0.2$
$Q_{8/11}$	$4/0.1$
$Q_{1/4}$	$9/0.1$

a half-folded cascode input stage, followed by a common source gain stage and terminated by beefy push pull output stage. Each of these stages will be analyzed in detail in the coming subsections. All together we estimate that the circuit has the following nominal characteristics: a gain of $3.96KV/V$, a unity loop gain frequency of $718MHz$, a slew rate of $240V/\mu s$, a power consumption of $355\mu W$, an area of $271\mu m^2$. Unfortunately the input referred offset is large and the phase margin is nearly unstable. These shortcomings are further explained in the discussion, Sec. V.

A. Input Stage

The input stage starts with a canonical diff-pair, $Q_{2/3}$. We elected to use PMOS devices due to their lower threshold

voltages and lack of body effect which significantly improve input common mode range. We were further able to improve the headroom by folding the current mirror load $Q_{5/6}$. Unfortunately the folding process hindered the gain due to insufficient output resistance so we setup some common gate transistors $Q_{9/10}$ to buffer the output resistance.

We biased the diff-pair with $5\mu A$ of current which resulted in a $gm_{2/3} = 108\mu A/V$, $r_{o_{2/3}} = 315K\Omega$, $V_{OV_{5/6}} = 26.2mV$ and a $|V_{TH_{5/6}}| = 418mV$. The tail current source, I_2 has an output resistance $353K\Omega$ and a maximum voltage of $614.3mV$. $I_{3/5}$ have an output resistance of $249K\Omega$ and a $V_{min} = -569mV$ while pulling $20\mu A$ of current each. The current buffers, $Q_{9/10}$, have $gm_{9/10} = 129\mu A/V$, $r_{o_{9/10}} = 180K\Omega$ and $V_{GS_{9/10}} = 644mV$ (without body effect). This yields a input common mode range $-543mV$ to $170mV$ which exceeds spec and leaves plenty of room for the current buffers and their body effect. The current mirror load, $Q_{5/6}$ has a $gm_{5/6} = 60.4\mu A/V$, $r_{o_{5/6}} = 317K\Omega$, $V_{OV_{5/6}} = 358mV$, $|V_{TH_{5/6}}| = 422mV$. Checking the headroom, here we see that the output of the half folded cascode can swing from $-276mV$ to $-30mV$. Now we can finally say that the gain is $A_V \approx gm_{2/3} * \frac{r_{o_{2/3}} || R_{I_{3/5}}}{\frac{r_{o_{9/10}} + r_{o_{5/6}}}{1 + gm_{9/10} r_{o_{9/10}}} + r_{o_{2/3}} || R_{I_{3/5}}}$, a good start to meeting the gain spec.

Gain without bandwidth is quite useless in the context of an op-amp. Looking at the frequency response of the input stage next, we see that the input node has a pole at $p_{in} \approx \frac{1}{2\pi R_s C_{GS_{2/3}}} = 20GHz$. Where the miller effect is avoided due to the low input resistance of the current buffers. The next node in the signal path has a pole at $p_{reflect} \approx \frac{1}{2\pi 20.5K\Omega C_{GD_{2/3}}} = 40GHz$. The current buffers also introduce a pole, $p_{cb} \approx \frac{gm_{9/10}}{2\pi C_{GS_{9/10}}} = 30GHz$. Lastly, the current mirror load introduces yet another pole at $p_{mir} \approx \frac{gm_{9/10}}{4\pi C_{GS_{9/10}}} = 19GHz$. In other words, the input stage is designed to have no phase delay before the unity gain frequency of about $100MHz$. As there are no explicit capacitors in this stage and the sizes are comparable there is no need to worry about slew in this stage.

In summary the input stage has a common mode input range of -543 to $170mV$, a gain of $30V/V$ and a bandwidth in the gigahertz. To do this it uses an area of $1.43\mu m^2$ and $60\mu W$ of power.

B. Gain Stage

The gain stage is a simple common source stage with an active load formed by Q_7 and I_1 . To improve the slew rate we set I_1 to $30\mu A$. Furthermore, $gm_7 = 64.8\mu A/V$, $r_{o_7} = 238K\Omega$. The active load I_1 has an output resistance of $165.8K\Omega$. This translates to a gain of $6.33V/V$. The small size of the transistor improves its bandwidth considerably. Its input pole $p_{in} \approx \frac{1}{2\pi(C_{GS_7} + 7C_{GD_7})317K\Omega} = 1.45GHz$. The output pole will be set by the compensation capacitor and will be considered in the output stage analysis, next.

In summary the gain stage provides a gain of $6.33V/V$ and a bandwidth of $1.45GHz$. The input impedance is large and

the output resistance is $R_{OUT} = 165.8K\Omega$. To do so it uses $0.048\mu m^2$ and $45\mu W$ of power.

C. Output Stage

The output stage is based on the traditional push-pull topology. In order to meet the bandwidth/phase margin requirement lots of Gm is required here. To accomplish this we used parallel sets of large transistors. However to control the quiescent current, a voltage level shifter had to be inserted between the NMOS and PMOS gates. This was accomplished using a set of carefully sized source follower transistors as in [1]. One buffer voltage transistor was not sufficient due to the large capacitive load (formed by the $C_{GS_{1/4}}$ and the Miller multiplied $C_{GS_{1/4}}$), so there are four. On the bright side, this also lightens the slew rate requirement of the gain stage.

Specifically, the source followers are biased at $5\mu A$ each which translates to $gm_{12-15} = 115\mu A/V$, $r_{o_{12-15}} = 293K\Omega$, and a level shift of $426mV$. The output resistance is then, $2.17K\Omega$. The output resistance of I_4 is $176K\Omega$ keeping the gain of the stage reasonable at $927mV/V$.

Due to the level shifting, the output transistors are biased to a current of about $60\mu A$. Taking into consideration the source follower the PMOS and NMOS transistors function as one large transistor. Combined they have $Gm = 3.4mA/V$ and $R_{out} = 6.5K\Omega$ or $A_V = 22V/V$.

Due to the large Gm there are significant parasitic capacitances associated with this stage, in addition to the load capacitance. The pole due to the load capacitance is, $p_L \approx \frac{Gm}{C_L} = 1.1GHz$. The PMOS side has a pole at $p_{PMOS} \approx \frac{1}{2\pi(C_{GS_{1/4}} + 22C_{GD_{1/4}})2.17K\Omega} = 1.6GHz$. The NMOS side with the compensation capacitor forms the dominant pole. With $C_1 = 120fF$, the dominant pole ends up at about $363KHz$. This sets the cross over frequency well above the required $100MHz$ required bandwith around $718MHz$ and significantly reduces the phase margin. This choice was a compromise to meet as many specs as possible. See Sec. V for a much more detailed explanation.

Lastly with the large capacitances present is good to check the slew rate. The output transistors are biased (all together) at $120\mu A$ and drive a $500fF$ load which should then slew at $240V/\mu s$. The gain stage has to drive the compensation capacitor so it should slew at $250V/\mu s$.

In summary, the output stage has a gain $A_v = 22V/V$, bandwidth around $718MHz$ (due to the dominant single pole) and a slew rate of $240V/\mu s$. To do so it uses an area of $118\mu m^2$, and a power of $210\mu W$.

III. NOMINAL SIMULATION

To see how well the circuit performed we modeled it in cadence and simulated the results. Plots of its performance are included in IX-C. For brevity, the results of key metrics are tabulated in Table II. Note the following acronyms were used in Table II: CMV, Common Mode Voltage, ULGF unity loop gain frequency, SR slew rate, PWR power consumption. Also cadence ran into errors due to poor circuit performance

TABLE II
NOMINAL PERFORMANCE OF CIRCUIT

Temp. ($^{\circ}C$) CMV (V)	0			27			100		
	-0.1	0	0.1	-0.1	0	0.1	-0.1	0	0.1
$A_V \left(\frac{V}{V}\right)$	3.8k	3.7K	3.5K	2.3K	2.2K	2.1K	281	273	259
$V_{OS} (mV)$	-12	-13	-13	-15	-15	-16	-48	-49	-50
ULGF (MHz)	586	577	563	428	420	405	80	78	74
PM ($^{\circ}$)	-4.8	-3.7	-2.0	16	17	19	78	78	79
Swing+ (mV)	631	632	628	636	637	630m	677	670	635
Swing- (mV)	559	561	546	448	442	401	-91	-115	-220
SR+ ($\frac{V}{\mu s}$)	256	256	254	254	254	252	251	251	-
SR- ($\frac{V}{\mu s}$)	165	158	151	131	126	118	53	47.3	-
PWR (μW)	348	349	348	365	366	365	392	392	392
Area (μm^2)	271	271	271	271	271	271	271	271	271

at temperatures beyond the nominal $27^{\circ}C$ hence the empty entries.

Overall this design does not meet the desired specifications. As mentioned in the hand analysis section, there is a trade-off between slew rate, bandwidth, swing, and phase margin. The limited performance is analyzed in detail in the discussion, Sec. V.

IV. MONTE CARLO ANALYSIS

Despite the flaws present in the circuit, we proceeded with the Monte Carlo analysis to see how the circuit performs against process variation. Specifically we used 1000 samples for each corner, that is, each common mode voltage, $-100mV$, $0V$, $100mV$ at $27^{\circ}C$. By aggregating the net yield we were able to create Table III. Unsurprisingly, due to the phase margin, the overall yield was poor.

TABLE III
YIELD AND FOM

Temp. ($^{\circ}C$) CMV (V)	27		
	-0.1	0	0.1
Yield (%)	0	0	0
FOM	0	0	0

More detailed information detailing the distribution across all metrics at all common mode voltage corners at $27^{\circ}C$ is included in Sec. IX-E.

V. DISCUSSION

This project was ripe with challenges. Specifically we ran into two main issues. The first issue was the relationship between gain, bandwidth, phase margin, and slew. The second issue was the input referred offset voltage. Additionally, though not an official specification, the circuit is also significantly temperature sensitive.

1) *Dynamic Response Issues:* Unsurprisingly in analog design a variety of key metrics were linked. Specifically in our case the bandwidth, phase margin, slew and swing were difficult to meet with the same compensation capacitor.

These metrics are all linked for a few simple reasons. The first is that the output swing is measured at $60MHz$. To swing $1V_{pkpk}$ this requires a slew rate of $377V/\mu s$. As this is only at one point, it is possible to use less and still achieve

the specification. Indeed the output stage when simulated in isolation is able to produce the desired swing at this frequency (and a slew of $250V/\mu s$) without anywhere close to needing rail-to-rail input swing. This also exculpates the source followers in this particular implementation. On the other hand, the compensation capacitor also factors into the slew rate of the gain stage. As gain stage has a low output resistance ($166K\Omega$), a large compensation capacitor is required to improve the phase margin and reduce the bandwidth at the expense of slew (roughly $47V/\mu s$ instead of $240V/\mu s$).

This relationship is easy to observe by comparing Fig. 3 which uses a $640fF$ compensation capacitor to Fig. 9 which uses a $120fF$ capacitor. This makes sense as the bandwidth is reduced so the phase margin should improve as the response is always better at lower frequencies. Sadly, the output fails to swing adequately as the output stage's gain is heavily reduced at $60MHz$ and the gain stage struggles to swing that large of a capacitive load far enough. We tried to counteract this, by increasing the bias current of the gain stage. This change helped, but it was not sufficient to meet the specification.

All things considered, to fix the amplifier we would redesign the input and gain stages to have a larger bandwidth and a higher output resistance. One way to do this is to cascode the gain stage transistor, Q_7 . This breaks the miller effect allowing for a faster stage and increases the output resistance. A higher output resistance would reduce the required size of the compensation capacitor which lightens the slew rate requirement on the gain stage. By increasing the bandwidth of the input stage we will be able to move the dominant pole up a bit which eases the swing constraint as the output stage will have a higher gain.

2) *Systematic Input Referred Offset:* While the systematic input referred offset metric may appear to be independent of the others it is in fact quite tied together as well. In our circuit, the input referred offset comes from a combination of threshold and overdrive voltages (and hence its temperature response). The $|V_{GS}|$'s involved are that of the current mirror, $Q_{5/6}$, the gain stage Q_7 , and the output stage $Q_{1/4}$. Unfortunately changing the threshold or the overdrive significantly changes the device performance and that of the amplifier as a whole.

To meet this specification, the aforementioned transistors

	Parameter				C0	C1	C2	C3	C4	C5	C6	C7	C8		
	Iref				10u	10u									
	Vcm				-100m	0	100m	-100m	0	100m	-100m	0	100m		
	gdk045.scs				tt	tt									
	temperature				0	0	0	27	27	27	100	100	100		
Test	Output	Spec	Weight	Pass/Fail	Min	Max	C0	C1	C2	C3	C4	C5	C6	C7	C8
DP2:testbench:1	Av Open Loop	> 600		fail	259.2	3.802k	3.802k	3.701k	3.548k	2.257k	2.202k	2.112k	280.7	273.3	259.2
DP2:testbench:1	InputOffsetV	range -1m 1m		fail	-51.64m	-12.3m	-12.3m	-12.55m	-12.95m	-14.94m	-15.22m	-15.72m	-48.34m	-49.36m	-51.64m
DP2:testbench:1	UGF	> 100M		fail	14.2M	173.5M	173.5M	168.8M	161M	108.8M	106M	100.9M	15.38M	15.01M	14.2M
DP2:testbench:1	PM_v2	> 70		fail	49.45	87.86	49.45	50.48	52.03	64.25	64.88	65.91	87.55	87.65	87.86
DP2:testbench:1	PWR Closed Loop	< 550u		pass	347.9u	392.4u	347.9u	348.5u	348.1u	365u	365.7u	365.4u	392.1u	392.4u	391.7u
DP2:testbench:1	Vout3pkp_Pos_vcm	> 500m		fail	378.4m	596.5m	378.4m	381.2m	387.6m	441.7m	444.5m	451.7m	596.1m	596.5m	589.3m
DP2:testbench:1	Vout3pkp_Neg_vcm	< -500m		fail	68.94m	494.9m	68.94m	74.41m	86.01m	174.2m	180.1m	194.3m	464.6m	471.2m	494.9m
DP2:testbench:1	SR_Rising_pos2	> 100M		fail	48.42M	49.5M	49.28M	49.37M	49.5M	49M	49.08M	49.21M	48.42M	48.52M	eval err
DP2:testbench:1	SR_Rising_neg2	< -100M		fail	-31.18M	-24.27M	-31.18M	-30.45M	-28.75M	-25.08M	-24.27M	eval err	eval err	eval err	eval err
DP2:testbench:1	/vout3														
DP2:testbench:1	Vo_swingSignal														
DP2:testbench:1	Vo_slewSignal														
DP2:testbench:1	Phase_vout3														
DP2:testbench:1	/I20/VSS														
DP2:testbench:1	/I20/VD														
DP2:testbench:1	/I20/ref														
DP2:testbench:1	/I20/Vin_p														
DP2:testbench:1	/I20/Vin_n														
DP2:testbench:1	/vout1														
DP2:testbench:1	/vout2														

Fig. 3. Circuit performance with a large compensation capacitor of 640fF exemplifying the trade-off between bandwidth, swing, slew rate and phase margin when compared with Fig. 9 which uses a 120fF compensation capacitor

would have to be resized and re-biased carefully. Some techniques that may help are switching to a NMOS gain stage as this could move the quiescent voltage to a better point. Most importantly, however, the problem would be greatly simplified if the input stage had a higher gain. The higher the gain on the input, the less offset mismatches later down the line matter. It is also important to note that due to the current source biasing and matching, the input stage is quite resilient to changes in threshold voltage due to process variation/temperature.

3) *Temperature Sensitivity*: In the same way that this circuit has limited control over the input referred offset voltage due to a variety of threshold and overdrive voltages these create significant temperature response. This is most notable when comparing the metrics for 27°C and 100°C. Unfortunately the higher temperature reduces the gain of the device and shifts around the quiescent point. The testbench compensates to maintain the common mode voltage and then pushes one of the common-gate current buffers into triode (Q_9).

As with the improvements for the input referred offset voltage, a higher gain input stage would have a better response across temperature as the current source biasing tends to keep devices in saturation while the differential nature often cancels the changes in threshold.

VI. CONCLUSION

In conclusion, this amplifier is close to meeting spec. While there are many metrics that need fixed, they are almost all due to the interface between the input and the output stages. This low resistance and slightly slow bandwidth node created a variety of problems that impacted the bandwidth, phase margin, slew rate and output swing performance of the whole amplifier. We compromised phase margin for swing, slew and bandwidth by choosing a small compensation capacitor in order to meet as many specifications as possible.

By taking a closer look at the source of the problems of this design it is easy to see what a better design would be.

Specifically having a high speed and high gain input stage would improve performance in many ways. First it would reduce the effect of offset in later stages (like the output stage). More importantly it would allow the dominant pole to be moved to meet both the bandwidth and phase margin specs with less compensation capacitance. A lighter compensation capacitance in turn reduces the slew rate requirement on gain stage. Lastly, the gain stage may even be unnecessary which would simplify the circuit and make it easier to improve the delay-free bandwidth.

REFERENCES

- [1] S. A. Mahmoud and A. M. Soliman, "Current-feedback differential difference amplifier: new CMOS realization with rail to rail class-AB output stage," *Proceedings - IEEE International Symposium on Circuits and Systems*, vol. 2, 1999.

Design Project 2: Layout Report

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VII. LAYOUT CONSIDERATIONS AND TECHNIQUES

To complete any good analog design, one must complete a conscientious layout. The input and output stages have different sensitivities and hence we chose different mitigation techniques as explained next. The full layout screenshot is reproduced in Fig. 4 on the next page. Overall the layout is $38.52\mu m$ by $66.62\mu m$ yielding a total area consumption of $2566\mu m^2$.

A. Input Stage Layout

The layout of the input stage of a differential amplifier seeks primarily to mitigate any offset voltage that may occur as a result of variations within and between processes. Mitigation of random variations was largely undertaken in the design phase of this project, as has been chronicled elsewhere in this report. However, die-specific variations such as a linear variation can and ought to be taken into account in the layout. To this end, several mitigation techniques were employed. Firstly, the differential pair was placed at the center of the layout, ensuring that any linear gradient would be minimal. The transistor pair were placed close together to minimize variations across the die. Additionally, the differential pair offset voltage is sensitive to bias current. To ensure that the current biasing of the differential pair is stable, a common centroid strategy was utilized in placing all current mirrors. This strategy places similar devices at an equal distance from the die center, balancing process variations and improving current matching. As with all design decisions in analog design, these benefits came with some trade-offs. Placing the input devices near the center of the amplifier required the use of long traces to connect to input/output. This will cause some increased input resistance, and may have detrimental effects on the performance of a final, taped-out chip.

Some consideration was given to balancing parasitic capacitance and optimizing die usage. From a cost perspective, placing devices in a dense manner can decrease die usage and increase device yield per wafer. However, as our design is already very sensitive to second and higher-order poles, care was taken to avoid route crossing as would likely result from minimizing of die usage. This minimally interferes with circuit operation and allows for maximally nominal, minimally impeded circuit operation.

Next, the use of dummy devices was investigated. Placement of non-operational transistors in the common centroid layout paradigm has been shown to have an advantageous effect on the nominal operation of those adjacent elements. This effect

can be understood as ensuring that all transistors are biased in a matched fashion. Nearby circuit elements can impact transient, such as ground bounce, or steady state influence upon neighboring circuit elements. "Dummy" devices are electrically useless devices used to mimic the effect of a neighboring circuit. In this way, all active elements are placed in similar circuit conditions.

While the usage of dummy devices was investigated, final submission of this amplifier will not contain such devices. The placement of dummy devices impeded clean LVS operation. These authors attempted to mitigate this effect by placing analog dummy devices on the circuit schematic to no avail.

Finally, the use of guard rings was considered to protect critical circuit elements such as the input differential pair. Further circuit simulation and parasitic extraction may be performed to examine the necessity of this strategy.

B. Output Stage Layout

Similarly, this stage is sensitive to changes in threshold voltage. If the threshold moves too much the quiescent bias current can be quite large. Furthermore, changes in threshold can also affect the systematic offset. To control these effects while maintaining a good layout aspect ratio we chose to selected as to place the output transistors close together to maximize matching. We were also careful to when routing to minimize overlap.

C. Conclusion

Ultimately, a design to minimize device variation was selected. Space was maintained to minimize parasitic capacitance and allow for future addition of dummy devices. To ensure that all pins were near the periphery of the device, some long routing was required for input and output ports.

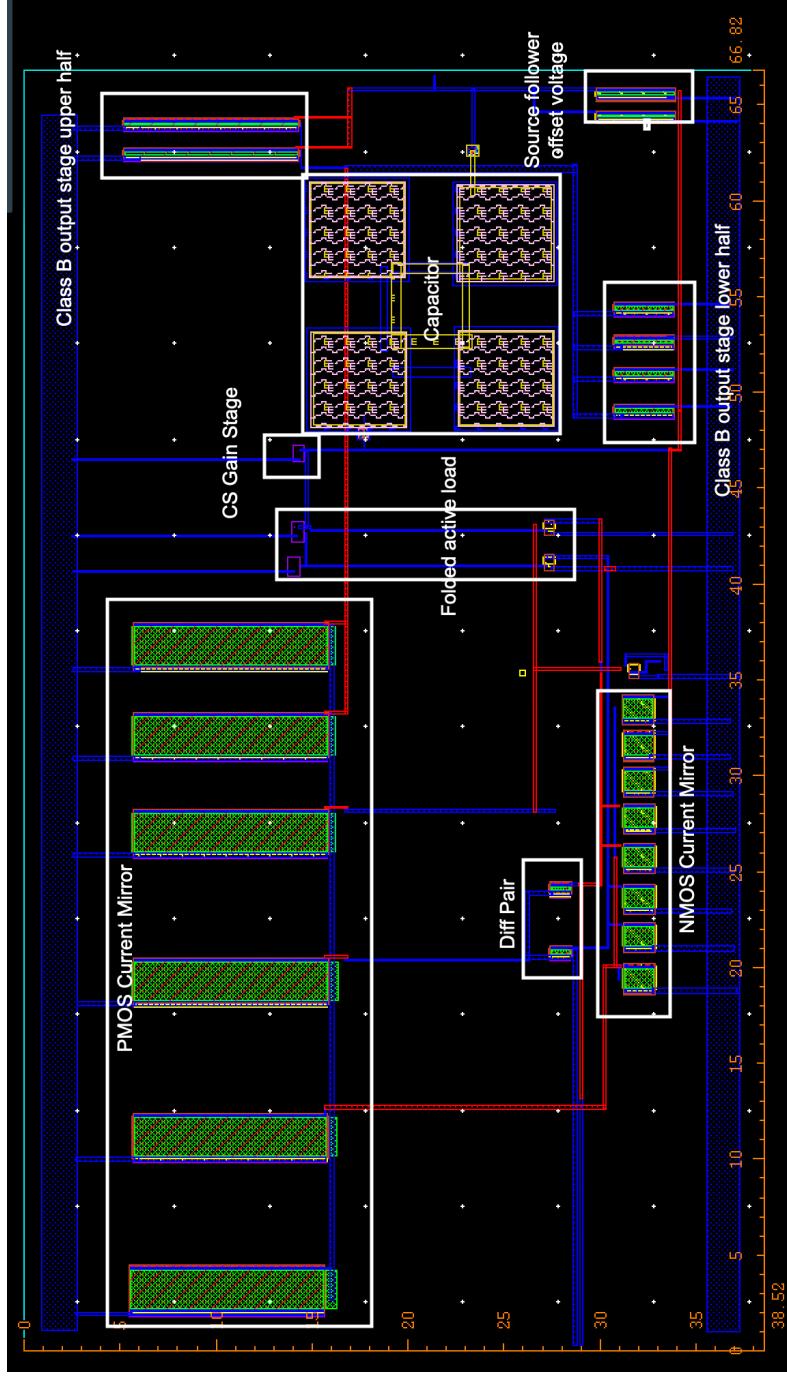


Fig. 4. Our Proposed Layout. The circuit is $38.52\mu m$ by $66.62\mu m$ yielding a total area consumption of $2566\mu m^2$.

VIII. LAYOUT ERROR CHECKING

We ran into a variety of errors while performing the layout. They were largely related to sizing varies sub-elemnts with sufficient size and spacing. Eventually, we finally achieved clean DRC and LVS as shown in Fig. 5 and 6 respectively.

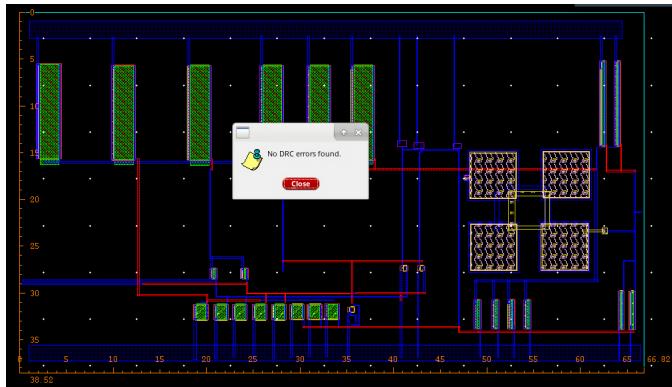


Fig. 5. Our Final Design Rule Check

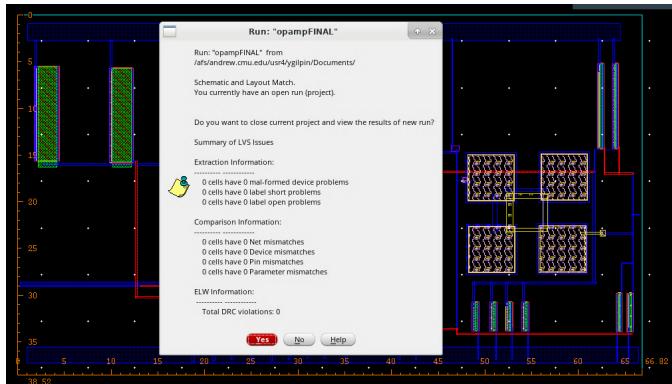


Fig. 6. Our Final Layout vs Schematic Check

IX. APPENDIX

To dig deeper into this circuit we included many more details here. Specifically the appendix starts with the complete circuit schematic in sec. IX-B, proceeds to all device sizes in sec. IX-A, observes the performance through a variety of nominal waveforms in sec. IX-C (including all necessary circuit conditions to replicate the behavior), and ends with the Monte Carlo histograms for all metrics and all corners at $27^\circ C$, sec. IX-E.

A. Device Sizes

Table IV, details the sizes and subtotal of estimated area consumption of all components used in our layout. Where the Mult. is the multiplier, which only applies to the compensation capacitor as it is formed out of four sub-elements. Note as all devices are included here, we opted for the naming convention to match the cadence schematic (Fig. 2).

TABLE IV
TABLE OF DEVICE SIZES

Element	$W(\mu m)$	$L(\mu m)$	Mult.	Area (μm^2)
$PM_{11/12}$	1	0.2	-	0.96
$NM_{12/13}$	0.4	0.15	-	0.344
$PM_{13/14}$	0.15	0.15	-	0.129
PM_{15}	0.12	0.12	-	0.048
PM_{3-6}	1.5	1	-	7.68
$PM_{0,2}$	9	0.1	-	3.04
$NM_{1,4}$	4	0.1	-	6.84
$PM_{8,9,15,16,17,19}$	10	2	-	136.8
$NM_{3,4,5,6,8,9,14,15}$	1.5	1	-	15.36
NM_{11}	0.4	0.15	-	0.172
NM_{10}	0.15	0.5	-	0.117
C_0	5	5	4	100

B. Circuit Schematic

The complete circuit schematic, Fig. 7, is nearly redundant compared to Fig. 2 except the biasing details have been included. These take the form of a few current steering transistors to spread the reference bias current of $10\mu A$ and generate the gate voltage for the common gate.

C. Nominal Simulation Plots: Fig. 10 - 15

To get a good sense of the amplifier as a whole, let's look some plots of its nominal response. To understand these plots it is helpful to first look at the equation/waveform setup in ADE XL as displayed in Fig. 8. The full output, including all corner conditions, of a "single point run" using the tt library is shown in Fig. 9. Now let's confirm these numbers by looking at the waveforms directly. The open loop magnitude response is shown in Fig. 10. Clearly the open loop gain is within spec across all corners at or below $27^\circ C$. Next, let's check unity loop gain frequency in Fig. 11. Recalling that the input has a magnitude of $100\mu V$ it is clear that the unity gain frequency is past $100MHz$ for temperatures $\leq 27^\circ C$. Having bandwidth is not particularly helpful if there is not sufficient phase margin. The phase responses are reproduced in Fig. 12. Once again we see that the amplifier is very stable with a phase margin $> 70^\circ$.

Thus far the analyses have all been linear, however amplifiers are inherently non-linear devices and have clipping and slew limits. To verify the output swing, see Fig. 13. Continuing the non-linear analysis, the rising slew response is shown in Fig. 14. With slew rate, it is important to check the falling slew as well. This is shown in Fig. 15. Overall the waves added additional detail, while confirming the quantified metric responses in Table II.

D. Monte Carlo Summary

In this section, one can find the summary of the Monte Carlo results, Fig. 16 which helps explain the low yield as the phase margin is never satisfactory.

E. Monte Carlo Histograms: Fig 17 - 43

Here we have included the histograms for all metrics across all common mode voltages at $27^\circ C$. They are organized by increasing common mode voltage. Within each corner the metrics are in the order of open loop gain, offset, ULGF, phase margin, swing high, swing low, rising slew rate, falling slew rate, and power consumption.

- 1) Corner 3: $27^\circ C$, $V_{CM} = -100mV$: Fig. 17 - 25
- 2) Corner 4: $27^\circ C$, $V_{CM} = 0V$: Fig. 26 - 34
- 3) Corner 5: $27^\circ C$, $V_{CM} = 100mV$: Fig. 35 - 43

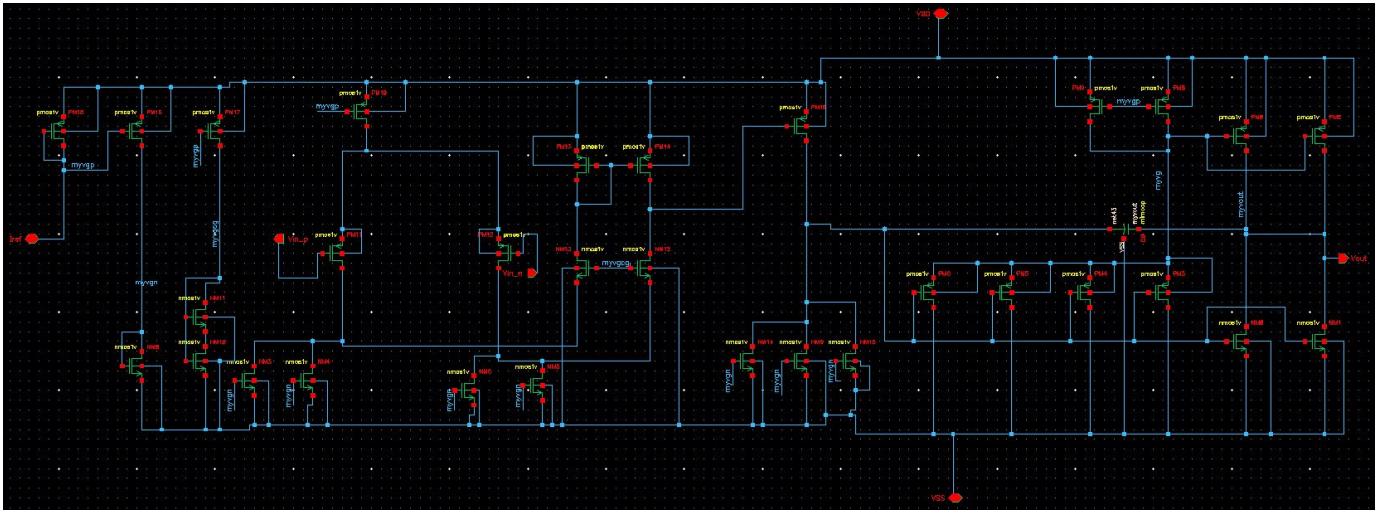


Fig. 7. A screen shot of our complete schematic in Cadence.

Test	Name	Type	Details	EvalType	Plot	Save	Spec
DP2:testbench:1	Av Open Loop	expr	mag(value(VF("/vout1") / (VF("/...))	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	> 600
DP2:testbench:1	InputOffsetV	expr	VDC("/offset")	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	range -1m 1m
DP2:testbench:1	UGF	expr	cross(mag((VF("/vout2") / VF("/n...))	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	> 100M
DP2:testbench:1	PM_v2	expr	(value(phaseDeg(VF("/vout2")) c...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	> 70
DP2:testbench:1	PWR Closed Loop	expr	((IDC("/I20/VSS") * VDC("/vss!")) +...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	< 550u
DP2:testbench:1	Vout3pkpk_Pos_vcm	expr	ymax(clip(VT("/vout3") 9.6e-06 ...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	> 500m
DP2:testbench:1	Vout3pkpk_Neg_vcm	expr	ymin(clip(VT("/vout3") 9.6e-06 1...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	< -500m
DP2:testbench:1	SR_Rising_pos2	expr	slewRate(clip(VT("/vout3") 1.98e...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	> 100M
DP2:testbench:1	SR_Rising_neg2	expr	slewRate(clip(VT("/vout3") 2.98e...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	< -100M
DP2:testbench:1	/vout3	signal	/vout3	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
DP2:testbench:1	Vo_swingSignal	expr	clip(VT("/vout3") 9.6e-06 1e-05)	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
DP2:testbench:1	Vo_slewSignal	expr	clip(VT("/vout3") 1.92e-06 3.09e...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
DP2:testbench:1	Phase_vout3	expr	phaseDeg(VF("/vout2"))	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
DP2:testbench:1	/I20/VSS	signal	/I20/VSS	point	<input type="checkbox"/>	<input checked="" type="checkbox"/>	
DP2:testbench:1	/I20/VDD	signal	/I20/VDD	point	<input type="checkbox"/>	<input checked="" type="checkbox"/>	
DP2:testbench:1	/I20/Iref	signal	/I20/Iref	point	<input type="checkbox"/>	<input checked="" type="checkbox"/>	
DP2:testbench:1	/I20/Vin_p	signal	/I20/Vin_p	point	<input type="checkbox"/>	<input checked="" type="checkbox"/>	
DP2:testbench:1	/I20/Vin_n	signal	/I20/Vin_n	point	<input type="checkbox"/>	<input checked="" type="checkbox"/>	
DP2:testbench:1	/I20/mydput	signal	/I20/mydput	point	<input type="checkbox"/>	<input type="checkbox"/>	
DP2:testbench:1	Half Gain	expr	mag(value((VF("/V_interface") / (...))	point	<input type="checkbox"/>	<input type="checkbox"/>	
DP2:testbench:1	/vout1	signal	/vout1	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
DP2:testbench:1	/vout2	signal	/vout2	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	

Fig. 8. ADE XL Equation Setup for metric quantification.

ADE XL Nominal Response Across All Corners															
	Parameter					C0	C1	C2	C3	C4	C5	C6	C7	C8	
DP2:testbench1	Iref					10u									
DP2:testbench1	Vcm					-100m	0	100m	-100m	0	100m	-100m	0	100m	
DP2:testbench1	gpdk045.scs					tt									
DP2:testbench1	temperature					0	0	0	27	27	27	100	100	100	
Test	Output	Spec	Weight	Pass/Fail	Min	Max	C0	C1	C2	C3	C4	C5	C6	C7	C8
DP2:testbench1	Av Open Loop	> 600		fail	259.2	3.802k	3.802k	3.701k	3.548k	2.257k	2.202k	2.112k	280.7	273.3	259.2
DP2:testbench1	InputOffsetV	range -1m 1m		fail	-51.64m	-12.3m	-12.3m	-12.55m	-12.95m	-14.94m	-15.22m	-15.72m	-48.34m	-49.36m	-51.64m
DP2:testbench1	UGF	> 100M		fail	74.2M	586M	577.3M	562.6M	428M	420.1M	405.4M	80.12M	78.11M	74.2M	
DP2:testbench1	PM_v2	> 70		fail	-4.817	78.87	-4.817	-3.671	-1.994	16.19	17.2	18.82	78.18	78.47	78.87
DP2:testbench1	PWR Closed Loop	< 550u		pass	347.9u	392.4u	347.9u	348.5u	348.1u	365u	365.7u	365.4u	392.1u	392.4u	391.7u
DP2:testbench1	Vout3pkp_Pos_vcm	> 500m		pass	627.6m	676.9m	631m	631.8m	627.6m	636.4m	636.6m	629.3m	676.9m	669.8m	634.9m
DP2:testbench1	Vout3pkp_Neg_vcm	< 500m		fail	-560.8m	219.8m	-558.9m	-560.8m	-546.4m	-447.6m	-441.6m	-400.8m	91.3m	114.9m	219.8m
DP2:testbench1	SR_Rising_pos2	> 100M		fail	250.7M	256.2M	256.2M	256.1M	253.7M	254.5M	254.2M	252.1M	251.3M	250.7M	eval err
DP2:testbench1	SR_Rising_neg2	< -100M		fail	-162.5M	-47.28M	-162.5M	-158.2M	-150.9M	-130.8M	-126.2M	-117.5M	-52.98M	-47.28M	eval err
DP2:testbench1	/vout3														
DP2:testbench1	Vo_swingSignal														
DP2:testbench1	Vo_slewSignal														
DP2:testbench1	Phase_vout3														
DP2:testbench1	/I20/SS														
DP2:testbench1	/I20/DD														
DP2:testbench1	/I20/Iref														
DP2:testbench1	/I20/in_p														
DP2:testbench1	/I20/in_n														
DP2:testbench1	/vout1														
DP2:testbench1	/vout2														

Fig. 9. Aggregate ADE XL nominal response across all corners. This information is also tabulated in Table II. This figure uses a 100fF compensation capacitor to meet as many specs as possible. The phase margin can be improved by increasing the compensation capacitor as in Fig. 3.

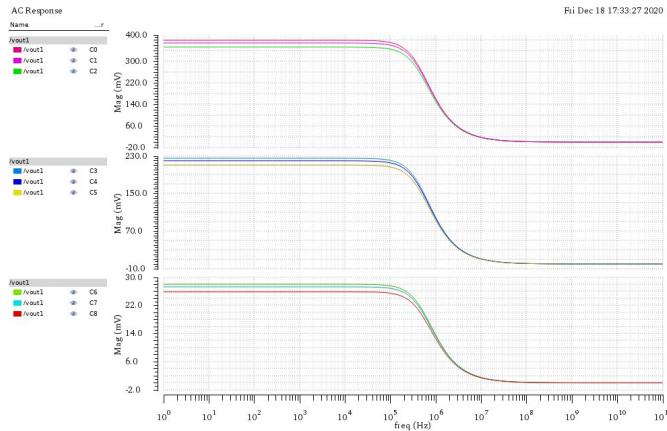


Fig. 10. Nominal open loop magnitude response split by temperature to a $100\mu V$ input.

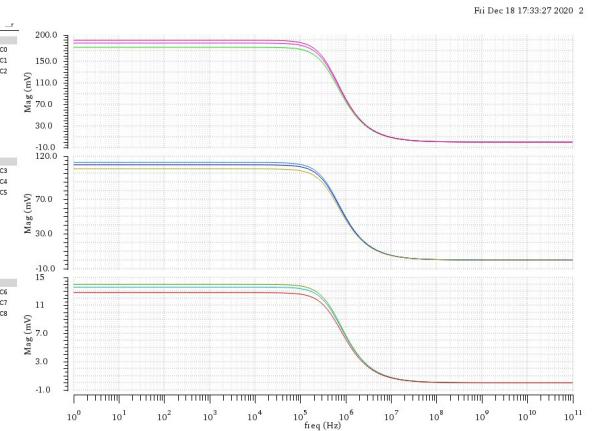


Fig. 11. Nominal loop gain magnitude responses split by temperature to a $100\mu V$ input.

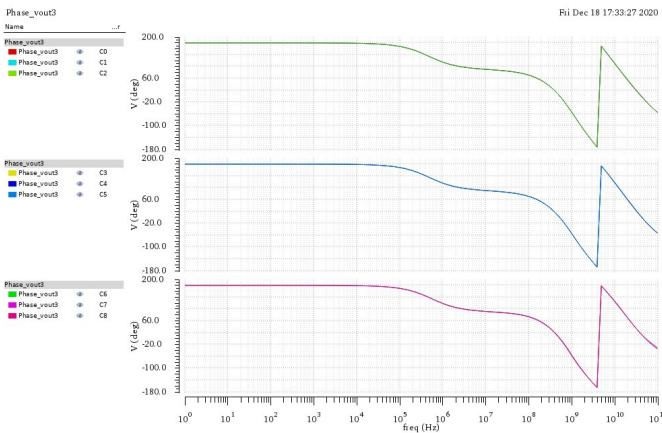


Fig. 12. Nominal loop gain phase responses split by temperature.

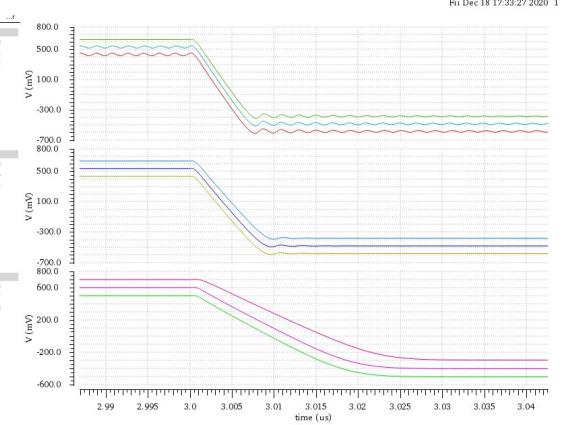


Fig. 15. Nominal falling slew response split by temperature.

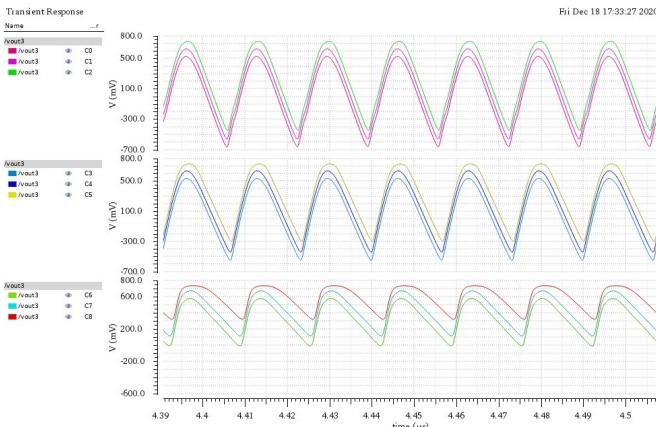


Fig. 13. Nominal transient responses at 60MHz with an input of 600mVpk split by temperature.

Test	Name	Yield	Min	Target	Max	Mean	Std Dev	Cpk	Errors
Yield Estimate: 0 % (0 passed/1000 pts) Confidence Level: <not set> Filter: <not set>									
-	DP2:bestbeh1								
-	Av Open Loop(summary)	64.9	444.9	3.05k	2.135k	578.2	0.841	349	
-	Av Open Loop_C3	74.6	489.6	> 600	3.95k	2.204k	603.8	0.886	253
-	Av Open Loop_C4	69	474.5	> 600	3.97k	2.145k	592.8	0.869	368
-	Av Open Loop_C5	68.2	444.9	> 600	3.749k	2.059k	578.2	0.841	316
-	InputOffsetV(summary)	1.7	-55.6m	19.22m	-15.5m	12.37m	-0.402	349	
-	InputOffsetV_C3	2.4	-52.6m	range -1m 1m	18.26m	-15.1m	11.6m	-0.402	253
-	InputOffsetV_C4	2.2	-53.7m	range -1m 1m	18.59m	-15.51m	12.06m	-0.401	368
-	InputOffsetV_C5	2	-55.6m	range -1m 1m	19.29m	-15.91m	12.37m	-0.402	316
-	UGf(summary)	65.1	178.6M	699.3M	407.4M	78.49M	1.26	349	
-	UGf_C3	74.7	193.3M	> 100M	699.3M	416.2M	79.49M	1.33	253
-	UGf_C4	69.2	180.6M	> 100M	601.9M	409.2M	79.46M	1.3	368
-	UGf_C5	68.4	178.6M	> 100M	588.8M	396.9M	78.49M	1.26	316
-	PWk (fz) (summary)	0	-4.399	> 70	54.02	18.54	10.77	-1.59	349
-	PWk_V2_C3	0	-4.399	> 70	54.02	18.54	10.77	-1.59	253
-	PWk_V2_C4	0	-3.351	> 70	54.88	19.54	10.83	-1.55	368
-	PWk_V2_C5	0	-1.913	> 70	56.3	21.14	10.77	-1.51	316
-	PWk Closest Loop (summary)	65.1	319.6M	419.8M	365.1M	15.74M	3.91	349	
-	Voutpink_Pos_vcm_summary	64.7	561.2M	711.3M	634.3M	24.01M	1.92	353	
-	Voutpink_Pos_vcm_C3	74.7	564.9M	> 500M	711.3M	638M	24.01M	1.92	253
-	Voutpink_Pos_vcm_C4	69	563.7M	> 500M	707.9M	638.8M	23.88M	1.94	310
-	Voutpink_Pos_vcm_C5	68.1	561.2M	> 500M	646.8M	626.1M	15.04M	2.79	319
-	Voutpink_Neg_vcm_summary	9.8	-607.8M	75.99M	-408.6M	150.2M	-0.339	353	
-	Voutpink_Neg_vcm_C3	17.6	-591.6M	< 500M	-114.2M	-430.9M	87.18M	-0.264	253
-	Voutpink_Neg_vcm_C4	16.2	-607.8M	< 500M	-92.9M	-423.4M	94.01M	-0.272	310
-	Voutpink_Neg_vcm_C5	10.6	-606.1M	< 500M	75.99M	-371.2M	126.2M	-0.339	319
-	SR_Rising_pos2(summary)	64	217.5M	303.5M	253.2M	13.05M	3.87	360	
-	SR_Rising_pos2_C3	74.7	218.6M	> 100M	303.5M	254.1M	12.93M	3.97	253
-	SR_Rising_pos2_C4	69	218.6M	> 100M	302.8M	254.1M	13M	3.95	310
-	SR_Rising_pos2_C5	67.3	217.5M	> 100M	300.6M	251.5M	13.05M	3.87	327
-	SR_Rising_neg2(summary)	51.3	-186.6M	-58.81M	-123.6M	19.73M	0.276	358	
-	SR_Rising_neg2_C3	70.3	-186.6M	< -100M	-76.51M	-129.5M	18.97M	0.519	253
-	SR_Rising_neg2_C4	62.7	-181.6M	< -100M	-72.08M	-125M	19.21M	0.433	310
-	SR_Rising_neg2_C5	54.1	-172.8M	< -100M	-58.81M	-116.3M	19.73M	0.276	324

Fig. 16. Summary of Monte Carlo simulation results. The low yield is explained in detail in Sec. V

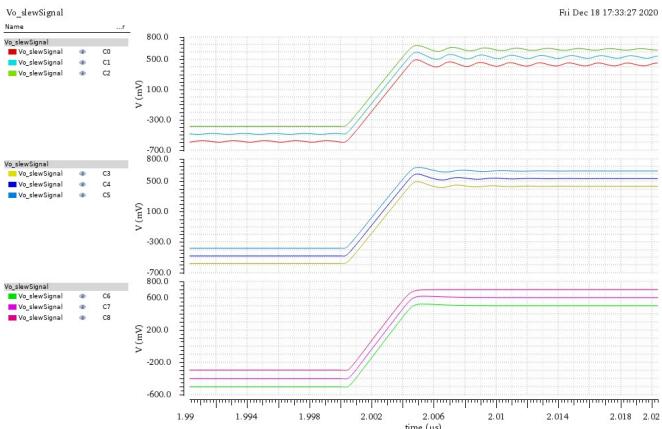


Fig. 14. Nominal rising slew response split by temperature.

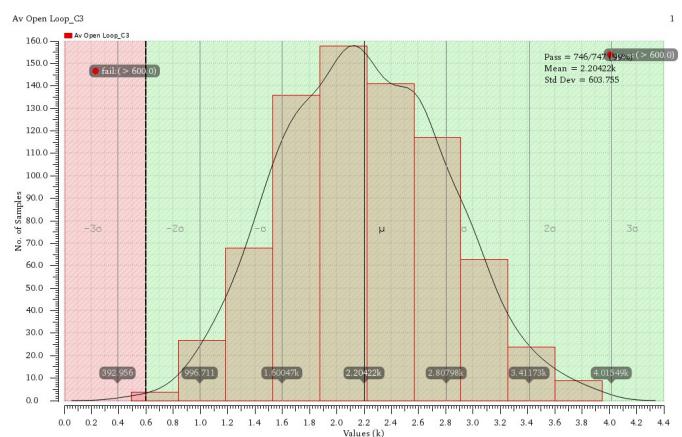


Fig. 17. Open loop gain histogram at 27°C and $V_{CM} = -100\text{mV}$.

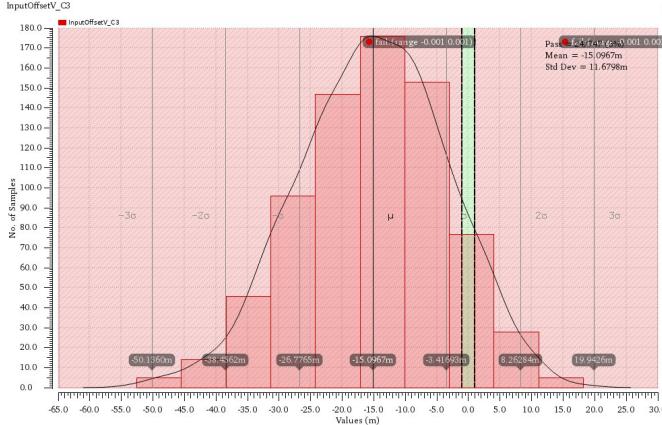


Fig. 18. Input offset (V) histogram at $27^\circ C$ and $V_{CM} = -100mV$.

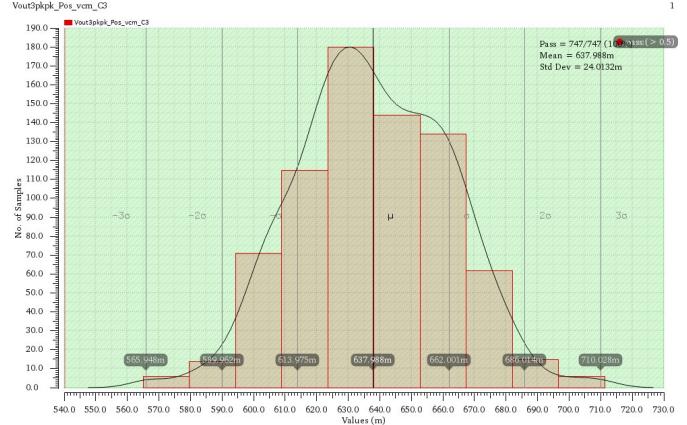


Fig. 21. Swing high (V) histogram at $27^\circ C$ and $V_{CM} = -100mV$.

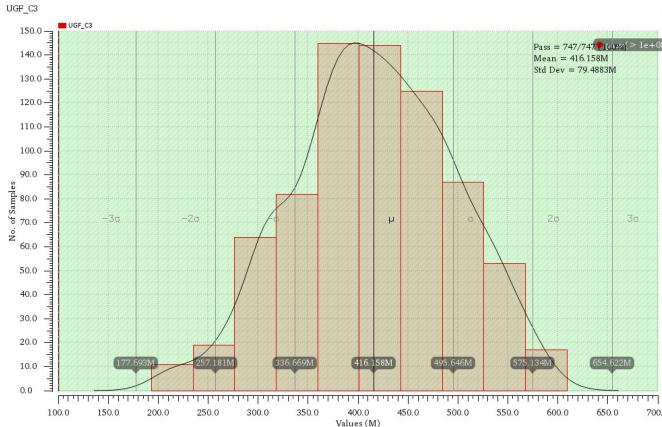


Fig. 19. ULGF histogram (Hz) at $27^\circ C$ and $V_{CM} = -100mV$.

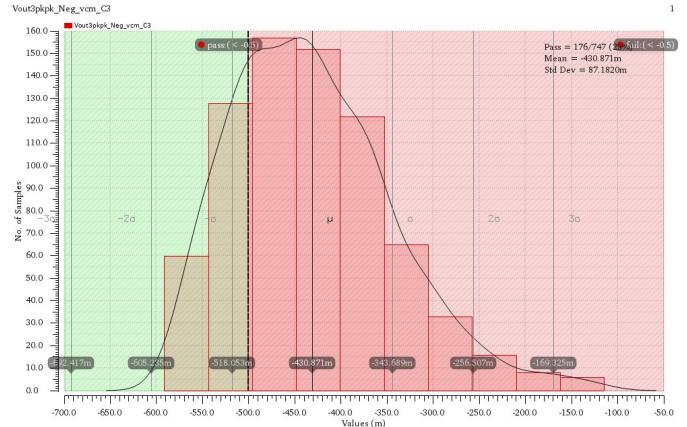


Fig. 22. Swing low (V) histogram at $27^\circ C$ and $V_{CM} = -100mV$.

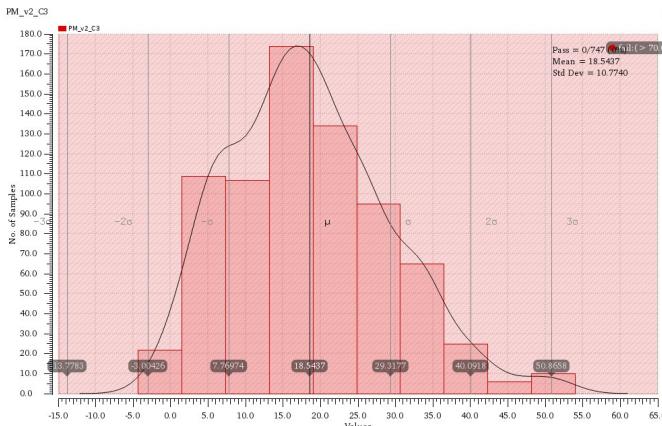


Fig. 20. Phase Margin (°) histogram at $27^\circ C$ and $V_{CM} = -100mV$.

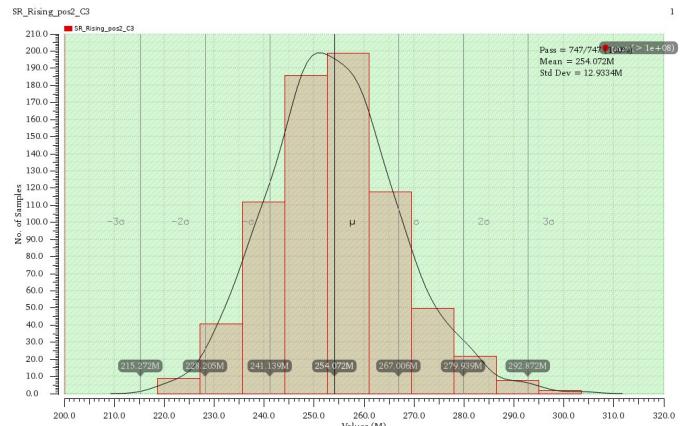


Fig. 23. Rising slew rate (V/s) histogram at $27^\circ C$ and $V_{CM} = -100mV$.

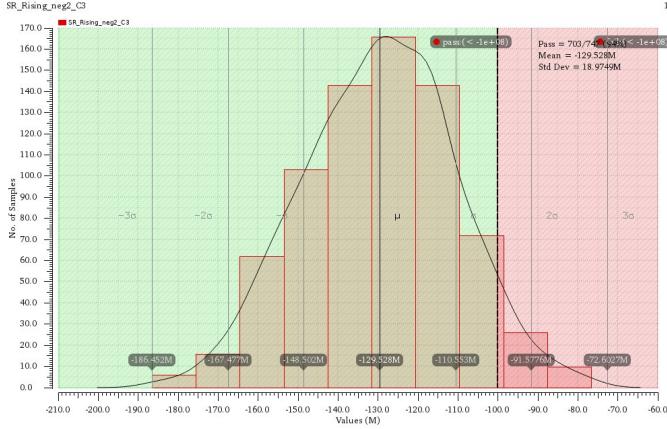


Fig. 24. Falling slew rate (V/s) histogram at $27^\circ C$ and $V_{CM} = -100mV$.

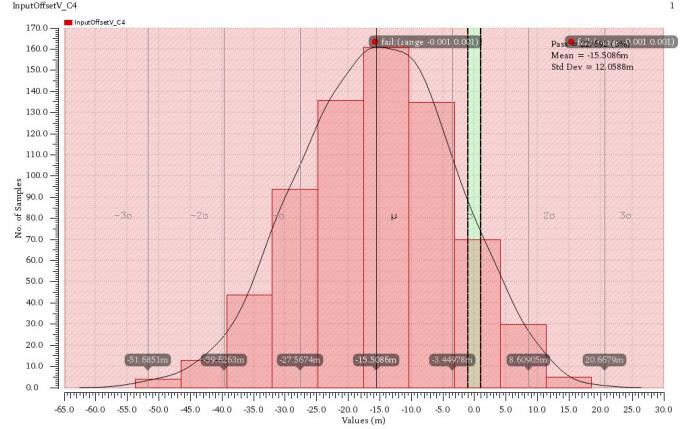


Fig. 27. Input offset (V) histogram at $27^\circ C$ and $V_{CM} = 0V$.

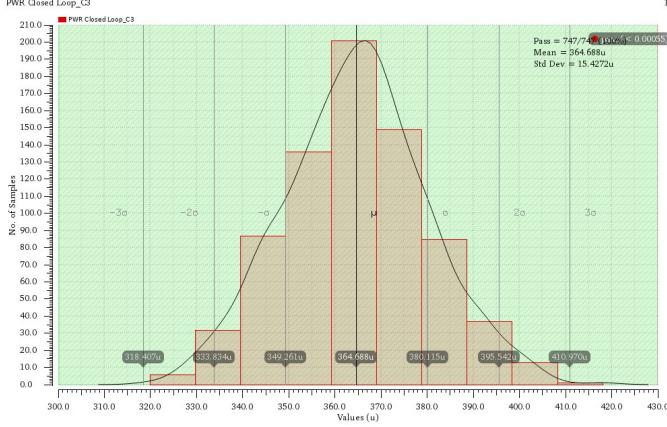


Fig. 25. Power consumption (W) histogram at $27^\circ C$ and $V_{CM} = -100mV$.

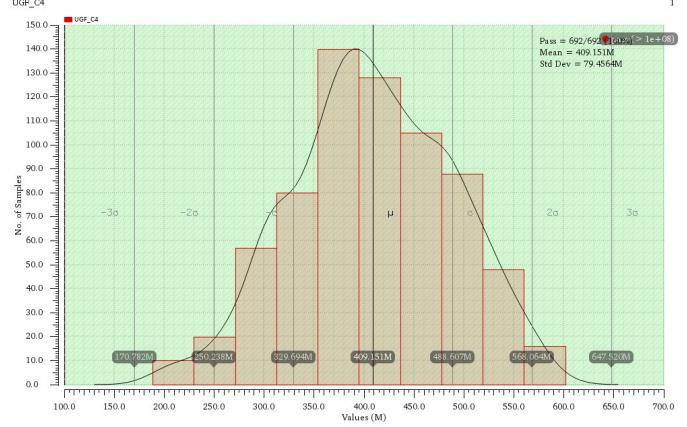


Fig. 28. ULGF histogram (Hz) at $27^\circ C$ and $V_{CM} = 0V$.

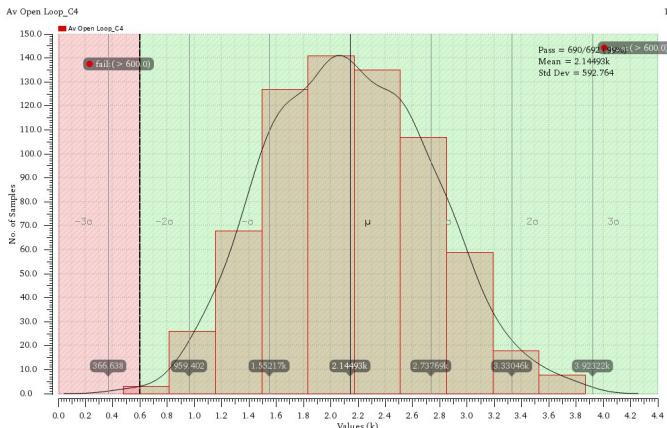


Fig. 26. Open loop gain histogram at $27^\circ C$ and $V_{CM} = 0V$.

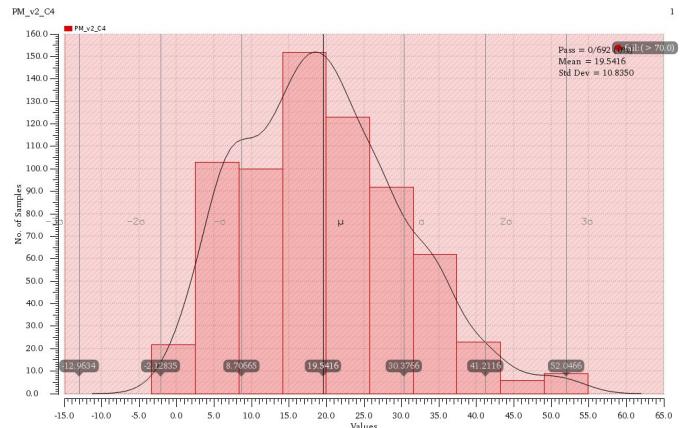


Fig. 29. Phase Margin (°) histogram at $27^\circ C$ and $V_{CM} = 0V$.

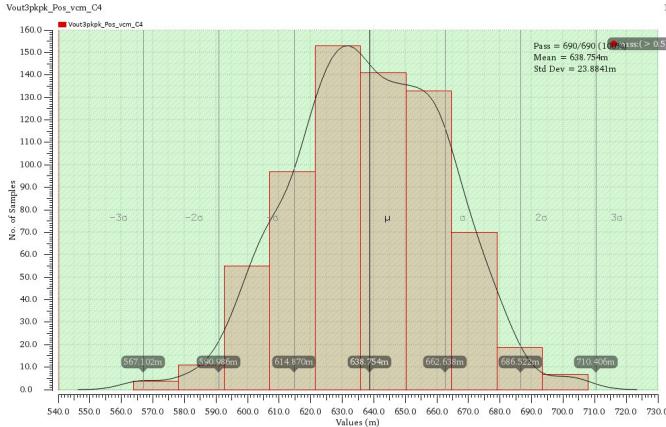


Fig. 30. Swing high (V) histogram at $27^\circ C$ and $V_{CM} = 0V$.

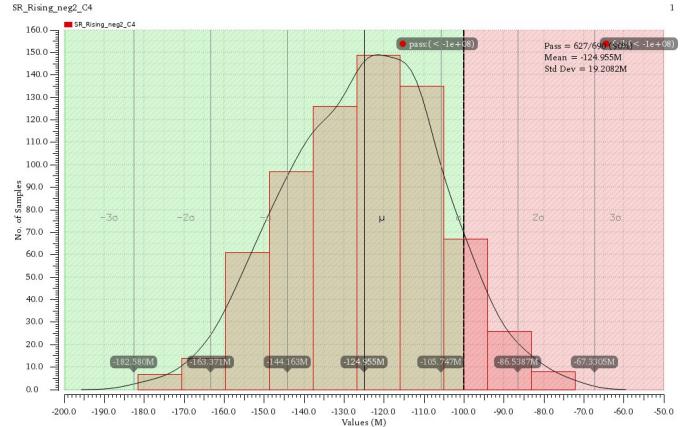


Fig. 33. Falling slew rate (V/s) histogram at $27^\circ C$ and $V_{CM} = 0V$.

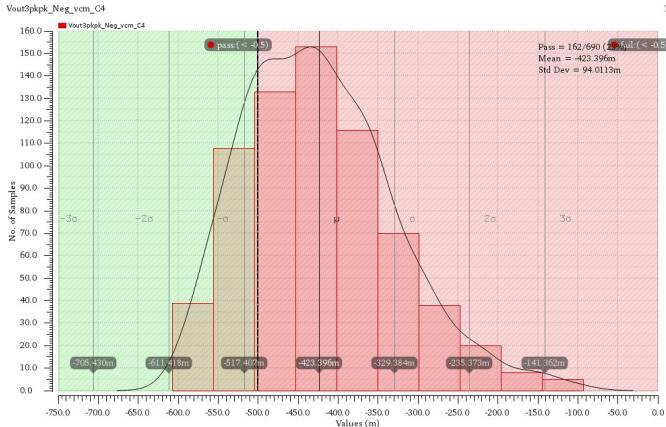


Fig. 31. Swing low (V) histogram at $27^\circ C$ and $V_{CM} = 0V$.

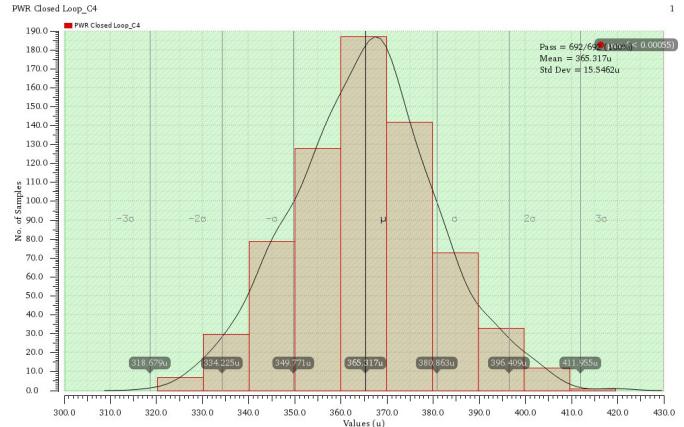


Fig. 34. Power consumption (W) histogram at $27^\circ C$ and $V_{CM} = 0V$.

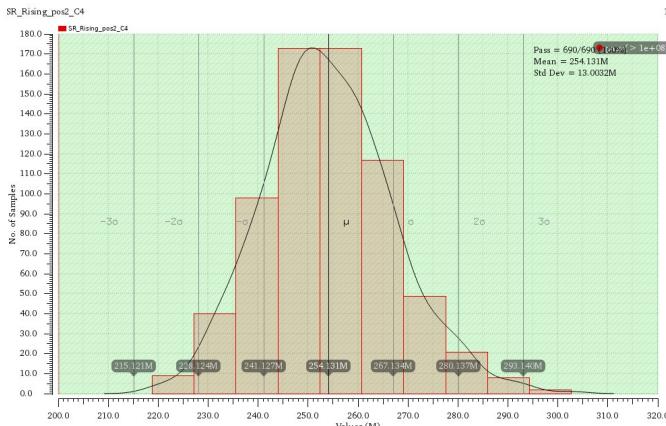


Fig. 32. Rising slew rate (V/s) histogram at $27^\circ C$ and $V_{CM} = 0V$.

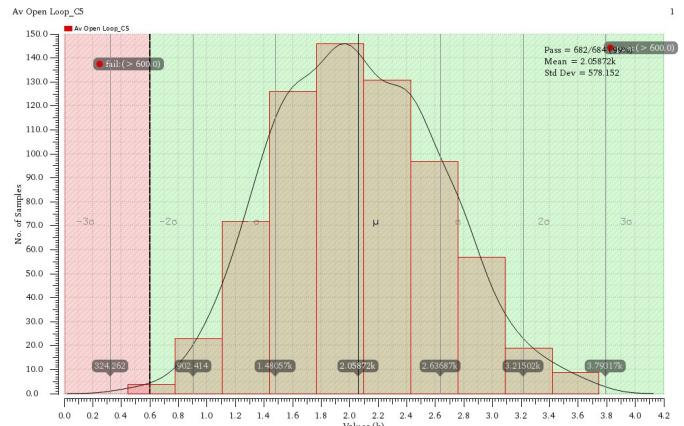


Fig. 35. Open loop gain histogram at $27^\circ C$ and $V_{CM} = 100mV$.

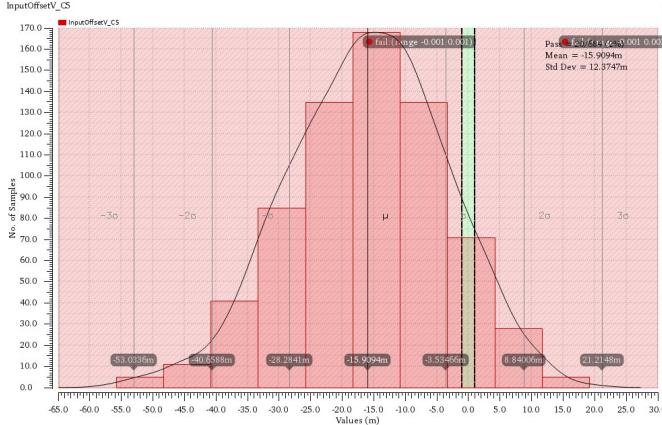


Fig. 36. Input offset (V) histogram at $27^\circ C$ and $V_{CM} = 100mV$.

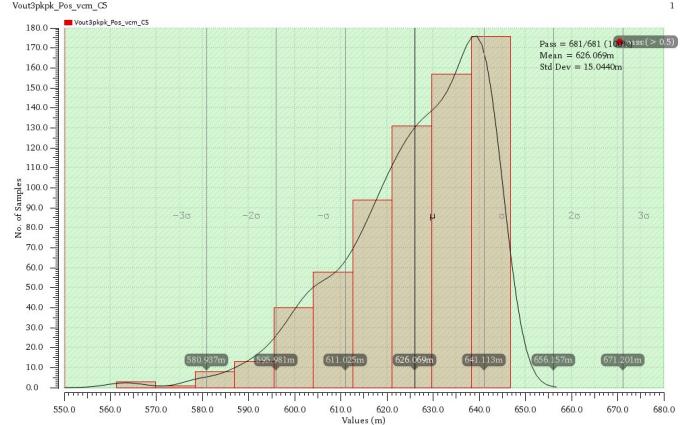


Fig. 39. Swing high (V) histogram at $27^\circ C$ and $V_{CM} = 100mV$.

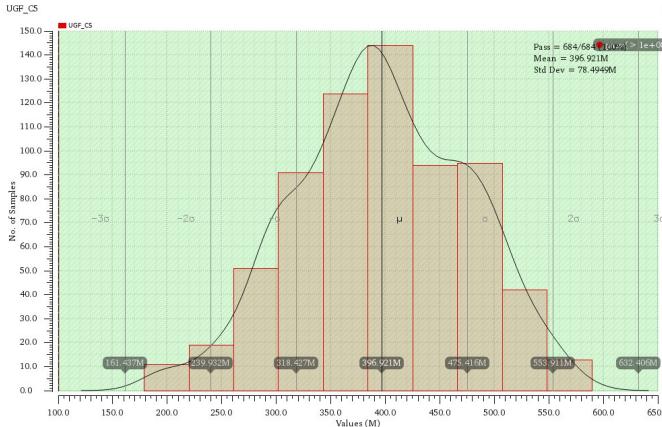


Fig. 37. ULGF histogram (Hz) at $27^\circ C$ and $V_{CM} = 100mV$.

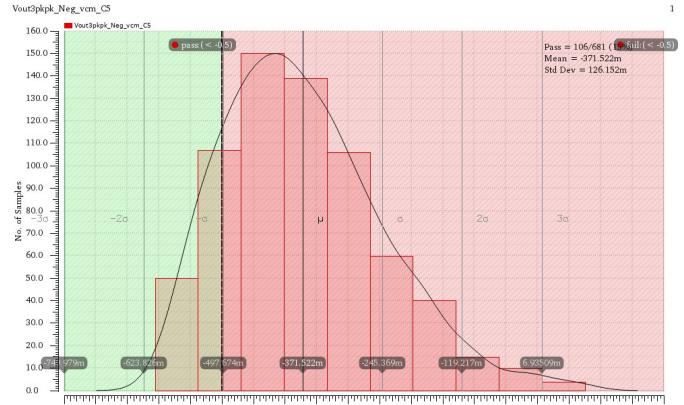


Fig. 40. Swing low (V) histogram at $27^\circ C$ and $V_{CM} = 100mV$.

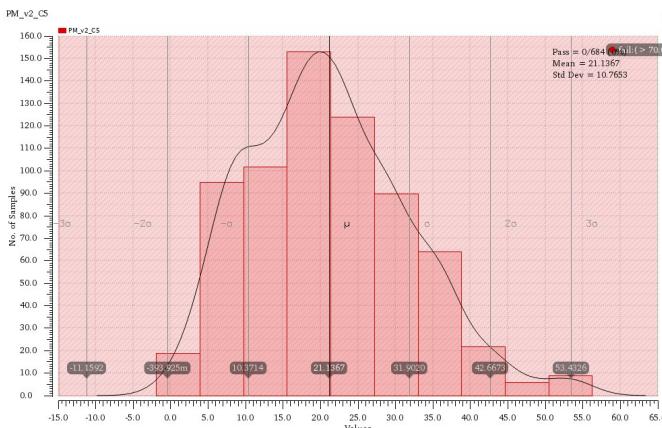


Fig. 38. Phase Margin (°) histogram at $27^\circ C$ and $V_{CM} = 100mV$.

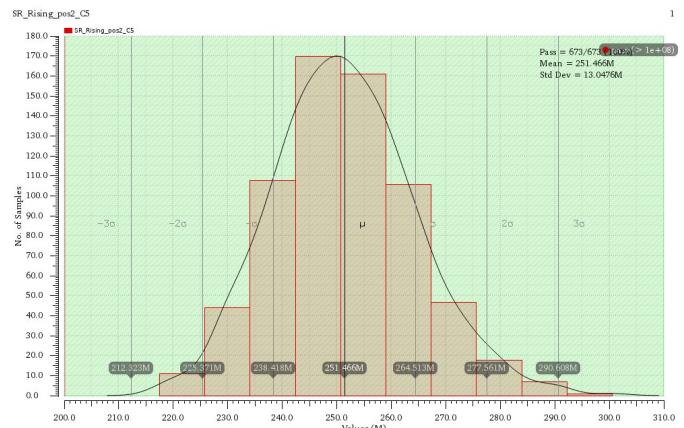


Fig. 41. Rising slew rate (V/s) histogram at $27^\circ C$ and $V_{CM} = 100mV$.

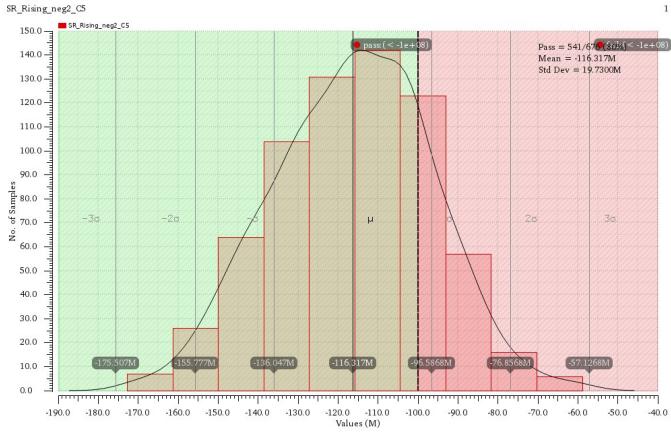


Fig. 42. Falling slew rate (V/s) histogram at $27^\circ C$ and $V_{CM} = 100mV$.

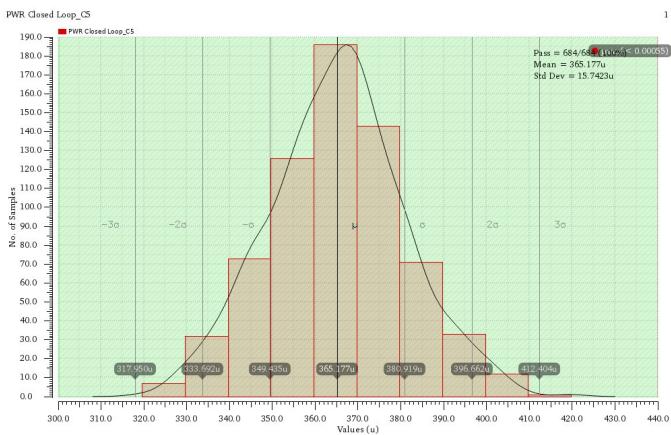


Fig. 43. Power consumption (W) histogram at $27^\circ C$ and $V_{CM} = 100mV$.