USER MANUAL

LRU Test System Reference Architecture 1.0

Discrete Acquisition Signal Path Excerpt

The (LRUTS) provides system integrators with information necessary to implement a signal path in their test system design by defining a standard, vendor-agnostic approach to designing hardware-in-the-loop (HIL) test systems for the validation of line replaceable units (LRUs).

Using the reference architecture, system integrators can easily:

- Design their test system using hardware and software components that have been electrically tested and validated by NI.
- Customize signal paths to ensure adequate coverage at the pin of the unit under test (UUT).
- Assemble test systems using standardized cabling and connections defined using signal banking.
- Integrate hardware into VeriStand.

Note LRUTS is an extensible architecture and using the designs in this document does not preclude you from using additional designs.

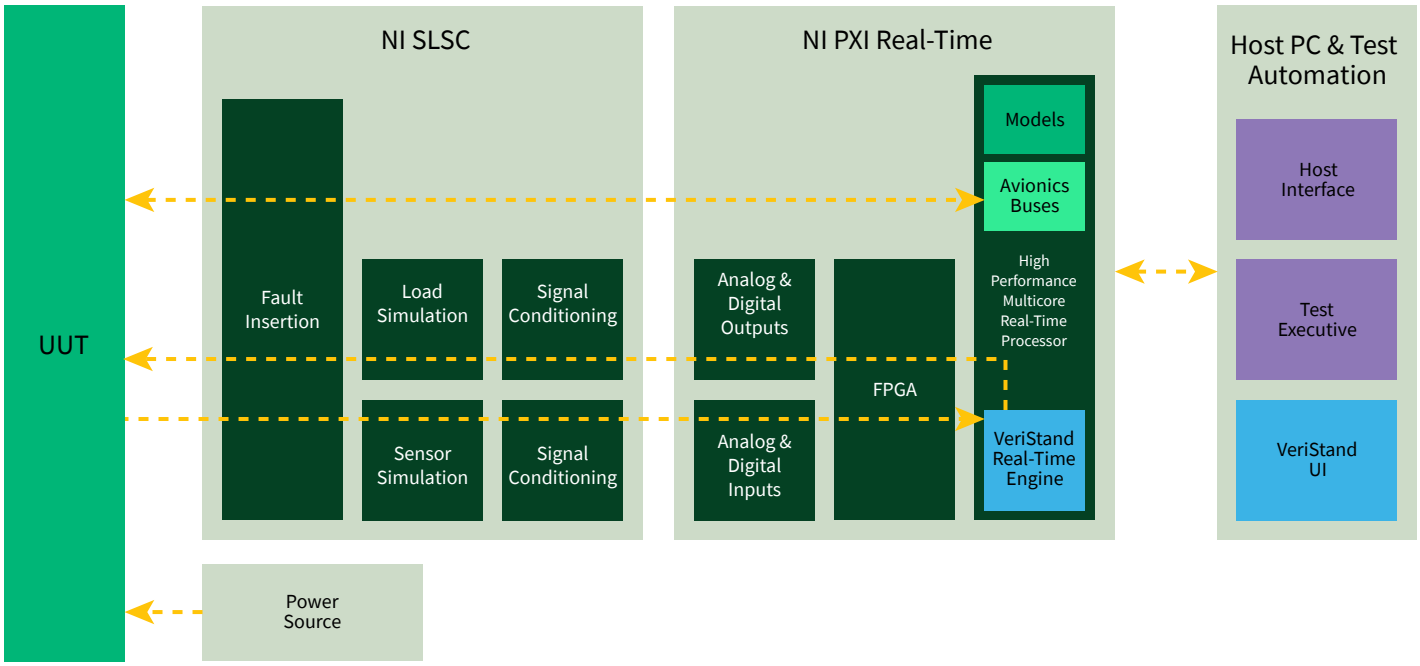
Contents

Hardware Overview

The reference architecture provides validated hardware configurations using off-the-shelf components from the NI Switch Load Signal Conditioning (SLSC) and PXI platforms.

The reference architecture defines a standard way to route signals and define connector pinouts, allowing you to reuse standard cabling and reduce the number of cable variants required to assemble your system.

Figure 1. Hardware Architecture



Validated Signal Paths

NI offers validated signal paths for common signal types within an LRU test system. Using these signal paths, you can take hardware configurations for standard signal types and modify them to meet the test coverage requirements of your UUT. The signal paths include

functionality for emulating sensors, actuators, loads, and electrical errors; connecting to real and simulated hardware; and taking lab measurements of real and simulated I/O.

Note The hardware configurations used in this reference architecture are intended for implementation in rack-based test systems; however, the reference architecture does not currently provide the mechanical layout of the test system.

Refer to the theory of operation section for each signal path for more information.

Software Overview

The core software for is VeriStand, which provides a deterministic, low-latency software framework for real-time control and monitoring of mechanical test cell applications.

Your implementation may also require additional application development environments, hardware driver software, and VeriStand custom devices.

Hardware Reference

Refer to this section for more information about the NI-supported signal paths, including hardware and software implementation details, key features, and specifications.

Note All specifications in this document are typical unless otherwise noted. *Typical* specifications describe the performance met by a majority of models.

Discrete Acquisition Signal Path Theory of Operation

The discrete acquisition signal path acquires signals from the UUT that toggle between two discrete states, such as those used to control lamps and actuators. These signals can be slow-toggling digital signals between two discrete states. The signal path can also acquire pulse width modulation (PWM) signals from the UUT, decode them, and pass the information encoded in the PWM to the hardware-in-the-loop test system. The discrete acquisition signal path can be configured to sample any of the following configurations for both discrete and high-speed PWM:

- **High/Open**—A single-ended signal that toggles between a power bus (High) and open state.
- **GND/Open**—A single-ended signal that toggles between a GND and open state.
- **High/GND**—A single-ended signal that toggles between a power bus (High) and GND state.

Note The discrete acquisition signal path supports power bus voltages between 0 V and 33 V.

Features

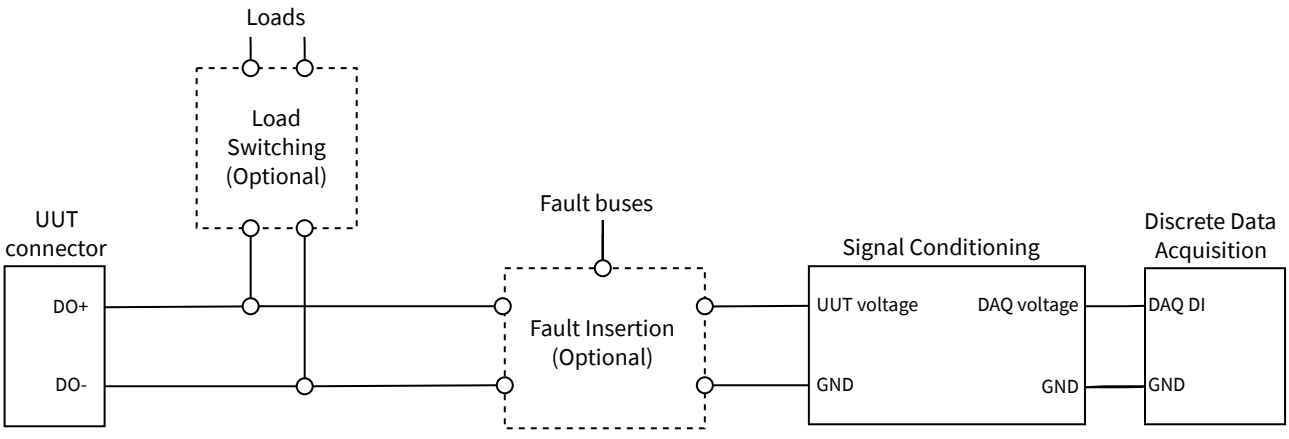
The discrete acquisition signal path supports the following features:

- Discrete signal sampling
- FPGA for additional processing needs
- Load switching
- Electrical error simulation

Modular Signal Path Components

The following figure shows the high-level modular components required to implement the discrete acquisition signal path.

Figure 2. Discrete Acquisition Signal Path Components



Refer to the following sections for more information about the reusable, modular components shown in the previous diagram:

- *Discrete Data Acquisition*
- *Signal Conditioning*

- *(Optional) Load Switching*
- *(Optional) Fault Insertion*

Discrete Acquisition Signal Path Implementation

One implementation of the discrete acquisition signal path uses the PXIe-7820, PXIe-7821, or PXIe-7822 as the discrete acquisition component.

Refer to the following sections for specifications, hardware requirements, and implementation details.

Specifications

Refer to the following specifications for key characteristics of the discrete acquisition signal path.

Note The following specifications apply to a single implementation of the discrete acquisition signal path. Making any customizations to the signal path may change these specifications.

Number of banks	8 per PXIe-782x DIO connector
Number of signals per bank	4
Signal type	Differential
Voltage range	0 V to 5 V 0 V to 33 V
Input configurations	Sourcing Sinking
Sourcing pull-up resistor	24 kΩ
Maximum signal frequency	100 kHz
SLSC-12201 Specifications (5 V range)	
Hysteresis	0.7 V
Input threshold setting range	0.74 V to 4.2 V
Input threshold setting resolution	4.4 mV
Input impedance (sinking input)	200 kΩ
SLSC-12201 Specifications (33 V range)	
Hysteresis	3.7 V
Input threshold setting range	4 V to 27.5 V
Input threshold setting resolution	23.3 mV
Input impedance (sinking input)	110.4 kΩ

Recommended Hardware

The following hardware components are recommended to configure this signal path. You can purchase these components from NI.

Table 1. Discrete Acquisition Signal Path Recommended Hardware

Hardware Component	Description
PXIe-1085 or PXIe-1095	PXI Chassis
PXIe-8880, PXIe-8861, or PXIe-8881	PXI Controller
SLSC-12001	Chassis for SLSC
PXIe-7820, PXIe-7821, or PXIe-7822	PXI Digital Reconfigurable I/O Module
RTI-12309	Rear Transition Interface
SLSC-12201	Digital I/O Module for SLSC
SET-2010	Routing Module for SLSC
SET-2310	Routing Module Mezzanine Board for SLSC
SH68M-4IXBF DIO DIFF	
SHDB44M-4IXBF DIFF	

Component Installation

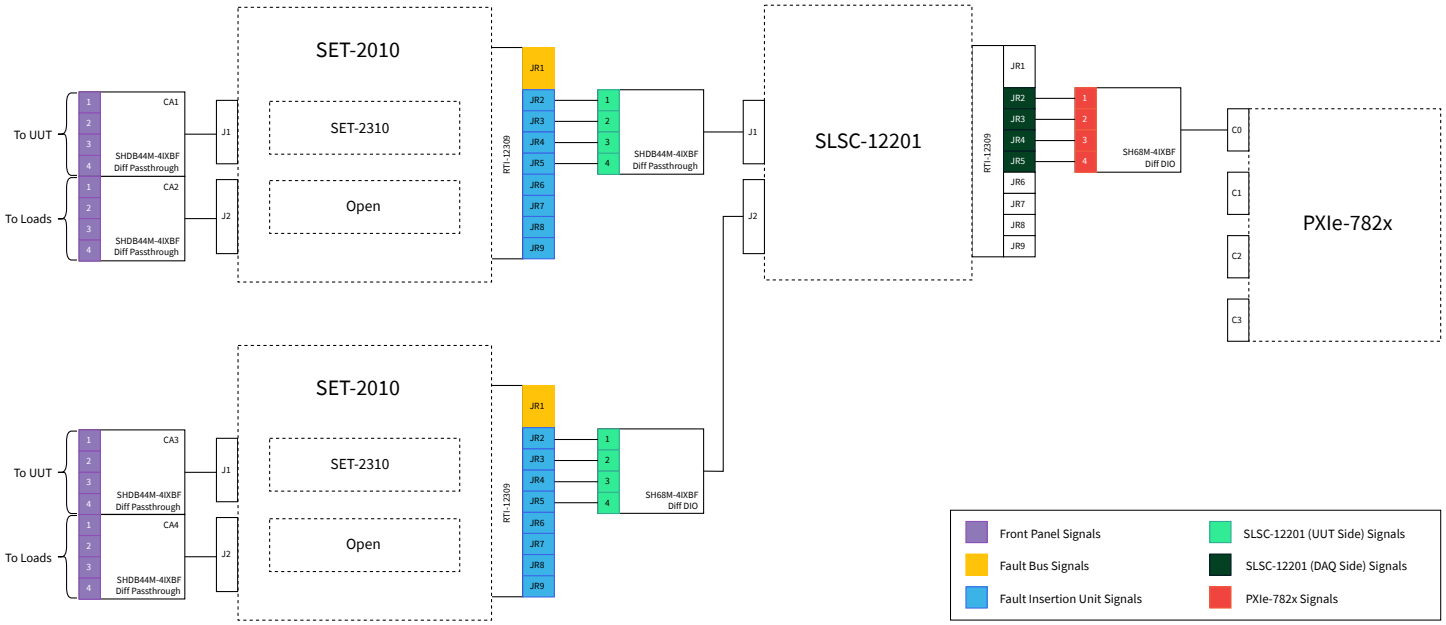
For detailed instructions on installing each component into a chassis, refer to the documentation for each component. Refer to *GUID-4A0F02EF-9CEA-4CC4-93AE-2A5EDC973005* for a list of relevant component documentation.

Banking Reference

The standard NI cables recommended in the allow you to organize the signals into banks for easy testing and customization of the signal path.

The following figure shows an example of a discrete acquisition signal path implementation, which includes support for 8 banks of discrete acquisition signals, fault insertion, and load switching. This implementation can be scaled up or down based on your needs.

Figure 3. Connection Diagram



Discrete Acquisition Pinout Summary

The following table shows an example of how one bank of signals is defined in each hardware interface.

Note The SLSC-12201 converts signals from single-ended to differential, which changes the way the signals are banked.

Table 2. Bank Mapping Example

Bank Element (Differential)	ix Industrial Connector Pin	User-Facing Banks	Internal Banks				Bank Element (Single-Ended)
		Front Panel Signal (Differential)	Fault Insertion Signal (Differential)	SLSC-12201 (UUT Side) Signal (Differential)	SLSC-12201 (DAQ Side) Signal (Single-Ended)	PXIe-782x Signal (Single-Ended)	
A (IO)	1	DI0+	P0.0+	P0.0	DI0	DI0	A (IO)
B (IO)	2	DI0-	P0.0-	GND			
C (IO)	4	DI1+	P0.1+	P0.1	DI1	DI1	B (IO)
D (IO)	5	DI1-	P0.1-	GND			
E (IO)	6	DI2+	P0.2+	P0.2	DI2	DI2	C (IO)
F (IO)	7	DI2-	P0.2-	GND			
G (IO)	9	DI3+	P0.3+	P0.3	DI3	DI3	D (IO)
H (IO)	10	DI3-	P0.3-	GND			
I (REF)	3	REF	GND	GND	GND	GND	I (REF)
J (AUX)	8	AUX	AUX	AUX	GND	GND	J (AUX)
A (IO)	1	DI4+	P0.4+	P0.4	DI4	DI4	E (IO)
B (IO)	2	DI4-	P0.4-	GND			
C (IO)	4	DI5+	P0.5+	P0.5	DI5	DI5	F (IO)
D (IO)	5	DI5-	P0.5-	GND			

Table 2. Bank Mapping Example (Continued)

Bank Element (Differential)	ix Industrial Connector Pin	User-Facing Banks	Internal Banks				Bank Element (Single-Ended)
		Front Panel Signal (Differential)	Fault Insertion Signal (Differential)	SLSC-12201 (UUT Side) Signal (Differential)	SLSC-12201 (DAQ Side) Signal (Single-Ended)	PXIe-782x Signal (Single-Ended)	
E (IO)	6	DI6+	P0.6+	P0.6	DI6	DI6	G (IO)
F (IO)	7	DI6-	P0.6-	GND			
G (IO)	9	DI7+	P0.7+	P0.7	DI7	DI7	H (IO)
H (IO)	10	DI7-	P0.7-	GND			
I (REF)	3	REF	GND	GND	GND	GND	I (REF)
J (AUX)	8	AUX	AUX	AUX	GND	GND	J (AUX)

You can also provide reference voltages for the SLSC-12201 and fault insertion signals for the SET-2010 via the RTI-12309 connected to each module. The following table shows the pinouts for those connectors.

Table 3. Faulting and Reference Voltage Connectors

RTI-12309 JR1 Pin	SET-2010 Fault Mapping	SLSC-12201 Supply Mapping
JR1.6	FAULT_A	NC
JR1.2	FAULT_B	NC
JR1.5	FAULT_C	NC
JR1.1	FAULT_D	NC
JR1.8	NC	SUPPLY0
JR1.4	NC	GND
JR1.7	NC	SUPPLY1
JR1.3	NC	GND

End User-Accessible Signal Pinouts

After the hardware is configured, the user will be able to access signals from the front panel to connect the UUT, loads, and power supplies. The following table shows the signals accessible from each connector.

Note Each connector and bank in the following table corresponds to a label in the previous wiring diagram. For example, CA1.2 corresponds to bank 2 on CA1.

Table 4. End User-Accessible Signals

Signal Type	Connector	Signals
To UUT	CA1.1	DI0:3
	CA1.2	DI4:7
	CA1.3	DI8:11
	CA1.4	DI12:15
	CA3.1	DI16:19
	CA3.2	DI20:23
	CA3.3	DI24:27
	CA3.4	DI28:31

Table 4. End User-Accessible Signals (Continued)

Signal Type	Connector	Signals
To Loads	CA2.1	LOAD0:3
	CA2.2	LOAD4:7
	CA2.3	LOAD8:11
	CA2.4	LOAD12:15
	CA4.1	LOAD16:19
	CA4.2	LOAD20:23
	CA4.3	LOAD24:27
	CA4.4	LOAD28:31
Fault Bus Signals	SET-2010: JR1	FAULT A:D
SLSC Power Supply	SLSC-12201: JR1	SUPPLY0:1

Modular Signal Path Components

Each signal path is made up of modular components that can be combined, duplicated, and arranged to create a custom signal path. Refer to the following sections to understand and use each of the modular signal path components.

Discrete Data Acquisition

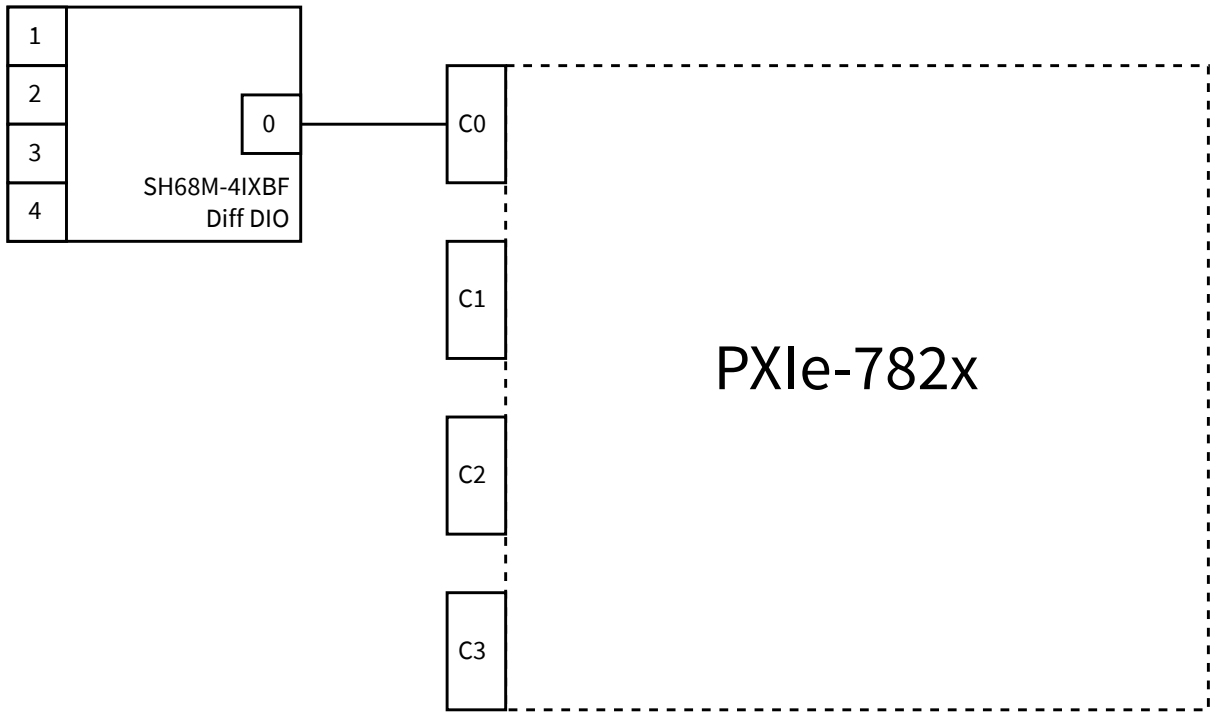
The discrete data acquisition portion of a signal path is implemented using a PXIe-7820, PXIe-7821, or PXIe-7822 FPGA DIO card and an .

This component enables the following functionality:

- Sampling high speed digital signals
- Performing analysis of digital signals in the FPGA such as computing PWM value, etc.
- Streaming data to software

The following figure shows the hardware components of the discrete data acquisition portion of a signal path.

Figure 4. Discrete Data Acquisition Modular Component



PXIe-782x to Banking

The data acquisition portion of the signal path supports up to 128 discrete data acquisition signals (4 front panel connectors, 4 banks per connector, 8 signals per bank), organized into banks.

For example, the following table shows that by connecting the to the front panel of the PXIe-782x, signals DIO0 through DIO7 are made available on the P1 ix Industrial connector of the cable, forming bank 1. Signals DIO8 through DIO15 are made available on the P2 ix Industrial connector of the cable, and so on for the 4 ix Industrial connectors of the cable.

Table 5. PXIe-782x to Bank 1 Pinout

Bank Element	P1 ix Industrial Connector Pin	PXIe-7822R Pin Name
A (IO)	1	DI0
B (IO)	2	DI1
C (IO)	4	DI2
D (IO)	5	DI3
E (IO)	6	DI4
F (IO)	7	DI5
G (IO)	9	DI6
H (IO)	10	DI7
I (REF)	3	GND
J (AUX)	8	GND

Signal Conditioning

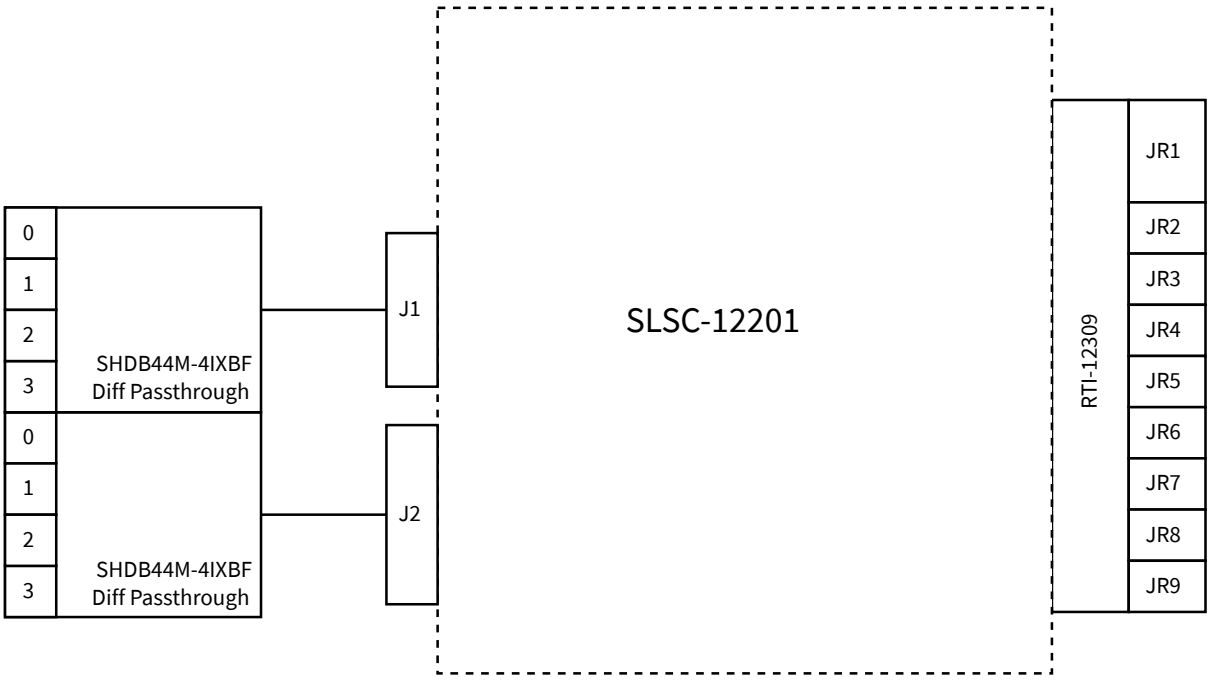
The signal conditioning portion of a signal path is implemented using an SLSC-12201, an RTI-12309, and an s. Signals are conditioned in the SLSC-12201 in order to match the high voltages from the UUT to levels acceptable to the PXIe-782x. This module converts a bank of 8 single-ended signals to a bank of 4 differential signals.

The signal conditioning component enables the following functionality:

- Signal conditioning the high voltage levels on the UUT side to levels acceptable on the DAQ side
- Converting single-ended signals to differential signals
- Performing at multiple ranges (0-5V, 0-33V)
- Configuring the discrete input threshold
- Configuring the input type (sinking, sourcing)
- Protecting from short circuits

The following figure shows the hardware necessary for the signal conditioning portion of the signal path.

Figure 5. Signal Conditioning Modular Component



SLSC-12201 Banking

The SLSC-12201 has the capacity to intake 32 discrete signals (2 front panel connectors, 4 banks per connector, 4 signals per bank) from the UUT using a .

For example, the following table shows that signals P0.0 through P0.3 from the SLSC-12201 are made available on the P1 ix Industrial connector of the cable. P1.0 through P1.3 are made available on the P2 ix Industrial connector, and so on.

The RTI-12309 (on the DAQ side of the signal path) makes available 32 signals from the SLSC-12201 (4 connectors, 1 bank per connector, 8 signals per bank).

Table 6. SLSC-12201 Banking Pinout

Bank Element (Differential)	P1 ix Industrial Connector Pin	SLSC-12201 (UUT Side) Signal (Differential)	SLSC-12201 (DAQ Side) Signal (Single-Ended)	Bank Element (Single-Ended)
A (IO)	1	P0.0	DI0	A (IO)
B (IO)	2	GND		
C (IO)	4	P0.1	DI1	B (IO)
D (IO)	5	GND		
E (IO)	6	P0.2	DI2	C (IO)
F (IO)	7	GND		
G (IO)	9	P0.3	DI3	D (IO)
H (IO)	10	GND		
I (REF)	3	NC	GND	I (REF)
J (AUX)	8	NC	GND	J (AUX)
A (IO)	1	P0.4	DI4	E (IO)
B (IO)	2	GND		
C (IO)	4	P0.5	DI5	F (IO)
D (IO)	5	GND		
E (IO)	6	P0.6	DI6	G (IO)
F (IO)	7	GND		
G (IO)	9	P0.7	DI7	H (IO)
H (IO)	10	GND		
I (REF)	3	NC	GND	I (REF)
J (AUX)	8	NC	GND	J (AUX)

The SLSC-12201 supports two reference voltages through the JR1 connector on its paired RTI-12309.

Table 7. SLSC-12201 Reference Voltage Pinouts

Signal	SLSC-12201 XJ3/RTI-12309 XP3 Pin	RTI-12309 JR1 Pin	SLSC-12201 Signal Name
V1+	H	8	V_{sup_0}
V1-	G	4	GND
V2+	F	7	V_{sup_1}
V2-	E	3	GND
V3+	D	6	NC
V3-	C	2	NC
V4+	B	5	NC
V4-	A	1	NC

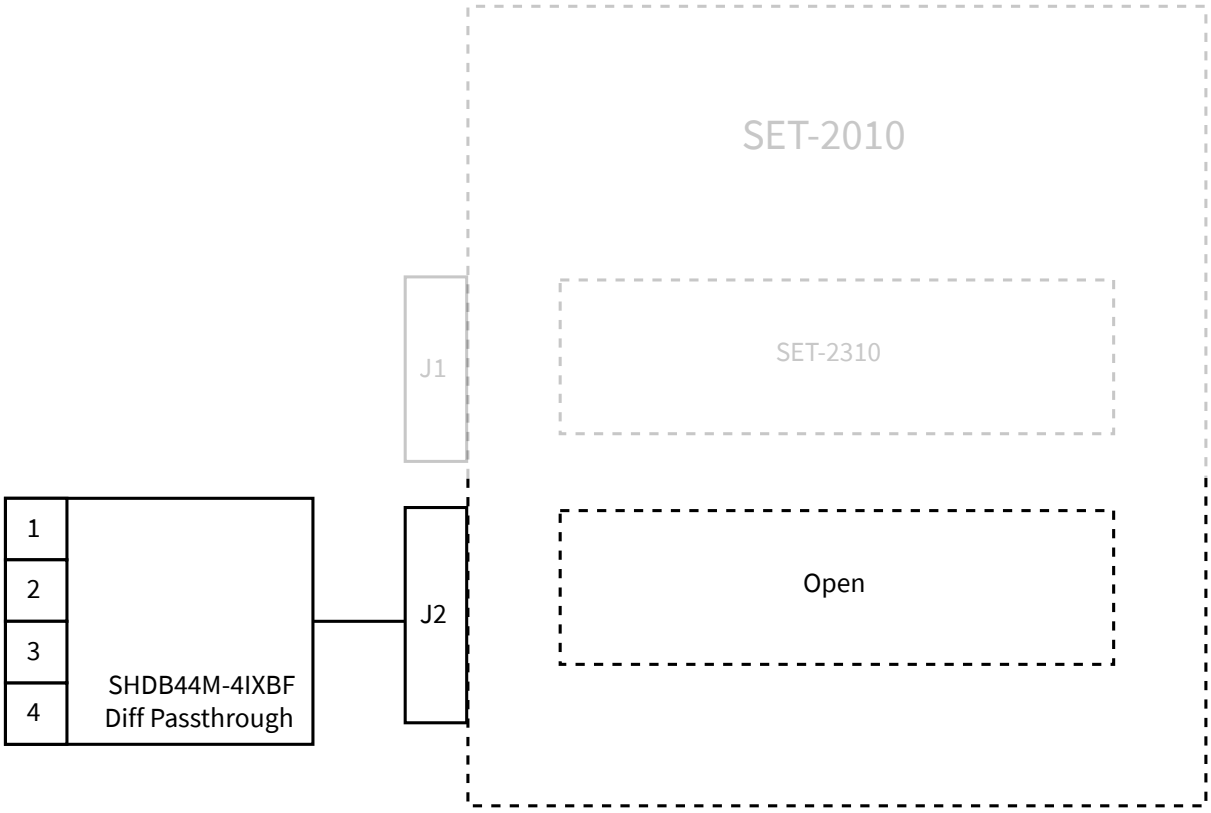
(Optional) Load Switching

The load switching portion of a signal path is implemented using one slot of the SET-2010 without a daughter card, an RTI-12309, and an .

This component enables users to switch in and out loads.

The following figure shows the hardware required to implement load switching in a signal path.

Figure 6. Load Switching Modular Component



The loading portion of the signal path supports the routing of 16 signals from the loads using a connected to the J2 connector of the SET-2010 (1 connector, 4 banks per connector, 4 signals per bank), organized into banks.

For example, the following table shows the signals that are made available from the SET-2010 on the P1 ix Industrial connector of the .

Table 8. SET-2010 to Bank 1 Pinout

Banking Element	P1 ix Industrial Connector Pin	Front Panel Signal (Differential)
A (IO)	1	P0.0+
B (IO)	2	P0.0-
C (IO)	4	P0.1+
D (IO)	5	P0.1-
E (IO)	6	P0.2+
F (IO)	7	P0.2-
G (IO)	9	P0.3+
H (IO)	10	P0.3-
I (REF)	3	REF
J (AUX)	8	AUX

Load Switching Specifications

Refer to the following specifications for key characteristics of load switching.

Number of banks	4 per SET-2310
Number of signals	4 per differential bank 8 per single-ended bank
Maximum load current	1.5 A per SET-2010 pin

(Optional) Fault Insertion

The fault insertion component allows you to perform electric error simulation and inject those errors into the signal path for more robust testing of the UUT.

The fault insertion portion of a signal path is implemented using one slot of the SET-2010 with one SET-2310 daughter card, an RTI-12309, and an to connect to the UUT.

This component enables the following functionality:

- Fault to four possible fault buses
- Fault open
- Fault short to differential pair signal
- Route REF from front panel to fault bus
- Differential or single-ended faulting

The following block diagrams show where to add a fault insertion component into a signal path with differential or single-ended signals.

Figure 7. Differential Fault Insertion Component Block Diagram

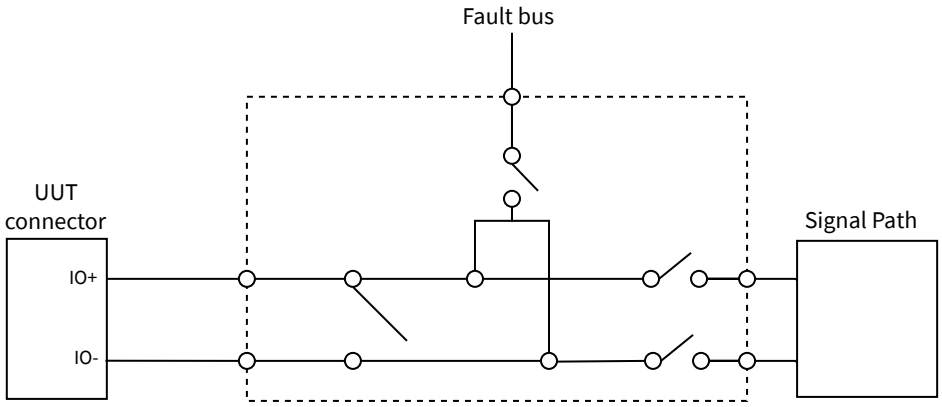
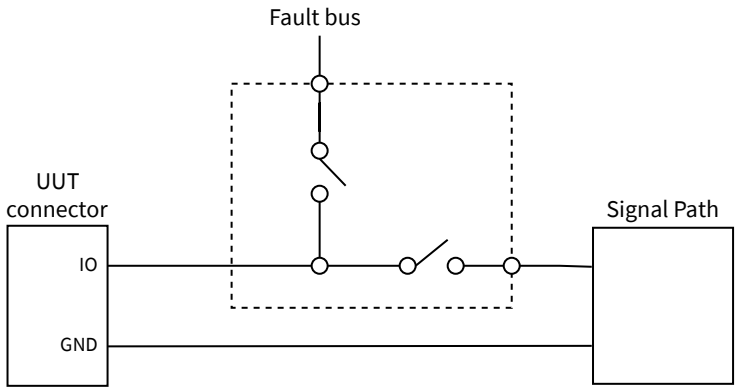
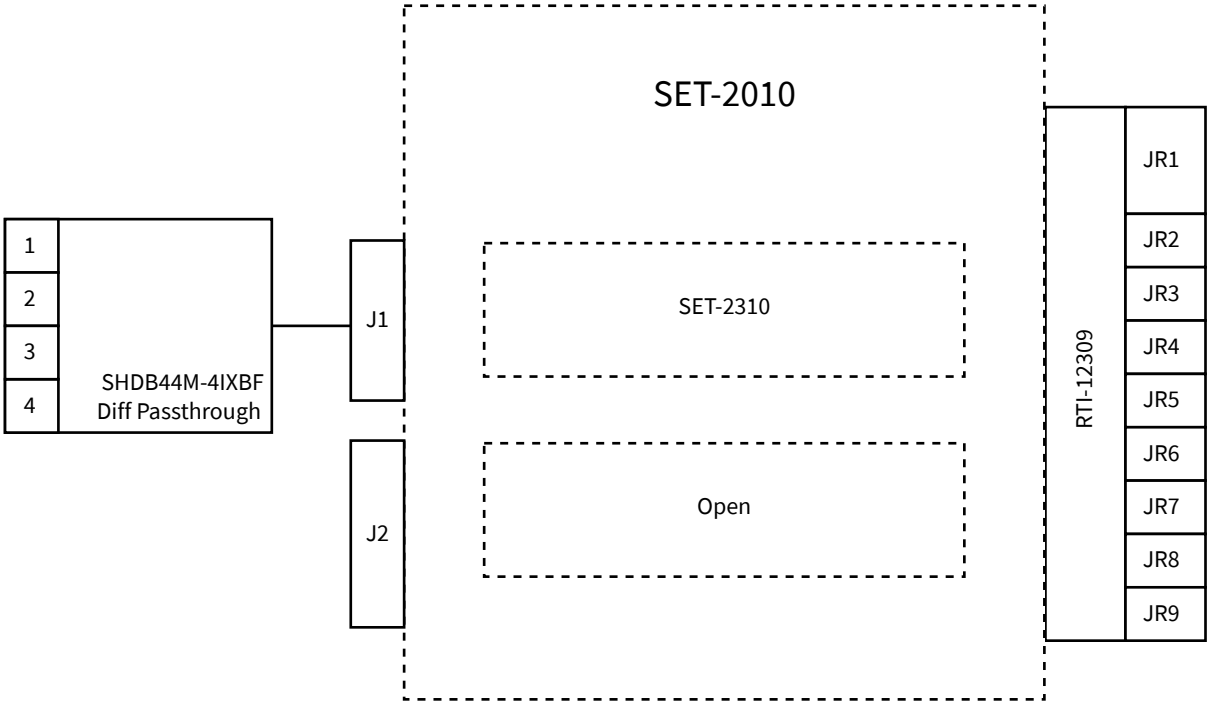


Figure 8. Single-Ended Fault Insertion Component Block Diagram



The following figure shows the hardware required to create a fault insertion component.

Figure 9. Fault Insertion Modular Component



The fault insertion portion of a signal path supports up to 32 signals from the UUT using a connected to the J1 connector of the SET-2010 (2 connector, 4 banks per connector, 4 signals per bank). For example, the following table shows the signals that are made available from the SET-2010 on the P1 ix Industrial connector of the . The same signals are also accessible from the RTI-12309 mounted on the back panel of the SET-2010.

Table 9. SET-2010 to Bank 1 Pinout

Bank Element	P1 ix Industrial Connector Pin	Internal Fault Insertion Signal (Differential)
A (IO)	1	P0.0+
B (IO)	2	P0.0-
C (IO)	4	P0.1+
D (IO)	5	P0.1-
E (IO)	6	P0.2+
F (IO)	7	P0.2-
G (IO)	9	P0.3+
H (IO)	10	P0.3-
I (REF)	3	REF
J (AUX)	8	AUX

Note Each connector on the RTI-12309 can accommodate one bank of signals.

Faulting signals are provided via the JR1 pin of the RTI-12309 connector paired with the SET-2010. The following table shows the pinout for that connector.

Table 10. Faulting Signals

RTI-12309 JR1 Pin	SET-2010 Fault Mapping
JR1.6	FAULT_A
JR1.2	FAULT_B
JR1.5	FAULT_C
JR1.1	FAULT_D

Table 10. Faulting Signals (Continued)

RTI-12309 JR1 Pin	SET-2010 Fault Mapping
JR1.8	NC
JR1.4	NC
JR1.7	NC
JR1.3	NC

The following end user-accessible signals are available when using the fault insertion component.

Table 11. End User-Accessible Signal Pinouts

Signal Type	Connector	Signal
User-accessible front panel signal	CA1.1	P0.0:3
	CA1.2	P0.4:7
	CA1.3	P1.0:3
	CA1.4	P1.4:7
	CA2.1	P2.0:3
	CA2.2	P2.4:7
	CA2.3	P3.0:3
	CA2.4	P3.4:7
Fault	JR1	FAULT A:D

Fault Insertion Unit Specifications

Refer to the following specifications for key characteristics of fault insertion units.

Note The following specifications apply to a single implementation of the fault insertion unit. These specifications will change when you customize your signal path.

Number of banks	4 per SET-2310
Number of signals	4 per differential bank 8 per single-ended bank
Fault conditions	Short/open/fault to bus
Maximum output current	1.5 A per SET-2010 pin
Maximum output current[1]	8 A per SET-2010 connector

Getting Started

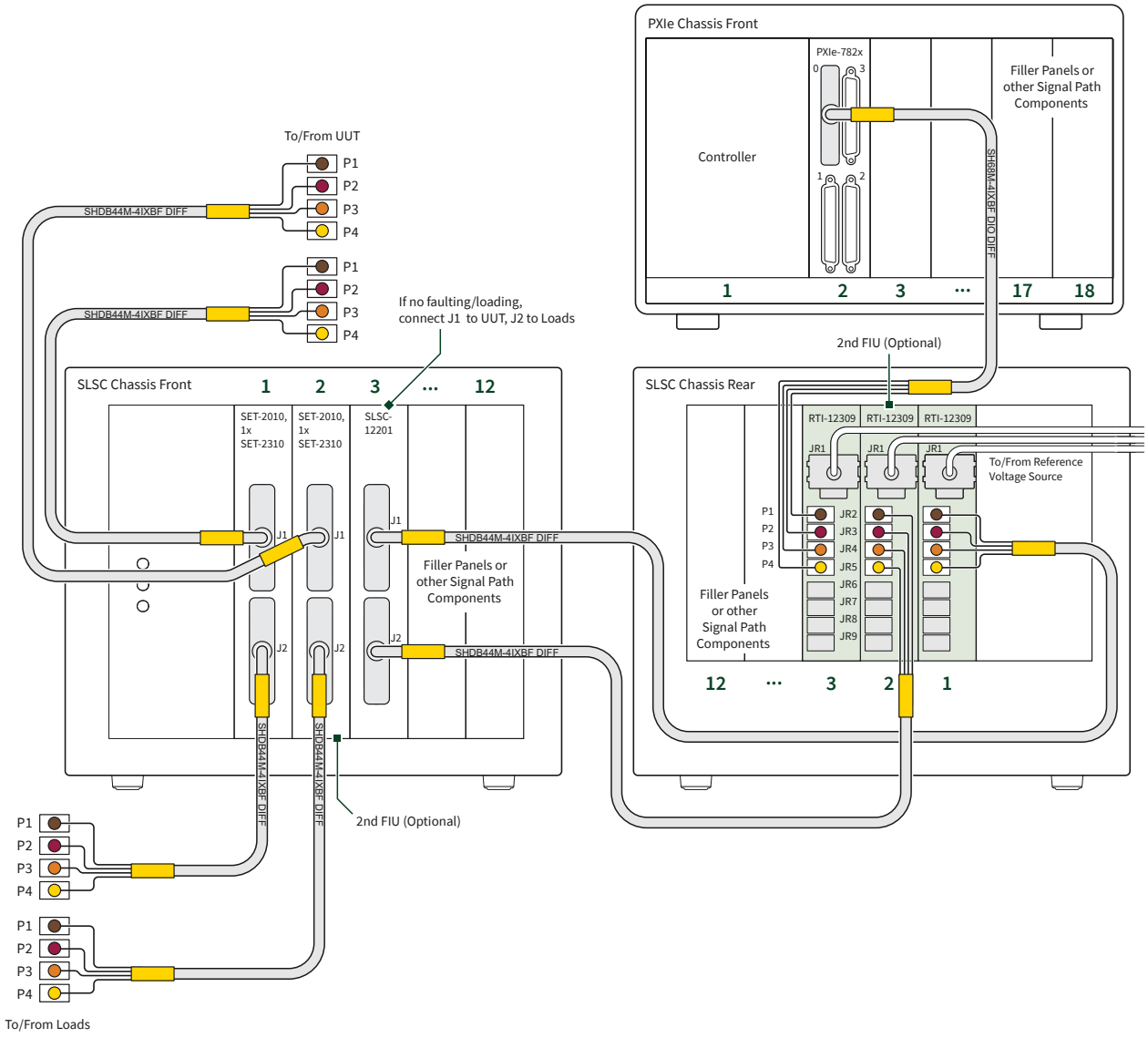
After you design your , refer to the following sections for information on how to install, configure, and begin using your test system.

Connecting Hardware for the Discrete Acquisition Signal Path

The following figure shows an example of a discrete acquisition signal path implementation, which includes support for 8 banks of discrete acquisition signals, faulting, and loading. This implementation can be scaled up or down based on your needs.

[1] If faulting all 32 signals of the SET-2010, the maximum current per line is 250 mA.

Figure 10. Discrete Acquisition Signal Path Hardware Connections



Complete the following steps to connect your hardware for a basic implementation of the discrete acquisition signal path. Adapt these steps as necessary to incorporate additional modular components or to combine signal paths.

1. Install the controller into the PXI chassis.
2. Assemble and install one or more *discrete data acquisition* components into the PXI chassis.
3. Assemble and install one or more *signal conditioning* components into the SLSC chassis. Connect the data acquisition component to the RTI-12309 of the signal conditioning component using a .
4. (Optional) If your implementation includes faulting, assemble and install one or more *fault insertion* components into the SLSC chassis.
   a) Connect the signal conditioning component to the fault insertion component using a .
   b) Connect the fault bus signals to JR1 of the RTI-12309 of the fault insertion component.
5. (Optional) If your implementation includes loading, assemble and install one or more *load switching* components into the SLSC chassis.
   a) Connect the signal conditioning component to the load switching component using a . Skip this step if you have already implemented a fault insertion component using the same SET-2010.
   b) Connect the load switching component to external load signals using a .
6. Connect the UUT according to whether you implemented any fault insertion or load switching components.
   a) If you implemented a fault insertion and/or load switching component, connect the UUT to the appropriate connector on the SET-2010 using a .
   b) If you did not implement a fault insertion and/or load switching component, connect the UUT to the signal conditioning component using a .

Note To add more banks, complete these steps using the additional DIO connectors on the PXIe-782x or additional PXIe-782x modules.

When the hardware installation is complete, install and configure software for the components in your implementation.

Creating an FPGA Bitfile

NI provides fixed FPGA personalities for discrete input, discrete output, PWM generation, and PWM measurement on the *LRU bitfiles community page*. If these are not sufficient, use the following steps to create a custom bitfile that fits your needs.

The following steps are an example of how to create an FPGA bitfile for a PXIe-782x digital reconfigurable I/O module that uses a combination of PWM and digital I/O.

Note These steps are intended to simplify the process of creating an FPGA bitfile. You may also create a file from scratch.

1. Download the following repositories from GitHub to configure the FPGA personality. You do not need to install the additional dependencies in these repositories.

GitHub Location	Repository
FPGA Addon Specialty IO	Entire repository
VeriStand FPGA Generation Wizard: `VeriStand-FPGA-Generation-Wizard\Source\Templates\`	`VeriStand-FPGA-Generation-Wizard\Source\Templates\`

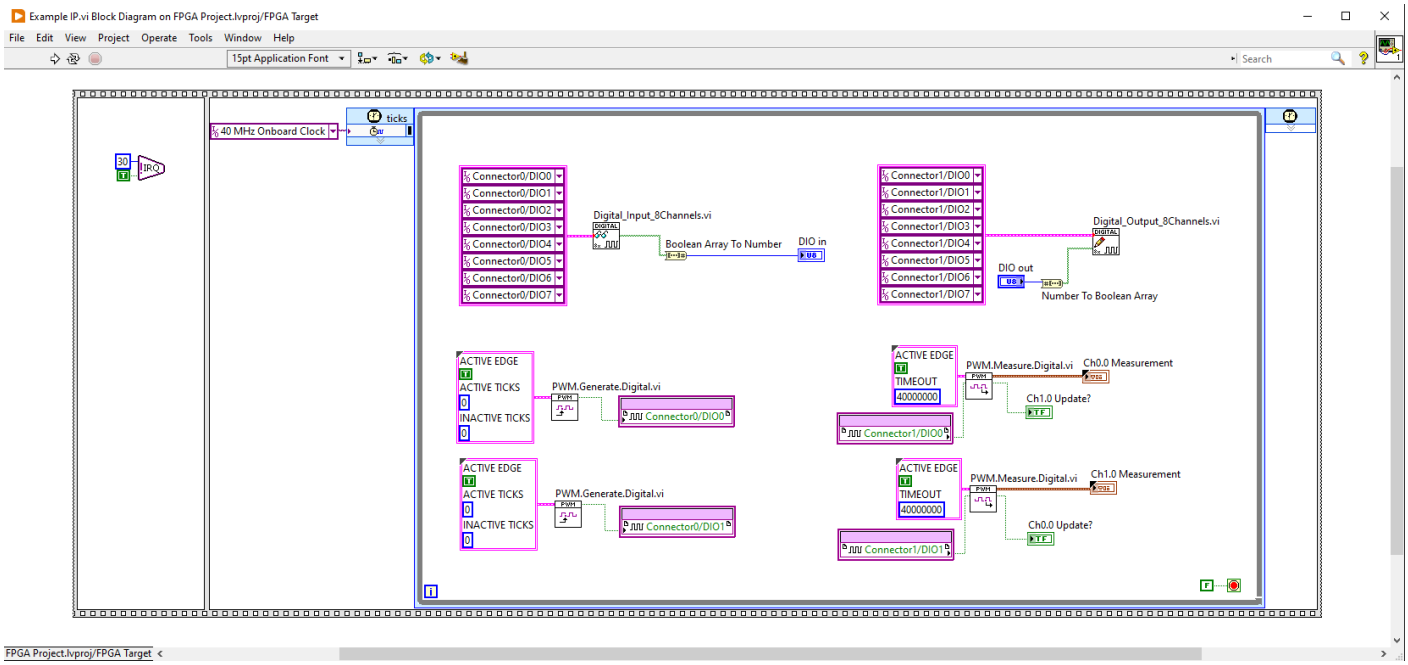
2. Create a new project in LabVIEW using the **LabVIEW FPGA Project Template**, found in the downloaded location at `VeriStand-FPGA-Generation-Wizard-master\Source\Templates\FPGA Wizard Templates`.
3. In the **Create New LabVIEW FPGA Project** window, select your project type and system setup, then click **Finish**.
4. Create an FPGA VI within your LabVIEW FPGA project.
   a) From the configuration tree in **Project Explorer**, right-click the FPGA target and select **New** » **VI** .
   b) Write the FPGA code using the following VIs included in the GitHub repositories that you installed.

   For discrete signals, you can use the 40 MHz timed loop with the FPGA Generation Wizard VIs Digital_Output_8Channels and Digital_Input_8Channels.

   For PWM simulation and acquisition signals, you can use the FPGA Addon Specialty IO VIs PWM.Generate.Digital and PWM.Measure.Digital.

   Refer to the following block diagram as an example.

Figure 11. Example FPGA Block Diagram



Per the *FPGA Addon Quick Start Guide*, you must use the Interrupt VI shown in the first frame of the sequence structure, as this helps to synchronize with the custom device. Set the timed loop to 40 MHz.

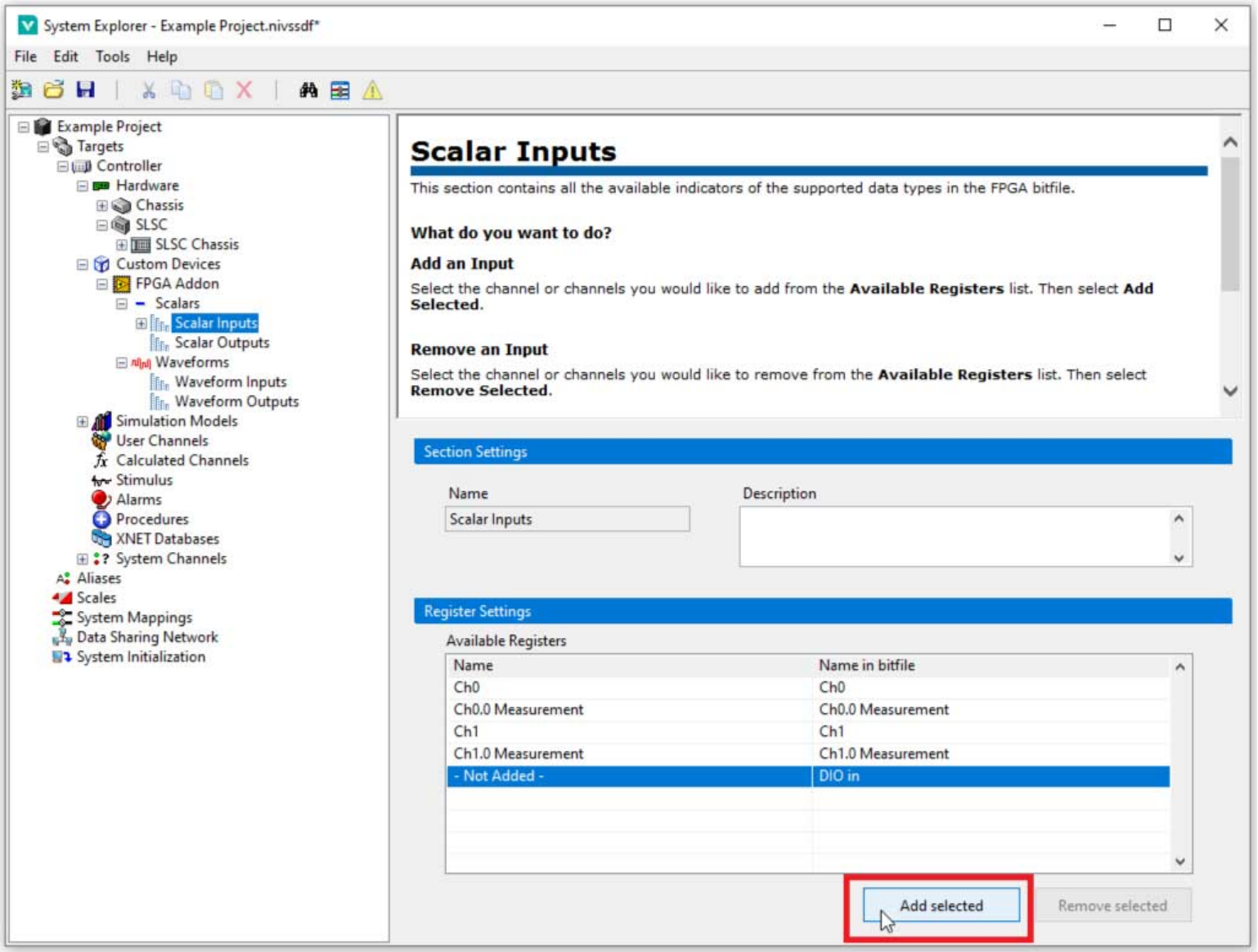
5. Compile the FPGA bitfile for use in VeriStand. Refer to *LabVIEW FPGA Compilation Process: From Run Button to Bitfile* on ni.com for more information.

Configuring the FPGA Addon Custom Device to VeriStand

Complete the following steps to add and configure the FPGA Addon custom device using the FPGA bitfile that you created in *Creating an FPGA Bitfile* on page 13.

1. Launch VeriStand **System Explorer**.
2. In the **System Explorer** configuration tree, expand **Targets** »**Controller** and right-click **Custom Devices**.
3. Select **National Instruments** »**FPGA Addon** to add the custom device.
4. In the **Select configuration to import** dialog box, enable the **New Instance?** and **Group Scalars?** checkboxes, then click **OK**. The window to the right will show the newly-created custom device settings.
5. In FPGA Settings, specify the path to the bitfile that you created.
6. In the configuration tree, expand **FPGA Addon** and configure **Scalar Inputs** and **Scalar Outputs** for the discrete signals that correspond to values from your bitfile. These values are specified in the Register Settings section, as shown in the following figure.

Figure 12. Configure Scalar Inputs in VeriStand

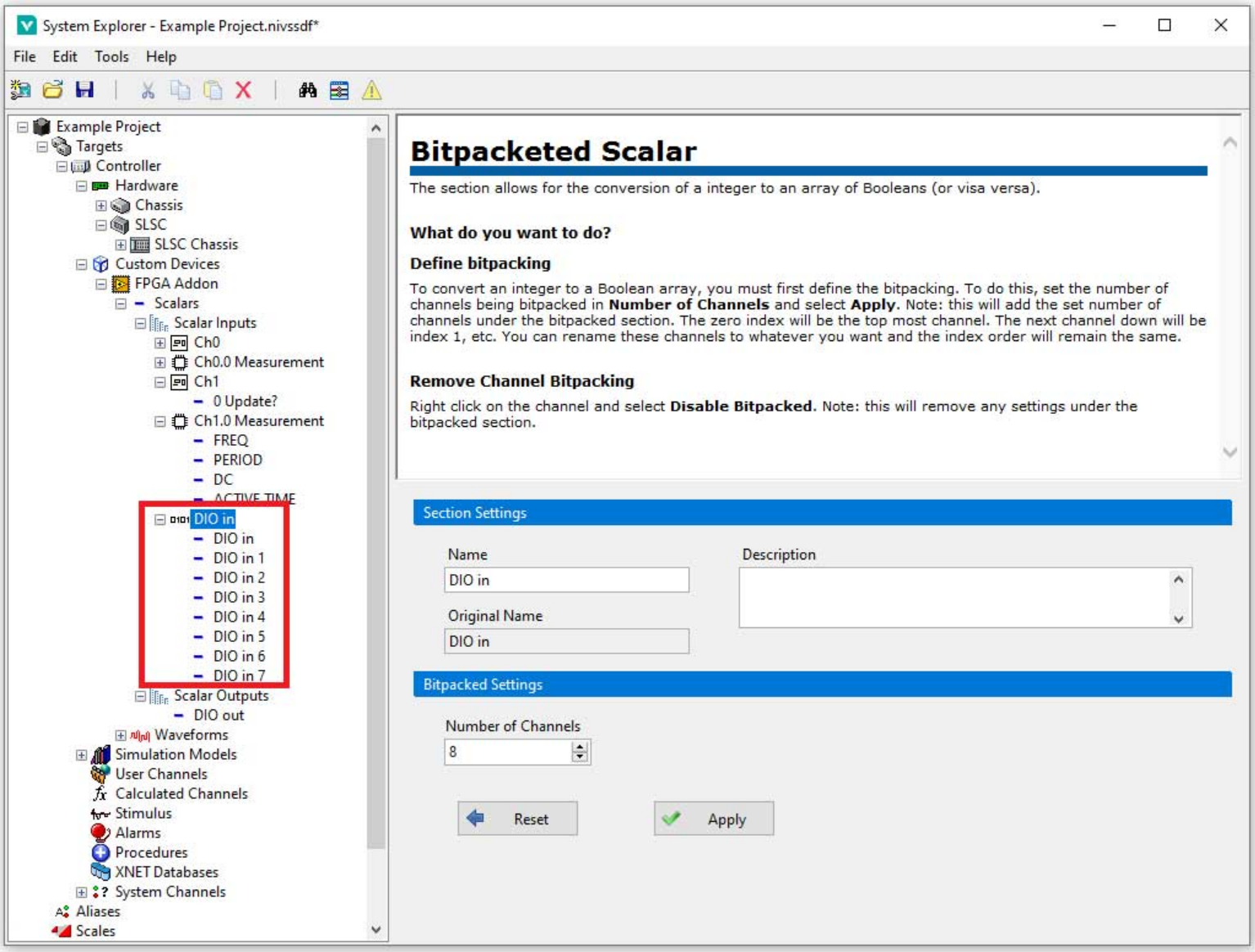


After you configure the scalar inputs and outputs, the inputs and outputs appear underneath **FPGA Addon** in the configuration tree.

7. (Optional) By default, the U8 scalar inputs are configured as a single channel in System Explorer. Complete the following steps if you would like to break the inputs into eight unique single-bit channels.
   a) Right-click the U8 channel from the configuration tree and select **Enable Bitpacked**
   b) In the Bitpacked settings section, set the **Number of Channels** to `8` (one per bit).
   c) Click **Apply**.

   The U8 is now divided into eight, as shown in the following figure.

Figure 13. Single-Bit Channels in VeriStand



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