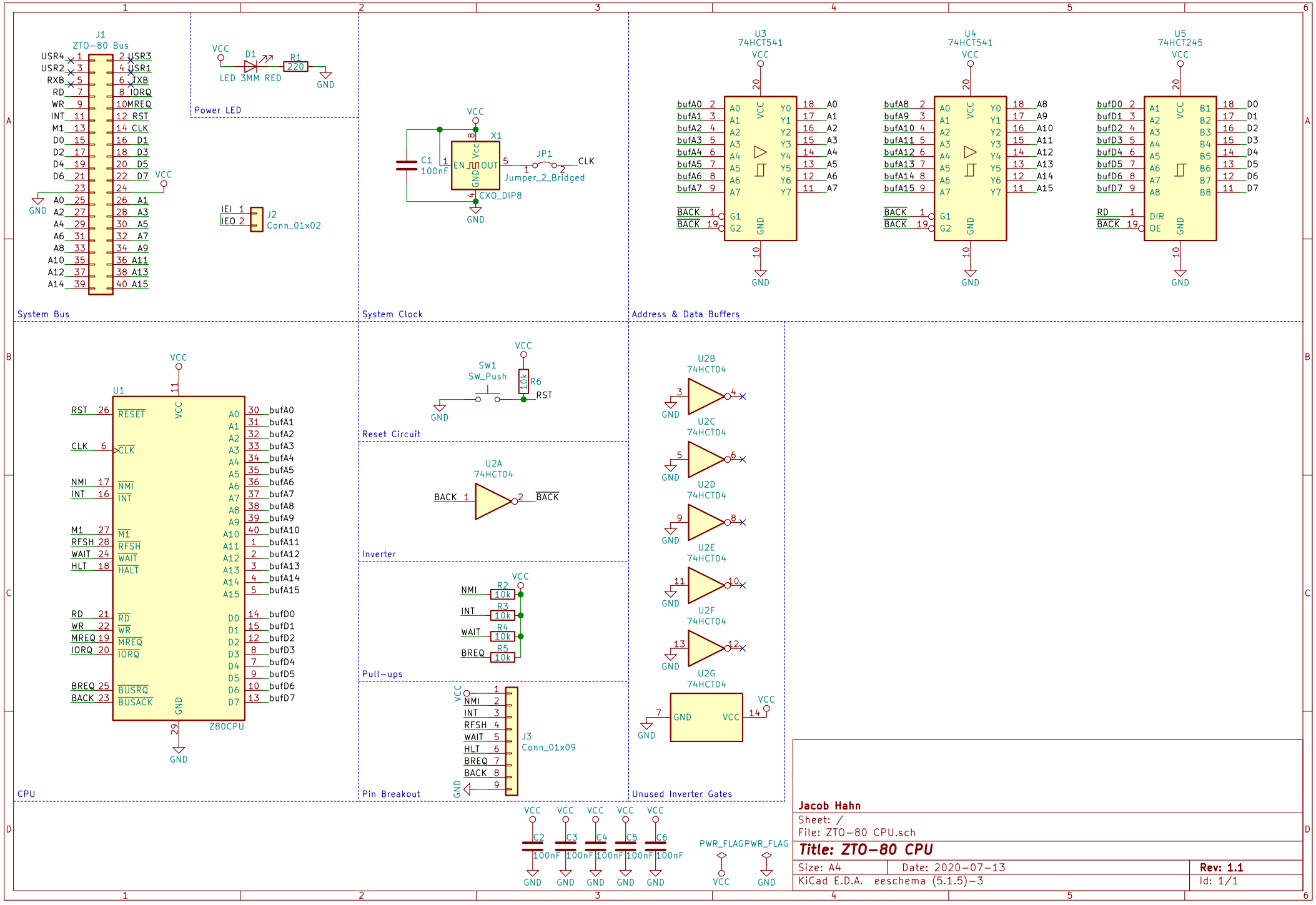
J1
ZTO-80 Bus
USR4 1
USR2 3
RXB 5
RD 7
WR 9
INT 11
M1 13
D0 15
D2 17
D4 19
D6 21
23
A0 25
A2 27
A4 29
A6 31
A8 33
A10 35
A12 37
A14 39
2 USR3
4 USR1
6 TXB
8 IORQ
10 MREQ
12 RST
14 CLK
16 D1
18 D3
20 D5
22 D7
24
26 A1
28 A3
30 A5
32 A7
34 A9
36 A11
38 A13
40 A15
VCC
GND
System Bus
VCC
D1
LED 3MM RED
R1
220
GND
Power LED
IEI 1
IEO 2
J2
Conn_01x02
VCC
X1
C1
100nF
EN
OUT
GND
CXO_DIP8
JP1
Jumper_2_Bridged
CLK
GND
System Clock
U3
74HCT541
U4
74HCT541
U5
74HCT245
bufA0 2
bufA1 3
bufA2 4
bufA3 5
bufA4 6
bufA5 7
bufA6 8
bufA7 9
BACK 1
BACK 19
A0 18
A1 17
A2 16
A3 15
A4 14
A5 13
A6 12
A7 11
bufA8 2
bufA9 3
bufA10 4
bufA11 5
bufA12 6
bufA13 7
bufA14 8
bufA15 9
A8 18
A9 17
A10 16
A11 15
A12 14
A13 13
A14 12
A15 11
bufD0 2
bufD1 3
bufD2 4
bufD3 5
bufD4 6
bufD5 7
bufD6 8
bufD7 9
RD 1
BACK 19
D0 18
D1 17
D2 16
D3 15
D4 14
D5 13
D6 12
D7 11
DIR
OE
Address & Data Buffers
U1
RST 26
CLK 6
NMI 17
INT 16
M1 27
RFSH 28
WAIT 24
HLT 18
RD 21
WR 22
MREQ 19
IORQ 20
BREQ 25
BACK 23
RESET
BUSRQ
BUSACK
Z80CPU
bufA0 30
bufA1 31
bufA2 32
bufA3 33
bufA4 34
bufA5 35
bufA6 36
bufA7 37
bufA8 38
bufA9 39
bufA10 40
bufA11 1
bufA12 2
bufA13 3
bufA14 4
bufA15 5
bufD0 14
bufD1 15
bufD2 12
bufD3 8
bufD4 7
bufD5 9
bufD6 10
bufD7 13
CPU
SW1
SW_Push
R6
10k
RST
Reset Circuit
U2A
74HCT04
BACK 1
2 BACK
Inverter
NMI
INT
WAIT
BREQ
R2
R3
R4
R5
10k
Pull-ups
J3
Conn_01x09
NMI 2
INT 3
RFSH 4
WAIT 5
HLT 6
BREQ 7
BACK 8
9
Pin Breakout
U2B
U2C
U2D
U2E
U2F
U2G
74HCT04
GND
VCC
Unused Inverter Gates
C2
C3
C4
C5
C6
100nF
PWR_FLAG
Jacob Hahn
Sheet: /
File: ZTO-80 CPU.sch
Title: ZTO-80 CPU
Size: A4
Date: 2020-07-13
Rev: 1.1
KiCad E.D.A. eeschema (5.1.5)-3
Id: 1/1