FE
Block Guide

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Revision Control

Table 1 - Revision Control

Version	Date	Description	Authors	Revised by
1.0	31/08/2016	Preliminary	Tomazine, L	Krüger, C
1.1	12/12/2016	Revised	Tomazine, L	

Contents

1 Introduction 4

1.1 Acronyms and Abbreviations 4
1.2 Nomenclatures, Bit and Sample Representation 4
1.3 References 5

2 High-level Functional Description 6

2.1 Features 6

3 Macro Architecture 7

3.1 Description 7
3.2 External Interface 7
3.3 Register Map 8
3.3.1 IP Memory Map 11
3.3.2 IP Register Description 12
3.4 Modes of Operation 12
3.4.1 Functional mode 12
3.4.2 Test mode 12
3.5 Clock and reset 12

4 Micro Architecture 12

4.1 Power 4 Module 12
4.1.1 Power 4 Interface 13
4.1.2 Power 4 Complexity Estimation 13
4.2 FFT 512 Module 13
4.2.1 FFT 512 Interface 14
4.2.2 FFT 512 Complexity Estimation 14
4.3 Peak Module 14
4.3.1 Peak Interface 14
4.3.2 Peak Complexity Estimation 15

FE

1 Introduction

This document describes the behavioral SystemC implementation of the frequency offset estimator based on the frequency domain Mth power algorithm. At the SystemC model the algorithm was named FE (Frequency Offset Estimator).

1.1 Acronyms and Abbreviations

Table 2 contains sample acronyms and abbreviations used in a document.

Table 2 - Acronyms and Abbreviated Terms

Term	Meaning
FE	Frequency Offset Estimator
DFT	Discrete Fourier Transform
FFT	Fast Fourier Transform
N	FFT size (Default 512 samples)

1.2 Nomenclatures, Bit and Sample Representation

Next it is present the representation of bits used on the document. Types of registers and wires.

Table 3 – Nomenclatures, Bit and Sample Representation

Sample Representation	MSS	Most Significant Sample	(*MSS:LSS)*
	LSS	Least Significant Sample	
Bit Representation	MSB	Most Significant Bit	[*MSB:LSB*]
	LSB	Least Significant Bit	
Fixed Point Representation	WL	Total Number of Bits - Word length	*<WL,IWL[,QUANT][,OVFLW][,NBITS]* > bits
	IWL	Number of Integer portion length	
	QUANT	Quantization by default: SC_TRN	
	OVFLW	Overflow by default: SC_WRAP	
	NBITS	Number of saturated bits, only used for overflow mode and specifies how many bits will be saturated	
Logic Values	'1'	Bit asserted	
	'0'	Bit de-asserted	
	'x'	Bit don't care	

QUANT mode can be one of the following:

- SC_TRN – Truncation
- SC_RND – Round toward plus infinity

OVFLW mode can be one of the following:

- SC_WRAP – Wrap-around
- SC_SAT - Saturation

1.3 References

The references must include full references, such as standards, others documents and so on.

- MORELLI, MENGALI, 1998
- NAKAGAWA2011, Wide-Range and Fast-Tracking Frequency Offset Estimator for Optical Coherent Receivers

2 High-level Functional Description

In coherent reception systems, the signal received is mixed with the transmitted signal by and a local oscillator. For accurate detection of this signal, it is necessary that local oscillator laser has been locked in frequency and phase with the laser transmitter. This is a complicated task due to the laser phase noise and the high cost to maintaining the transmitter local oscillator operating exactly at same frequency. Fortunately, it is possible to estimate and compensate the differences between the phases and frequencies of the lasers in digital domain by a carrier recovery module. If this error phase is not compensated, the constellation of a modulation system with a format M-QAM or M-PSK will suffer rotations for each symbol, affecting the correct symbol estimation.

This block aims to estimate the frequency offset between transmitter and local oscillator lasers. The estimation employs the frequency domain Mth power method.

Assuming a signal modulation format M-PSK, when to it is applied an Mth power, it becomes with a non-zero average. Spectrally, this means that appears an impulse at zero frequency (DC level). In this case if a frequency offset exist, this impulse will be shifted. It is possible to implement a frequency offset estimator checking if the peak is shifted, using an approach in the frequency domain.

Figure 1 - FE Block Diagram.

2.1 Features

The features of the block are listed below:

- Mth Power:
  - Each input sample is individually elevated to the Mth power
- 512 point FFT:
  - This block receives the Mth power signal and calculates its FFT
- Peak Position:
  - Finds the position of the maximum absolute value of the FFT result

3 Macro Architecture

3.1 Description

Description of the top module.

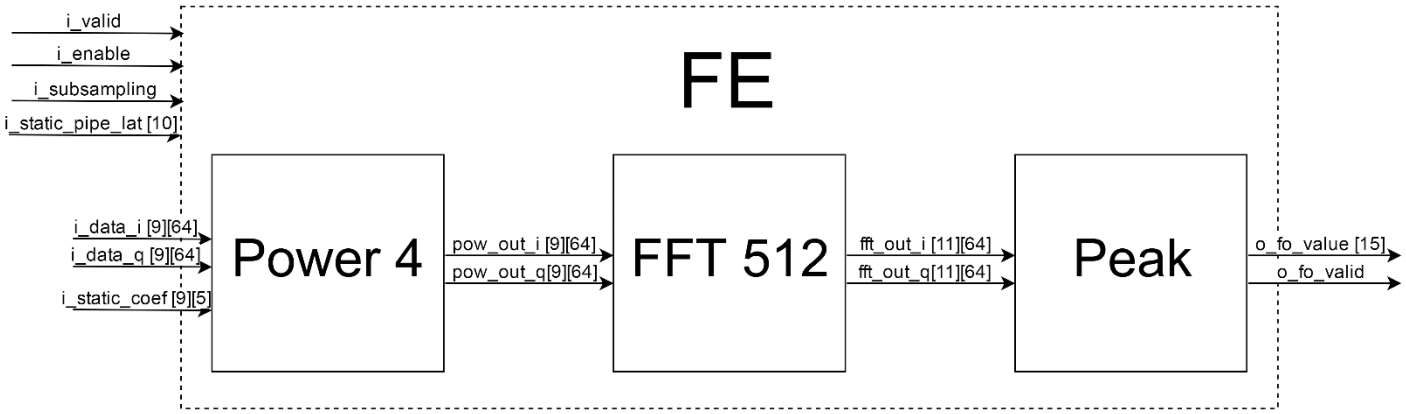

Figure 2 – FE Diagram

3.2 External Interface

External interface and parameters of the top module. List of I/O pins and communication with other blocks.

Table 3 – External Interface

Signal	Width (bits)	I/O	Description
clk	1	I	Input clock (437.5 MHz with duty cycle of 50%)
rst_async_n	1	I	Input reset - Active Low
i_valid	1	I	Valid input signal – Active High
i_enable	1	I	Block enable signal – Active High
i_subsampling	1	I	Sub sampling mode flag – Active High
i_static_pipe_lat	10	I	Latency clock cycles between two operations
i_static_coef [5]	9	I	Fir filter coefficients for sub-sampling mode on
i_data_i [64]	9	I	In phase symbol component
i_data_q [64]	9	I	Quadrature symbol component
o_fo_valid	1	O	Valid output signal – Active High
o_fo_value	15	O	Frequency Offset estimation

Table 4 – Parameters

Parameter name	Description	Value
NBW_IN	Number of word bits of the input	9
NBI_IN	Number of integer bits of the input	2
NBW_FFT	Number of word bits of the FFT output	11
NBI_FFT	Number of integer bits of the FFT output	2
FE_NS_IN	Number of input samples	64
FE_NS_FFT	Number of samples for the FFT	512
FE_NB_MAX	Number of bits for the max tree input	8
FE_NS_FIR	FIR filter order	5

3.3 Register Map

3.3.1 IP Memory Map

IPxyz Control Register - Base Address = 0x1000			
ADDRESS OFFSET (*ADDR[11:1]*)	**REGISTER NAME**	**TYPE**	**DEFAULT**
0x000	i_enable	R/W	0x0000
0x001	i_static_pipe_lat	R/W	0x0064
0x002	i_static_coef_0	R/W	0x0003
0x003	i_static_coef_1	R/W	0x001E
0x004	i_static_coef_2	R/W	0x003C
0x005	i_static_coef_3	R/W	0x001E
0x006	i_static_coef_4	R/W	0x0003
0x007	o_fo_value	R/W	0x0000

3.3.2 IP Register Description

i_enable Register

Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	reserved							
Default	0	0	0	0	0	0	0	0

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	reserved							enable
Default	0	1	1	0	0	1	0	0

Bit 15-1: reserved

Register field *15 to 1* are reserved bits for future applications and should not be written.

Bit 0: enable

The *enable* bit is the block enable signal.

i_static_pipe_lat Register

Bits	15	14	13	12	11	10	9	8
Field	reserved						pipe9	pipe8
Default	0	0	0	0	0	0	0	0

Bits	7	6	5	4	3	2	1	0
Field	pipe7	pipe6	pipe5	pipe4	pipe3	pipe2	pipe1	pipe0
Default	0	1	1	0	0	1	0	0

Bit 15-10: reserved

Register field *15 to 10* are reserved bits for future applications and should not be written.

Bit 9-0: pipe

The *pipe9-pipe0* bits determine the number of clock cycles between 2 operations.

i_static_coef_0 Register

Bits	15	14	13	12	11	10	9	8
Field	reserved							coef0_8
Default	0	0	0	0	0	0	0	0

Bits	7	6	5	4	3	2	1	0
Field	coef0_7	coef0_6	coef0_5	coef0_4	coef0_3	coef0_2	coef0_1	coef0_0
Default	0	0	0	0	0	0	1	1

Bit 15-9: reserved

Register field *15 to 9* are reserved bits for future applications and should not be written.

Bit 8-0: coef0

The *coef0_8- coef0_0* are the coefficient values of the FIR filter used in the sub-sampling mode.

i_static_coef_1 Register

Bits	15	14	13	12	11	10	9	8
Field	reserved							coef1_8
Default	0	0	0	0	0	0	0	0

Bits	7	6	5	4	3	2	1	0
Field	coef1_7	coef1_6	coef1_5	coef1_4	coef1_3	coef1_2	coef1_1	coef1_0
Default	0	0	0	1	1	1	1	0

Bit 15-9: reserved

Register field *15 to 9* are reserved bits for future applications and should not be written.

Bit 8-0: coef1

The *coef1_8- coef1_0* are the coefficient values of the FIR filter used in the sub-sampling mode.

i_static_coef_2 Register

Bits	15	14	13	12	11	10	9	8
Field	reserved							coef2_8
Default	0	0	0	0	0	0	0	0

Bits	7	6	5	4	3	2	1	0
Field	coef2_7	coef2_6	coef2_5	coef2_4	coef2_3	coef2_2	coef2_1	coef2_0
Default	0	0	1	1	1	1	0	0

Bit 15-9: reserved

Register field *15 to 9* are reserved bits for future applications and should not be written.

Bit 8-0: coef2

The *coef2_8- coef2_0* are the coefficient values of the FIR filter used in the sub-sampling mode.

i_static_coef_3 Register

Bits	15	14	13	12	11	10	9	8
Field	reserved							coef3_8
Default	0	0	0	0	0	0	0	0

Bits	7	6	5	4	3	2	1	0
Field	coef3_7	coef3_6	coef3_5	coef3_4	coef3_3	coef3_2	coef3_1	coef3_0
Default	0	0	0	1	1	1	1	0

Bit 15-9: reserved

Register field *15 to 9* are reserved bits for future applications and should not be written.

Bit 8-0: coef3

The *coef3_8- coef3_0* are the coefficient values of the FIR filter used in the sub-sampling mode.

i_static_coef_4 Register

Bits	15	14	13	12	11	10	9	8
Field	reserved							coef4_8
Default	0	0	0	0	0	0	0	0

Bits	7	6	5	4	3	2	1	0
Field	coef4_7	coef4_6	coef4_5	coef4_4	coef4_3	coef4_2	coef4_1	coef4_0
Default	0	0	0	0	0	0	1	1

Bit 15-9: reserved

Register field *15 to 9* are reserved bits for future applications and should not be written.

Bit 8-0: coef4

The *coef4_8- coef4_0* are the coefficient values of the FIR filter used in the sub-sampling mode.

o_fo_value Register

Bits	15	14	13	12	11	10	9	8
Field	reserved	value14	value13	value12	value11	value10	value9	value8
Default	0	0	0	0	0	0	0	0

Bits	7	6	5	4	3	2	1	0
Field	value7	value6	value5	value4	value3	value2	value1	value0
Default	0	0	0	0	0	0	0	0

Bit 15: reserved

Register field *15* is reserved bits for future applications and should not be written.

Bit 14-0: value

The *value14 – value0* is the frequency offset estimation value.

3.4 Modes of Operation

There are basically two modes of operation for the FE block: normal mode and sub-sampling mode. In normal mode the input samples are directly sent through the Mth power block and the result is sent to the FFT block, taking 8 clock cycles to complete the 512 samples needed to compute de 512 point FFT (8 cycles x 64 samples/cycle).

For the sub-sampling mode the block will consider only 1 sample in every 16 input samples. In that way, there will be only 4 valid samples in each clock cycle. To prevent aliasing, the samples are filtered using a 5 order FIR filter after the Mth power block. So, in the sub-sampling mode it is necessary 128 clock cycles (8*16) to feed the FFT input.

In both modes there will be a configurable latency between a valid output and the start of a new operation, defined by the *i_static_pipe_lat* input value. Also is important to mention that the output value will be the current value (calculated) plus the last output value and the sub-sampling flag will be registered only in an output valid (*o_fo_valid*) occurrence.

3.4.1 Functional mode

For an operation in the functional mode the *i_enable* port must be active, along with the *rst_async_n* signal.

3.4.2 Test mode

3.5 Clock and reset

The clock of the system, droved by the port *clk*, is 437.5 MHz with a 50% duty cycle. For the reset functionality, it is used the *rst_async_n* port, which have an asynchronal behavior and is active low. The reset port needs to be active for 2 cycles to a proper system restart.

4 Micro Architecture

4.1 Power 4 Module

This block basically raises the input signal to the power of 4 aiming to undo the modulation. The relation between the input data and the output data is given by the equation:

$$pow\_out\_i[N] = i\_data\_i[N]^4 + i\_data\_q[N]^4 - 6.i\_data\_i[N]^2.i\_data\_q[N]^2$$
$$pow\_out\_q[N] = 4.(i\_data\_i[N]^3.i\_data\_q[N] - i\_data\_i[N].i\_data\_q[N]^3)$$

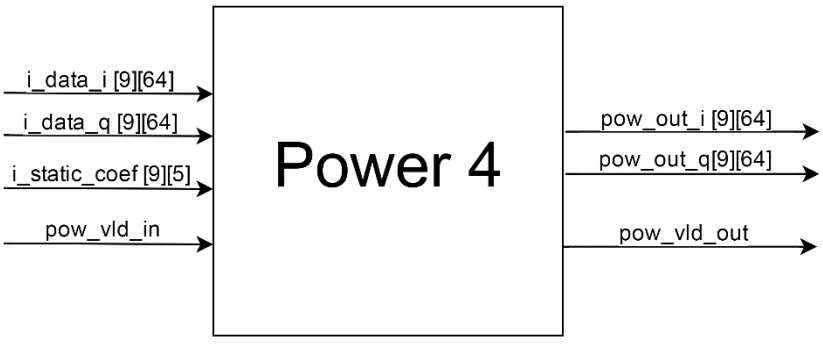

Figure 3 – Power 4 Diagram

4.1.1 Power 4 Interface

Block I/O pins.

Table 6 – Power 4 Interface

Signal	I/O	Description	From/To
clk	I	Input clock at 437.5Mhz with duty cycle of 50%	FE
rst_async_n	I	Input reset - Active Low	FE
pow_vld_in	I	Valid input signal – Active High	FE
i_data_i [64]	I	In phase symbol component	FE
i_data_q [64]	I	Quadrature symbol component	FE
i_coef [5]	I	Fir filter coefficients for sub-sampling mode on	FE
pow_out_i [64]	O	Signal raised to power of 4 (in phase component)	FFT 512
pow_out_q [64]	O	Signal raised to power of 4 (quadrature component)	FFT 512
pow_vld_out	O	Valid output signal – Active High	FFT 512

4.1.2 Power 4 Complexity Estimation

Complexity estimation of the sub-block using the number of arithmetic operators.

Table 9 – Power 4 Complexity

Operator	Number of instantiations
Adder	64
Subtractor	128 (2*64)
Multiplier	576 (9*64)

4.2 FFT 512 Module

This module is aimed to perform the discrete Fourier transform (DFT) through the fast algorithm (FFT). The porpoise of pass the signal to the frequency domain is to estimate the frequency peak and therefore the frequency offset. The FFT is calculated using 64 instances of an 8 points serial FFT and 1 instance of a 64 points FFT. In this way the 512 points FFT is calculated in 8 steps of 64 points each one.

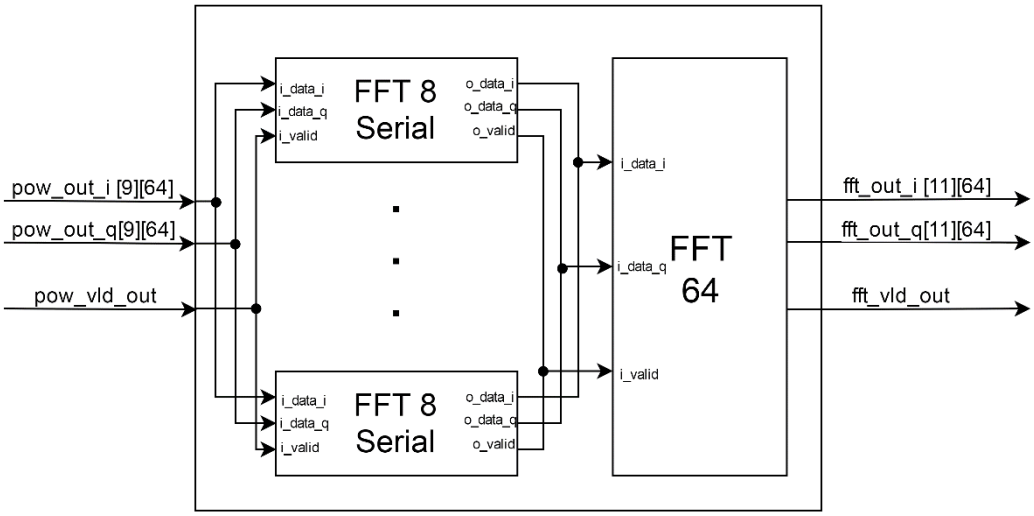

Figure 3 –FFT 512 Diagram

4.2.1 FFT 512 Interface

Block I/O pins.

Table 6 – FFT 512 Interface

Signal	I/O	Description	From/To
clk	I	Input clock at 437.5Mhz with duty cycle of 50%	FE
rst_async_n	I	Input reset - Active Low	FE
pow_out_i [64]	I	Signal raised to power of 4 (in phase component)	POWER 4
pow_out_q [64]	I	Signal raised to power of 4 (quadrature component)	POWER 4
pow_vld_out	I	Valid input signal – Active High	POWER 4
fft_out_i [64]	O	FFT result data (in phase component)	PEAK
fft_out_q [64]	O	FFT result data (quadrature component)	PEAK
fft_vld_out	O	Valid output signal – Active High	PEAK

4.2.2 FFT 512 Complexity Estimation

Resources: the DIT FFT radix-2 has 5N(log2 N) operations. So, for an N equal to 64: 1920 operations and for an N equal to 8: 120 operations. Then for this block the estimated resources are 1920+64*120 = 9600.

4.3 Peak Module

This module is aimed to obtain the absolute value of the complex FFT output signal and then find the peak position of the these values. With this information, the block also calculate the frequency offset of the estimator input data.

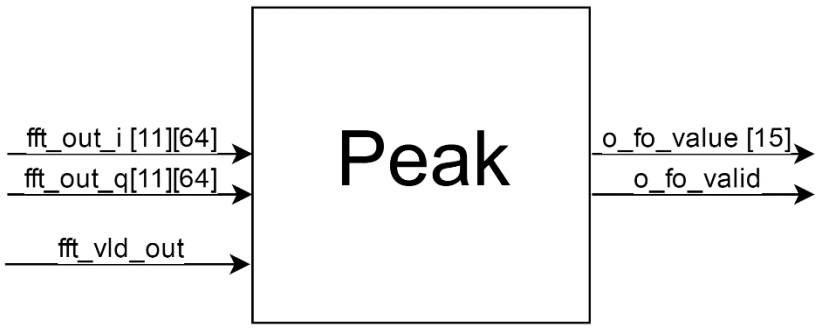

Figure 3 – Peak Diagram

4.3.1 Peak Interface

Block I/O pins.

Table 6 – Peak Interface

Signal	I/O	Description	From/To
clk	I	Input clock at 437.5Mhz with duty cycle of 50%	FE
rst_async_n	I	Input reset - Active Low	FE

Signal	I/O	Description	From/To
fft_out_i [64]	I	FFT result data (in phase component)	FFT 512
fft_out_q [64]	I	FFT result data (quadrature component)	FFT 512
fft_vld_out	I	Valid input signal – Active High	FFT 512
o_fo_value	O	Valid output signal – Active High	FE
o_fo_valid	O	Frequency Offset estimation	FE

4.3.2 Peak Complexity Estimation

Complexity estimation of the sub-block using the number of arithmetic operators.

Table 9 – Peak Complexity

Operator	Number of instantiations
Adder	64
Multiplier	128 (64*2)
Comparators	63 (32+16+8+4+2+1)