CS 2110 Timed Lab 2: Finite State Machines

Your TAs

Spring 2020

Contents

Please take the time to read the entire document before starting the assignment. It is your responsibility to follow the instructions and rules.

1 Timed Lab Rules - Please Read

1.1 General Rules

1. You are allowed to submit this timed lab starting at the moment the assignment is released, until you are checked off by your TA as you leave the recitation classroom. Gradescope submissions will remain open until 7:15 pm - but you are not allowed to submit after you leave the recitation classroom under any circumstances. **Submitting or resubmitting the assignment after you leave the classroom is a violation of the honor code - doing so will automatically incur a zero on the assignment and might be referred to the Office of Student Integrity.**
2. Make sure to give your TA your Buzzcard before beginning the Timed Lab, and to pick it up and get checked off before you leave. **Students who leave the recitation classroom without getting checked off will receive a zero.**
3. Although you may ask TAs for clarification, you are ultimately responsible for what you submit. **The information provided in this Timed Lab document takes precedence.** If in doubt, please make sure to indicate any conflicting information to your TAs.
4. Resources you are allowed to use during the timed lab:
   - Assignment files
   - Previous homework and lab submissions
   - Your mind
   - Blank paper for scratch work (please ask for permission from your TAs if you want to take paper from your bag during the Timed Lab)
5. Resources you are **NOT** allowed to use:
   - The Internet (except for submissions)
   - Any resources that are not given in the assignment
   - Textbook or notes on paper or saved on your computer
   - Email/messaging
   - Contact in any form with any other person besides TAs
6. **Before you start, make sure to close every application on your computer.** Banned resources, if found to be open during the Timed Lab period, will be considered a violation of the Timed Lab rules.
7. We reserve the right to monitor the classroom during the Timed Lab period using cameras, packet capture software, and other means.

1.2 Submission Rules

1. Follow the guidelines under the Deliverables section.
2. You are also responsible for ensuring that what you turned in is what you meant to turn in. After submitting you should be sure to download your submission into a brand new folder and test if it works. No excuses if you submit the wrong files, what you turn in is what we grade. In addition, your assignment must be turned in via Gradescope. Under no circumstances whatsoever we will accept any email submission of an assignment. Note: if you were granted an extension you will still turn in the assignment over Gradescope.

3. Do not submit links to files. We will not grade assignments submitted this way as it is easy to change the files after the submission period ends.

1.3 Is collaboration allowed?

Absolutely NOT. No collaboration is allowed for timed labs.

2 Overview

In this timed lab, you will implement a **Binary Encoded State Machine** in CircuitSim, and use k-maps to simplify the circuit logic. This Finite State Machine will take in one 1-bit input (G), and it will output two 1-bit outputs. The state machine is a Moore State Machine, where your output is based solely on the current state. Diagrams and detailed instructions are provided below.

3 Instructions

3.1 State Transition Diagram

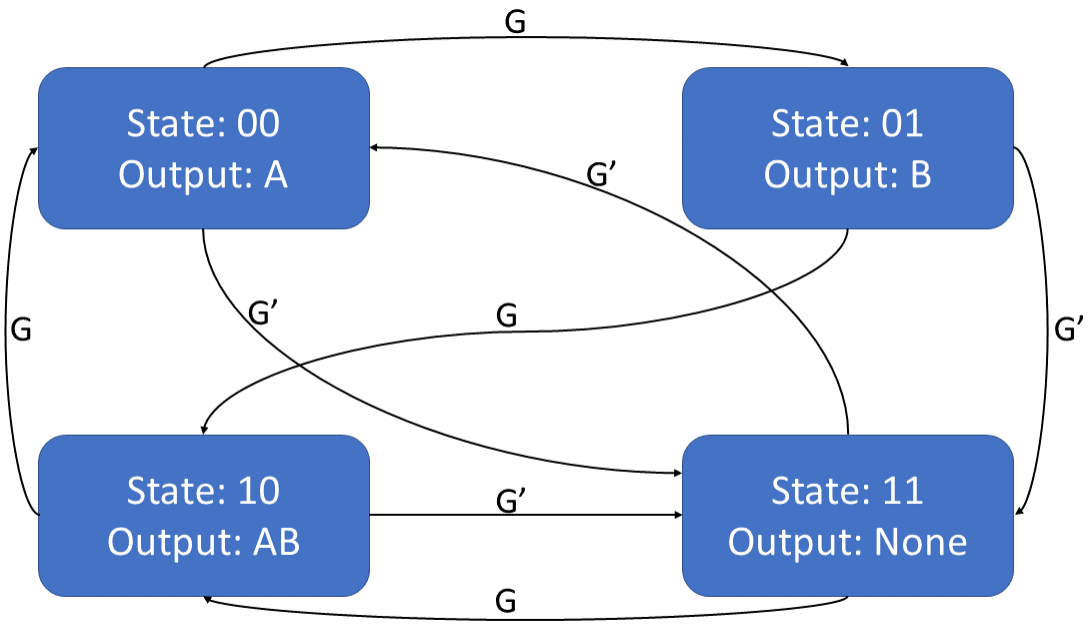

Figure 1: Transition diagram.

3.2 Simplifying the Circuit

To help you to simplify the state machine logic, you are given a excel sheet you can use to construct the truth table and k-maps for the circuit; however, you are not going to submit the excel sheet for grading. Use the k-maps to find the **fully reduced** circuit for the state machine. Non-optimal circuits will not receive full credit.

3.3 Building the Circuit

Build your circuit using the tl2.sim file provided on CircuitSim. Complete the circuit so that the logic matches the diagram above. Functional circuits that are not fully reduced won't receive full credit.

3.4 Restrictions

The input / output pins we have given you in the skeleton file must not be renamed. Do not add any additional input / output pins other than the ones we have given you. Do not rename the sub-circuit we have given you. If you have issues, check out the "Common Errors" section below.
If you have any questions on what you may not use then assume you can't use it and ask a TA.

You are only allowed to use the following components in CircuitSim:

- Basic logic gates (NAND, NOR, AND, OR, NOT)
- Registers (for this assignment, **exactly ONE**).
- Wires, splitters/joiners, tunnels, constants, plexers

You are **not** allowed to use XOR/XNOR

4 Common Errors

Use the autograder's output to determine where you have gone wrong. The names of the tests you fail should usually (but not always) point you in the right direction.
Some common errors and their remedies:

1. Make sure you haven't added extra any input / output pins to your circuit. It is common to confuse constants with input pins, and probes with output pins.
2. Make sure the input / output pins are named the way they were when we gave you the file. If you change the names of the pins (including from upper-case to lower-case, etc), the autograder will not be able to feed input in, and read your circuit's output.
3. Make sure you haven't changed the name of your sub-circuit. Keep it the same as what was given to you.
4. A common cause of short-circuits is two pins (on an AND gate, splitter, etc) being unintentionally connected. These are often hard to spot, since the pins are so close to each other, but if you zoom into your circuit you may find such an error and fix it.
5. Sometimes the bits on your splitter may be not be ordered correctly. For example, if the bits are ordered opposite to what you intended, you may fail all your tests (that depend on the splitter) since for each case, its complementary case is being tested.
6. Make sure the names on your tunnels match. The tunnel labels are case-sensitive, and they do not trim off whitespace. If two tunnels look the same but for some reason they aren't connecting, there may be a "space" hidden in the tunnel's label.

5 Rubric

To run the autograder locally, navigate to the directly containing your timed lab and the tester and run the following command:

```
java -jar tl2-tester.jar
```

The output of the autograder is an approximation of your score on this timed lab. It is a tool provided to students so that you can evaluate how much of the assignment expectations your submission fulfills. However, **we reserve the right to run additional tests, fewer tests, different tests, or change individual tests** - your final score will be determined by your instructors and no guarantee of tester output correlation is given.

6 Deliverables

Please upload the following files to Gradescope:

1. tl2.sim

Download and test your submission to make sure you submitted the right files