Instructor

Hyesoon Kim

Office: KACB 2344
email: hyesoon@cc.gatech.edu
office hours: M/F 12:00-12:30 or by appointment

Teaching Assistants

- All TA office hours are in CoC 104b

Kyle Kelly
Email: kkelly39@gatech.edu
Office Hours: MWF 10-11am
Victor Lee
Email: vlee9@gatech.edu
Office Hours: MF 1:30-3pm
Kim Yie
Email:yiek888@gatech.edu
Office Hours: M 3-4 W 12-1 R 12:30-1:30pm
Dave Kearns
Email: dkearns6@gatech.edu
Office Hours: T 12-1:30 W 1-2:30
Samarth Agarwal
Email: sagarwal62@gatech.edu
Office Hours: MWF 9-10am
Sagar Laud
Email: slaud3@gatech.edu
Office Hours: TR 1:30 PM - 3:00 PM
Brandon Gaudet
Email:bgaudet6@gatech.edu
Office Hours: W 3-6pm
Sai Paladugu
Email: spaladugu3@gatech.edu
Office Hours: MWF 1:00 PM - 2:00 PM

Purpose & Outcomes

Purpose

Provide a broad exposure to computer system structure and networking including software abstractions in operating systems for orchestrating the usage of the computing resources:

Organization of the processor

Memory hierarchy

Storage devices

Parallel processors

Networking hardware

Software abstractions in the operating systems for orchestrating their usage

Networking protocols to connect the computer system to its environment

Outcomes

(Competency Knowledge) Understand the difference between RISC and CISC architectures. Be able to identify the strengths and weaknesses of each paradigm.

(Competency Knowledge) Understand and be able explain runtime system concepts such as procedure calls and register saving. Be able to write recursive subroutines in assembly.

(Competency Application) Understand how a processor is controlled. Given a datapath and an instruction set be able to write the finite state machine steps in a high-level meta language.

(Competency Knowledge) Understand and be able to explain (at a high level) hardware modifications required to implement an interrupt system and to understand the basic concepts required to write an interrupt handler (in assembly language).

(Competency Knowledge) Understand the basic principles of pipelining:

- **Pipelining registers**
- **Potential performance improvements with pipelining**

Pipelining Hazards: Structural, Data and Control

(Competency Knowledge) Understand basic concepts of processor scheduling: Process vs program, PCB, scheduling algorithms (Round Robin, Shortest Job First, First Come First Served, Priority, Multilevel Queues), types of scheduler (short, medium and long term) and context switching.

(Competency Comprehension) Given a set of processes with appropriate parameters show scheduling behavior under different scheduling algorithms.

(Competency Application) Be able to calculate the proper size required for pipeline register and speedups with pipelining.

(Competency Application) Be able to solve basic word problems involving Amdahl's Law.

(Competency Knowledge) Be able to identify and explain how to avoid or minimize the effect of the different types of pipelining hazards.

(Competency Knowledge) Understand the drivers of memory cache designs: Temporal locality, spatial locality and working set. Be able to match the design with the motivator.

(Competency Knowledge) Understand the basic operation of virtual memory and typical components: Page table, virtual pages, physical frames, TLB, page/frame offset, page replacement algorithms (LRU, Random, FCFS, Optimum). Be able to describe the basic operation and identify the necessary subsystems.

(Competency Knowledge) Understand the basic design of typical caches including index, tag, dirty and valid bits as well as multi-word blocks, set-associative and fully associative caches. Given selected design parameters (i.e. word size,

memory available for data)

(Competency Knowledge) Understand basic concepts of parallel processing: UMA (SMP) vs NUMA configurations, multiprocessor cache coherency, network interconnection schemes, threads, mutex, condition variables.

(Accomplishment Application) Be able to write multi-threaded programs using the pthreads package. An example would be a multithreaded producer consumer application.

(Competency Knowledge) Understand basic networking concepts: Ethernet (CSMA/CD), Token Ring, Payload vs. header and trailer, checksums, bandwidth, effective bandwidth, latency, MAC addresses, Network (IP) addresses, protocol stacks, TCP/IP, routing, hubs/repeaters, bridges, VLANS, routers.

(Competency Knowledge) Understand fundamentals of I/O devices such as polling versus interrupts, memory mapped I/O, device registers (data, control and status), disk memory concepts (sectors, tracks, platters, cylinders, seek time, rotational latency), disk scheduling algorithms (FCFS, SSTF, scan, c-scan, look, c-look)

(Accomplishment Synthesis) Write and debug medium sized C programs that simulate various of the above subsystems (interrupt enabled processor, virtual memory, multi-threaded operating system schedulers, reliable transport layer protocol which will be examples of operating-system-like coding.

Textbooks

* Wireless PRS Unit.

* Textbook

Ramachandran & Leahy

Computer Systems: An Integrated Approach to Architecture and Operating SystemsPublisher: PEARSON

ISBN: 9780321486134

*** Logisim**

Course Rules

CS 2200 Rules and Regulations

1. You are responsible for turning in assignments on time. This includes allowing for unforeseen circumstances. You are also responsible for insuring that what you turned in is what you meant to turn in. T-Square includes a "retrieve" feature: This allows you to retrieve exactly what you submitted and insure that it works. Take advantage of this feature.

2. In general, programming assignments should be turned in with a Makefile and all files needed to compile and run the program. The TA grading your submission should be able to make and run your program without adding files, repairing things etc. This supersedes all instructions in the project or homework files. If you do not turn in files that we can run, you will lose 20 * the homework/project number.

3. Demos are required from Projects 1-4. Demo times are to be signed up with TAs via T-Square. If you cannot attend one of the predetermined slots, e-mail the Head TA to set up another time slot. You must contact the Head TA before the demos for that project end. If you sign up for a demo and miss it without a valid excuse you will get 50% of the points off. Speeding tickets, sleeping late, etc are NOT valid excuses. If you know you are going to miss a demo ahead of time, remove your name from the list and email the TA you are supposed to demo with about why you are missing the time. After that, you may sign up again or arrange another time with the Head TA.

4. Tests and examinations must be taken at the scheduled date and time. Please do not ask for special treatment because you (or your parents) have purchased non-refundable airline tickets. The safe time to travel is at the end of or after finals week. The finals schedule published at the beginning of the semester is TENTATIVE. The official schedule gets published very late in the semester.

5. The deadline for re-grades is 2 weeks after an assignment grade is posted or returned to you. This deadline also applies to picking up items that are returned in class. After this deadline no grade changes will be made and tests not picked up will be destroyed.

6. The T-Square announcements should be read every day. Official announcements about course matters will be posted there. The general course forum is for posting technical questions about assignments, tests etc. Complaints, questions about your personal problems, etc. should be discussed with your instructor in person or via email.

7. If you have any major personal problems (family/illness/etc.) please go to the Dean of Student's office located in the Student Services Building (Flag Building) next to the Student Center. She is equipped and authorized to verify the problems and she will issue a note to all your instructors making them aware of the problem and requesting whatever extension, etc. is necessary.

8. If you need a certain grade in order to stay in school, maintain a scholarship, etc. the time to worry about this is right from the beginning of the course not during the week before finals. Grades are based on demonstrated performance not individual need based on factors external to the course. Please do not request special consideration based on this type of situation.

9. Final grades will be available from OSCAR normally sometime the week after finals. You may review your final and discuss your grades during the following semester in which you are attending Ga Tech. Grades will not be discussed over

break.

10. Out of consideration to your fellow students please turn off cell phones, beepers, wristwatch alarms, etc. Also, make every effort to be on time for class. If you unavoidably late, please sit near the back and try to avoid as much disruption to the class as possible.

11. If you are graduating and need this course to do so please inform your instructor as soon as possible.

12. Complaints about TAs should be directed to the course instructors during office hours or via email.

13. Please be courteous in your correspondence with TAs and instructor.

Projects Grading Criteria

1. Student submits project as his/her own (this is what is expected of the students):

- We will grade the project (out of 100%) as their own submission

- Use 0 to 1 multiplier from oral to assess final grade

Note: discussion among the students on how to do the project through piazza and other means are encouraged. HOWEVER, THE CODING OF THE PROJECT HAS TO BE DONE INDIVIDUALLY FOR FULL CREDIT. ZERO TOLERANCE FOR PLAGIARISM (SEE next item).

2. Student submits project as his/her own:

- The TAs determine the project is plagiarized. TRUST US, IT IS REAL EASY TO DETERMINE THIS….

- The projects get a ZERO and all the colluders are reported directly to the dean of students

3. Student says at the time of submission he/she obtained the project from a peer just to learn though he/she did not do any coding themselves (the student should show that he/she has obtained such permission from the peer)

- The TAs will grade their knowledge of the project through the oral interview on a scale of 0 to 25% (MAX)

CS2200 Assignment Instructions

The following list is designed to help you submit assignments that can be effectively graded giving you the best possible results.

1. ALWAYS retrieve your files from T-Square and check that what you turned in is what you intended to turn in. NO EXCEPTIONS.

2. If you have any problems submitting, email your grading TA what you would have submitted BEFORE the deadline for the assignment.

3. Homework and Project Assignments may be worked on collaboratively.

4. Tests and Project demos are individual efforts.

5. Submit text as plain ascii text. Do NOT submit word/wordstar/excel/123/dbase2/etc. files.

6. For written (as opposed to code) submissions: Only submit the answers (properly numbered). Do not submit the questions.

7. Wrap text to 80 characters of less.

8. Put your name and prism ID number at the top of each file (if code, as a comment)

9. Coding guidelines

a. You must provide a Makefile that compiles and links your code by default.

b. Your code must compile with gcc on the States Lab Machines. If your code does not compile you will get a zero for the assignment.

c. You will be penalized if your code produces warnings when compiled with the following flags: -Wall -pedantic -O2

d. You must turn in ALL files that are used to build your executable, including the files which we provide you - no matter what make submit returns or what the assignment says.

e. Code should be well commented and use a clean, consistent (readable) style i.e. proper indenting, etc.

10. Failure to follow these guidelines will make you lose 20*project/homework number or a zero where appropriate. Please be careful when submitting assignments and double check each one! Ask a TA if you are unsure on the procedure.

Prerequisites

CS2110 or ECE 2030 & CS2130

Examinations

PLEASE CHECK "Schedule" under Resources Course tools

Grade Breakdown

*** Participation (Turning Tech Response + Class interaction) 5%**

*** Projects (weighted equally) 25%**

*** Homeworks 10%**

*** Tests 40%**

*** Final Exam 20%**

*** Total 100%**

Week	Date	Day	Lec. #	Subject	Reading	Assignments Release	Due	Recitation Help
1	1/6/14	M	1	introduction	Chap 1			
		W	2	preassesment/processors	Chap 2			
		F	3	processors	Chap 2	HW1		
2	1/13/14	M	4	processors	Chap 2			
		W	5	processors	Chap 2			HW1 review
		F	6	datapath	Chap 3	P1: processors		
3	1/20/14	M		School Holiday				
		W	7	datapath	Chap 3			P1 review/HW1QA
		F	8	datapath	Chap 3	HW2		
4	1/27/14	M	9	interrupts	Chap 4		HW1	
		W	10	interrupts	Chap 4			HW2 review/P1QA
		F	11	performance/pipelining	Chap 5			
5	2/3/14	M	12	pipelining	Chap 5		P1	
		W	13	pipelining	Chap 5			Hw2 QA
		F	14	pipelining	Chap 5	P2: interrupts		
6	2/10/14	M	15	pipelining	Chap 5		HW2	
		W	16	Test-1				P2 review
		F	17	pipelining	Chap 6	HW3		
7	2/17/14	M	18	process scheduling	Chap 6			
		W	19	process scheduling	Chap 6			HW3 review/P2 QA
		F	20	process scheduling	Chap 6	P3:VM		
8	2/24/14	M	21	memory management	Chap 7&8		P2	
		W	22	memory management	Chap 7&8			P3 review/P2 QA
		F	23	memory management	Chap 7&8	HW4		
9	3/3/14	M	24	memory hierarchy	Chap 9	EC	HW3	
		W	25	memory hierarchy	Chap 9			HW4 review/P3 QA
		F	26	memory hiearchy	Chap 9	P4:MTOS		
10	3/10/14	M	27	parallel systesms	Chap 12		P3	
		W	28	parallel systems	Chap 12			P4 reivew/HW4 QA
		F	29	parallel systems	Chap 12	HW5		
11	3/17/14	M		School Holiday				
		W		School Holiday				
		F		Schoool Holiday				
12	3/24/14	M	30	parallel systems	Chap 12		HW4	
		W	31	parallel systems	Chap 12			HW5 review
		F	32	I/O	Chap 10			
13	3/31/14	M	33	networking	Cahp 13			
		W	34	Test-2				P4 QA
		F	35	networking	Chap 13	P5:Networking		
14	4/7/14	M	36	networking	Chap 13		P4	
		W	37	networking	Chap 13			P5 reivew/HW5 QA
		F	38	networking	Chap 13		EC	
15	4/14/14	M	39	networking	Chap 13		HW5	
		W	40	disk scheduling	Chap 10			P5 QA
		F	41	file systems	Chap 11			
16	4/21/14	M	42	file systems	Chap 11		P5	
		W	43	file systems	Chap 11			QA
		F	44	Review				
17	4/28/14	M		Final Exam (8-10:50 AM)				