

# **ECE3150 Course Syllabus**

## **ECE3150**

### **VLSI and Advanced Digital Design (3-0-3-4)**

#### **CMPE Degree**

This course is Elective for the CMPE degree.

#### **EE Degree**

This course is Elective for the EE degree.

#### **Lab Hours**

3 supervised lab hours and 0 unsupervised lab hours

#### **Prerequisites**

ECE 2031 [min C] and ECE 2040 [min C]

#### **Corequisites**

None

#### **Catalog Description**

Advanced digital design issues in the context of VLSI systems. Introduction to a design methodology that encompasses the range from architectural models to circuit simulation.

#### **Textbook(s)**

Wolf, *Modern VLSI Design: IP-Based Design* (4th edition), Prentice Hall, 2008. ISBN 0137145004, ISBN 978-0137145003 (required)

Sutherland, Sproull & Harris, *Logical Effort: Designing Fast CMOS Circuits*, Morgan Kaufmann, 1999. ISBN 1558605576, ISBN 978-1558605572 (required)

#### **Course Outcomes**

Upon successful completion of this course, students should be able to:

1. demonstrate a clear understanding of important concepts in CMOS technology and fabrication that affect design.
2. design a gate of any given arbitrary logic function at the transistor-level.
3. layout a gate in CMOS VLSI technology.
4. size the gates of the given VLSI layout to minimize the delay.
5. design a network of complex gates with the ideal number of stages that computes the function with minimum delay.
6. simulate a VLSI design in SPICE to obtain delay and power performance measures.
7. find a test vector to test given faults in a logic network.
8. design and characterize synchronized circuits for asynchronous external inputs.
9. design and layout a variety of adders and multipliers.
10. analyze and simulate interconnect delay.
11. design and layout a datapath that consists of various functional, memory, communication, and interface units.
12. understand system issues such as floorplanning and power/ground distribution

#### **Student Outcomes**

In the parentheses for each Student Outcome:

"P" for primary indicates the outcome is a major focus of the entire course.

"M" for moderate indicates the outcome is the focus of at least one component of the course, but not majority of course material.

"LN" for "little to none" indicates that the course does not contribute significantly to this outcome.

1. ( P ) An ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics
2. ( LN ) An ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors
3. ( LN ) An ability to communicate effectively with a range of audiences
4. ( LN ) An ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts
5. ( LN ) An ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives
6. ( M ) An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions
7. ( M ) An ability to acquire and apply new knowledge as needed, using appropriate learning strategies.

### Topical Outline

1. Design Methodology (1 week)
2. Switches and Layout (3 weeks)
  - a. Switch based design
  - b. Complex gates
  - c. Layout and technology
  - d. Registers
  - e. Adders
3. Circuit design issues (4 weeks)
  - a. MOSFET models
  - b. Delay models
  - c. Hazards, metastability, synchronization
  - d. Alternate logic structures
  - e. Timing and clocking
  - f. Power models
  - g. Sleep transistors
4. Advanced digital issues (3 weeks)
  - a. Logical effort
  - b. Ideal number of stages
  - c. Asymmetric gates
  - d. Calibrating the model
  - e. Branches and Interconnect
5. Test Logic (1 week)
  - a. Combinational test
  - b. Sequential test
  - c. Scan design
6. Advanced Modules (2 weeks)
  - a. ROM, PLA
  - b. Advanced adders
  - c. Multipliers

- d. Barrel shifter
- e. Decoders