MICROELECTRONICS SYSTEM PACKAGING
Introduction to SOP, SOC, SIP, 3D ICs and 3D Systems

AN INTERDISCIPLINARY ELECTRONIC SYSTEM PERSPECTIVE
ECE/ME/MSE 6776
FALL 2016

CLASS HOURS	Tuesday / Thursday, 12:05 p.m. – 1:25 p.m. Instructional Center (Instr Ctr) #217	
CREDIT	3 Hours	
PREREQUISITES	Introductory packaging course including EE4058 or the consent of an instructor	
INSTRUCTOR	Prof. Rao R. Tummala, Petit Chair Professor, ECE and MSE	
EXPERTS	Prof. G.K. Chang, ECE Prof. Joungho Kim, KAIST University Prof. Suresh Sitaraman, ME Prof. Klaus Wolter, ECE Dr. Beth Keser, Qualcomm Dr. P.M. Raj, MSE, ECE Dr. Sesh Ramaswami, Applied Materials Dr. Himani Sharma, CHEM Dr. Vanessa Smet, EE Dr. Venky Sundaram, MSE, ECE Dr. Melinda Varga, ECE Mr. Chris White, ECE	
TEACHING ASSISTANT	Mr. Ninad Shahane MaRC 156 Office Hours Thursday, 2:30 p.m. – 3:30 p.m. ninad.shahane@gatech.edu	Mr. Zihan Wu MaRC 342 Office Hours Thursday, 10:00 a.m. – 11:00 a.m. zwu77@gatech.edu
PROF. TUMMALA'S ASSISTANT	Ms. Karen May MaRC 351 karen.may@ece.gatech.edu 404 385-1220	
TEXT BOOKS	• "Fundamentals of Microsystems Packaging," McGraw Hill, Tummala, 2001 • "Introduction to System-On-Package (SOP), McGraw-Hill," Tummala and Swaminathan, 2008	
COURSE OVERVIEW	This is a system level overview and a cross-disciplinary microsystems packaging course that introduces the new and advanced systems packaging technology concepts that have been explored and developed during the last decade for highly-miniaturized convergent electronic and bio-electronic systems for smart consumer, computer, telecom, wireless, healthcare and automotive systems. The course integrates various disciplines including electrical, materials, chemical, mechanical and bio- engineering to form the basis of new concepts that include SOP, SIP, 3DICs and 3D Systems. Within SOP and 3D Systems, it introduces digital, RF, optical and thermal SOP technologies. This course is intended for graduate students in ECE, ME, MSE, ChemE, Physics and Chemistry. It provides both fundamental and applied aspects of digital and bio-convergent system technologies based on 15 years of intense research advances at the Microsystems Packaging Research Center at Georgia Tech by 35	

	faculty, 500 graduate students and more than 100 electronic companies. This course will be taught by multiple faculty and some industry experts in their area of expertise.
COURSE FORMAT	1. Lectures 2. Invited Presentations 3. Student Team Term Papers
COURSE OBJECTIVES	• Provide a system level perspective with an overview of all system technologies and their applications. • Explain what is meant by SOP, SOC, SOB, SIP, MCM, 3D ICs and 3D Systems and why miniaturize components and systems. • Explain two basic laws: Moore's Law for transistor scaling ICs and Systems scaling for Systems • Explain, compare and contrast the 7 key microsystems technologies: SOB, SOC, MCM, SIP, 3D, SOP, and 3D Systems • Explain the implications of SOP and 3D technologies for digital convergence. • Explain the role of such disciplines as ECE, ME, ChE, MSE in SOP R&D & Manufacturing, as well as in job careers in the industry. • Focus on and review SOP technologies: Mixed signal design, Digital SOP, Thermal SOP, RF SOP, MEMS SOP, Opto SOP, Bio SOP, WL SOP each involving organic or inorganic substrates thin film components, interconnections at IC and system level, and their reliability. • Explain future of SOP, such all-Si based 3D ASSM, as a potential disruptive technology. • Prepare students for industry culture by team work, interdisciplinary, selection of an R&D topic to write and present a term paper with individual contributions

GRADING	• Short quiz: 10%
	• Mid-term exam: 25% including specific problems
	• One page summary of 2 chapters: 20%
	• Attendance: 10%
	• Final exam: 35%
	  ○ Individual oral presentation: 15%
	  ○ Term paper: 20%

Fall 2016 6776 CLASS SCHEDULE

TUESDAY / THURSDAY, 12:05 P.M. – 1:25 P.M., Instr Ctr 217

Date	Class Topic	Instructor	Special Notes
August			
Tues – 23	1. Introduction to ECE 6776 Class	Tummala	
Thurs – 25	2. What is Packaging and Why? A. Overview	Tummala	
Tues – 30	B. Three Types of Packaging and Their Value-add	Tummala	
September			
Thurs – 1	C. System Scaling for all Electronic Systems	Tummala	
Tues – 6	D. SOC – Its Evolution and Its Future	Tummala	
Thurs – 8	3. Design A. Electrical Design for Signal Design	Wolter	
Tues – 13	B. Electrical Design for RF, 5G and mm-Wave	Tentzeris	Chpt. Summary #1 Due
Thurs – 15	C. Thermal Design and Technologies	Joshi	
Tues – 20	D. Mechanical Design	Sitaraman	Short In-Class Quiz
Thurs – 22	4. Packaging Materials A. Materials and Properties	Sharma	
Tues – 27	B. Nanopackaging and Future Materials	Sharma	
Thurs – 29	C. High temperature Materials for Automotive	Pulugurtha	
October			
Tues – 4	5. Packaging Technologies A. Substrate Technologies – Ceramic, Organic, Silicon and Glass	Sundaram	
Thurs – 6	B. 3D ICs with TSV	Sesh Ramaswami, Guest Lecturer AMAT	
Tues – 11	**Fall Break – No Class**		
Thurs – 13	C. Stacked ICs and Packages (SIP)	Tummala	
Tues – 18	D. 2.5D Interposers –Glass vs. Si vs. Organic Interposers	Sundaram	Chpt. Summary #2 Due
Thurs – 20	E. 3D System Package – A Fundamental Concept	Tummala	
Tues – 25	F. Embedded Components: Chip-First, Chip-Last	Beth Keser Guest Lecturer Qualcomm	
Thurs – 27	6. Components A. RF Components and Modules	Pulugurtha	Midterm Exam Given Out
November			
Tues – 1	B. Power Components and Modules	Pulugurtha	
Thurs – 3	7. Optical Electronics	Chang	
Tues – 8	Packaging Technologies, cont'd G. Logic-to-Memory for Bandwidth	Prof. Joungho Kim Guest Lecturer KAIST	Midterm Exam Due
Thurs – 10	8. Automotive Electronics A. Sensing Electronics	Wolter	
Tues – 15	B. High-power Electronics for Automotive	Smet	

Thurs – 17	9. Bioelectronics	Varga	
Tues – 22	10. Term Paper Topics and Discussion 11. Interconnections and Assembly A. Chip-level	Tummala Smet	
Thurs – 24	**Official School Holiday – Thanksgiving – No Class**		
Tues – 29	B. Board-level	Smet	
December			
Thurs – 1	12. Comparison of System Technologies and Course Wrap-up	Wolter	
Tues – 6	13. Term Papers Team Presentations	Tummala	
Thurs – 8	14. Lab Tours	White	
Sun - 11	15. Term Papers Due – Submit Online	Shahane / May	

ECE / ME / MSE 6776 INSTRUCTOR BIOGRAPHIES

Prof. Rao Tummala	Professor Rao Tummala holds the Joseph M. Pettit Chair in Electronics Packaging in the School of Electrical and Computer Engineering and holds a joint faculty appointment in the School of Materials Science and Engineering at Georgia Tech. He is also the Founding Director of the first NSF Engineering Research Center (ERC) at GT called the Microsystems Packaging Research Center (PRC) pioneering the Second Law of Electronics (the first being Moore's Law) by his System-On-Package (SOP) vision. The PRC is currently the largest and most comprehensive microsystems packaging research, education and industry collaboration Center involving on the average about 100-200 graduate students and 15-30 faculty from ECE, ME, ChBE and MSE departments, collaborating with 70 global companies from the U.S., Europe, Japan, Korea, India, China and Morocco. He is also a Georgia Research Alliance Eminent Scholar. Prof. Tummala may be contacted at rao.tummala@ece.gatech.edu.
Prof. G.K. Chang	Professor Chang received his bachelor's degree in physics from National Tsinghua University in Taiwan and his doctoral degree from the University of California, Riverside. Professor Chang expertise in in the areas of optoelectronic devices, high speed integrated circuits, telecommunication switching components and systems, WDM optical networking systems and networks, optical network security, optical label switching and optical interconnect technologies, TDM- and WDM-PONs, and radio-over-fiber and wireless-over-fiber systems and networks. He has been an active contributor to many IEEE Photonics Society. Optical Society of America (OSA) sponsored journals, conferences, and committees. He is a pioneer and champion of broadband wireless over fiber technologies for convergence of wireless and optical access networks that provides high bandwidth, high capacity, and mobile access to future Internet users. Prof. Change may be contacted at geekung.chang@ece.gatech.edu.
Prof. Joungho Kim	Dr. Joungho Kim is currently professor at electrical engineering department of KAIST. Also, he is director of 3DIC-RC (3DIC Research Center) supported by SK Hynix Inc, and SAE-RC (Smart Automotive Electronics Research Center) supported by KET Inc. Since joining KAIST, his research centers on EMC modeling, design, and measurement methodologies of 3D IC, TSV, Interposer, System-in-Package, multi-layer PCB, and wireless power transfer (WPT) technologies. Especially, his major research topic is focused on chip-package-PCB co-design and co-simulation for signal integrity, power integrity, ground integrity, timing integrity, and radiated emission in 3D IC, TSV and Interposer. He has authored and co-authored over 440 technical papers published at refereed journals and conference proceedings. Also, he has given more than 242 invited talks and tutorials at the academia and the related industries. Prof. Kim may be contacted at joungho@kaist.ac.kr.
Prof. Suresh Sitaraman	Professor Sitaraman's research is in the areas of micro- and nano-scale structure fabrication, characterization, physics-based modeling and reliable design. His micro- and nano-scale research focuses on a wide range of application areas such as aerospace and defense, automotive, computers and telecommunications, portable electronics, and medical. In particular, his research is developing micro-scale and nano-scale structures that can be used as compliant packaging interconnects. Dr. Sitaraman's research also aims to understand the long-term reliability of lead-based and lead-free solder interconnects through thermo-mechanical modeling, material microstructure evolution, reliability experiments, and laser moire interferometry. In parallel, Dr. Sitaraman's research focuses on the next-generation integrated substrates that have high-density interconnects and microvias, embedded passives, and optoelectronic waveguides. In particular, Dr. Sitarman's group has done work in material length scale effects for microvia reliability, cure kinetics and interlayer dielectric cracking and delamination, reliability modeling and experiments for embedded passives and optical waveguides. Visit www.me.gatech.edu/caspar for more information about his research. Prof. Sitaraman may be contacted at suresh.sitaraman@me.gatech.edu.
Prof. Klaus Wolter	Prof. Klaus Wolter is Associate Director of the PRC at Georgia Tech. His previous academic

	experience was at Dresden University of Technology where he was Senior Professor of the Electronic Packaging Lab. Prof. Wolter received his M.SC in Electrical Engineering as well as Dr.-Ing. (PhD) and Dr.-Ing. Habil. at TU Dresden. His research focus is on system integration in electronics, electronics materials, substrate technologies, assembly and interconnect technologies, reliability, and non-destructive testing. Prof. Wolter has co-authored four books in Electronics Packaging, and was Editor of three book series. His research activities have resulted in more than 90 conference presentations/proceedings and 13 patents. At the PRC, he is heading up the Automotive Electronics Global Industry Consortium. Prof. Wolter may be contacted at klaus.wolter@ece.gatech.edu.
Dr. Beth Keser	Dr. Beth Keser, a recognized global leader in the semiconductor packaging industry with over 17 years of experience, received her B.S. degree in Materials Science and Engineering from Cornell University and her Ph.D. from the University of Illinois at Urbana-Champaign. Beth's excellence in developing revolutionary electronic packages for semiconductor devices has resulted in 8 patents, 17 patents pending, and over 40 publications in the semiconductor industry. Based in San Diego, Beth leads the Fan-Out Packaging, both chips first and chips last, Technology initiative at Qualcomm. Earlier in her tenure at Qualcomm, Beth's team qualified over 50 products resulting in over 6 billion units shipped-technology consumers around the world enjoy in cell phones today. Beth is also an IEEE CPMT Distinguished Lecturer. Dr. Keser may be contacted at bkeser@qti.qualcomm.com.
Dr. P.M. Raj	Dr. P. Markondeya Raj is a Senior Research Scientist and Program Manager for the Passives and their Integration with Actives program at the PRC. He received his PhD from Rutgers University in 1999 in ceramic engineering, ME from the Indian Institute of Science, Bangalore and BS from the Indian Institute of Technology, Kanpur (1993). His research expertise spans from functional thin film components (capacitors, antennas, inductors), MEMS components, interconnections, packaging substrates, device and system integration. He managed and led several government and industry funded programs in these areas. He coauthored 3 book chapters and 120 publications, received 3 patents with several pending. He received 7 "Best Paper" awards for his conference and journal publications which include the "Distinguished Scholar Award" from the Microbeam Analysis Society, IEEE Transactions of Advanced Packaging Commendable paper Award, IEEE Outstanding Technical Paper Award and the Philips Best Paper Award. Dr. Raj may be contacted at raj.pulugurtha@ece.gatech.edu.
Dr. Sesh Ramaswami	Sesh Ramaswami is Sr. Director, Strategy in the Silicon Systems Group at Applied Materials. In this capacity, his responsibilities include program definition and execution, defining and driving external collaboration and co-leading internal process integration programs for Through-Silicon-Via (TSV) within the wider context of wafer level processing for advanced packaging. He is a co-author and contributor of a book recently published, entitled 3D IC Stacking Technology. Sesh has over 25 years of semiconductor industry experience. Over the past 16 years at Applied Materials, he has had varied technical contributions and business experience in product management, product development and advanced materials development. Prior to joining Applied Materials in 1994, Sesh had thin film process development responsibilities for seven years at Advanced Micro Devices and four years at National Semiconductor. A holder of 35 US patents and several publications, Sesh has undergraduate and graduate degrees in Chemical Engineering from Indian Institute of Technology, Kanpur, and Syracuse University respectively and a MBA. Dr. Ramaswami may be contacted at Sesh_Ramaswami@amat.com.

Dr. Himani Sharma	Dr. Himani Sharma received her B.S. (2000), M.S. (2002) and Ph.D. degree in Chemistry (2006) from University of Delhi, India. She worked as a research associate in Electrical Engineering department in Alabama A&M University on NSA-funded project, before joining Georgia Institute of Technology as a Postdoctoral Fellow. Her research focuses on developing materials for next-generation electronics and packaging. She has authored more than 30 publications in international peer-reviewed journals and conferences. She has co-authored 1 book and another book-chapter and 1 pending patent. She has been awarded Best Poster Award for her recent work on high density capacitors in 2012 IEEE-Electronic Component and Technology conference. Dr. Sharma may be contacted at himani.sharma@ece.gatech.edu.
Dr. Vanessa Smet	Vanessa is a Research Scientist and Program Manager for Interconnections and Assembly Program at the PRC, focusing on ultra-fine pitch first-level interconnections and MEMS packaging. She received her PhD from University of Montpellier 2, France, in 2010 in electrical engineering (reliability assessment of power modules), BS and MS in applied physics from the ENS Cachan & University of Paris XI, France, in 2007 and 2004, respectively. She was a postdoctoral researcher in Tyndall National Institute, Ireland (2010-2012), working on novel high-temperature high-power die-attachment solutions for power chips and µBGA assembly. Her research interests include power electronics, thermomechanical modeling, 3D integration, interconnections, assembly processes (flip-chip, thermo-compression, SLID) and MEMS packaging. Her work has been presented and publishes in international conferences and high impact-factor journals. Dr. Smet may be contacted at vanessa.smet@prc.gatech.edu.
Dr. Venky Sundaram	Venky Sundaram is the Associate Director of Industry Programs at PRC, Georgia Tech and also serves as Program Manager for the Glass Package Consortium. He has been with the PRC since 1997 focusing on System on a Package (SOP) technology, ultra-high density substrates and systems integration research. He is a globally recognized expert on 3D packaging, substrates and interposers. He is currently serving as the chair of the IEEE CPMT Technical Committee of High Density Substrates, and as the Director of Student Programs on the Executive Council of IMAPS. Venky is a co-founder of Jacket Micro Devices, an RF substrate and module Georgia Tech PRC Spin-off Company acquired by AVX. He received BS in Metallurgical Engineering from IIT Mumbai, and MS and PhD in Materials Science and Engineering from Georgia Tech. He has several US and international patents and has more than 100 publications in the systems packaging technology. Dr. Sundaram may be contacted at vs24@mail.gatech.edu.
Dr. Melinda Varga	Melinda Varga is a Research Scientist and a Program Manager for Bioelectronics at PRC. Her research focus is biocompatible electronic packaging, embedding and encapsulation for medical devices, implantable devices, especially orthopedic implants, design and fabrication of neural electrodes and integration of electronic components and sensors into biomedical systems. She received her PhD and M.Sc. from the University of Technology Dresden, Germany in 2011 and 2006, respectively. Before joining Georgia Tech PRC, she worked as a postdoctoral fellow for four years at the Electronic Packaging Laboratory of TU Dresden, one of the largest university research institutions in Germany active in the field of Electronic Packaging. Dr. Varga may be contacted at melinda.varga@ece.gatech.edu
Mr. Chris White	Chris White is the Laboratory Coordinator at the PRC, and also provides Packaging Support for the Institute for Electronics and Nanotechnology (IEN). He has been with the PRC since 2009 focusing on Assembly support and Laboratory Infrastructure. He received his BS in Electrical Engineering from Georgia Tech. Mr. White may be contacted at chris.white@ece.gatech.edu.