# ECE-3057: ~~Architecture, Concurrency, and Energy in Computation~~ Architecture, Systems, Concurrency and Energy in Computation

## Summary

This course introduces the basic organizational principles of the major components of a processor – the core, memory hierarchy, and the I/O subsystem and basic operating system constructs that utilize them. Students also gain an understanding of the sources of performance and energy dissipation in modern processors and learn the multiple forms and levels of parallelism that have been employed to sustain performance improvements in the industry. Assignments using architecture-level simulators enable the students to explore the operation and tradeoffs in performance and energy and reinforce the concepts learned in the classroom. Students also implement assignments that implement basic components of the operating system.

Prerequisites: ECE 2035, ECE 2031

**Textbook(s):**
Patterson & Hennessey, *Computer Organization & Design: The Hardware/Software Interface* (4th edition), Morgan Kaufmann, 2008. (required)

Operating Systems(?): TBD (required)  **(Currently covered through lecture notes)**

**Course Objectives** - As part of this course, students:
1. Understand the organizational principles of modern computer architecture related to cores, memory, and input/output subsystems
2. Acquire an in depth understanding of the concept of an instruction set architecture and its implications for software and hardware implementations
3. Understand fundamentals of concurrent execution and requirements for hardware and software implementation
4. Understand the sources, models, and impact of energy dissipation in modern computing systems
5. Learn common techniques for improving metrics such as performance and energy
6. Are exposed to case studies
7. Gain experience in simulating processor architectures and memory systems and learn to use such simulators to understand the operation of hardware, software, and their interactions
8. Understand the role of operating systems in managing processor resources for executing processes and multithreaded programs.
9. Learn basic synchronization, memory management, and scheduling techniques
10. Learn the basic HW/SW management principles of I/O

**Course Outcomes** - Upon successful completion of this course, students should be able to have the following capabilities.
1. Evaluate the cycles per instruction (CPI) for multi-cycle and pipelined data paths.
2. Schedule machine-instruction-level programs on a pipelined datapath with and without hazard handling.
3. Define different types of data and control dependences and describe multiple methods of handling them.
4. Understand the hardware organization and behavior of cache memories of different sizes and associativity.

5. Know the basic elements of scheduling and how they are used in the OS.
6. Define and understand virtual memory, including the concepts of paging, TLB, and page table.
7. Define and distinguish between basic I/O mechanisms such as polling, DMA, interrupts. Enumerate the basic techniques of support within an operating system
8. Understand the operation of storage devices and network interfaces and how they are managed (OS)
9. Define and distinguish between various forms of parallelism: instruction level parallelism (ILP), thread level parallelism (TLP), and data level parallelism (DLP)
10. Perform a performance/energy analysis of data paths and the memory system

## Topical Coverage
1. Architecture
   - Instruction set architectures
   - Multicycle and pipelined datapaths
   - Branch Prediction and concepts of speculation
   - Caches, Virtual Memory and the memory hierarchy
2. Concurrency
   - Instruction Level Parallelism (ILP), Data Level Parallelism (DLP), Thread Level Parallelism (TLP) basics and introduction to Processes
3. Exceptions, Interrupts, and I/O
4. Energy & Power:
   - Basics of energy dissipation: dynamic and static
   - Microarchitecture power models

## Topical Outline:
1. Instruction Set Architectures
   a. Instructions, addressing modes, and sample ISAs
   b. Multi-cycle data path and control
   c. Controller implementation: state machine vs. microprogramming
2. Pipelining
   a. Pipelining basics
   b. Pipeline stages: fetch, decode, execute, memory write-back
   c. Hazards and solutions
   d. Branch prediction and delayed branches
3. Memory Systems
   a. Basic organization of caches and main memory
   b. Virtual memory basics, memory management including OS level management algorithms
4. Concurrency
   a. Basics of Processes and threads: state and architecture execution model
   b. Synchronization primitives: architecture implementation and OS usage models
   c. ILP, DLP, TLP
   d. Introduction the concept of data coherence
5. Energy and Power dissipation
   a. Dynamic and static energy dissipation fundamentals
   b. Microarchitecture-level energy dissipation and power models
   c. Power virus, kernel benchmarks and power
   d. Basics of voltage and frequency scaling
6. I/O Architectures & Operating System Support
   a. Buses and interconnects
   b. Interrupts, DMA, polling
   c. Disk structures, I/O scheduling

       d.   LANs, network interfaces, & basic interprocessor communication
7. ==Process Management==
       a.   ==Processes, threads, and CPU scheduling==
       b.   ==Deadlocks, protection, and security==

## Laboratory Assignments

Candidates Assignments: roughly every two weeks starting week 2/3
1. Datapath Implementation - 1
2. Datapath Implementation  - 2
3. Energy-Power
4. ==OS-Arch: Memory Systems==
5. ==OS: Scheduling==
6. ==OS: Network Stack==

## Grading

| Lab Assignments | 30% |
|---|---|
| Quizzes | 45% |
| Final | 25% |
| Total | 100% |

**Attendance:**

Students are responsible for all material covered in class, including changes in exam schedules announced in class. There will be no make-up exams. In case you have to miss an exam, please inform the instructor of the absence prior to the exam date.

**Honor Code:**

Students are expected to abide by the Georgia Tech Academic Honor Code. Honest and ethical behavior is expected at all times. All incidents of suspected dishonesty will be reported to and handled by the office of student affairs. You will have to do all assignments individually unless explicitly told otherwise. You may discuss with classmates but you may not copy any solution (or any part of a solution).

**Learning Accommodations:**
If needed, we will make classroom accommodations for students with documented disabilities. These accommodations must be arranged in advance and in accordance with the Office of Disability Services (http://disabilityservices.gatech.edu).