ECE4273 Course Syllabus

ECE4273

Design Synthesis of Application-Specific Signal Processors (2-3-3)

CMPE Degree
This course is Elective for the CMPE degree.

EE Degree
This course is Elective for the EE degree.

Course Coordinator
Madisetti,Vijay K

Prerequisites
ECE 4270

Corequisites
None

Catalog Description
Fundamentals of theory and practice of DSP chip design in VHDL. Exposure to tools and environments for chip design, simulation, and verification.

Textbook(s)
Meyer-Baese, Uwe, *Digital Signal Processing with Programmable Gate Arrays* (3rd edition), Springer, 2008. ISBN 9783540726128 (required)

Student Outcomes
In the parentheses for each Student Outcome:
"P" for primary indicates the outcome is a major focus of the entire course.
“M” for moderate indicates the outcome is the focus of at least one component of the course, but not majority of course material.
“LN” for “little to none” indicates that the course does not contribute significantly to this outcome.

1. (LN) An ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics
2. (LN) An ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors
3. (LN) An ability to communicate effectively with a range of audiences
4. (LN) An ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts
5. (LN) An ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives
6. (LN) An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions

7. (LN) An ability to acquire and apply new knowledge as needed, using appropriate learning strategies.

Topical Outline

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[6 hours]   Introduction to DSP processors and ASICs
                Transformational and Reactive Systems
                Characersitics of DSP applications
                Characteristics of DSP architectures

[9 hours]        DSP Datapath Design
                   Arithmetic Unit Design
                   Pipelining issues and control
                   Flow graph optimizations
                   Examples

[15 hours]         VHDL Language Fundamentals
                    Language fundamentals
                    Simulation-based Design
                    Laboratory issues

[9 hrs]             Register Transfer Level Chip Design
                        FSM models
                        Synthesis issues
                        Verification

[3 hrs]           Filter and FFT chip designs

[3 hrs]               Exams
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