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Design and Implementation of Therapeutic Ultrasound Generating Circuit for Dental Tissue Formation and Tooth-Root Healing

Woon Tiong Ang, Cristian Scurtescu, Wing Hoy, Tarek El-Bialy, Ying Yin Tsui, and Jie Chen, *Senior Member, IEEE*

Abstract—Biological tissue healing has recently attracted a great deal of research interest in various medical fields. Trauma to teeth, deep and root caries, and orthodontic treatment can all lead to various degrees of root resorption. In our previous study, we showed that low-intensity pulsed ultrasound (LIPUS) enhances the growth of lower incisor apices and accelerates their rate of eruption in rabbits by inducing dental tissue growth. We also performed clinical studies and demonstrated that LIPUS facilitates the healing of orthodontically induced teeth-root resorption in humans. However, the available LIPUS devices are too large to be used comfortably inside the mouth. In this paper, the design and implementation of a low-power LIPUS generator is presented. The generator is the core of the final intraoral device for preventing tooth root loss and enhancing tooth root tissue healing. The generator consists of a power-supply subsystem, an ultrasonic transducer, an impedance-matching circuit, and an integrated circuit composed of a digital controller circuitry and the associated driver circuit. Most of our efforts focus on the design of the impedance-matching circuit and the integrated system-on-chip circuit. The chip was designed and fabricated using 0.8- μm high-voltage technology from Dalsa Semiconductor, Inc. The power supply subsystem and its impedance-matching network are implemented using discrete components. The LIPUS generator was tested and verified to function as designed and is capable of producing ultrasound power up to 100 mW in the vicinity of the transducer's resonance frequency at 1.5 MHz. The power efficiency of the circuitry, excluding the power supply subsystem, is estimated at 70%. The final products will be tailored to the exact size of teeth or biological tissue, which is needed to be used for stimulating dental tissue (dentine and cementum) healing.

Index Terms—Dental tissue formation, dental traumatology, low intensity pulsed ultrasound (LIPUS), system-on-a-chip design, therapeutic ultrasonic device, tissue engineering.

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I. INTRODUCTION

ULTRASOUND is being used in many therapeutic applications. For instance, therapeutic ultrasound is being used to treat various soreness and injuries in athletes and is used after injections in order to disperse the injected fluids [1]. Ultrasound has been effectively used for the treatment of rheumatic diseases [1]. Due to its heating effect, ultrasound is also used for treating cancer by ultrasound-induced hyperthermia [2]. Ultrasound-enhanced delivery of therapeutic agents, such as genetic materials, proteins, and chemotherapeutic agents, is another increasingly important area for the application of ultrasound techniques [3]. High-intensity focused ultrasound (HIFU) is used to kill tumors by rapidly heating and destroying pathogenic tissues [4]. HIFU treatment for uterine fibroids was approved by the Food and Drug Administration (FDA) in October 2004 [5].

A. Our Previous Work

In addition to HIFU, another form of therapeutic ultrasound is low-intensity pulsed ultrasound (LIPUS), which can be used in tissue engineering. Our recently published results have shown that LIPUS has the potential for treating orthodontically induced tooth-root resorption [6]. After traumatic luxation and avulsion injury to teeth, root resorption becomes the major concern [7]–[9]. The root surface is damaged as a result of the injury and the subsequent inflammatory response [8]. The healing pattern depends on the degree and surface area of the damaged root and on the nature of the inflammatory stimulus [8], [10]. If the root damage is small, healing can be performed through the deposition of new cementum and periodontal ligament (favorable healing). However, if the root damage is large, the bone will attach directly onto the root surface and result in ankylosis and osseous replacement [11], [12]. Infection can cause a progressive inflammatory resorption that can cause tooth loss in a very short period of time. Sixty-six percent of tooth loss has been reported due to root resorption following trauma, and half of these cases involve the progressive type of root resorption [13]. Noninvasive methods for tissue healing include electric stimulation [14], pulsed electromagnetic field (PEMF) [15], and LIPUS [16]. LIPUS's ability to enhance the healing and to stimulate dental tissue formation in human patients was investigated by El-Bialy *et al.* [6]. In animal studies involving rabbits, LIPUS was used for bone healing and formation during mandibular distraction osteogenesis [17]. The results show that

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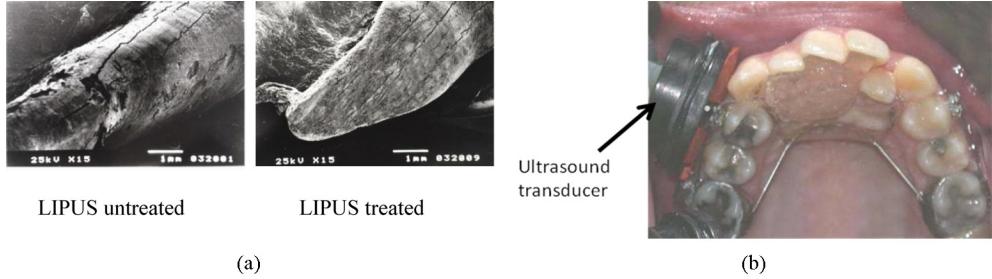


Fig. 1. (a) SEM photographs of the buccal surfaces. (b) The ultrasound transducer is too large to be used inside the mouth. (Courtesy of the *American Journal of Orthodontics and Dentofacial Orthopedics*).

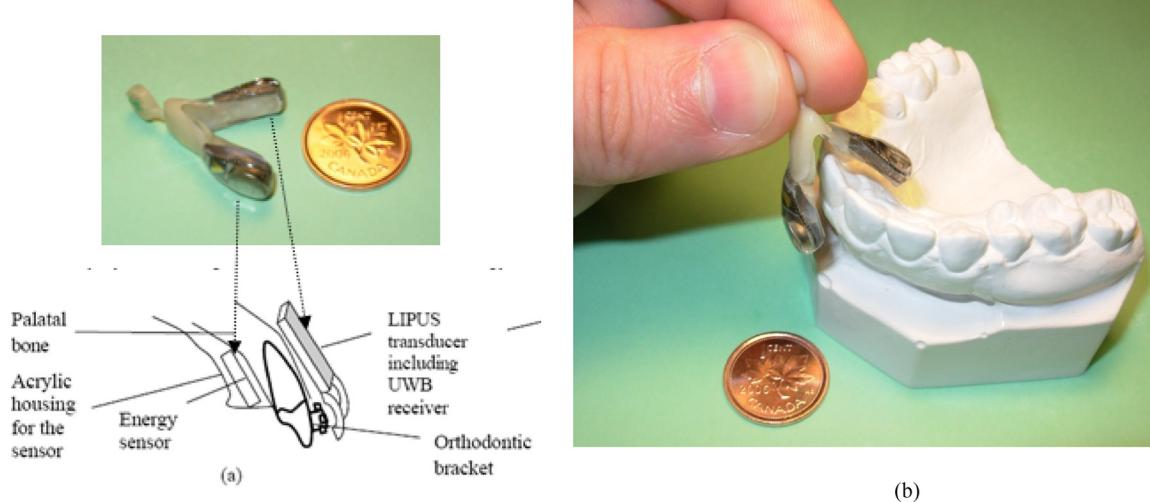


Fig. 2. (a) Illustration of the LIPUS transducer with hooks to orthodontic braces and its sensing unit. (b) The view of the transducer attached to the patient's dental cast. Here, the dimension of the LIPUS transducer including the UWB receiver [or the shaded rectangular piece in Fig. 2(a)] will be custom made to fit an individual patient's tooth size. Acrylic will be used for covering the device.

LIPUS stimulated dental tissue formation and enhanced teeth eruption [16]. In the human studies, LIPUS was utilized for the healing of orthodontically induced teeth root resorption [6]. Our studies show that our prototype LIPUS is very effective for enhancing dental-tissue healing and for treating the tooth-shortening problem as shown in Fig. 1(a). With this proven success in using therapeutic ultrasound, we have developed a prototype LIPUS device. However, problems with the LIPUS device include the following:

- 1) The ultrasound transducers are too large to be used inside the mouth as shown in Fig. 1(b).
- 2) The existing LIPUS devices utilize wire connections to interconnect the transducer and the power supply. The saliva from patients' mouths can cause short circuits and endanger the patients.
- 3) Patients usually experience difficulties and discomfort from holding the transducers within their mouths for 20 minutes per day in tight contact with the gingival tissues close to the involved teeth.

B. Our Current Work

The previously mentioned shortcomings prevent us from recruiting more patients for clinical studies. Therefore, we are motivated to seek portable and small-sized intraoral devices for dental tissue formation and tooth-root healing. The novelty of

our device is as follows: the resulting device will be tailored in various sizes so that it can be mounted onto an individual tooth, as shown in Fig. 2. The LIPUS transducer will be hooked to the orthodontic brackets on the tooth, and the energy sensor will be housed in an acrylic plate that can be easily fabricated on each patient's dental cast (a positive replica of the patient's teeth and jaw). The proposed design will eliminate the need for patients to press down on the device for 20 min per day. We will cover the device with materials that allow for the propagation of the produced waves. These materials will be electrical insulators so that patients will not experience the risk of a potential short circuit between the device's material and any filling material within the patient's mouth. We can also treat different teeth simultaneously by networking the LIPUS transducers and energy sensors together.

In this paper, we present a low-power LIPUS design. Although not fully integrated on a single chip yet, the proposed design requires minimal off-chip components and, thus, makes a miniaturized system-in-package (SIP) solution possible. The paper is organized as follows: In Section II, we present the detailed design of individual components of the LIPUS device. In Section III, we describe how to map the system design onto a chip. In Section IV, we present our chip layout and real-time measurement results. Finally, we conclude our work in Section V.

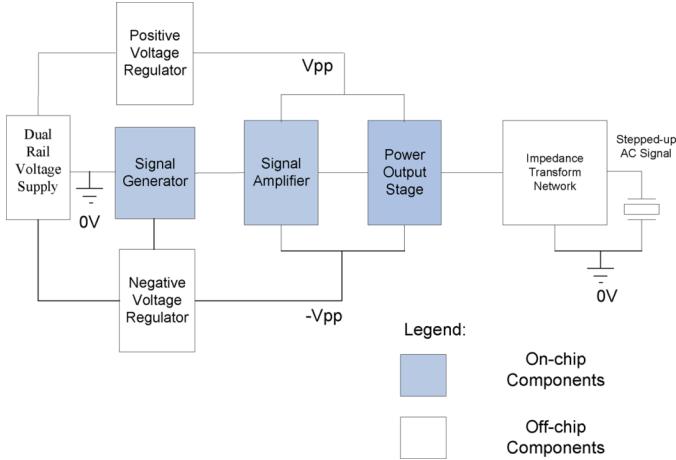


Fig. 3. Proposed architecture for the LIPUS generator.

II. LIPUS SYSTEM DESIGN

The design specifications of the LIPUS generator are as follows: intensity = 30 mW/cm² on the transducer surface, ultrasonic frequency = 1.5 MHz, pulse repetition rate = 1 kHz, and pulse duty cycle = 20%. These design specifications are determined based on previous biological and clinical studies [6], [16]. To achieve this design goal, the system architecture is proposed as shown in Fig. 3. The functionality of each block is as follows: the signal generator produces signals with variable frequency and pulse duty cycle. The signal amplifier then amplifies the signal to the desired amplitude, whereas the power output stage provides sufficient current to drive the transducer via the impedance transform network. The impedance transform network is used to amplify and provide sufficient voltage and relaxes the voltage swing requirement on the voltage regulators. To fit the LIPUS generator on a single chip, the signal generator, the signal amplifier, and the power-output stage need to be integrated on a chip. Since the voltage regulator blocks require relatively large capacitors that occupy a significant portion of the chip area, they are preferably implemented off-chip. Similarly, the impedance transform network is best implemented off-chip due to the large values of inductance and capacitance required.

A. System Tradeoffs and Design Challenges

One of the great challenges in the design of this portable ultrasound generator is the large voltage and current required to drive the transducer. This poses significant design challenges on the power-supply subsystem and the power-output stage; both of these play a critical role in determining the size and efficiency of the overall generator. In order to generate large voltage oscillation without much chip area, several methods can be used. A direct method is to use dc–dc upconverters to boost the supply voltage and, thus, increase the magnitude of voltage oscillation. This method, however, can present a formidable challenge when a large step-up ratio, high efficiency, and high-current capability are expected for the dc–dc upconverters. A complementary metal–oxide semiconductor (CMOS)

high-voltage dc–dc upconverter dedicated for ultrasonic applications was proposed in [21], which can handle relatively low drive current. Alternatively, with the combination of a dc–dc upconverter, an impedance transform network can be used to amplify an ac voltage signal. Traditionally, electromagnetic (EM) transformers are used [22], but EM transformers are known to be bulky and are not suitable for miniaturization. To overcome this problem, an impedance transform network with LC components is used in our design.

An output stage capable of efficiently driving the transducer, either directly or through an impedance transform network, was proposed. The use of a conventional class-B linear amplifier results in a theoretical maximum efficiency of 78% [18]. In order to achieve greater efficiency, switching amplifiers that have the potential for very high efficiency [18] can be used. These amplifiers have been applied in piezoelectric transducers [19]–[21]. A drive amplifier was proposed by R. Chebli and Sawan [21] that is based on a level-shifter stage and a class D switching output. A level shifter is a commonly used technique for generating high-voltage pulses [24]–[26] and can be used to drive piezoelectric transducers and the capacitive microelectromechanical-system (MEMS) ultrasonic transducers (cMUTs). The circuit presented by R. Chebli and Sawan [21] was designed to produce output voltages up to 200 V [21]. However, the circuit operates far from the resonance region, and the circuit can only handle currents in the order of hundreds of microamperes. Another class-D amplifier using pulse-width modulation (PWM) has been reported, which can operate with high efficiency at resonance frequencies between 10 kHz and 100 kHz [19]. Despite the examples listed before, there is no straightforward design to guarantee power efficiency when a class-D switching amplifier is used for higher frequency operations. Parasitic losses become significant in these designs. Careful consideration is required to evaluate whether the extra cost of designing a switching amplifier is worthwhile. In this paper, a level shifter is used in the power-output stage to drive the transducer through an impedance transform network without using PWM.

Integrating the electronics into an IC presents yet another level of challenge. Most modern fabrication technologies have scaled down the supply voltage significantly to reduce power consumption. Consequently, voltage tolerance on most CMOS technologies has also diminished. In order to design a circuit that supports large voltage swing and large current driving capability, a high-voltage technology from Dalsa Semiconductor is used for our LIPUS chip design.

B. Impedance Transform Network

Different circuit topologies (e.g., L-match, T-match, and PI-match) can be used as impedance transform networks. An L-match circuit shown in Fig. 4(a) is used in our LIPUS generator circuit due to its simple implementation and easy integration on-chip. The impedance transform network consisting of L_{IT} and C_{IT} can effectively amplify input voltage signal by a factor of n to drive the load R_L .

The inductance L_{IT} and capacitance C_{IT} values depend on the desired voltage amplification factor n and the load resistance

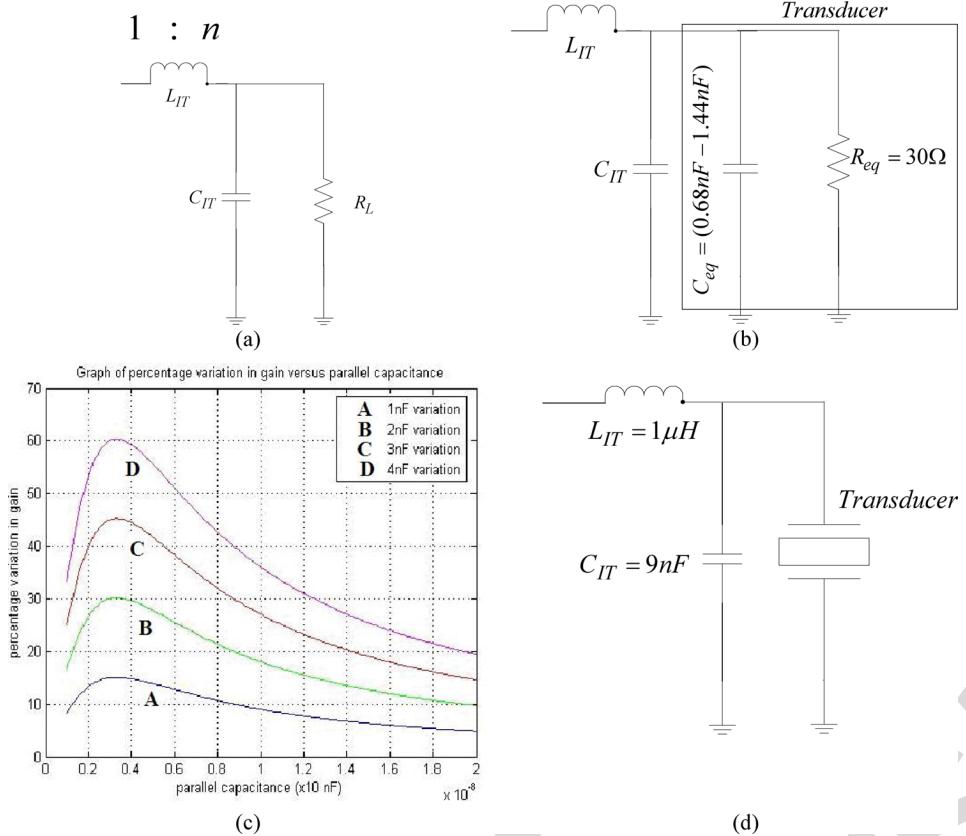


Fig. 4. (a) L-match consisting of an inductor L_{IT} and a capacitor C_{IT} connected to a load resistor R_L . (b) L-match circuit for impedance transformation. (c) Curves illustrating the percentage variation in gain due to the variation in capacitance. (d) L-match circuit for a voltage gain of three.

R_L . The input impedance of the circuit in Fig. 4(a) can be derived as

$$\overline{Z_{in}} = \frac{R_L + j\omega_s(L_{IT} - R_L^2C(1 - \omega_s^2L_{IT}C_{IT}))}{1 + \omega_s^2C_{IT}^2R_L^2} \quad (1)$$

where ω_s is the resonant frequency. It is undesirable to drive a reactive load because a reactive load can cause charge recycling and, thus, reduces power efficiency. It is favorable to create a purely resistive load for the driving circuitry at the operating frequency. Therefore, the imaginary part of (1) is made equal to zero, or $L_{IT} - R_L^2C_{IT}(1 - \omega_s^2L_{IT}C_{IT}) = 0$. By solving for L_{IT} , we obtain

$$L_{IT} = \frac{R_L^2C_{IT}}{1 + \omega_s^2C_{IT}^2R_L^2}. \quad (2)$$

With its imaginary part in (1) set to zero, (2) is reduced to

$$\overline{Z_{in}} = R_{in} = \frac{R_L}{1 + \omega_s^2C_{IT}^2R_L^2}. \quad (3)$$

By rearranging (3), we obtain

$$C_{IT} = \frac{1}{\omega_s R_L} \sqrt{\frac{R_L}{R_{in}} - 1}. \quad (4)$$

Realizing that $n = R_L/R_{in}$, (4) can be rewritten as

$$C_{IT} = \frac{1}{\omega_s R_L} \sqrt{n^2 - 1}. \quad (5)$$

In order to calculate the circuit parameter in Fig. 4(a), a simplified equivalent circuit model of the transducer is incorporated as shown in Fig. 4(b). The total capacitance C of the overall circuit is given by $C = C_{IT} + C_{eq}$. Since the value of C_{eq} significantly varies within the narrow frequency band, it is important to find a way to reduce gain variation due to the variation of C_{eq} .

To determine how gain varies with the parameters C , L , and R_L , where $C = C_{IT} + C_{eq}$, $L = L_{IT}$ and $R_L = R_{eq}$, we can rewrite (5) as

$$n^2 = (\omega_s R_L C)^2 + 1. \quad (6)$$

By rearranging (2), we obtain

$$(\omega_s R_L C)^2 + 1 = R_L^2 \frac{C}{L}. \quad (7)$$

Comparing (6) and (7), it is observed that

$$n^2 = R_L^2 \frac{C}{L} \text{ or } n = R_L \sqrt{\frac{C}{L}}. \quad (8)$$

The differential of n , or Δn can now be written as

$$\begin{aligned} \Delta n &= \frac{\delta n}{\delta R_L} \Delta R_L + \frac{\delta n}{\delta C} \Delta C + \frac{\delta n}{\delta L} \Delta L \\ &= \sqrt{\frac{C}{L}} \Delta R_L + \frac{R_L}{2\sqrt{LC}} \Delta C + \left(-\frac{R_L \sqrt{C}}{2\sqrt{L^3}} \right) \Delta L. \end{aligned} \quad (9)$$

TABLE I
C VALUES CALCULATED ACCORDING TO (5) GIVEN THAT $n = 2, 3, 4$, AND 5

Voltage Gain n	C (nF)
2	6.13
3	10.0
4	13.7
5	17.3

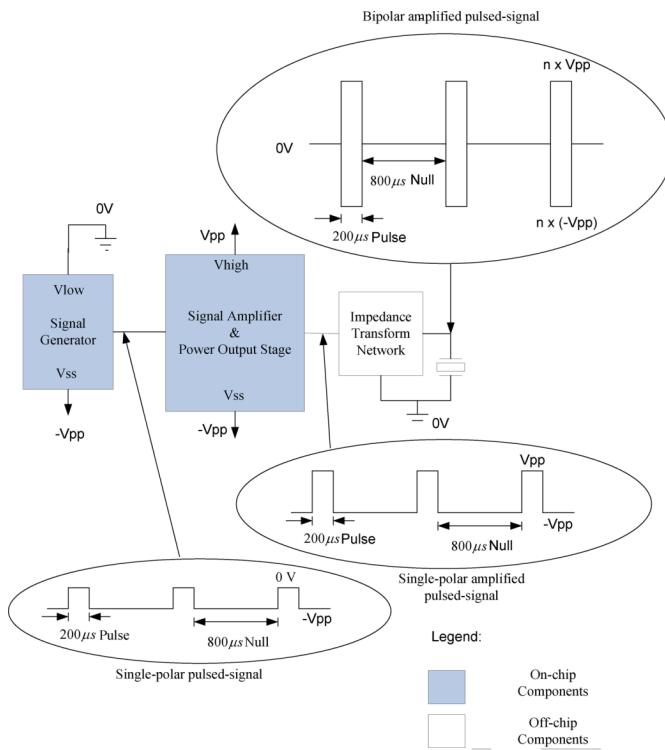


Fig. 5. Circuit generating a bipolar pulse-modulated signal from a single-polar pulsed signal.

Dividing (9) by (8), we obtain (10) that describes the percentage gain variation

$$\frac{\Delta n}{n} = \frac{\Delta R_L}{R_L} + \frac{1}{2} \frac{\Delta C}{C} + \left(-\frac{1}{2} \right) \frac{\Delta L}{L}. \quad (10)$$

The variation in (10) can be further reduced by reducing the percentage variation of parameters R_L , C , and L . For instance, the value of C due to variation in C_{eq} can be fixed because we can set C_{eq} between 0.68 nF and 1.44 nF. As a result, it is plausible to reduce the percentage variation $\Delta n/n$ by using a larger C . This is equivalent to a large voltage gain n , according to (8). Fig. 4(c) illustrates the effect of variation in capacitance on the percentage variation in gain.

From the graph, it is obvious that the percentage variation in gain is the greatest when $C = 3$ nF. As expected, larger capacitance reduces the percentage variation in gain. Next, the value of C can be determined by using (5), $C = (1/\omega_s R_L) \sqrt{n^2 - 1}$.

The values of n and the corresponding values of C are summarized in Table I, where $R_L = R_{eq} = 30 \Omega$ and ω_s is the resonant angular frequency $\omega_s = 2\pi(1.5 \times 10^6)$ [rad/s].

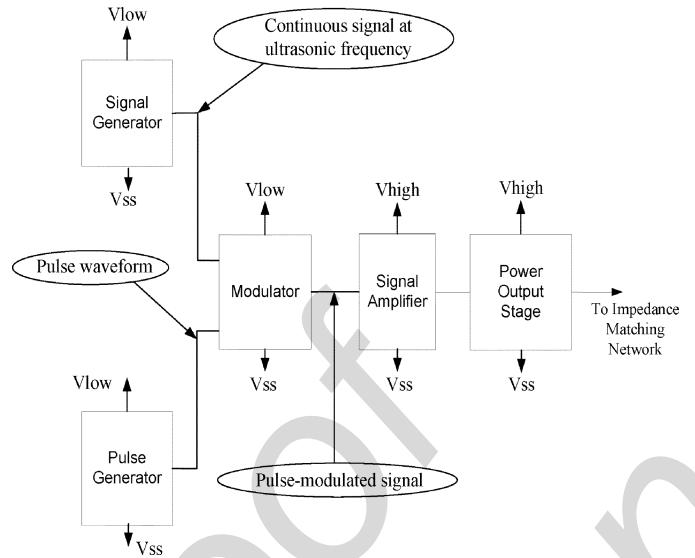


Fig. 6. Proposed single-polar pulse-modulated signal generator architecture.

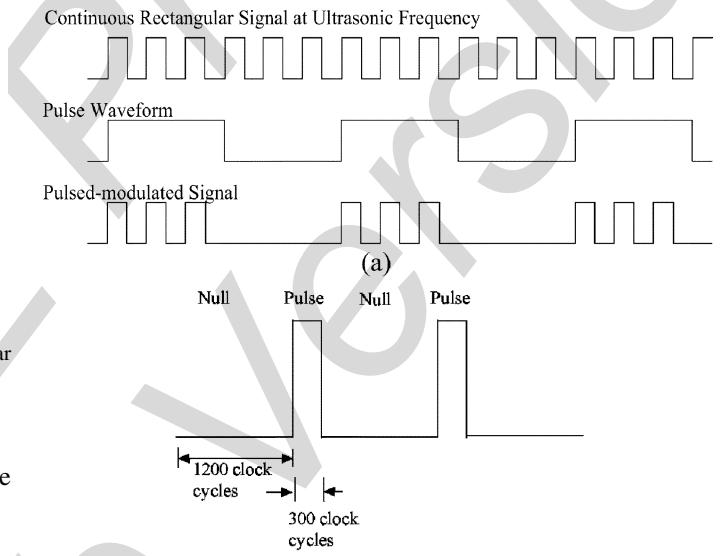


Fig. 7. (a) Illustration of pulse-modulated signal waveform generation. (b) Pulse diagram.

Three are chosen again, which requires a total parallel capacitance C of 10 nF. Since C_{IT} in $C = C_{IT} + C_{eq}$ can be measured to great accuracy using a digital multimeter (DMM), the uncertainty mainly comes from the C_{eq} term, which can also be easily quantified. By approximating C_{eq} to be 1 nF, somewhere in the known range of 0.68 nF to 1.44 nF, we can obtain the maximum variation of $C_{eq} = 0.44$ nF. From Fig. 4(c), we can see that the percentage variation in gain for 1 nF variation is about 10%. Consequently, the percentage variation in gain contributed by 0.44-nF uncertainty is estimated to be less than 10%. Following (2), we obtain $L_{IT} = L = R_L^2 C / (1 + \omega_s^2 C^2 R_L^2) = 1.0 \mu\text{H}$. The resulting L-match impedance transform network with calculated inductance and capacitance values is shown in Fig. 4(d).

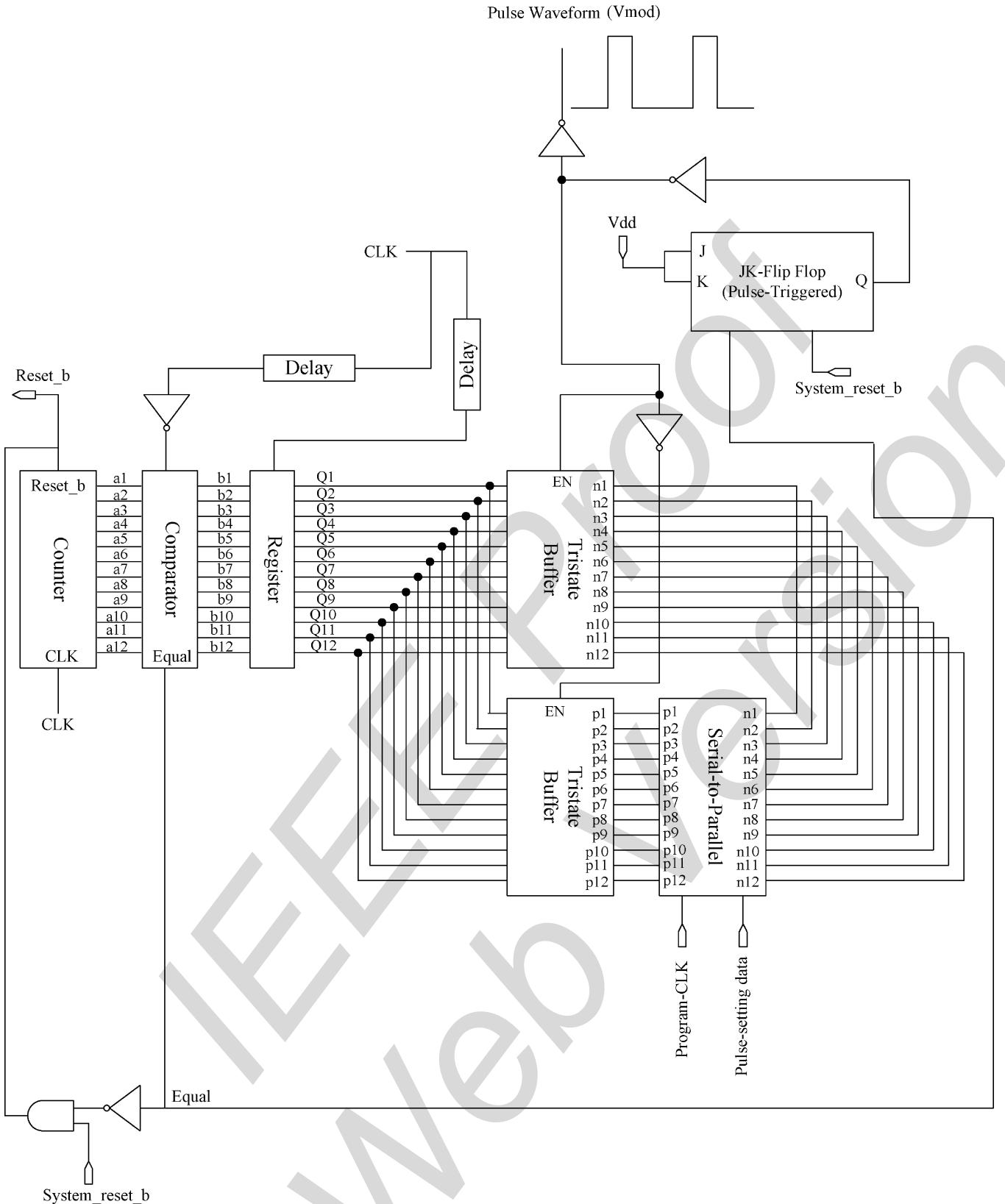


Fig. 8. Pulse generator circuitry.

C. Pulse-Modulated Signal Generator Integrated Circuit

Our design goal for the targeted IC is to produce pulse-modulated signals with sufficient amplitude to drive a piezoelectric

transducer through the impedance transform network designed in the previous section. Next, we present a design to vary signal frequency and the corresponding pulse duty cycle. To simplify the design, we choose a single-polar voltage signal as the output

instead of a bipolar signal as shown in Fig. 5. The single-polar signal is then amplified and converted to a bipolar signal by using the impedance transform network designed in the previous section. In this biasing scheme, the ground pin V_{ss} of the chip is connected to the negative rail ($-V_{pp}$) of the voltage supply. The power-supply pins V_{low} and V_{high} are connected to the voltage-supply ground (0 V) and the positive rail (V_{pp}), respectively. The chip output $-V_{pp}$ swings back and forth between, but not necessarily reaching, $-V_{pp}$ and V_{pp} during an oscillation period. Both the impedance transform network and the transducer have one end connected to ground as shown in Fig. 5.

Our preliminary investigation showed that 7.6-V voltage amplitude is required to generate sufficient acoustic power intensity. Since the impedance transform network provides a gain of three at resonance, a sinusoidal voltage of amplitude 2.53 V (peak-to-peak magnitude of 5.06 V) is needed in the IC. This voltage requirement is beyond the normal operating regime of conventional CMOS fabrication technologies and special high-voltage technology is required. As a result, we selected the 0.8- μ m CMOS/DMOS technology from Dalsa Semiconductor, Inc. for our chip fabrication. Dalsa technology enables us to use low-voltage CMOS and high-voltage DMOS processes capable of handling high-voltage designs beyond 100 V. The technology was expected to offer a solution for integrating a low-voltage digital controller and a high-voltage driver on a chip.

D. Pulse-Modulated Signal Generator Architecture

The proposed architecture of the single-polar pulse-modulated signal generator for on-chip implementation is shown in Fig. 6. The signal generator produces a continuous rectangular signal at the desired ultrasonic frequency. The pulse generator produces a rectangular pulse that corresponds to the envelope of the resulting pulse-modulated signal. As its name implies, the modulator modulates the continuous rectangular ultrasonic signal with the pulse to generate a pulse-modulated signal waveform as illustrated in Fig. 7(a). A signal amplifier in Fig. 6 is used to amplify the pulse-modulated signal waveform to the desired level. A power-output stage is integrated to provide sufficient current to drive the transducer through the impedance-matching network. Note that two separate supply voltages are needed to ensure that the device operates properly. V_{low} is the low-voltage supply to power the signal generation, pulse generation, and modulation blocks. V_{high} is used by the signal amplifier and the power-output stage to control the amplitude of the final amplified pulse-modulated signal waveform for driving the off-chip impedance transform network.

Fig. 7(a) shows an example in which each pulse only contains three cycles of rectangular waveforms. A method to control the pulse length, pulse repetition rate, and ultrasonic signal frequency in the targeted LIPUS generator is needed. In order to achieve a flexible design, a voltage-controlled oscillator is used to generate a tunable ultrasonic frequency. For instance, to ensure a specific duty cycle, we provide an embedded mechanism to count the number of clock cycles so that the system knows when to enter the “null” state or the “pulse” operation state. To generate the desired 1.5-MHz signal frequency, 1-kHz pulse repetition rate, and 20% duty cycle required in our design,

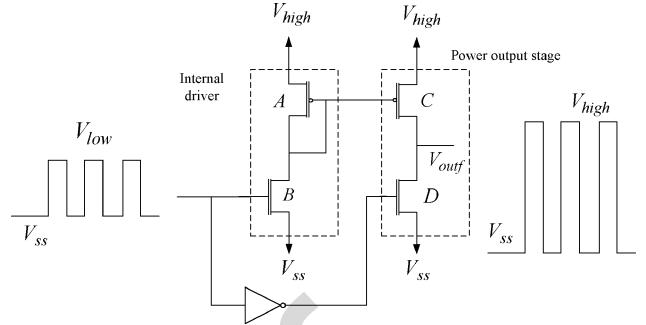


Fig. 9. Level-shifter circuit.

each pulse will contain 300 clock cycles of 1.5-MHz oscillations. The pulses are separated by 1200 clock cycles of "null" period. This schematic diagram is shown in Fig. 7(b).

III. CHIP DESIGN AND IMPLEMENTATION

In this section, a detailed low-level realization of the architecture proposed in Fig. 6 is presented. Since some of the components are pretty standard, we summarize the design as follows (we will mainly focus on the design of the signal amplifier and power-output stage in Section III-A).

- 1) The signal generator is realized by using a ring voltage-controlled oscillator (VCO), which is also used to generate the clock signals (CLK) for the entire chip.
 - 2) The pulse generator is realized using a counter, a comparator, two tristate buffers, and a JK-Flip Flop shown in Fig. 8.
 - 3) The modulator that modulates the continuous ultrasonic signal with a pulse waveform is easily realized by using an AND gate.

A. Signal Amplifier and Power-Output Stage

In order to amplify a low-voltage digital control signal to a high-voltage driving signal, a level shifter is needed. The level shifter can achieve both functions of the voltage amplifier and the power-output stage. Level-shifting techniques have been studied in [24]–[26] and applied to CMOS/DMOS [**Please define "DMOS"**] technology for generating high voltages [27]. Our design is directly adapted from [27]. As shown in Fig. 9, the level shifter is symbolically realized by using two p-channel DMOS transistors (A and C) and two n-channel DMOS transistors (B and D). Transistors A and B are responsible for generating a suitable driving voltage to turn transistor C on and off. The operation of transistor D is directly controlled by the digital input to the level shifter through an inverter. Transistors C and D drive the piezoelectric load through an impedance transform network. For this reason, transistors C and D are collectively labeled the “output power stage” while A and B are called “internal driver.”

A sinusoidal voltage of 2.53 V is needed to generate a sinusoidal voltage with an amplitude of 7.6 V across the transducer since the amplification factor is three in the impedance transform network. Since the level shifter is designed to generate a rectangular signal instead of a sinusoidal signal, it is instructive to consider the Fourier series of a rectangular waveform containing information in the coefficient of its constituent

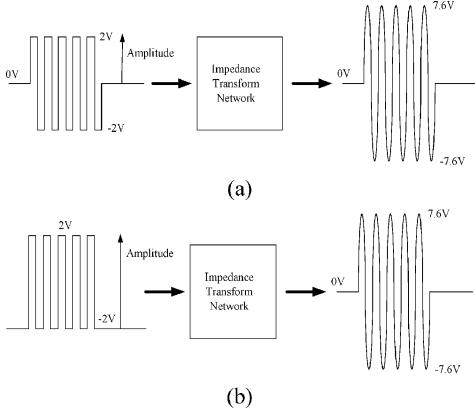


Fig. 10. (a) Bipolar rectangular waveform to bipolar sinusoidal waveform conversion. (b) Single-polar rectangular waveform to bipolar sinusoidal waveform conversion.

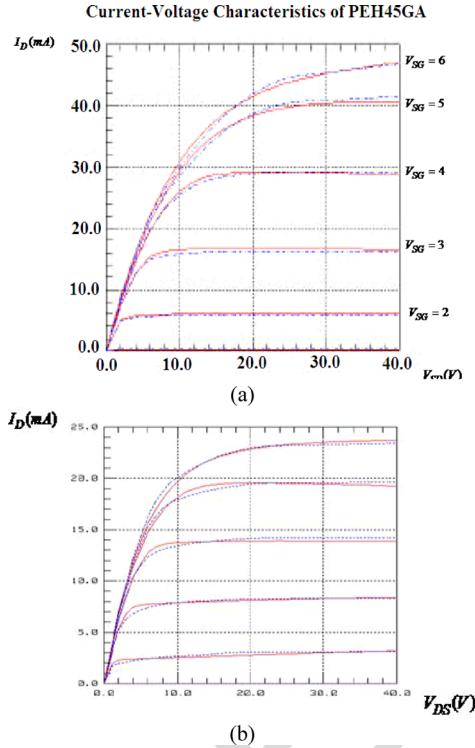


Fig. 11. (a) Plots of drain current versus source-to-drain voltage for PEH45GA EDMOS: measured (solid line) versus simulated (dotted line) curves provided by Dalsa Semiconductor, Inc. in [28]. (b) Plots of the drain current versus drain-to-source voltage for NDH16GC LDMOS: measured (solid line) versus simulated (dotted line) curves provided by Dalsa Semiconductor, Inc. in [28].

harmonics. The Fourier series for a rectangular waveform is $\text{rect}(t) = (4/\pi) \sum_{n=1,3,5,\dots}^{\infty} (\sin(2\pi nt/T))$, where T is the period of the rectangular waveform. This suggests that a rectangular bipolar wave of amplitude $2.53 \text{ V} \bullet \pi/4 \approx 2 \text{ V}$ can be used instead of a 2.53-V sinusoidal signal to generate a voltage of 7.6-V amplitude across the transducer as shown in Fig. 10(a). Since the level shifter designed herein generates a single-polar waveform, an amplitude of 4 V is needed as shown in Fig. 10(b).

It was decided that transistor model PEH45GA [28] would be used for the p-channel DMOS (A and C) while the NDH16GC

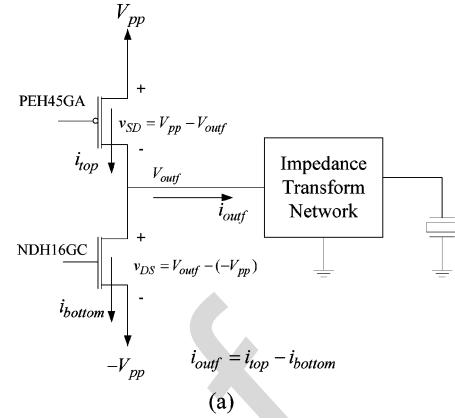


Fig. 12. (a) Illustration of currents and voltages in the power-output stage. (b) Expected output voltages and currents at the V_{outf} node of the pulse-modulated signal generator circuit.

model [28] would be used for the n-channel DMOS (B and D), owing to their relatively high current-to-size ratios. The electrical characteristics of these two transistors are shown in Fig. 11(a) and (b).

Considering the power-output stage of the level-shifter circuit, the source-to-drain voltage of PEH45GA transistor v_{SD} and drain-to-source voltage of the NDH16GC transistor v_{DS} are labeled in Fig. 12(a) for illustration. The drain currents i_D of PEH45GA and NDH16GC transistors are, respectively, labeled as i_{top} and i_{bottom} in Fig. 12(a). By Kirchhoff's current law $i_{outf} = i_{top} - i_{bottom}$, it is assumed the two types of transistors do not conduct simultaneously. Hence $i_{outf} = i_{top}$ when $i_{outf} > 0$, and $i_{outf} = -i_{bottom}$ when $i_{outf} < 0$. In other words, current i_{outf} delivered to the impedance transform network entirely comes from the PEH45GA transistor, while current i_{outf} from the impedance transform network is completely sunk into the NDH16GC transistor.

The voltage V_{pp} and the number of transistors to use in the power-output stage remains to be determined. The input impedance of the load is $|Z_{in}| = R_L/n^2 = 30 \Omega/3^2 = 3.33 \Omega$. From our previous Fourier analysis, a signal of 2-V amplitude is sufficient to generate a 7.6-V voltage on the load. Therefore, driving a sinusoidal signal of 2-V amplitude across the load

results in a current of $2 \text{ V}/3.33 \Omega = 600 \text{ mA}$. Since the load is mostly resistive in the vicinity of resonant frequency, the driving voltage is theoretically in phase with the current. Nevertheless, the power-output stage does not generate a sinusoidal signal. If only small current is required by the load, a rectangular voltage waveform is sufficient. However, due to the considerably large current required for the LIPUS generator, a larger v_{SD} is needed by the PEH45GA transistor to sustain 600-mA peak current. It is expected that a rectangular waveform with a sizable voltage dip in the middle would be produced. Due to the importance of reserving sufficient v_{SD} to sustain high peak current, a new term $v_{SD,\text{critical}}$, which corresponds to v_{SD} is needed for denotation when the output is in the "U"-shaped curve shown in Fig. 12(b). From Fig. 12(b), we obtain a magnitude for the "U" curve of $v_{SD,\text{critical}} = V_{pp} - v_{\min}$, where v_{\min} is the magnitude of the waveform at the bottom of the "U"-shaped waveform. To guarantee that the new waveform contains the first harmonics with sufficient amplitude (i.e., at least 2.53 V), v_{\min} must be greater than 2 V regardless of $v_{SD,\text{critical}}$, based on the principle of superposition and Fourier analysis.

The problem now becomes how large a $v_{SD,\text{critical}}$ is feasible for the current generation and how many transistors must be used for a chosen v_{SD} . From Fig. 11(b), it is observed that i_D is proportional to v_{SD} in the triode operation region when v_{SD} is small. Furthermore, as V_{pp} increases, the current i_D that each transistor can source also increases. As a result, there is a tradeoff between V_{pp} and the number of transistors. To use smaller V_{pp} , more transistors are needed (which translates to larger chip size) because each transistor sources less current and, thus, results in lower v_{SD} . We chose $V_{pp} = 4 \text{ V}$, which provides sufficient current with an acceptable number of transistors. This choice implies that the transistors need to source a current of amplitude 600 mA with a v_{SD} of 2 V. From Fig. 11(a), 8 mA of current can be generated with one PEH45GA at $v_{SD} = 2 \text{ V}$. Hence, 75 transistors need to be connected in parallel, which is acceptable because they add up to an area of only 3.99 mm^2 (each PEH45GA has an area of $53245 \mu\text{m}^2$ [28]). The number of transistors is rounded up to 80 in the design.

For symmetry, the negative rail voltage is set to -4 V . Since the rectangular voltage swings as low as -2 V , the NMOS transistors need to sink 600 mA of current when $v_{DS} = 2 \text{ V}$. However, each NDH16GC transistor can only sink 5 mA of current at $v_{DS} = 2 \text{ V}$ [refer to Fig. 11(b)]. One-hundred twenty transistors are used, or collectively, NDH16GC consumes only 1.476 mm^2 of chip area (each NDH16GC has an area of $12388 \mu\text{m}^2$ [28]).

The final design at the power-output stage is shown in Fig. 13. In our previous calculations, we assume that the transistors PEH45GA and NDH16GC can be fully turned on with $v_{GS} = 4 \text{ V}$ for NDH16GC and $v_{SG} = 4 \text{ V}$ for PEH45GA, respectively. This is achieved by appropriately sizing transistors A and B in order to determine the multiplicity factor m and n in Fig. 14 to generate v_x with sufficient swing. Transistors A and B are specifically designed so that voltage v_x swings low enough (i.e., $v_x < 0$) to ensure that it fully turns on transistor C. On the other hand, it has to be ensured that $v_x > -1 \text{ V}$ because the PEH45GA transistor has a voltage limitation of 5 V based on the high-voltage transistors provided by Dalsa Semiconductor,

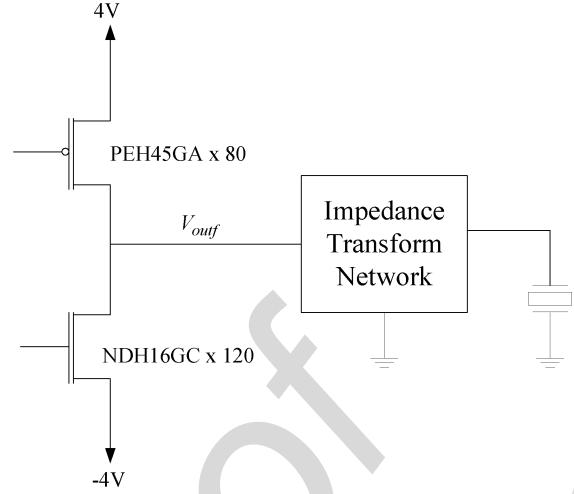


Fig. 13. Final design at the power-output stage.

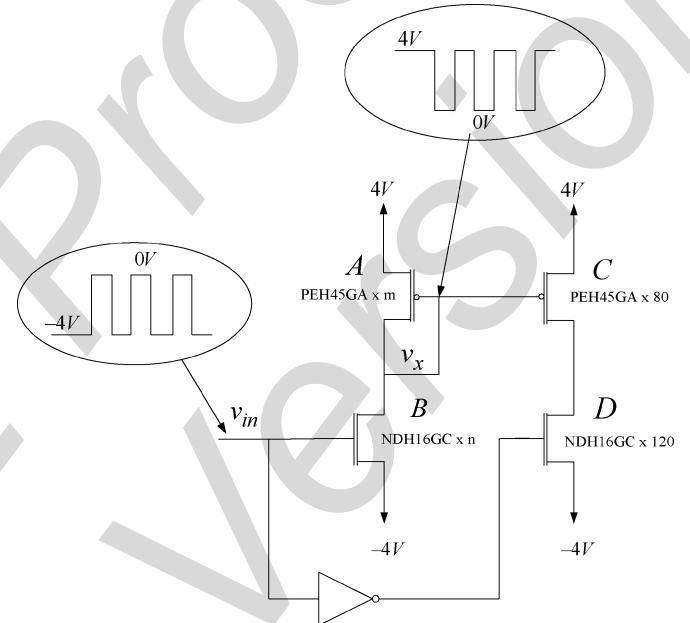


Fig. 14. Illustration of v_x in the level-shifter circuit.

Inc. [28]. If v_x swings to a voltage as low as 0 V, a drain current of $m*18 \text{ mA}$ will be developed. Similarly, a current of $n*10 \text{ mA}$ will flow into node B. According to Kirchhoff's current law, we can solve for the lowest integers m and n that satisfy $m*18 \text{ mA} = n*10 \text{ mA}$, which gives $m = 5$ and $n = 9$. Using these values, we can simulate to obtain a desirable v_x . Having discussed the design of all the modules in the proposed LIPUS generator, next we simulate the entire circuit functionalities to verify its performance.

IV. IC SIMULATION AND TESTING

A. Circuit Simulation Results

The schematic design of the pulse-modulated signal generator was simulated to verify its functionalities and its current driving capability. The simulation tool that we use is Cadence Spectre. V_p and V_n of the ring oscillator were set to 0.7 V and 2.3 V, respectively to produce 1.5-MHz oscillation. A V_{high} of

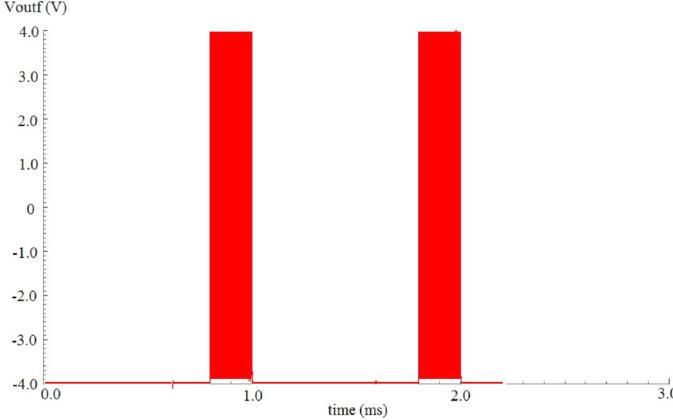


Fig. 15. Simulated output pulses, each $200\ \mu\text{s}$ wide and separated by $800\ \mu\text{s}$.

4 V, which translates to a rail-to-rail voltage of 8 V by symmetry, was applied to simulate the circuit's ability to produce sufficient voltage swing. The circuit was programmed to produce 300 clock cycles of oscillations and 1200 clock cycles of “null” periods as shown in Fig. 15. The simulated pulse waveform is shown in Fig. 15, in which the generated pulses (rectangular bars in figure) have a pulse repetition rate of 1.0 kHz and a pulselwidth of $200\ \mu\text{s}$. The output voltage V_{outf} swings from $-4\ \text{V}$ to $4\ \text{V}$ during the “pulse” phase, and stays at $-4\ \text{V}$ during the “null” phase as predicted. Nevertheless, due to the densely displayed waveforms within a “pulse” phase shown in Fig. 15, it is necessary to zoom into each pulse so that qualitative measurements on the oscillating voltage can be made.

A zoomed-in pulse allows us to closely examine current and voltage waveforms. Fig. 16(a) shows the simulated waveform of the voltage signal at V_{outf} . As expected, the waveforms display a “U”-shaped voltage dip in the middle. The amplitude of the voltage across the transducer slightly exceeds the minimum requirement of $7.6\ \text{V}$. The simulated current waveform is also shown in Fig. 16(b). The current amplitude reaches approximately $300\ \text{mA}$, which is expected to give the voltage amplitude of about $9\ \text{V}$. Having verified that the circuit meets the LIPUS design specifications, we layout the design for fabrication.

B. Circuit Layout

The final LIPUS signal generator chip, which contains transistors as summarized in Table II, is assembled in a layout measuring $2.8\ \text{mm}$ in width and $4.0\ \text{mm}$ in length, as shown in Fig. 17(a). Fig. 17(b) shows the picture of the fabricated LIPUS signal generator chip in a 40-pin dual-inline package (DIP40).

C. Chip Testing

The pulse-modulated signal generator chip is integrated on a breadboard for testing. The circuit diagram of the testing circuitry is shown in Fig. 17(c) and a photograph of the board-level testing circuit is shown in Fig. 17(d). The power-supply subsystem and the programming subsystem are described in the following subsections.

1) *Voltage Supply Subsystem:* The voltage supply subsystem consists of a pair of variable voltage regulators (LM317 and LM337) used to generate a dual-rail power supply of $\pm 4\ \text{V}$. Each voltage regulator is powered by a 9-V battery, which was

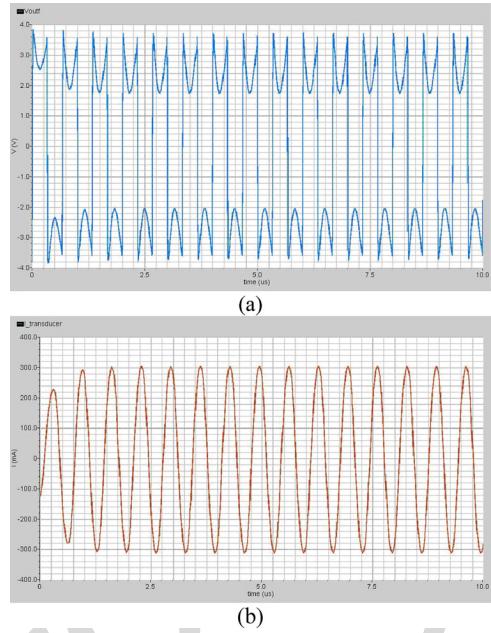


Fig. 16. (a) Simulated waveform showing the voltage at V_{outf} . (b) Simulated waveforms showing the current flows into the piezoelectric transducer.

chosen just for convenience. Another two LM317 chips are used to generate V_n and V_p , which are adjustable by using the potentiometers, and to set the clock frequency of the entire circuit.

2) *Serial Programming Subsystem:* An AVR butterfly board, which contains an Atmel Mega169PV microcontroller, is used to generate the pulse-setting serial stream and a corresponding programming clock for the fabricated IC. During initialization, 10010110000_2 (300 in the decimal number system) and 00100101100_2 (1200 in the decimal number system) are clocked into the pulse-setting module of the IC serially whenever the Atmel Mega169PV microcontroller is powered up. The fabricated pulse-modulated signal generator chip is programmed to output a pulsed-modulated ultrasonic signal of a 20% duty cycle (i.e., 300 clock cycles of oscillation, and 1200 clock cycles of “null period”).

3) *Circuit Test and Measurements:* Upon power up and completion of the initialization of the AVR butterfly, the voltages across the transducer are probed and displayed on an oscilloscope. V_n and V_p are then tuned to ensure that the ultrasonic signal frequency of $1.5\ \text{MHz}$ is generated at the CLK pin of the chip. The pulse duty cycle measured at the V_{outf} pin is 20% as expected, and the pulse waveform is shown in Fig. 18.

The rectangular waveform displays voltage dips in the middle of each rectangle, which is in line with our design and simulation. However, the measured waveforms have a “V”-shaped dip instead of a predicted “U”-shaped dip. This is attributed to a steep supply-voltage drop that occurs when a large amount of current is drawn from the power-supply subsystem. Fig. 19 shows the voltage (A) across the transducer and current (B) into the transducer. As expected, the pulse repetition rate is $1\ \text{kHz}$ and duty cycle is 20% duty.

Finally, an ultrasound power meter is used to measure the acoustic power of the LIPUS chip generated. By fixing the pulse duty cycle and supply voltage, acoustic power measurement is

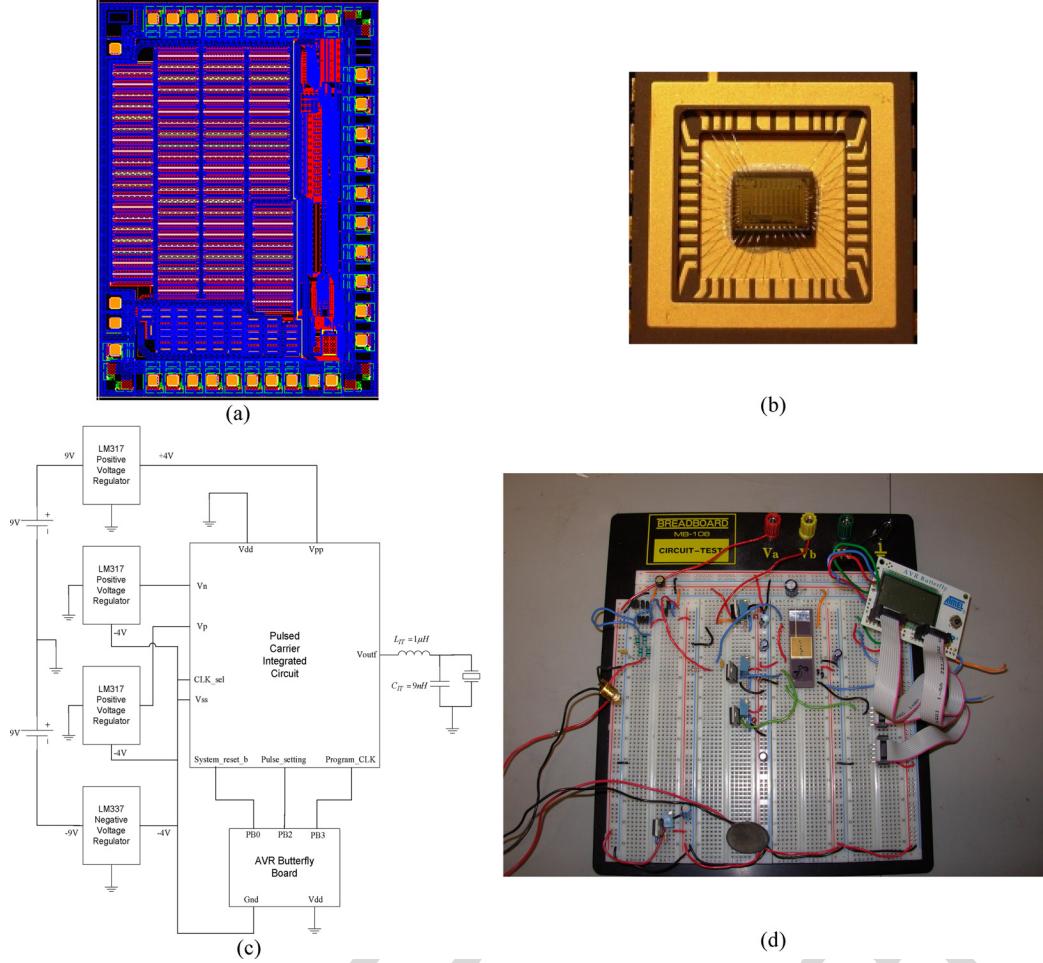


Fig. 17. (a) LIPUS signal generator IC layout. (b) Picture of the fabricated LIPUS signal generator chip in a 40-pin dual-in-line package (DIP40). (c) Testing circuit diagram. (d) Photograph of the board-level testing circuit.

TABLE II
SUMMARY OF THE TRANSISTORS USED IN THE LIPUS SIGNAL GENERATOR CHIP.

Transistor Types	Count (unit)
Low-voltage NMOS	2128
Low-voltage PMOS	2217
N-Channel LDMOS (NDH16GC)	129
P-Channel EDPMOS (PEH45GA)	85

performed for the following signal frequencies: 1.46 MHz, 1.48 MHz, 1.52 MHz, and 1.55 MHz. The measurement results are summarized in Table III.

From the measurement results, the maximum power of 118 mW is generated at 1.52 MHz. This translates to an intensity of 66.7 mW/cm², which is more than enough to meet the design specifications. Less power can easily be obtained by lowering the voltage regulators to supply a smaller dc supply voltage. It is also observed from Table II that within the frequency range of 1.50 MHz to 1.52 MHz, the power level reaches a plateau. It is, therefore, advisable to operate the circuit within this plateau to minimize power variation due to frequency

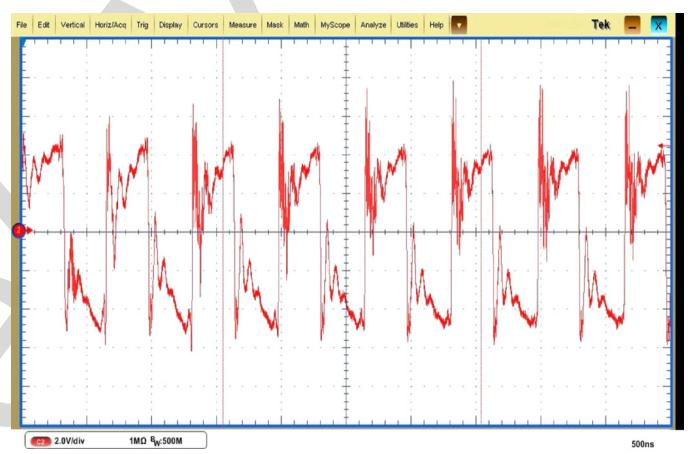


Fig. 18. Voltage waveforms at the V_{outf} pin of the LIPUS signal IC.

drift. The overall system's (including the transducer's) power consumption excluding the power of the voltage regulators is estimated at 800 mW on average, which gives an overall power efficiency of $\eta_{overall} = 14\%$. As previously determined, the transducer efficiency $\eta_{transducer}$ at 1.5 MHz was estimated to be approximately 20%. Therefore, it can be concluded that

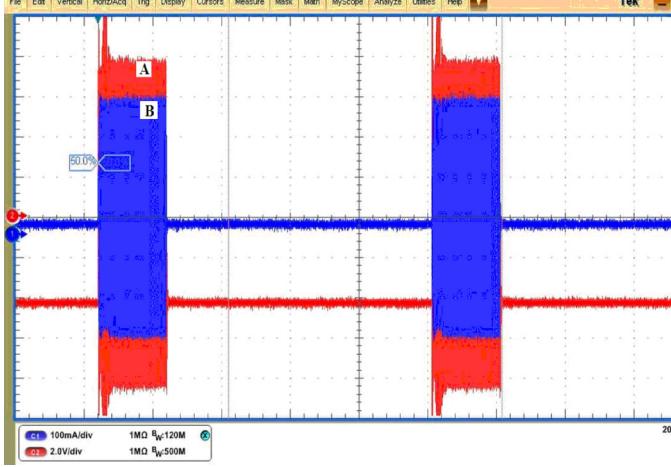


Fig. 19. Voltage A (a larger amplitude waveform) is overlapped with current B (a smaller amplitude waveform) pulses with microseconds pulse width and 800- μ s null width (color online).

TABLE III
ACOUSTIC POWER MEASURED WITH 20% DUTY CYCLE FOR DIFFERENT OPERATING FREQUENCIES

Signal Frequency (MHz)	Acoustic Power (mW)
1.46	72
1.48	86
1.50	116
1.52	118
1.55	110

TABLE IV
PERFORMANCE SUMMARY

Attribute	Performance
Chip size	2.8mm*4.0mm
Operating clock frequency	1.5MHz
Ultrasound carrier frequency	1.5MHz
Pulse repetition rate	1.0kHz
Duty Cycle	20%
Supply Voltage	3.3V
Overall Power Consumption (chip and transducer)	800mW
Power Consumption (chip)	220mW
Power Efficiency of Chip (at 1.5MHz)	70%

$200/200\eta_{electronics} \approx 14/20 \times 100\% = 70\%$. A summary of the chip performance is given in Table IV.

V. CONCLUSION AND FUTURE WORK

A LIPUS generator has been designed and implemented, which is composed of a power-supply subsystem, an impedance-matching network, a piezoelectric transducer, and an IC capable of pulse-modulated signal generation. The IC was fabricated using Dalsa 0.8 μ m high-voltage technology. The power-supply subsystem and impedance-matching network are implemented by using discrete components. An L-match

circuit is used to realize the impedance matching network, which allows the accurate delivery of power to the transducer for LIPUS generation. The LIPUS generator was verified and functions correctly. Even though the LIPUS generator was designed for 1.5-MHz pulsed-ultrasound with 1-kHz pulse repetition rate and 20% pulse duty cycle, it could be reprogrammed using an AVR butterfly board to generate pulsed-ultrasound at different frequencies, pulse repetition rates, and duty cycles. At the designated operating state, the generator produces an ultrasound up to 116 mW. The power efficiency of the circuit, excluding the power-supply subsystem, is estimated to be about 70%. The generator can also be tuned to output LIPUS waveforms at lower power by reducing the supplied voltage.

To achieve further miniaturization, future work will involve integrating the impedance-matching network and the power-supply subsystem on a chip to obtain a complete system-on-a-chip (SOI) design [29]. Our eventual medical application is to prevent patients' tooth-root resorption and to enhance dental tissue repair. We envision the device will be one-time use and affordable by middle-class patients. Since the final device will be user friendly and will have built-in wireless communication capability, the treatment can be performed by patients at home, and treatment data can be remotely monitored by dentists' offices. Since this device, to our best knowledge, is the first of its kind to help repair root resorption and enhance dental repair, the device can significantly enhance standards of care and minimize or prevent tooth loss due to trauma or severe root resorption by prolonged orthodontic treatment. We are testing the device in animals and seeking approval from the Health Canada before we can try it on humans.

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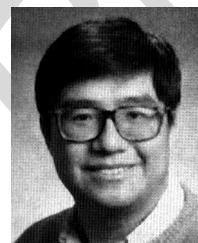
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Design and Implementation of Therapeutic Ultrasound Generating Circuit for Dental Tissue Formation and Tooth-Root Healing

Woon Tiong Ang, Cristian Scurtescu, Wing Hoy, Tarek El-Bialy, Ying Yin Tsui, and Jie Chen, *Senior Member, IEEE*

Abstract—Biological tissue healing has recently attracted a great deal of research interest in various medical fields. Trauma to teeth, deep and root caries, and orthodontic treatment can all lead to various degrees of root resorption. In our previous study, we showed that low-intensity pulsed ultrasound (LIPUS) enhances the growth of lower incisor apices and accelerates their rate of eruption in rabbits by inducing dental tissue growth. We also performed clinical studies and demonstrated that LIPUS facilitates the healing of orthodontically induced teeth-root resorption in humans. However, the available LIPUS devices are too large to be used comfortably inside the mouth. In this paper, the design and implementation of a low-power LIPUS generator is presented. The generator is the core of the final intraoral device for preventing tooth root loss and enhancing tooth root tissue healing. The generator consists of a power-supply subsystem, an ultrasonic transducer, an impedance-matching circuit, and an integrated circuit composed of a digital controller circuitry and the associated driver circuit. Most of our efforts focus on the design of the impedance-matching circuit and the integrated system-on-chip circuit. The chip was designed and fabricated using 0.8- μm high-voltage technology from Dalsa Semiconductor, Inc. The power supply subsystem and its impedance-matching network are implemented using discrete components. The LIPUS generator was tested and verified to function as designed and is capable of producing ultrasound power up to 100 mW in the vicinity of the transducer's resonance frequency at 1.5 MHz. The power efficiency of the circuitry, excluding the power supply subsystem, is estimated at 70%. The final products will be tailored to the exact size of teeth or biological tissue, which is needed to be used for stimulating dental tissue (dentine and cementum) healing.

Index Terms—Dental tissue formation, dental traumatology, low intensity pulsed ultrasound (LIPUS), system-on-a-chip design, therapeutic ultrasonic device, tissue engineering.

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I. INTRODUCTION

ULTRASOUND is being used in many therapeutic applications. For instance, therapeutic ultrasound is being used to treat various soreness and injuries in athletes and is used after injections in order to disperse the injected fluids [1]. Ultrasound has been effectively used for the treatment of rheumatic diseases [1]. Due to its heating effect, ultrasound is also used for treating cancer by ultrasound-induced hyperthermia [2]. Ultrasound-enhanced delivery of therapeutic agents, such as genetic materials, proteins, and chemotherapeutic agents, is another increasingly important area for the application of ultrasound techniques [3]. High-intensity focused ultrasound (HIFU) is used to kill tumors by rapidly heating and destroying pathogenic tissues [4]. HIFU treatment for uterine fibroids was approved by the Food and Drug Administration (FDA) in October 2004 [5].

A. Our Previous Work

In addition to HIFU, another form of therapeutic ultrasound is low-intensity pulsed ultrasound (LIPUS), which can be used in tissue engineering. Our recently published results have shown that LIPUS has the potential for treating orthodontically induced tooth-root resorption [6]. After traumatic luxation and avulsion injury to teeth, root resorption becomes the major concern [7]–[9]. The root surface is damaged as a result of the injury and the subsequent inflammatory response [8]. The healing pattern depends on the degree and surface area of the damaged root and on the nature of the inflammatory stimulus [8], [10]. If the root damage is small, healing can be performed through the deposition of new cementum and periodontal ligament (favorable healing). However, if the root damage is large, the bone will attach directly onto the root surface and result in ankylosis and osseous replacement [11], [12]. Infection can cause a progressive inflammatory resorption that can cause tooth loss in a very short period of time. Sixty-six percent of tooth loss has been reported due to root resorption following trauma, and half of these cases involve the progressive type of root resorption [13]. Noninvasive methods for tissue healing include electric stimulation [14], pulsed electromagnetic field (PEMF) [15], and LIPUS [16]. LIPUS's ability to enhance the healing and to stimulate dental tissue formation in human patients was investigated by El-Bialy *et al.* [6]. In animal studies involving rabbits, LIPUS was used for bone healing and formation during mandibular distraction osteogenesis [17]. The results show that

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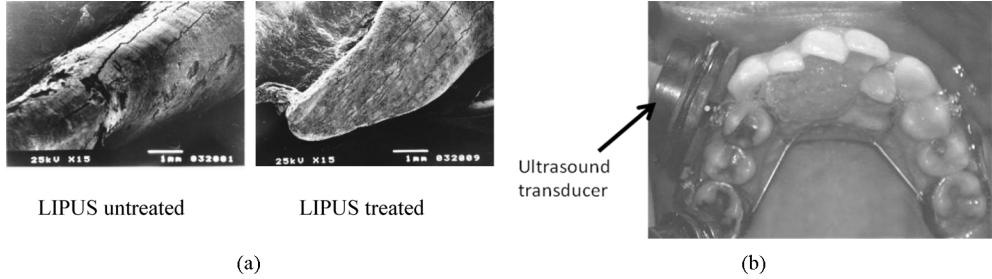


Fig. 1. (a) SEM photographs of the buccal surfaces. (b) The ultrasound transducer is too large to be used inside the mouth. (Courtesy of the *American Journal of Orthodontics and Dentofacial Orthopedics*).

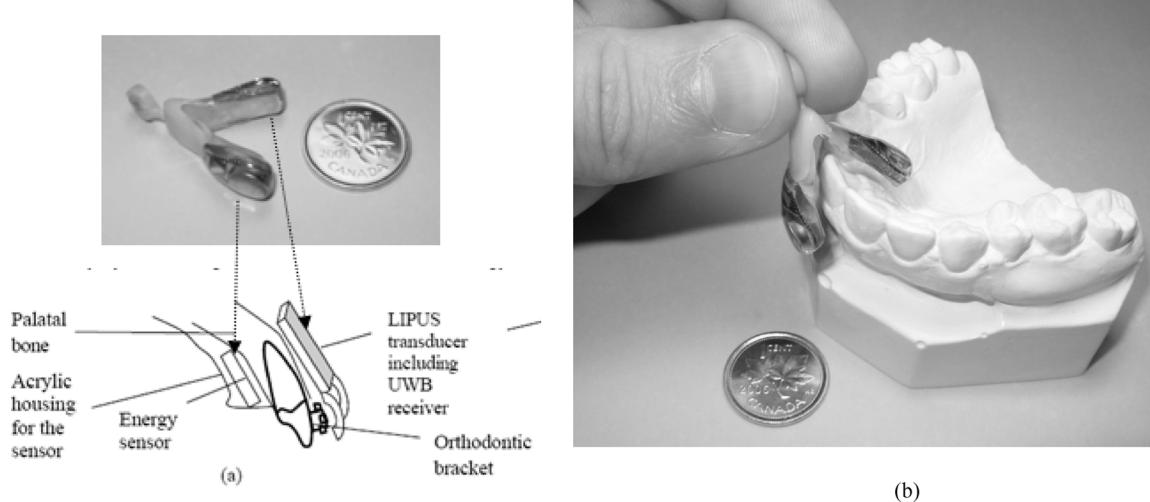


Fig. 2. (a) Illustration of the LIPUS transducer with hooks to orthodontic braces and its sensing unit. (b) The view of the transducer attached to the patient's dental cast. Here, the dimension of the LIPUS transducer including the UWB receiver [or the shaded rectangular piece in Fig. 2(a)] will be custom made to fit an individual patient's tooth size. Acrylic will be used for covering the device.

LIPUS stimulated dental tissue formation and enhanced teeth eruption [16]. In the human studies, LIPUS was utilized for the healing of orthodontically induced teeth root resorption [6]. Our studies show that our prototype LIPUS is very effective for enhancing dental-tissue healing and for treating the tooth-shortening problem as shown in Fig. 1(a). With this proven success in using therapeutic ultrasound, we have developed a prototype LIPUS device. However, problems with the LIPUS device include the following:

- 1) The ultrasound transducers are too large to be used inside the mouth as shown in Fig. 1(b).
- 2) The existing LIPUS devices utilize wire connections to interconnect the transducer and the power supply. The saliva from patients' mouths can cause short circuits and endanger the patients.
- 3) Patients usually experience difficulties and discomfort from holding the transducers within their mouths for 20 minutes per day in tight contact with the gingival tissues close to the involved teeth.

B. Our Current Work

The previously mentioned shortcomings prevent us from recruiting more patients for clinical studies. Therefore, we are motivated to seek portable and small-sized intraoral devices for dental tissue formation and tooth-root healing. The novelty of

our device is as follows: the resulting device will be tailored in various sizes so that it can be mounted onto an individual tooth, as shown in Fig. 2. The LIPUS transducer will be hooked to the orthodontic brackets on the tooth, and the energy sensor will be housed in an acrylic plate that can be easily fabricated on each patient's dental cast (a positive replica of the patient's teeth and jaw). The proposed design will eliminate the need for patients to press down on the device for 20 min per day. We will cover the device with materials that allow for the propagation of the produced waves. These materials will be electrical insulators so that patients will not experience the risk of a potential short circuit between the device's material and any filling material within the patient's mouth. We can also treat different teeth simultaneously by networking the LIPUS transducers and energy sensors together.

In this paper, we present a low-power LIPUS design. Although not fully integrated on a single chip yet, the proposed design requires minimal off-chip components and, thus, makes a miniaturized system-in-package (SIP) solution possible. The paper is organized as follows: In Section II, we present the detailed design of individual components of the LIPUS device. In Section III, we describe how to map the system design onto a chip. In Section IV, we present our chip layout and real-time measurement results. Finally, we conclude our work in Section V.

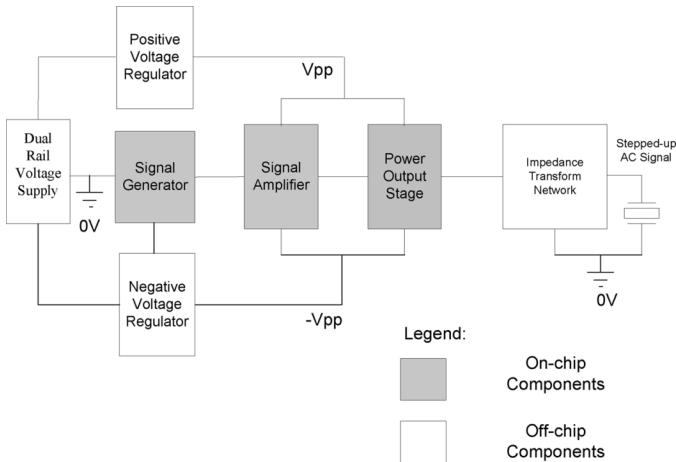


Fig. 3. Proposed architecture for the LIPUS generator.

II. LIPUS SYSTEM DESIGN

The design specifications of the LIPUS generator are as follows: intensity = 30 mW/cm² on the transducer surface, ultrasonic frequency = 1.5 MHz, pulse repetition rate = 1 kHz, and pulse duty cycle = 20%. These design specifications are determined based on previous biological and clinical studies [6], [16]. To achieve this design goal, the system architecture is proposed as shown in Fig. 3. The functionality of each block is as follows: the signal generator produces signals with variable frequency and pulse duty cycle. The signal amplifier then amplifies the signal to the desired amplitude, whereas the power output stage provides sufficient current to drive the transducer via the impedance transform network. The impedance transform network is used to amplify and provide sufficient voltage and relaxes the voltage swing requirement on the voltage regulators. To fit the LIPUS generator on a single chip, the signal generator, the signal amplifier, and the power-output stage need to be integrated on a chip. Since the voltage regulator blocks require relatively large capacitors that occupy a significant portion of the chip area, they are preferably implemented off-chip. Similarly, the impedance transform network is best implemented off-chip due to the large values of inductance and capacitance required.

A. System Tradeoffs and Design Challenges

One of the great challenges in the design of this portable ultrasound generator is the large voltage and current required to drive the transducer. This poses significant design challenges on the power-supply subsystem and the power-output stage; both of these play a critical role in determining the size and efficiency of the overall generator. In order to generate large voltage oscillation without much chip area, several methods can be used. A direct method is to use dc–dc upconverters to boost the supply voltage and, thus, increase the magnitude of voltage oscillation. This method, however, can present a formidable challenge when a large step-up ratio, high efficiency, and high-current capability are expected for the dc–dc upconverters. A complementary metal–oxide semiconductor (CMOS)

high-voltage dc–dc upconverter dedicated for ultrasonic applications was proposed in [21], which can handle relatively low drive current. Alternatively, with the combination of a dc–dc upconverter, an impedance transform network can be used to amplify an ac voltage signal. Traditionally, electromagnetic (EM) transformers are used [22], but EM transformers are known to be bulky and are not suitable for miniaturization. To overcome this problem, an impedance transform network with LC components is used in our design.

An output stage capable of efficiently driving the transducer, either directly or through an impedance transform network, was proposed. The use of a conventional class-B linear amplifier results in a theoretical maximum efficiency of 78% [18]. In order to achieve greater efficiency, switching amplifiers that have the potential for very high efficiency [18] can be used. These amplifiers have been applied in piezoelectric transducers [19]–[21]. A drive amplifier was proposed by R. Chebli and Sawan [21] that is based on a level-shifter stage and a class D switching output. A level shifter is a commonly used technique for generating high-voltage pulses [24]–[26] and can be used to drive piezoelectric transducers and the capacitive microelectromechanical-system (MEMS) ultrasonic transducers (cMUTs). The circuit presented by R. Chebli and Sawan [21] was designed to produce output voltages up to 200 V [21]. However, the circuit operates far from the resonance region, and the circuit can only handle currents in the order of hundreds of microamperes. Another class-D amplifier using pulse-width modulation (PWM) has been reported, which can operate with high efficiency at resonance frequencies between 10 kHz and 100 kHz [19]. Despite the examples listed before, there is no straightforward design to guarantee power efficiency when a class-D switching amplifier is used for higher frequency operations. Parasitic losses become significant in these designs. Careful consideration is required to evaluate whether the extra cost of designing a switching amplifier is worthwhile. In this paper, a level shifter is used in the power-output stage to drive the transducer through an impedance transform network without using PWM.

Integrating the electronics into an IC presents yet another level of challenge. Most modern fabrication technologies have scaled down the supply voltage significantly to reduce power consumption. Consequently, voltage tolerance on most CMOS technologies has also diminished. In order to design a circuit that supports large voltage swing and large current driving capability, a high-voltage technology from Dalsa Semiconductor is used for our LIPUS chip design.

B. Impedance Transform Network

Different circuit topologies (e.g., L-match, T-match, and PI-match) can be used as impedance transform networks. An L-match circuit shown in Fig. 4(a) is used in our LIPUS generator circuit due to its simple implementation and easy integration on-chip. The impedance transform network consisting of L_{IT} and C_{IT} can effectively amplify input voltage signal by a factor of n to drive the load R_L .

The inductance L_{IT} and capacitance C_{IT} values depend on the desired voltage amplification factor n and the load resistance

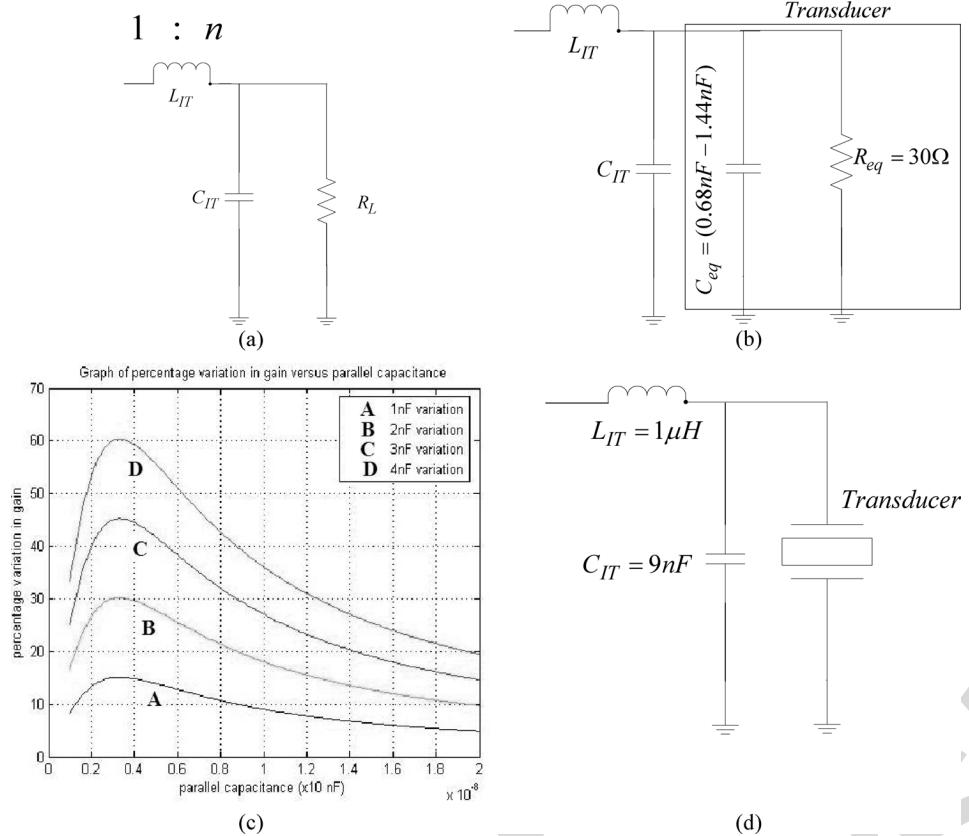


Fig. 4. (a) L-match consisting of an inductor L_{IT} and a capacitor C_{IT} connected to a load resistor R_L . (b) L-match circuit for impedance transformation. (c) Curves illustrating the percentage variation in gain due to the variation in capacitance. (d) L-match circuit for a voltage gain of three.

R_L . The input impedance of the circuit in Fig. 4(a) can be derived as

$$\overline{Z_{in}} = \frac{R_L + j\omega_s(L_{IT} - R_L^2C(1 - \omega_s^2L_{IT}C_{IT}))}{1 + \omega_s^2C_{IT}^2R_L^2} \quad (1)$$

where ω_s is the resonant frequency. It is undesirable to drive a reactive load because a reactive load can cause charge recycling and, thus, reduces power efficiency. It is favorable to create a purely resistive load for the driving circuitry at the operating frequency. Therefore, the imaginary part of (1) is made equal to zero, or $L_{IT} - R_L^2C_{IT}(1 - \omega_s^2L_{IT}C_{IT}) = 0$. By solving for L_{IT} , we obtain

$$L_{IT} = \frac{R_L^2C_{IT}}{1 + \omega_s^2C_{IT}^2R_L^2}. \quad (2)$$

With its imaginary part in (1) set to zero, (2) is reduced to

$$\overline{Z_{in}} = R_{in} = \frac{R_L}{1 + \omega_s^2C_{IT}^2R_L^2}. \quad (3)$$

By rearranging (3), we obtain

$$C_{IT} = \frac{1}{\omega_s R_L} \sqrt{\frac{R_L}{R_{in}} - 1}. \quad (4)$$

Realizing that $n = R_L/R_{in}$, (4) can be rewritten as

$$C_{IT} = \frac{1}{\omega_s R_L} \sqrt{n^2 - 1}. \quad (5)$$

In order to calculate the circuit parameter in Fig. 4(a), a simplified equivalent circuit model of the transducer is incorporated as shown in Fig. 4(b). The total capacitance C of the overall circuit is given by $C = C_{IT} + C_{eq}$. Since the value of C_{eq} significantly varies within the narrow frequency band, it is important to find a way to reduce gain variation due to the variation of C_{eq} .

To determine how gain varies with the parameters C , L , and R_L , where $C = C_{IT} + C_{eq}$, $L = L_{IT}$ and $R_L = R_{eq}$, we can rewrite (5) as

$$n^2 = (\omega_s R_L C)^2 + 1. \quad (6)$$

By rearranging (2), we obtain

$$(\omega_s R_L C)^2 + 1 = R_L^2 \frac{C}{L}. \quad (7)$$

Comparing (6) and (7), it is observed that

$$n^2 = R_L^2 \frac{C}{L} \text{ or } n = R_L \sqrt{\frac{C}{L}}. \quad (8)$$

The differential of n , or Δn can now be written as

$$\begin{aligned} \Delta n &= \frac{\delta n}{\delta R_L} \Delta R_L + \frac{\delta n}{\delta C} \Delta C + \frac{\delta n}{\delta L} \Delta L \\ &= \sqrt{\frac{C}{L}} \Delta R_L + \frac{R_L}{2\sqrt{LC}} \Delta C + \left(-\frac{R_L \sqrt{C}}{2\sqrt{L^3}} \right) \Delta L. \end{aligned} \quad (9)$$

TABLE I
C VALUES CALCULATED ACCORDING TO (5) GIVEN THAT $n = 2, 3, 4$, AND 5

Voltage Gain n	C (nF)
2	6.13
3	10.0
4	13.7
5	17.3

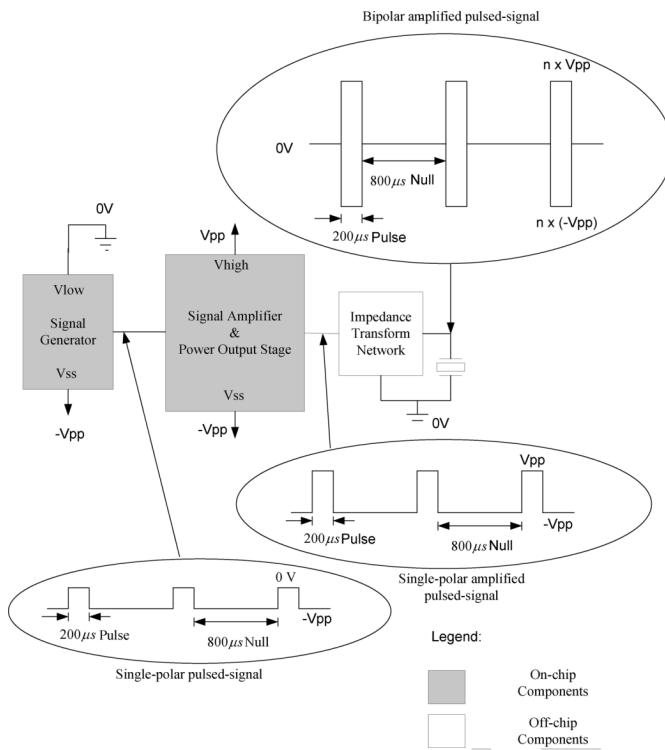


Fig. 5. Circuit generating a bipolar pulse-modulated signal from a single-polar pulsed signal.

Dividing (9) by (8), we obtain (10) that describes the percentage gain variation

$$\frac{\Delta n}{n} = \frac{\Delta R_L}{R_L} + \frac{1}{2} \frac{\Delta C}{C} + \left(-\frac{1}{2} \right) \frac{\Delta L}{L}. \quad (10)$$

The variation in (10) can be further reduced by reducing the percentage variation of parameters R_L , C , and L . For instance, the value of C due to variation in C_{eq} can be fixed because we can set C_{eq} between 0.68 nF and 1.44 nF. As a result, it is plausible to reduce the percentage variation $\Delta n/n$ by using a larger C . This is equivalent to a large voltage gain n , according to (8). Fig. 4(c) illustrates the effect of variation in capacitance on the percentage variation in gain.

From the graph, it is obvious that the percentage variation in gain is the greatest when $C = 3$ nF. As expected, larger capacitance reduces the percentage variation in gain. Next, the value of C can be determined by using (5), $C = (1/\omega_s R_L) \sqrt{n^2 - 1}$.

The values of n and the corresponding values of C are summarized in Table I, where $R_L = R_{eq} = 30 \Omega$ and ω_s is the resonant angular frequency $\omega_s = 2\pi(1.5 \times 10^6)$ [rad/s].

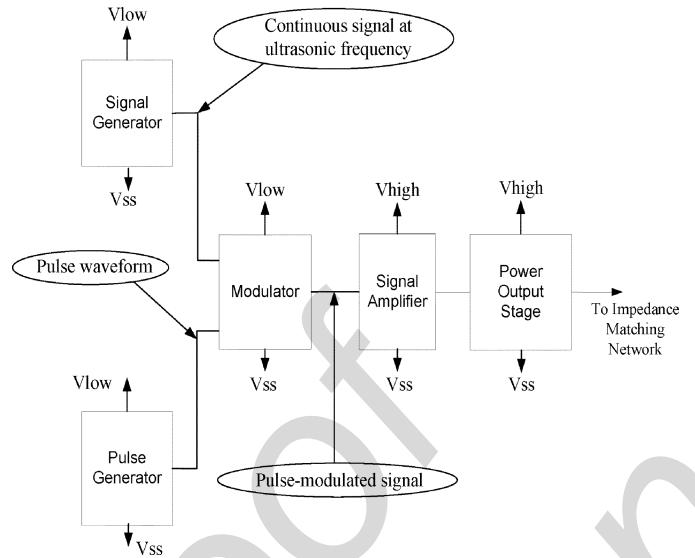


Fig. 6. Proposed single-polar pulse-modulated signal generator architecture.

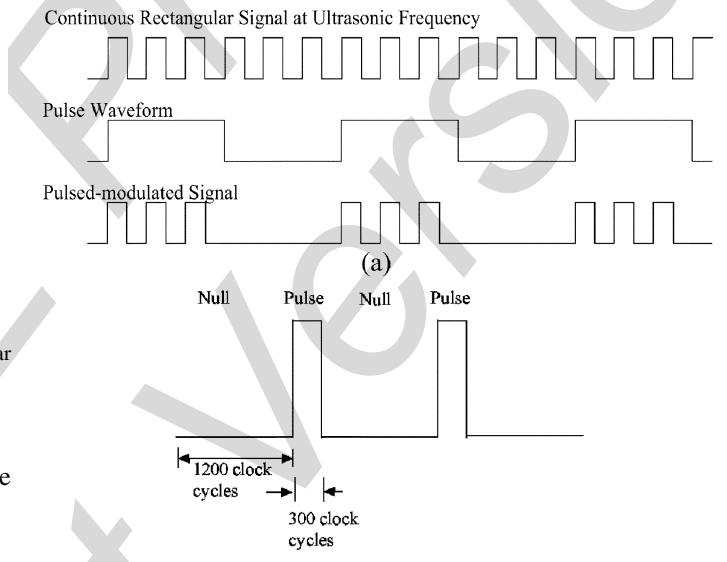


Fig. 7. (a) Illustration of pulse-modulated signal waveform generation. (b) Pulse diagram.

Three are chosen again, which requires a total parallel capacitance C of 10 nF. Since C_{IT} in $C = C_{IT} + C_{eq}$ can be measured to great accuracy using a digital multimeter (DMM), the uncertainty mainly comes from the C_{eq} term, which can also be easily quantified. By approximating C_{eq} to be 1 nF, somewhere in the known range of 0.68 nF to 1.44 nF, we can obtain the maximum variation of $C_{eq} = 0.44$ nF. From Fig. 4(c), we can see that the percentage variation in gain for 1 nF variation is about 10%. Consequently, the percentage variation in gain contributed by 0.44-nF uncertainty is estimated to be less than 10%. Following (2), we obtain $L_{IT} = L = R_L^2 C / (1 + \omega_s^2 C^2 R_L^2) = 1.0 \mu\text{H}$. The resulting L-match impedance transform network with calculated inductance and capacitance values is shown in Fig. 4(d).

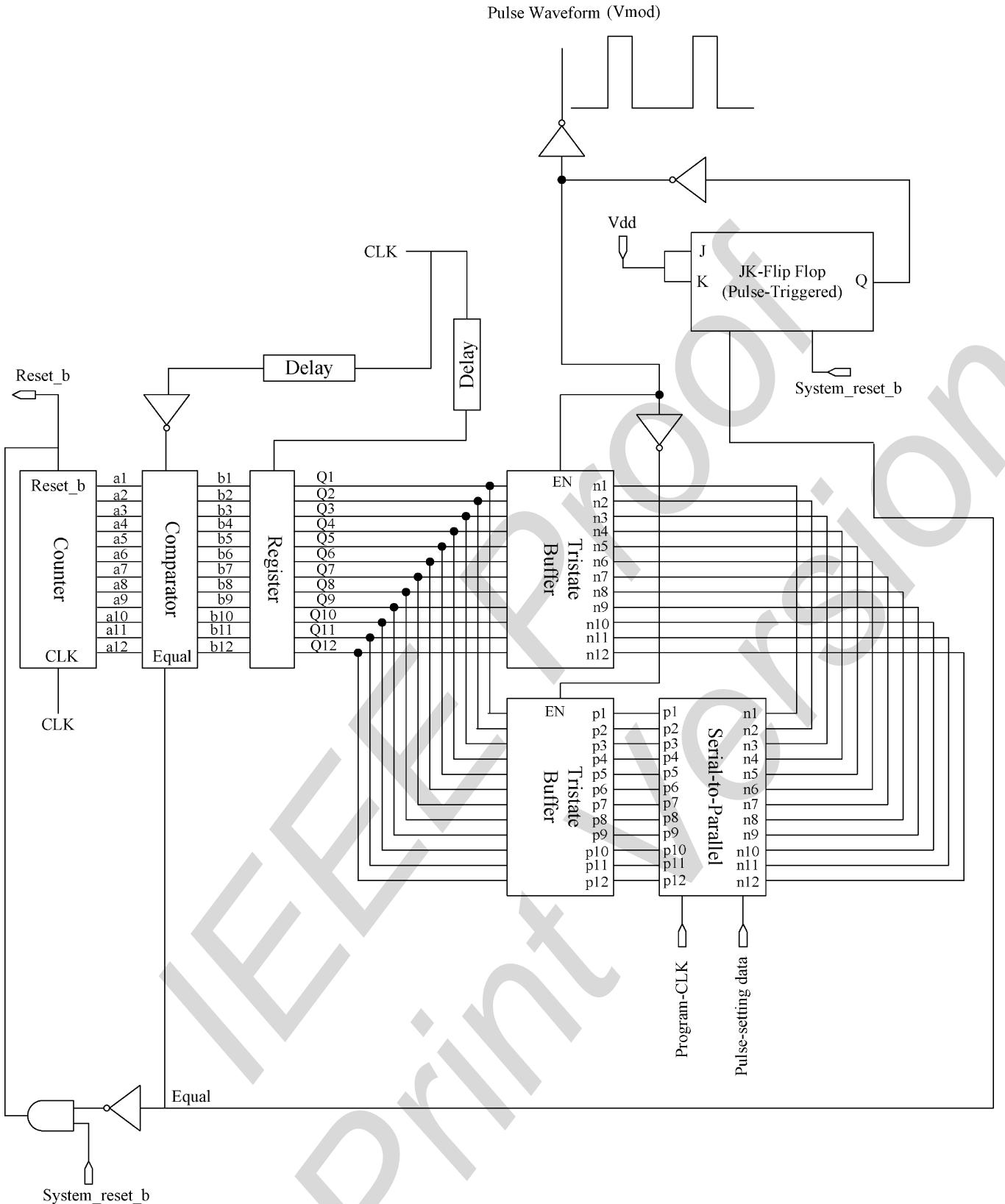


Fig. 8. Pulse generator circuitry.

C. Pulse-Modulated Signal Generator Integrated Circuit

Our design goal for the targeted IC is to produce pulse-modulated signals with sufficient amplitude to drive a piezoelectric

transducer through the impedance transform network designed in the previous section. Next, we present a design to vary signal frequency and the corresponding pulse duty cycle. To simplify the design, we choose a single-polar voltage signal as the output

instead of a bipolar signal as shown in Fig. 5. The single-polar signal is then amplified and converted to a bipolar signal by using the impedance transform network designed in the previous section. In this biasing scheme, the ground pin V_{ss} of the chip is connected to the negative rail ($-V_{pp}$) of the voltage supply. The power-supply pins V_{low} and V_{high} are connected to the voltage-supply ground (0 V) and the positive rail (V_{pp}), respectively. The chip output $-V_{pp}$ swings back and forth between, but not necessarily reaching, $-V_{pp}$ and V_{pp} during an oscillation period. Both the impedance transform network and the transducer have one end connected to ground as shown in Fig. 5.

Our preliminary investigation showed that 7.6-V voltage amplitude is required to generate sufficient acoustic power intensity. Since the impedance transform network provides a gain of three at resonance, a sinusoidal voltage of amplitude 2.53 V (peak-to-peak magnitude of 5.06 V) is needed in the IC. This voltage requirement is beyond the normal operating regime of conventional CMOS fabrication technologies and special high-voltage technology is required. As a result, we selected the 0.8- μ m CMOS/DMOS technology from Dalsa Semiconductor, Inc. for our chip fabrication. Dalsa technology enables us to use low-voltage CMOS and high-voltage DMOS processes capable of handling high-voltage designs beyond 100 V. The technology was expected to offer a solution for integrating a low-voltage digital controller and a high-voltage driver on a chip.

D. Pulse-Modulated Signal Generator Architecture

The proposed architecture of the single-polar pulse-modulated signal generator for on-chip implementation is shown in Fig. 6. The signal generator produces a continuous rectangular signal at the desired ultrasonic frequency. The pulse generator produces a rectangular pulse that corresponds to the envelope of the resulting pulse-modulated signal. As its name implies, the modulator modulates the continuous rectangular ultrasonic signal with the pulse to generate a pulse-modulated signal waveform as illustrated in Fig. 7(a). A signal amplifier in Fig. 6 is used to amplify the pulse-modulated signal waveform to the desired level. A power-output stage is integrated to provide sufficient current to drive the transducer through the impedance-matching network. Note that two separate supply voltages are needed to ensure that the device operates properly. V_{low} is the low-voltage supply to power the signal generation, pulse generation, and modulation blocks. V_{high} is used by the signal amplifier and the power-output stage to control the amplitude of the final amplified pulse-modulated signal waveform for driving the off-chip impedance transform network.

Fig. 7(a) shows an example in which each pulse only contains three cycles of rectangular waveforms. A method to control the pulse length, pulse repetition rate, and ultrasonic signal frequency in the targeted LIPUS generator is needed. In order to achieve a flexible design, a voltage-controlled oscillator is used to generate a tunable ultrasonic frequency. For instance, to ensure a specific duty cycle, we provide an embedded mechanism to count the number of clock cycles so that the system knows when to enter the “null” state or the “pulse” operation state. To generate the desired 1.5-MHz signal frequency, 1-kHz pulse repetition rate, and 20% duty cycle required in our design,

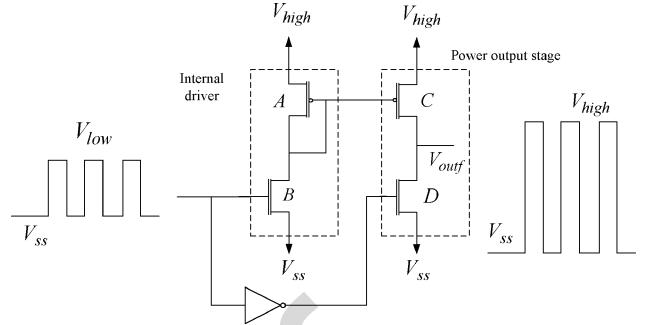


Fig. 9. Level-shifter circuit.

each pulse will contain 300 clock cycles of 1.5-MHz oscillations. The pulses are separated by 1200 clock cycles of “null” period. This schematic diagram is shown in Fig. 7(b).

III. CHIP DESIGN AND IMPLEMENTATION

In this section, a detailed low-level realization of the architecture proposed in Fig. 6 is presented. Since some of the components are pretty standard, we summarize the design as follows (we will mainly focus on the design of the signal amplifier and power-output stage in Section III-A).

- 1) The signal generator is realized by using a ring voltage-controlled oscillator (VCO), which is also used to generate the clock signals (CLK) for the entire chip.
- 2) The pulse generator is realized using a counter, a comparator, two tristate buffers, and a JK-Flip Flop shown in Fig. 8.
- 3) The modulator that modulates the continuous ultrasonic signal with a pulse waveform is easily realized by using an AND gate.

A. Signal Amplifier and Power-Output Stage

In order to amplify a low-voltage digital control signal to a high-voltage driving signal, a level shifter is needed. The level shifter can achieve both functions of the voltage amplifier and the power-output stage. Level-shifting techniques have been studied in [24]–[26] and applied to CMOS/DMOS [**Please define “DMOS”**] technology for generating high voltages [27]. Our design is directly adapted from [27]. As shown in Fig. 9, the level shifter is symbolically realized by using two p-channel DMOS transistors (A and C) and two n-channel DMOS transistors (B and D). Transistors A and B are responsible for generating a suitable driving voltage to turn transistor C on and off. The operation of transistor D is directly controlled by the digital input to the level shifter through an inverter. Transistors C and D drive the piezoelectric load through an impedance transform network. For this reason, transistors C and D are collectively labeled the “output power stage” while A and B are called “internal driver.”

A sinusoidal voltage of 2.53 V is needed to generate a sinusoidal voltage with an amplitude of 7.6 V across the transducer since the amplification factor is three in the impedance transform network. Since the level shifter is designed to generate a rectangular signal instead of a sinusoidal signal, it is instructive to consider the Fourier series of a rectangular waveform containing information in the coefficient of its constituent

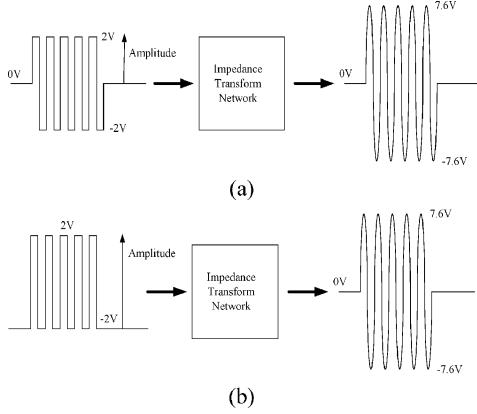


Fig. 10. (a) Bipolar rectangular waveform to bipolar sinusoidal waveform conversion. (b) Single-polar rectangular waveform to bipolar sinusoidal waveform conversion.

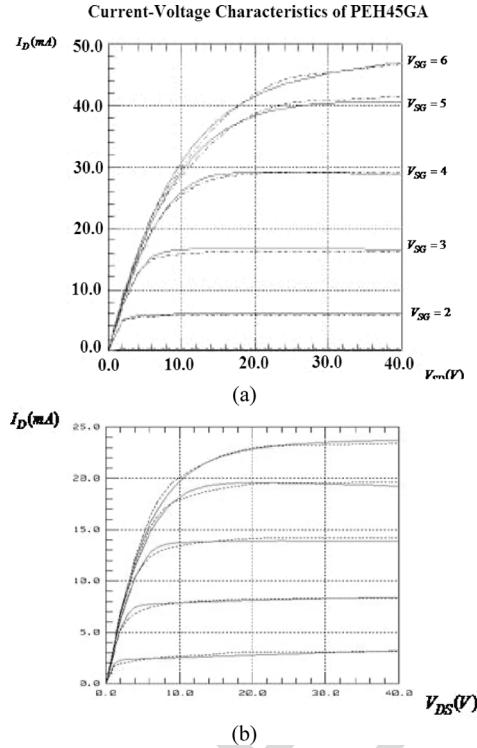


Fig. 11. (a) Plots of drain current versus source-to-drain voltage for PEH45GA EDMOS: measured (solid line) versus simulated (dotted line) curves provided by Dalsa Semiconductor, Inc. in [28]. (b) Plots of the drain current versus drain-to-source voltage for NDH16GC LDMOS: measured (solid line) versus simulated (dotted line) curves provided by Dalsa Semiconductor, Inc. in [28].

harmonics. The Fourier series for a rectangular waveform is $\text{rect}(t) = (4/\pi) \sum_{n=1,3,5,\dots}^{\infty} (\sin(2\pi nt/T))$, where T is the period of the rectangular waveform. This suggests that a rectangular bipolar wave of amplitude $2.53 \text{ V} \bullet \pi/4 \approx 2 \text{ V}$ can be used instead of a 2.53-V sinusoidal signal to generate a voltage of 7.6-V amplitude across the transducer as shown in Fig. 10(a). Since the level shifter designed herein generates a single-polar waveform, an amplitude of 4 V is needed as shown in Fig. 10(b).

It was decided that transistor model PEH45GA [28] would be used for the p-channel DMOS (A and C) while the NDH16GC

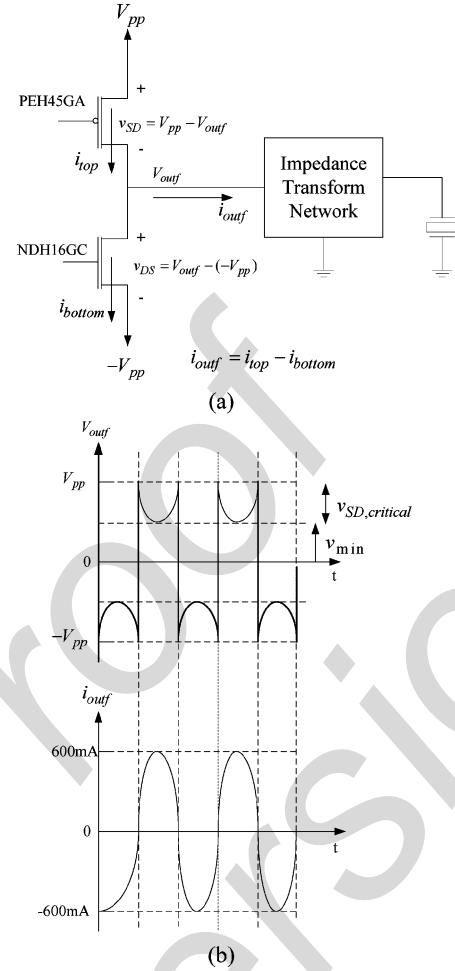


Fig. 12. (a) Illustration of currents and voltages in the power-output stage. (b) Expected output voltages and currents at the V_{outf} node of the pulse-modulated signal generator circuit.

model [28] would be used for the n-channel DMOS (B and D), owing to their relatively high current-to-size ratios. The electrical characteristics of these two transistors are shown in Fig. 11(a) and (b).

Considering the power-output stage of the level-shifter circuit, the source-to-drain voltage of PEH45GA transistor v_{SD} and drain-to-source voltage of the NDH16GC transistor v_{DS} are labeled in Fig. 12(a) for illustration. The drain currents i_D of PEH45GA and NDH16GC transistors are, respectively, labeled as i_{top} and i_{bottom} in Fig. 12(a). By Kirchhoff's current law $i_{outf} = i_{top} - i_{bottom}$, it is assumed the two types of transistors do not conduct simultaneously. Hence $i_{outf} = i_{top}$ when $i_{outf} > 0$, and $i_{outf} = -i_{bottom}$ when $i_{outf} < 0$. In other words, current i_{outf} delivered to the impedance transform network entirely comes from the PEH45GA transistor, while current i_{outf} from the impedance transform network is completely sunk into the NDH16GC transistor.

The voltage V_{pp} and the number of transistors to use in the power-output stage remains to be determined. The input impedance of the load is $|Z_{in}| = R_L/n^2 = 30 \Omega/3^2 = 3.33 \Omega$. From our previous Fourier analysis, a signal of 2-V amplitude is sufficient to generate a 7.6-V voltage on the load. Therefore, driving a sinusoidal signal of 2-V amplitude across the load

results in a current of $2 \text{ V}/3.33 \Omega = 600 \text{ mA}$. Since the load is mostly resistive in the vicinity of resonant frequency, the driving voltage is theoretically in phase with the current. Nevertheless, the power-output stage does not generate a sinusoidal signal. If only small current is required by the load, a rectangular voltage waveform is sufficient. However, due to the considerably large current required for the LIPUS generator, a larger v_{SD} is needed by the PEH45GA transistor to sustain 600-mA peak current. It is expected that a rectangular waveform with a sizable voltage dip in the middle would be produced. Due to the importance of reserving sufficient v_{SD} to sustain high peak current, a new term $v_{SD,\text{critical}}$, which corresponds to v_{SD} is needed for denotation when the output is in the "U"-shaped curve shown in Fig. 12(b). From Fig. 12(b), we obtain a magnitude for the "U" curve of $v_{SD,\text{critical}} = V_{pp} - v_{\min}$, where v_{\min} is the magnitude of the waveform at the bottom of the "U"-shaped waveform. To guarantee that the new waveform contains the first harmonics with sufficient amplitude (i.e., at least 2.53 V), v_{\min} must be greater than 2 V regardless of $v_{SD,\text{critical}}$, based on the principle of superposition and Fourier analysis.

The problem now becomes how large a $v_{SD,\text{critical}}$ is feasible for the current generation and how many transistors must be used for a chosen v_{SD} . From Fig. 11(b), it is observed that i_D is proportional to v_{SD} in the triode operation region when v_{SD} is small. Furthermore, as V_{pp} increases, the current i_D that each transistor can source also increases. As a result, there is a tradeoff between V_{pp} and the number of transistors. To use smaller V_{pp} , more transistors are needed (which translates to larger chip size) because each transistor sources less current and, thus, results in lower v_{SD} . We chose $V_{pp} = 4 \text{ V}$, which provides sufficient current with an acceptable number of transistors. This choice implies that the transistors need to source a current of amplitude 600 mA with a v_{SD} of 2 V. From Fig. 11(a), 8 mA of current can be generated with one PEH45GA at $v_{SD} = 2 \text{ V}$. Hence, 75 transistors need to be connected in parallel, which is acceptable because they add up to an area of only 3.99 mm^2 (each PEH45GA has an area of $53245 \mu\text{m}^2$ [28]). The number of transistors is rounded up to 80 in the design.

For symmetry, the negative rail voltage is set to -4 V . Since the rectangular voltage swings as low as -2 V , the NMOS transistors need to sink 600 mA of current when $v_{DS} = 2 \text{ V}$. However, each NDH16GC transistor can only sink 5 mA of current at $v_{DS} = 2 \text{ V}$ [refer to Fig. 11(b)]. One-hundred twenty transistors are used, or collectively, NDH16GC consumes only 1.476 mm^2 of chip area (each NDH16GC has an area of $12388 \mu\text{m}^2$ [28]).

The final design at the power-output stage is shown in Fig. 13. In our previous calculations, we assume that the transistors PEH45GA and NDH16GC can be fully turned on with $v_{GS} = 4 \text{ V}$ for NDH16GC and $v_{SG} = 4 \text{ V}$ for PEH45GA, respectively. This is achieved by appropriately sizing transistors A and B in order to determine the multiplicity factor m and n in Fig. 14 to generate v_x with sufficient swing. Transistors A and B are specifically designed so that voltage v_x swings low enough (i.e., $v_x < 0$) to ensure that it fully turns on transistor C. On the other hand, it has to be ensured that $v_x > -1 \text{ V}$ because the PEH45GA transistor has a voltage limitation of 5 V based on the high-voltage transistors provided by Dalsa Semiconductor,

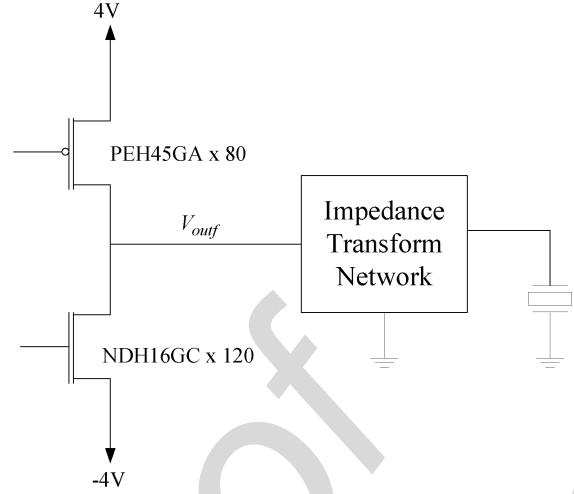


Fig. 13. Final design at the power-output stage.

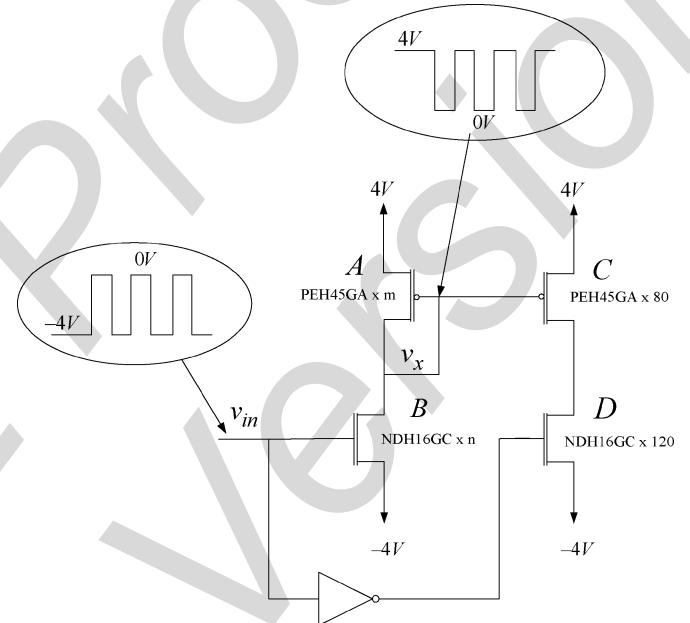


Fig. 14. Illustration of v_x in the level-shifter circuit.

Inc. [28]. If v_x swings to a voltage as low as 0 V, a drain current of $m*18 \text{ mA}$ will be developed. Similarly, a current of $n*10 \text{ mA}$ will flow into node B. According to Kirchhoff's current law, we can solve for the lowest integers m and n that satisfy $m*18 \text{ mA} = n*10 \text{ mA}$, which gives $m = 5$ and $n = 9$. Using these values, we can simulate to obtain a desirable v_x . Having discussed the design of all the modules in the proposed LIPUS generator, next we simulate the entire circuit functionalities to verify its performance.

IV. IC SIMULATION AND TESTING

A. Circuit Simulation Results

The schematic design of the pulse-modulated signal generator was simulated to verify its functionalities and its current driving capability. The simulation tool that we use is Cadence Spectre. V_p and V_n of the ring oscillator were set to 0.7 V and 2.3 V, respectively to produce 1.5-MHz oscillation. A V_{high} of

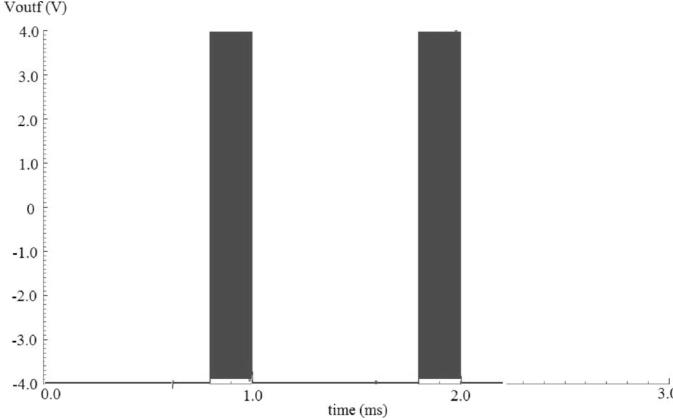


Fig. 15. Simulated output pulses, each $200\ \mu\text{s}$ wide and separated by $800\ \mu\text{s}$.

4 V, which translates to a rail-to-rail voltage of 8 V by symmetry, was applied to simulate the circuit's ability to produce sufficient voltage swing. The circuit was programmed to produce 300 clock cycles of oscillations and 1200 clock cycles of “null” periods as shown in Fig. 15. The simulated pulse waveform is shown in Fig. 15, in which the generated pulses (rectangular bars in figure) have a pulse repetition rate of 1.0 kHz and a pulsedwidth of $200\ \mu\text{s}$. The output voltage V_{outf} swings from $-4\ \text{V}$ to $4\ \text{V}$ during the “pulse” phase, and stays at $-4\ \text{V}$ during the “null” phase as predicted. Nevertheless, due to the densely displayed waveforms within a “pulse” phase shown in Fig. 15, it is necessary to zoom into each pulse so that qualitative measurements on the oscillating voltage can be made.

A zoomed-in pulse allows us to closely examine current and voltage waveforms. Fig. 16(a) shows the simulated waveform of the voltage signal at V_{outf} . As expected, the waveforms display a “U”-shaped voltage dip in the middle. The amplitude of the voltage across the transducer slightly exceeds the minimum requirement of $7.6\ \text{V}$. The simulated current waveform is also shown in Fig. 16(b). The current amplitude reaches approximately $300\ \text{mA}$, which is expected to give the voltage amplitude of about $9\ \text{V}$. Having verified that the circuit meets the LIPUS design specifications, we layout the design for fabrication.

B. Circuit Layout

The final LIPUS signal generator chip, which contains transistors as summarized in Table II, is assembled in a layout measuring $2.8\ \text{mm}$ in width and $4.0\ \text{mm}$ in length, as shown in Fig. 17(a). Fig. 17(b) shows the picture of the fabricated LIPUS signal generator chip in a 40-pin dual-inline package (DIP40).

C. Chip Testing

The pulse-modulated signal generator chip is integrated on a breadboard for testing. The circuit diagram of the testing circuitry is shown in Fig. 17(c) and a photograph of the board-level testing circuit is shown in Fig. 17(d). The power-supply subsystem and the programming subsystem are described in the following subsections.

1) *Voltage Supply Subsystem:* The voltage supply subsystem consists of a pair of variable voltage regulators (LM317 and LM337) used to generate a dual-rail power supply of $\pm 4\ \text{V}$. Each voltage regulator is powered by a 9-V battery, which was

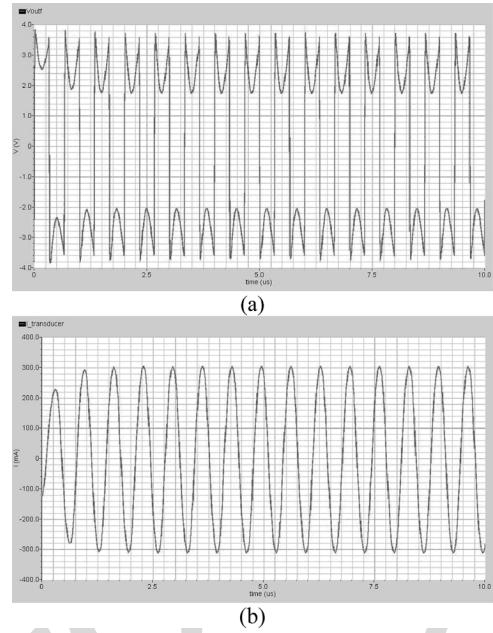


Fig. 16. (a) Simulated waveform showing the voltage at V_{outf} . (b) Simulated waveforms showing the current flows into the piezoelectric transducer.

chosen just for convenience. Another two LM317 chips are used to generate V_n and V_p , which are adjustable by using the potentiometers, and to set the clock frequency of the entire circuit.

2) *Serial Programming Subsystem:* An AVR butterfly board, which contains an Atmel Mega169PV microcontroller, is used to generate the pulse-setting serial stream and a corresponding programming clock for the fabricated IC. During initialization, 10010110000_2 (300 in the decimal number system) and 00100101100_2 (1200 in the decimal number system) are clocked into the pulse-setting module of the IC serially whenever the Atmel Mega169PV microcontroller is powered up. The fabricated pulse-modulated signal generator chip is programmed to output a pulsed-modulated ultrasonic signal of a 20% duty cycle (i.e., 300 clock cycles of oscillation, and 1200 clock cycles of “null period”).

3) *Circuit Test and Measurements:* Upon power up and completion of the initialization of the AVR butterfly, the voltages across the transducer are probed and displayed on an oscilloscope. V_n and V_p are then tuned to ensure that the ultrasonic signal frequency of $1.5\ \text{MHz}$ is generated at the CLK pin of the chip. The pulse duty cycle measured at the V_{outf} pin is 20% as expected, and the pulse waveform is shown in Fig. 18.

The rectangular waveform displays voltage dips in the middle of each rectangle, which is in line with our design and simulation. However, the measured waveforms have a “V”-shaped dip instead of a predicted “U”-shaped dip. This is attributed to a steep supply-voltage drop that occurs when a large amount of current is drawn from the power-supply subsystem. Fig. 19 shows the voltage (A) across the transducer and current (B) into the transducer. As expected, the pulse repetition rate is $1\ \text{kHz}$ and duty cycle is 20% duty.

Finally, an ultrasound power meter is used to measure the acoustic power of the LIPUS chip generated. By fixing the pulse duty cycle and supply voltage, acoustic power measurement is

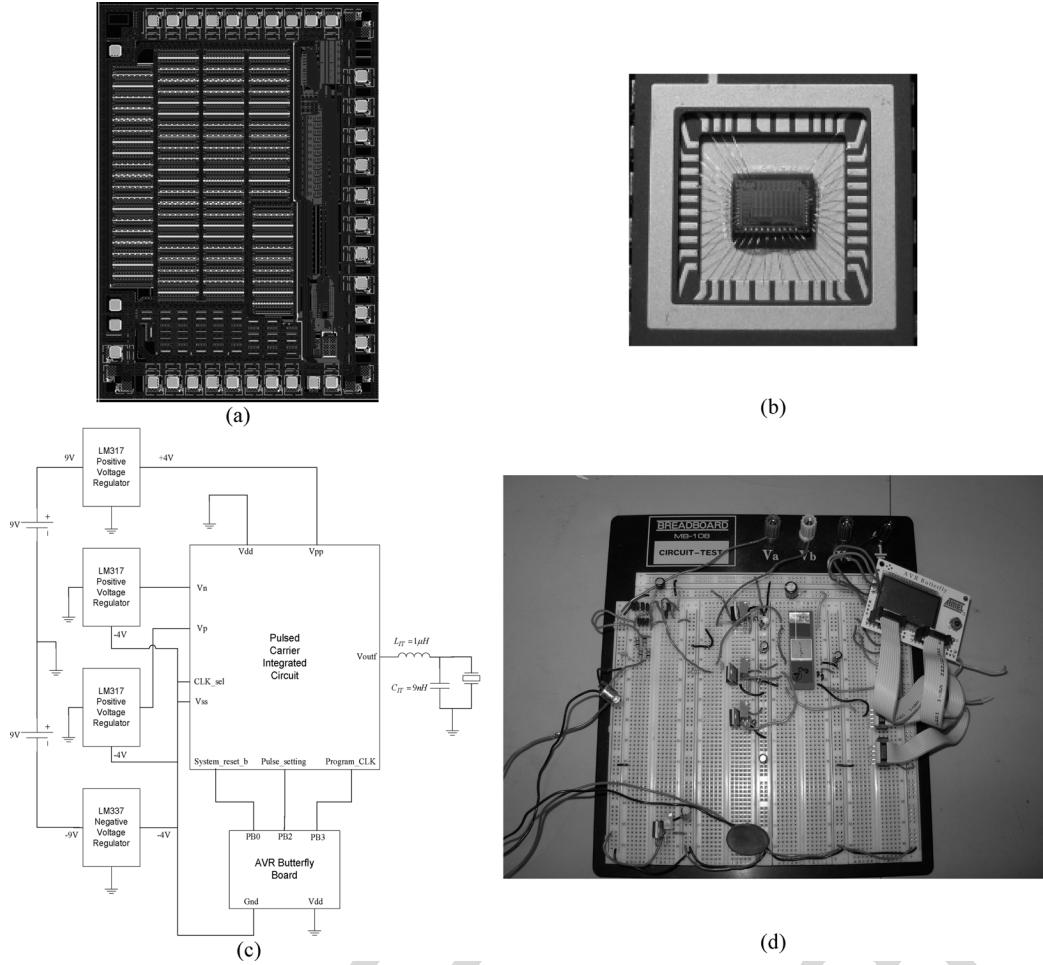


Fig. 17. (a) LIPUS signal generator IC layout. (b) Picture of the fabricated LIPUS signal generator chip in a 40-pin dual-in-line package (DIP40). (c) Testing circuit diagram. (d) Photograph of the board-level testing circuit.

TABLE II
SUMMARY OF THE TRANSISTORS USED IN THE LIPUS SIGNAL GENERATOR CHIP.

Transistor Types	Count (unit)
Low-voltage NMOS	2128
Low-voltage PMOS	2217
N-Channel LDMOS (NDH16GC)	129
P-Channel EDPMOS (PEH45GA)	85

performed for the following signal frequencies: 1.46 MHz, 1.48 MHz, 1.52 MHz, and 1.55 MHz. The measurement results are summarized in Table III.

From the measurement results, the maximum power of 118 mW is generated at 1.52 MHz. This translates to an intensity of 66.7 mW/cm², which is more than enough to meet the design specifications. Less power can easily be obtained by lowering the voltage regulators to supply a smaller dc supply voltage. It is also observed from Table II that within the frequency range of 1.50 MHz to 1.52 MHz, the power level reaches a plateau. It is, therefore, advisable to operate the circuit within this plateau to minimize power variation due to frequency

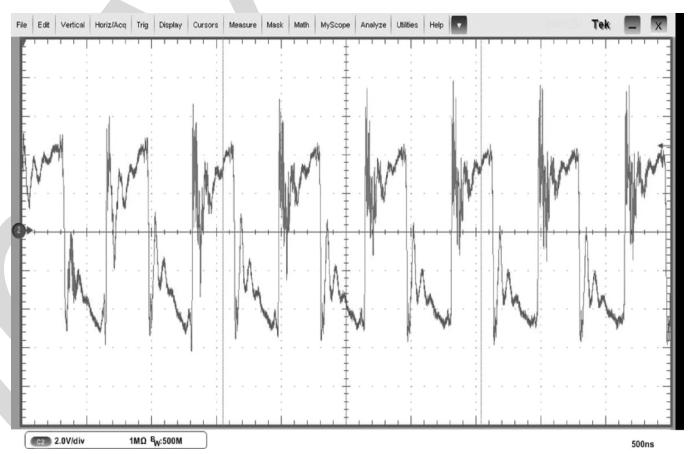


Fig. 18. Voltage waveforms at the V_{outf} pin of the LIPUS signal IC.

drift. The overall system's (including the transducer's) power consumption excluding the power of the voltage regulators is estimated at 800 mW on average, which gives an overall power efficiency of $\eta_{\text{overall}} = 14\%$. As previously determined, the transducer efficiency $\eta_{\text{transducer}}$ at 1.5 MHz was estimated to be approximately 20%. Therefore, it can be concluded that

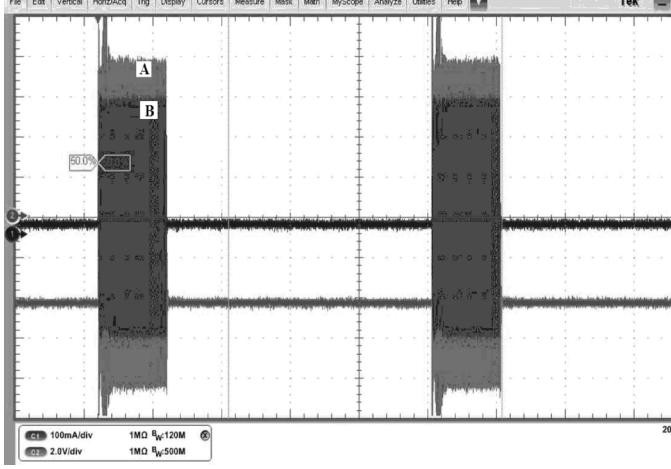


Fig. 19. Voltage A (a larger amplitude waveform) is overlapped with current B (a smaller amplitude waveform) pulses with microseconds pulse width and 800- μ s null width (color online).

TABLE III
ACOUSTIC POWER MEASURED WITH 20% DUTY CYCLE FOR DIFFERENT OPERATING FREQUENCIES

Signal Frequency (MHz)	Acoustic Power (mW)
1.46	72
1.48	86
1.50	116
1.52	118
1.55	110

TABLE IV
PERFORMANCE SUMMARY

Attribute	Performance
Chip size	2.8mm*4.0mm
Operating clock frequency	1.5MHz
Ultrasound carrier frequency	1.5MHz
Pulse repetition rate	1.0kHz
Duty Cycle	20%
Supply Voltage	3.3V
Overall Power Consumption (chip and transducer)	800mW
Power Consumption (chip)	220mW
Power Efficiency of Chip (at 1.5MHz)	70%

$200/200\eta_{electronics} \approx 14/20 \times 100\% = 70\%$. A summary of the chip performance is given in Table IV.

V. CONCLUSION AND FUTURE WORK

A LIPUS generator has been designed and implemented, which is composed of a power-supply subsystem, an impedance-matching network, a piezoelectric transducer, and an IC capable of pulse-modulated signal generation. The IC was fabricated using Dalsa 0.8 μ m high-voltage technology. The power-supply subsystem and impedance-matching network are implemented by using discrete components. An L-match

circuit is used to realize the impedance matching network, which allows the accurate delivery of power to the transducer for LIPUS generation. The LIPUS generator was verified and functions correctly. Even though the LIPUS generator was designed for 1.5-MHz pulsed-ultrasound with 1-kHz pulse repetition rate and 20% pulse duty cycle, it could be reprogrammed using an AVR butterfly board to generate pulsed-ultrasound at different frequencies, pulse repetition rates, and duty cycles. At the designated operating state, the generator produces an ultrasound up to 116 mW. The power efficiency of the circuit, excluding the power-supply subsystem, is estimated to be about 70%. The generator can also be tuned to output LIPUS waveforms at lower power by reducing the supplied voltage.

To achieve further miniaturization, future work will involve integrating the impedance-matching network and the power-supply subsystem on a chip to obtain a complete system-on-a-chip (SOI) design [29]. Our eventual medical application is to prevent patients' tooth-root resorption and to enhance dental tissue repair. We envision the device will be one-time use and affordable by middle-class patients. Since the final device will be user friendly and will have built-in wireless communication capability, the treatment can be performed by patients at home, and treatment data can be remotely monitored by dentists' offices. Since this device, to our best knowledge, is the first of its kind to help repair root resorption and enhance dental repair, the device can significantly enhance standards of care and minimize or prevent tooth loss due to trauma or severe root resorption by prolonged orthodontic treatment. We are testing the device in animals and seeking approval from the Health Canada before we can try it on humans.

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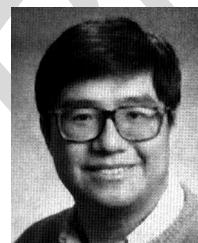
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