

EE 3124 Project #1  
Class A Power Amplifier Design  
Jaeha Huh

# EE3124 Design Project!

## Class A Power Amplifier Design

### Hand Calculation

Jaeha Huh

A) Given = Peak to Peak current swing at  $R_L$ ,

$$I_{L, pk-to-pk} = 250 \text{ mA}$$

$$\text{So, } I_{L, pk} = 125 \text{ mA}$$

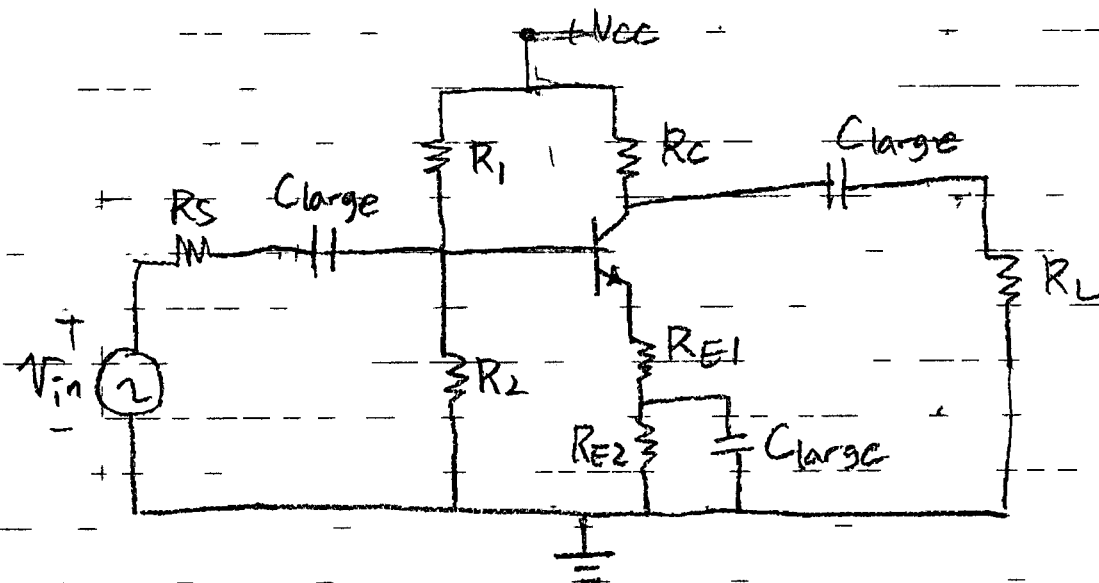
$$I_{L, pk} = I_{C, pk} \left( \frac{R_C}{R_C + R_L} \right) \Rightarrow 125 \text{ mA} = I_{C, pk} \left( \frac{R_C}{R_C + 16 \Omega} \right)$$

$$\text{Let, } I_{C, pk} = 150 \text{ mA} \text{ then } 125 \text{ mA} = 150 \text{ mA} \left( \frac{R_C}{R_C + 16 \Omega} \right)$$

$$\Rightarrow \boxed{R_C = 80 \Omega}$$

•  $I_{CQ}$  with Max swing

$$I_{CQ} = \frac{V_{CC}}{R_{DC} + R_{AC}}$$



$$R_{DC} = R_C + R_{E1} + R_{E2}$$

$$R_{AC} = (R_C \parallel R_L) + R_{E1}$$

$$I_{CQ} = 125 \text{ mA}$$

$$\text{Let } \boxed{V_{CC} = 18 \text{ V}}, \text{ then}$$

$$Q. 125 \text{ A} = \frac{18 \text{ V}}{R_{DC} + R_{AC}}$$

$$\text{So, } R_{DC} + R_{AC} = 144$$

$$(R_C + R_{E1} + R_{E2}) + ((R_C || R_L) + R_{E1}) = 144$$

$$(80 + R_{E1} + R_{E2}) + ((80 || 16) + R_{E1})$$

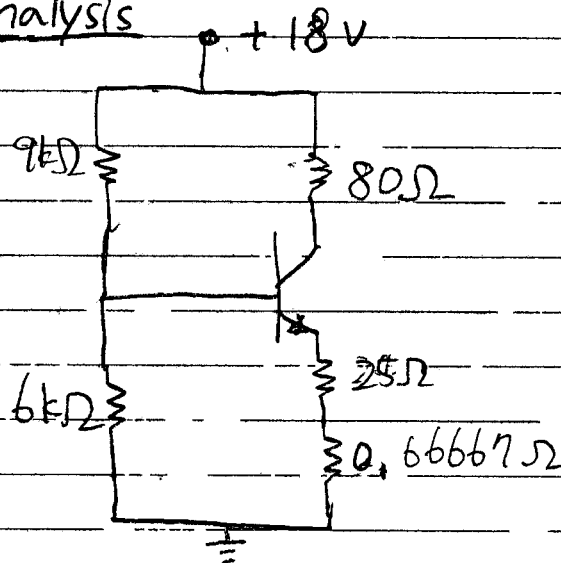
$$= 80 + R_{E1} + R_{E2} + (13.33333) + R_{E1} = 144$$

$$2 R_{E1} + R_{E2} = 144 - 93.33333 = 50.66667$$

$$\Rightarrow \text{Let } 2R_{E1} = 50 \Rightarrow \begin{cases} R_{E1} = 25 \Omega \\ R_{E2} = 50.6667 - 50 \\ R_{E2} = 0.66667 \Omega \end{cases}$$

$$\text{Pick } R_1 = 9k\Omega \quad R_2 = 6k\Omega$$

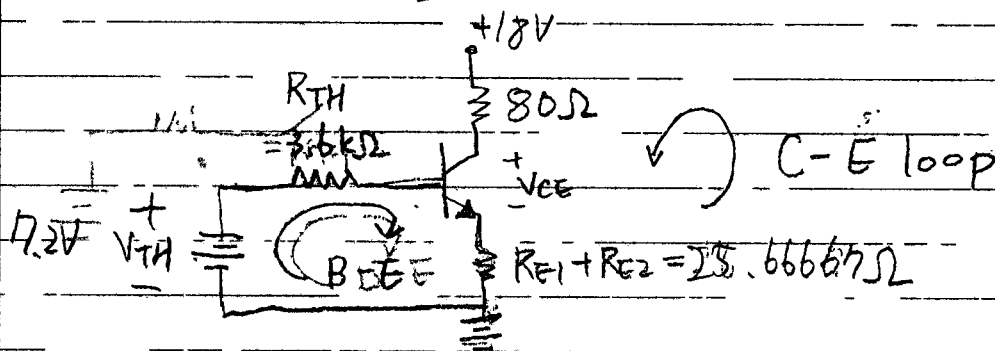
### • DC Analysis



$$V_{TH} = 18V \left( \frac{6k\Omega}{15k\Omega} \right) = 7.2V$$

$$R_{TH} = R_1 || R_2 = \frac{9k \times 6k}{15k}$$

$$= 3.6k\Omega$$



① KVL: B-E loop

$$0 = -V_{TH} + R_{TH}(I_{BQ}) + V_{BEQ} + (25.66667)(I_{EQ})$$

$$I_{EQ} = (\beta + 1) I_{BQ} \quad \beta = 200 - \text{Given}$$

$$0 = -V_{TH} + R_{TH}(I_{BQ}) + V_{BEQ} + (25.66667)(\beta + 1) I_{BQ}$$

$$0 = -17.2 + (3.6k)(I_{BQ}) + 0.7 + (25.66667)(201)I_{BQ}$$

$$I_{BQ} = \frac{17.2 - 0.7}{3600 + 5159} = \frac{6.5}{8759} = 0.000742A \approx 0.742mA$$

$$I_{CQ} = \beta(I_{BQ}) = (200)(0.742mA) = 0.148A$$

$$I_{EQ} = (\beta + 1)(I_{BQ}) = (201)(0.725mA) = 0.149A$$

② KVL: C-E loop

$$0 = -V_{CC} + R_C(I_{CQ}) + V_{CE} + R_E(I_{EQ})$$

$$\begin{aligned} V_{CE} &= V_{CC} - R_C(I_{CQ}) - R_E(I_{EQ}) \\ &= 18 - 80(0.148) - 25.66667(0.149) \\ &= 18 - 11.84 - 3.824 \\ &= 2.336 \end{aligned}$$

$$\therefore V_{CEQ} = 2.336V$$

$$V_{CEQ} > V_{CE, sat} \checkmark$$

$$2.336V > 0.3V$$

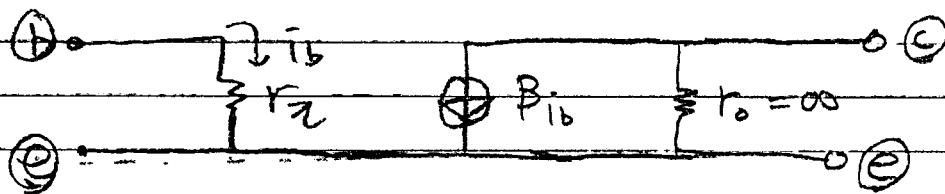
$\Rightarrow$  Forward Active

③  $r_o \neq \infty$

$$r_{\pi} = \frac{\beta V_T}{I_{CQ}} = \frac{200(26mA)}{(148mA)} = 35.14$$

$$g_m = \frac{\beta}{r_{\pi}} = \frac{200}{35.14} = 5.692$$

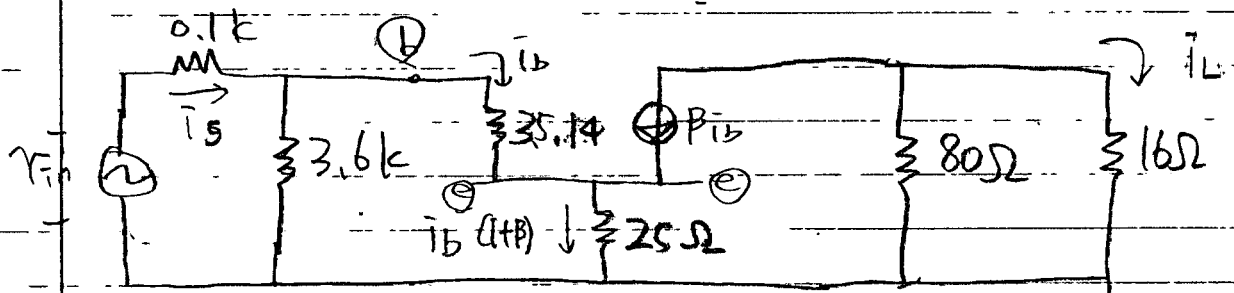
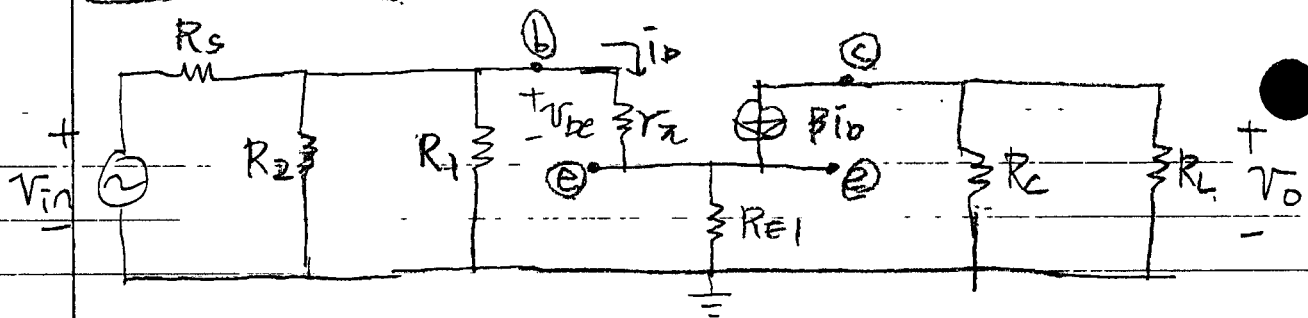
④ Small Signal



transistor model

Plug transistor model into circuit

## ⑤ AC Analysis



$$35.14 + 25(201) = 4859.86 \Omega$$

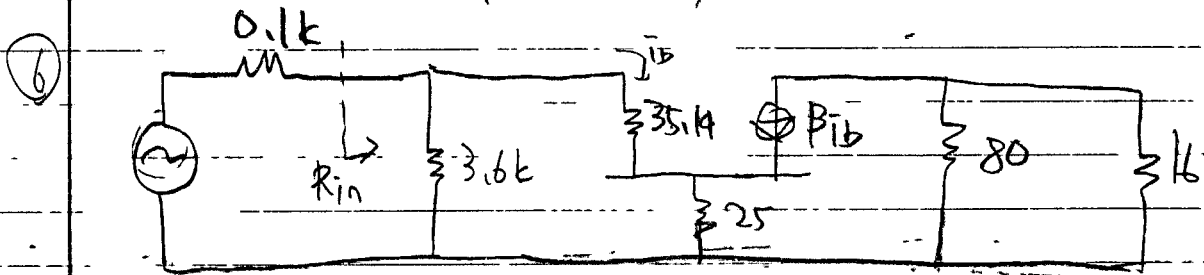
$$i_b = i_s \left( \frac{3600}{3600 + 4859.86} \right) i_s = 0.4157 i_s$$

$$i_s = \frac{1}{0.4157} i_b = 2.4056 i_b$$

$$i_o = -\beta i_b \left( \frac{80}{80 + 16} \right) = -200 \left( \frac{80}{80 + 16} \right) i_b$$

$$i_o = -166.66667 i_b$$

$$\therefore A_i = \left| \frac{i_o}{i_s} \right| = \left| \frac{-166.66667 i_b}{2.4056 i_b} \right| = \boxed{69.28}$$

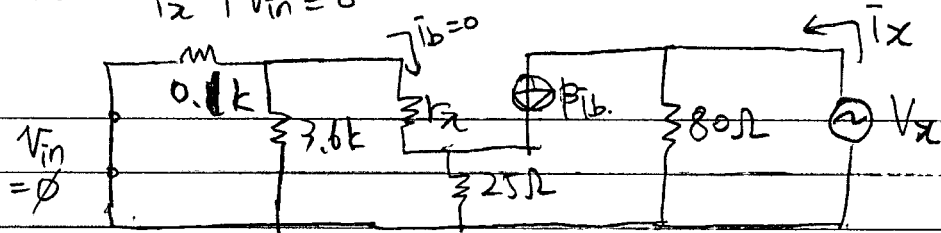


$$R_{in} = 3.6k \parallel (35.14 + 25) = 3600 \parallel 60.14$$

$$R_{in} = \frac{3600 \times 60.14}{3660.14} = 59.15$$

$$\therefore \boxed{R_{in} = 59.15 \Omega}$$

$$R_o = \frac{V_x}{I_x} \Big|_{V_{in}=0}$$



$$I_b = 0, \quad \beta I_b = 0$$

$$\Rightarrow V_x = I_x 80\Omega$$

$$\therefore R_{out} = 80\Omega$$

$$B) \quad P_s = V_{cc} (I_{CQ}) = 18V \times 0.148A = 2.664W$$

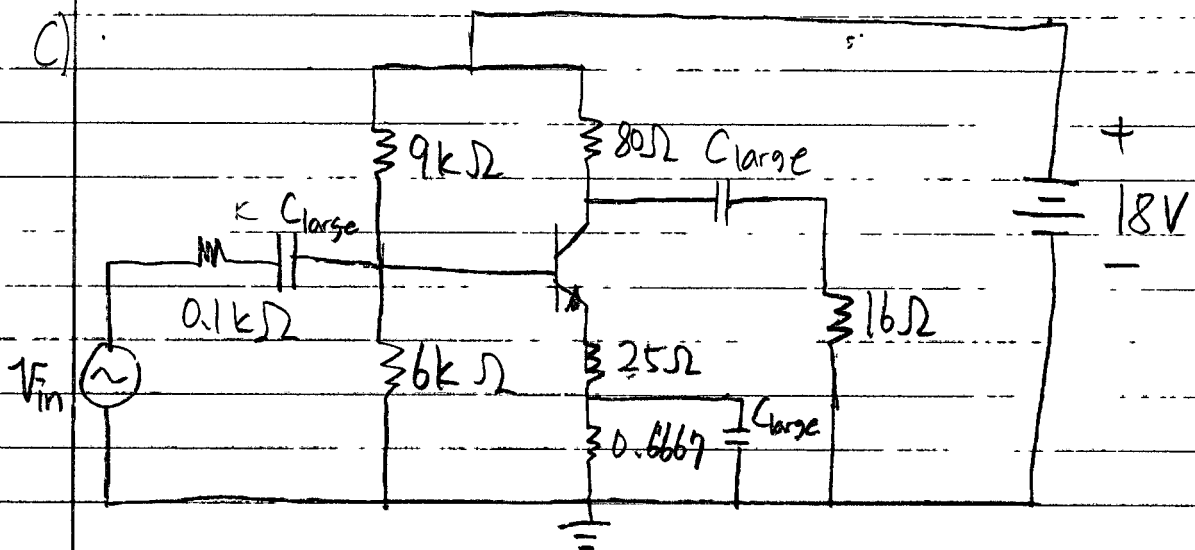
$$P_L = \left( \frac{V_{pk}}{\sqrt{2}} \right) \left( \frac{I_{pk}}{\sqrt{2}} \right) = \left( \frac{V_{CEQ}}{\sqrt{2}} \right) \left( \frac{I_{CQ}}{\sqrt{2}} \right)$$

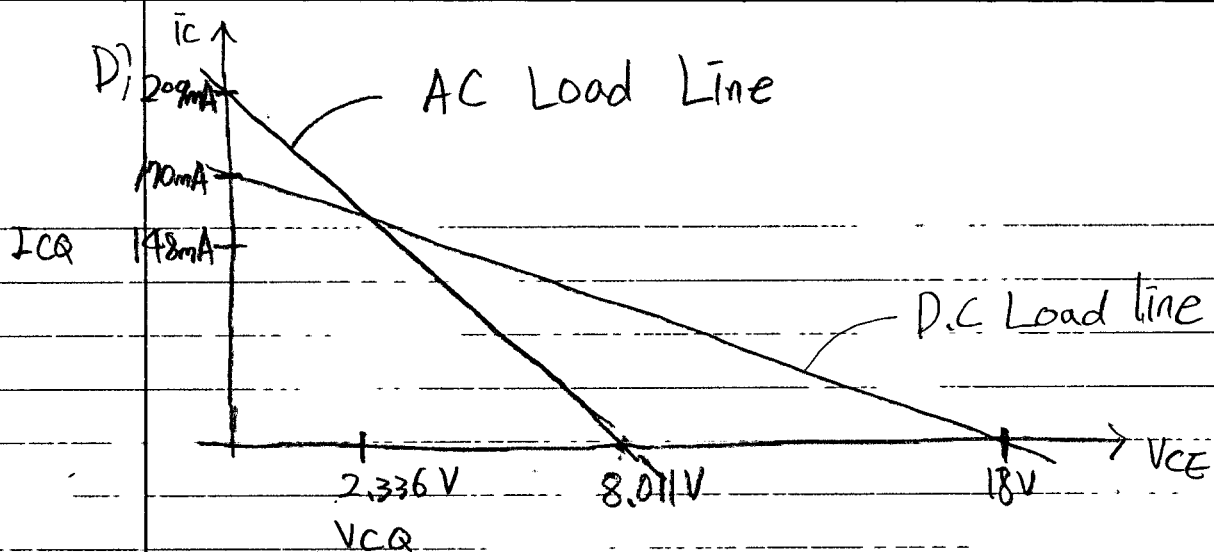
$$= \left( \frac{2.336}{\sqrt{2}} \right) \left( \frac{0.148}{\sqrt{2}} \right) = 0.172864W$$

$$\eta \text{ (power conversion efficiency)} = \frac{P_L}{P_s} = \frac{0.172864}{2.664}$$

$$= 0.06488 \approx 0.065$$

$$\therefore \eta = 6.5\%$$





$$\text{slope of AC Load line} = -\frac{1}{R_{AC}} = -\frac{1}{38.3333}$$

$$\text{slope of DC Load Line} = -\frac{1}{R_{DC}} = -\frac{1}{105.66667}$$

E)

$V_{CC}$	$I_{CQ}$	$V_{CEQ}$	$P_D$
18V	148mA	2.336V	346mW

$$P_D \approx (V_{CEQ})(I_{CQ}) = (2.336)(0.148) = 0.346W$$

F)

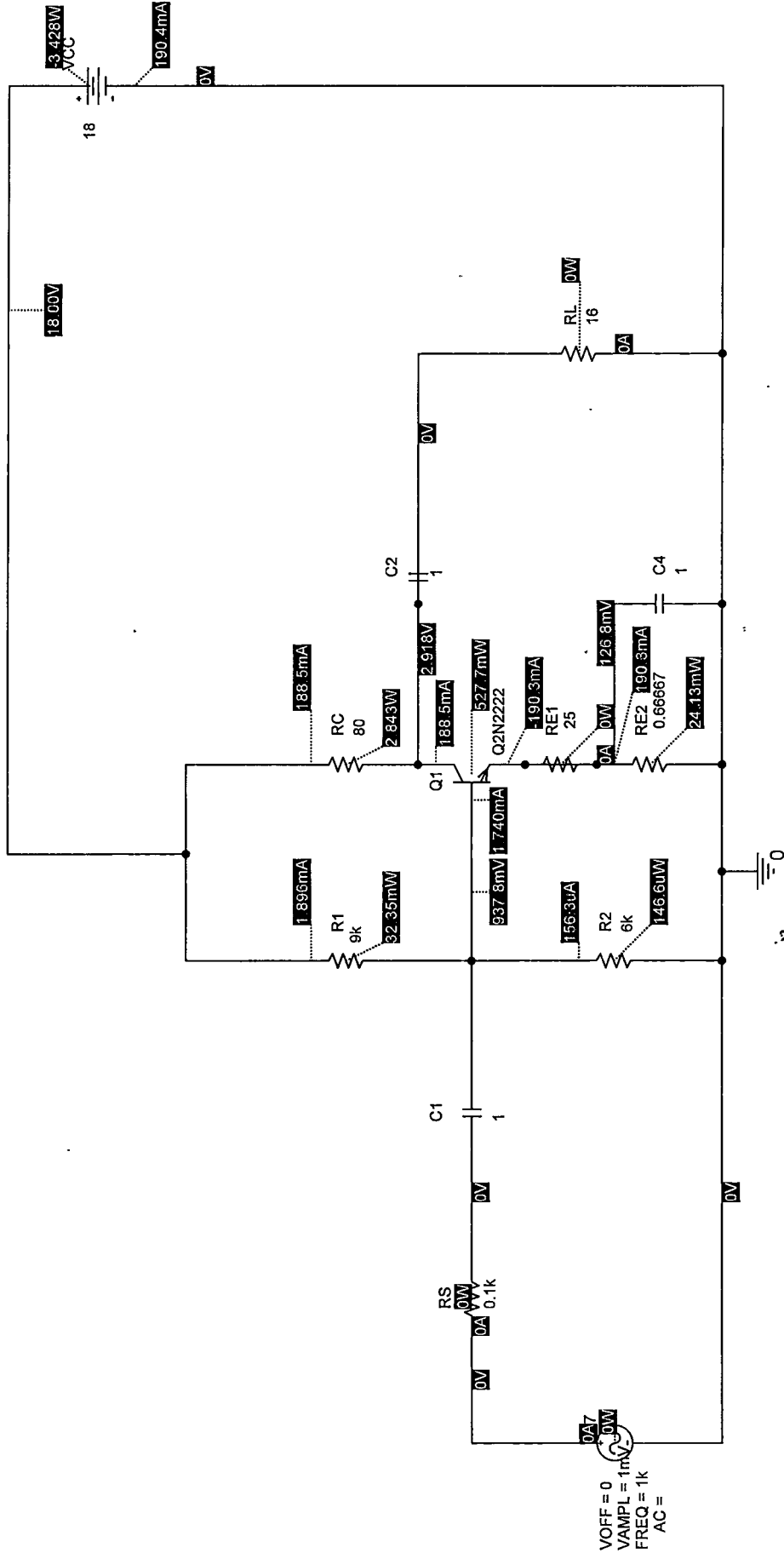
$A_i$	$R_{in}$	$R_{out}$
69.28	59.15 $\Omega$	80 $\Omega$

$$G) P_{RC} = (I_{CQ})^2 R_C = (0.148)^2 (80) = 1.75W$$

$$P_{RE1} = 0.5476W$$

$$P_{RE2} = 0.0146W = 14.6mW$$

# A) Pspice Schematic



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## PSpice part

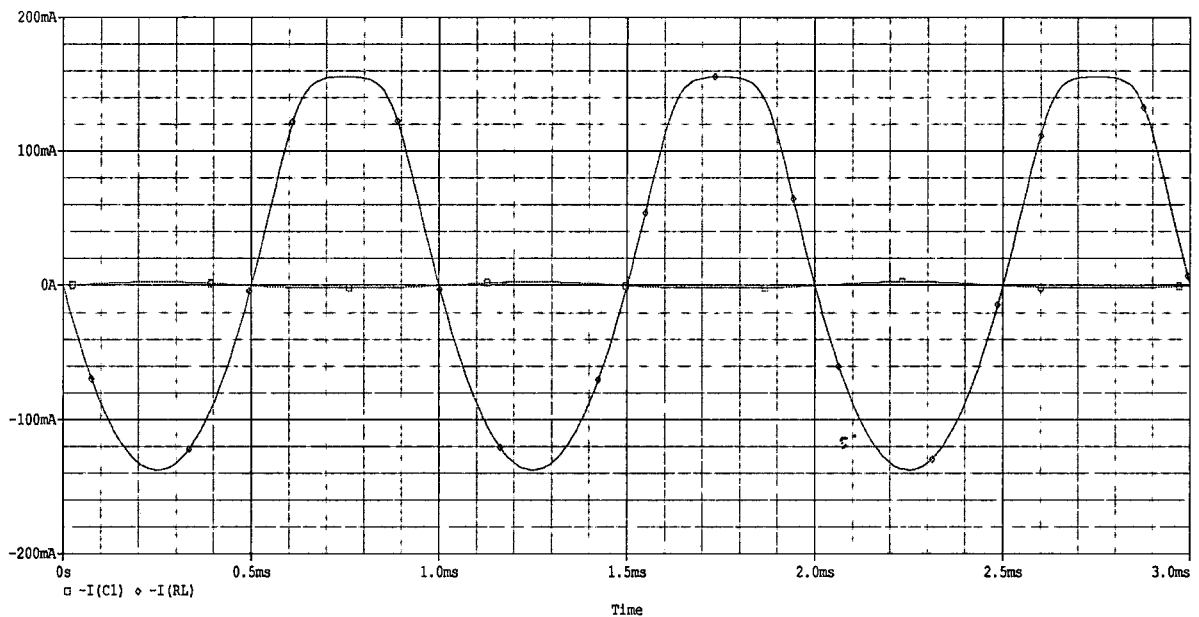
### B) SIMLATED DC BIAS

Simulated value		Hand-calculated value	
ICQ	188.5mA	ICQ	148mA
VCEQ	2.918V	VCEQ	2.336V
VBEQ	0.94V	VBEQ	0.7V
PD,transistor	527.7mW	PD,transistor	346mW

### C) SIMLATED POWER SUPPLY BIAS

DC power Supply Current ( $I_{ps}$ ) = 190.4mA. It is less than 200mA. Thus, I achieve the specification for maximum current

### D) SIMULATED CURRENT SWING



It is clipping to 125 mA at the top. Therefore, my design achieves the 250mA peak-to-peak swing.

### E) SIMULATED EFFICIENCY

$$PS = (V_{cc})(I_{ps}) = 18 * 0.1904 = 3.4272W$$

$$PL = \left(\frac{i_L}{\sqrt{2}}\right)^2 (RL) = (0.0884)^2 (16) = 0.125W$$

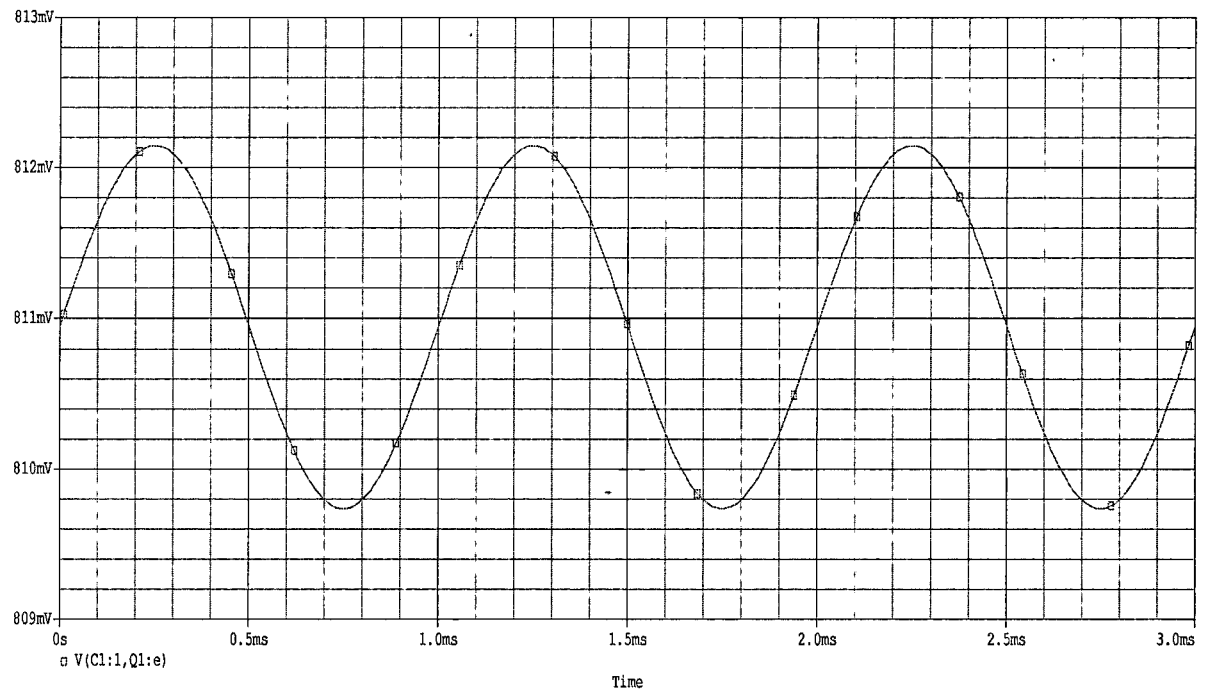
$$\eta = \frac{PL}{PS} = \frac{0.125}{3.4272} = 0.03647 = 3.65\%$$

$\eta$ , simulated	$\eta$ , hand-calculated
3.65%	6.5%

#### F) SIMULATED SMALL SIGNAL OPERATION

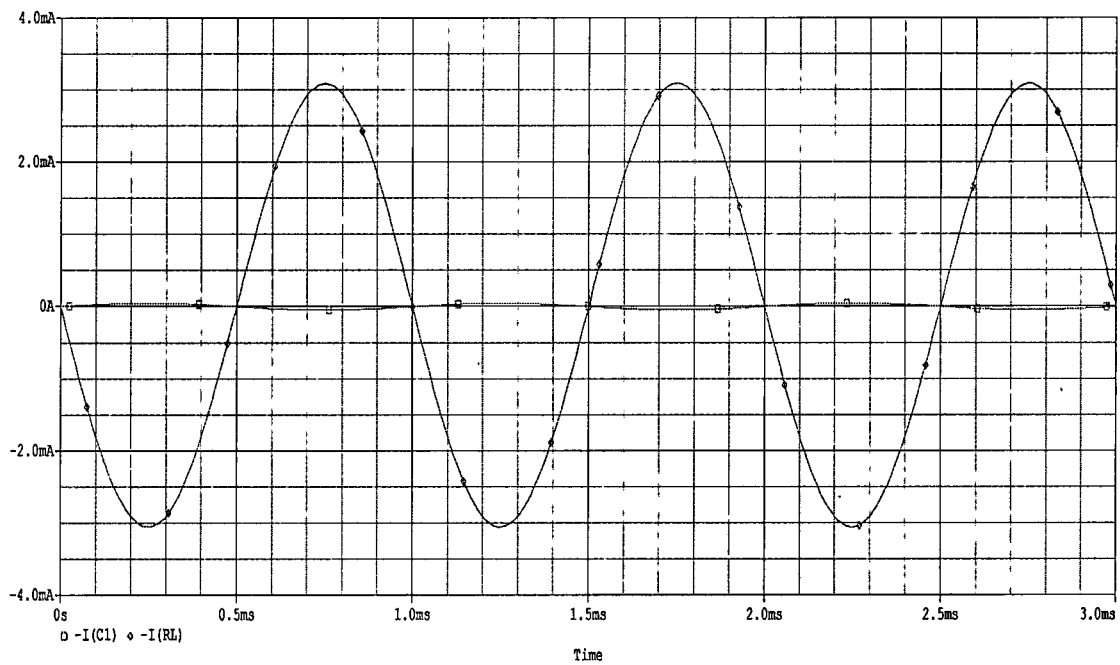
The amplitude value of the source voltage for small signal operation is 6mV.

Plot (Vbe for  $\beta = 200$ )

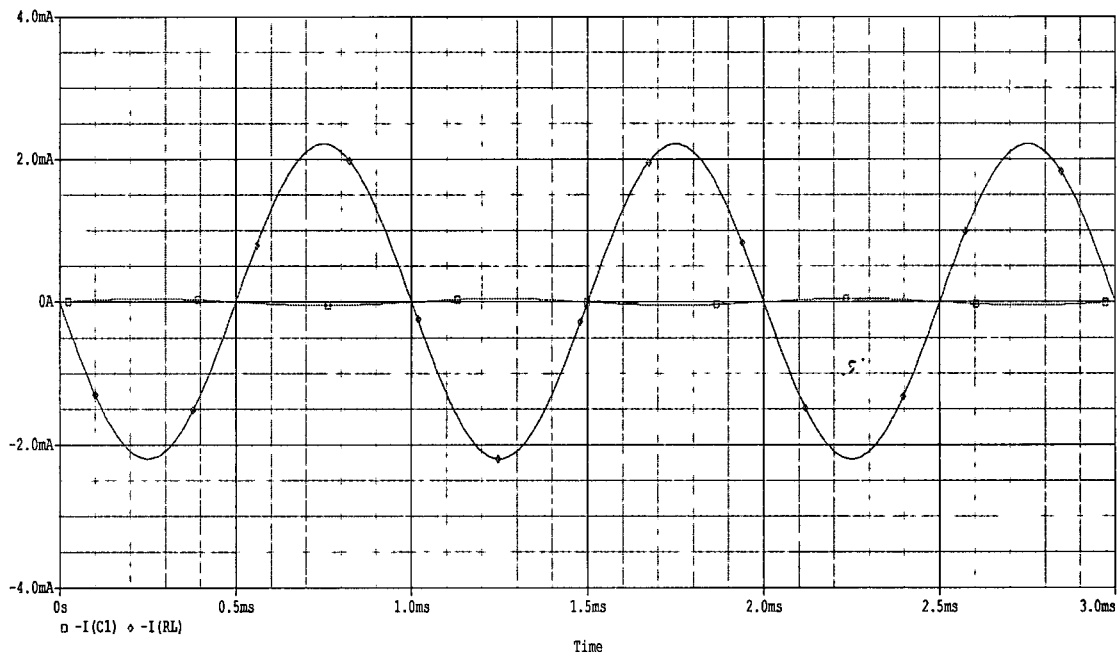


#### G) SIMULATED GAIN

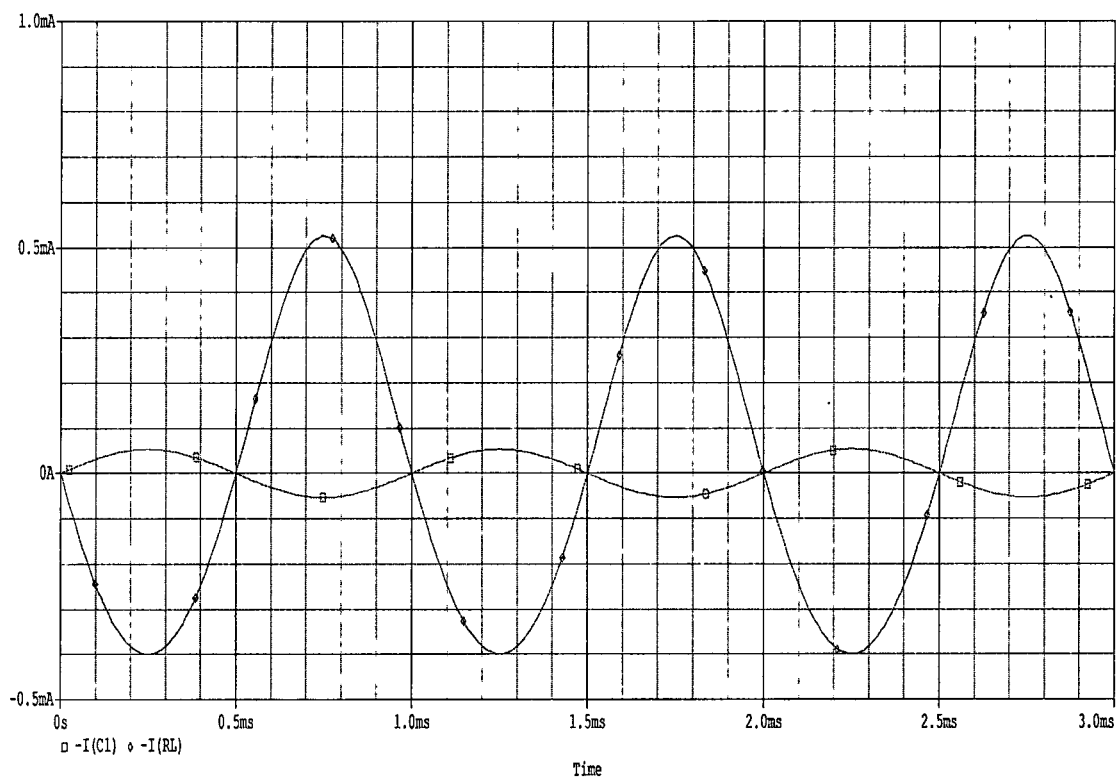
$$\beta = 200, A_i = \frac{3.0868mA}{48\mu A} = 64.31$$



$$\beta = 100, A_i = \frac{2.2145 \text{ mA}}{48.123 \text{ uA}} = 46.02$$

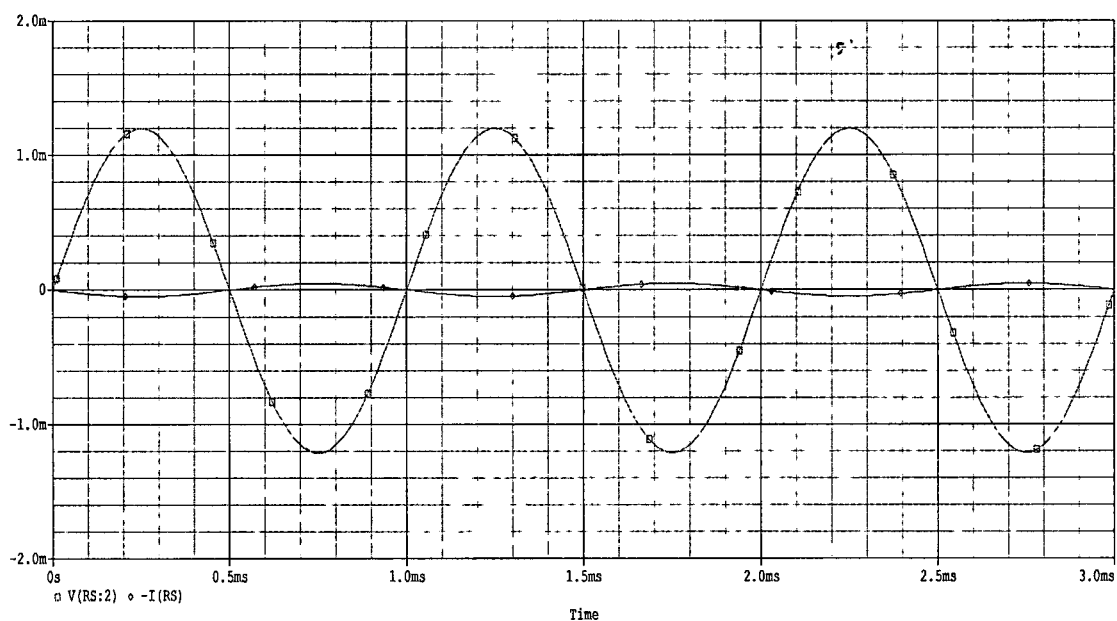


$$\beta = 300, A_i = \frac{526.211 \text{ uA}}{53.469 \text{ uA}} = 9.84$$



#### H) SIMULATED INPUT RESISTANCE

$$\beta = 200, R_{in} = \frac{1.1983mV}{47.841\mu A} = 25.05\Omega$$



$\beta = 100$	$\beta = 200$	$\beta = 300$
24.72 $\Omega$	25.05 $\Omega$	12.3 $\Omega$

I) Pspice schematic, R<sub>out</sub>

The schematic shows a common-emitter amplifier circuit. The input signal source is connected through a resistor R<sub>S</sub> (0.1kΩ) to the base of the transistor Q1 (Q2N2222). A coupling capacitor C1 (1μF) connects the input to the base. The base is biased by a voltage divider consisting of resistors R1 (9kΩ) and R2 (6kΩ), connected to a 18V DC supply VCC. An AC noise source is also connected to the base. The emitter is connected to ground through a resistor RE1 (25Ω). The collector is connected to VCC through a resistor RC (80Ω) and a load resistor RL (1kΩ). A coupling capacitor C2 (1μF) connects the collector to the output. The output is measured across RL. Simulation parameters are set to VOFF = 0, VAMPL = 1mV, FREQ = 1k, and AC = 1.

Component	Value	Power
R <sub>S</sub>	0.1kΩ	0W
C1	1μF	0W
R1	9kΩ	32.57mW
R2	6kΩ	129.1μW
RE1	25Ω	127.7mW
RC	80Ω	1.268W
RL	1kΩ	10.87mW
Q1	Q2N2222	988.8mW
VCC	18V	-2.301W

Simulation Parameters:  
VOFF = 0  
VAMPL = 1mV  
FREQ = 1k  
AC = 1

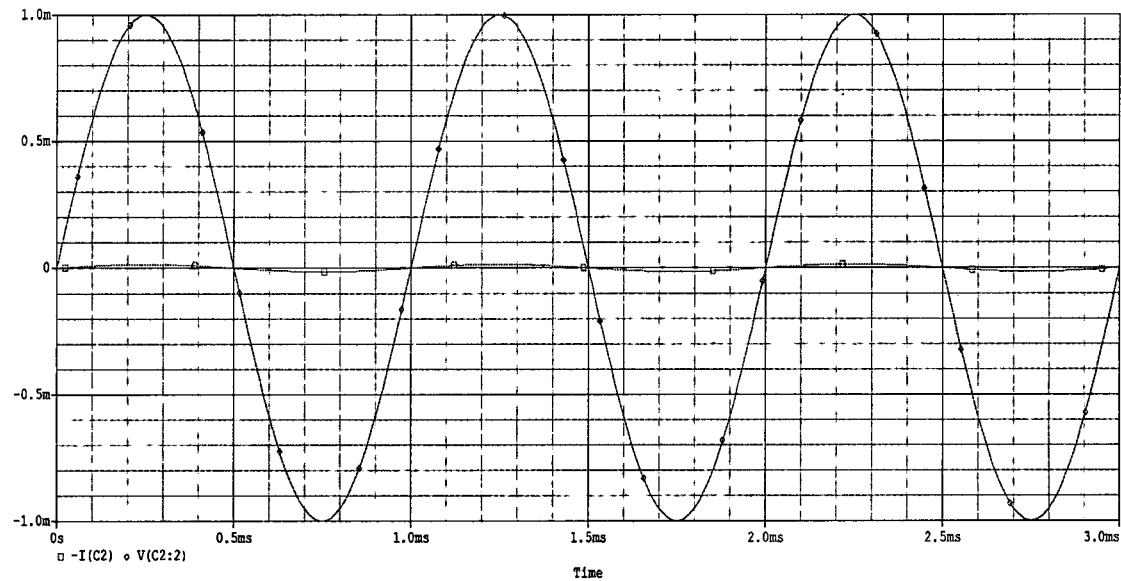
Results Summary:

Node	Voltage (V)	Current (mA)
Base	880.0mV	1.756mA
Emitter	0A	146.7μA
Collector	7.928V	125.9mA

[illegible]

I) SIMULATED OUTPUT RESISTANCE

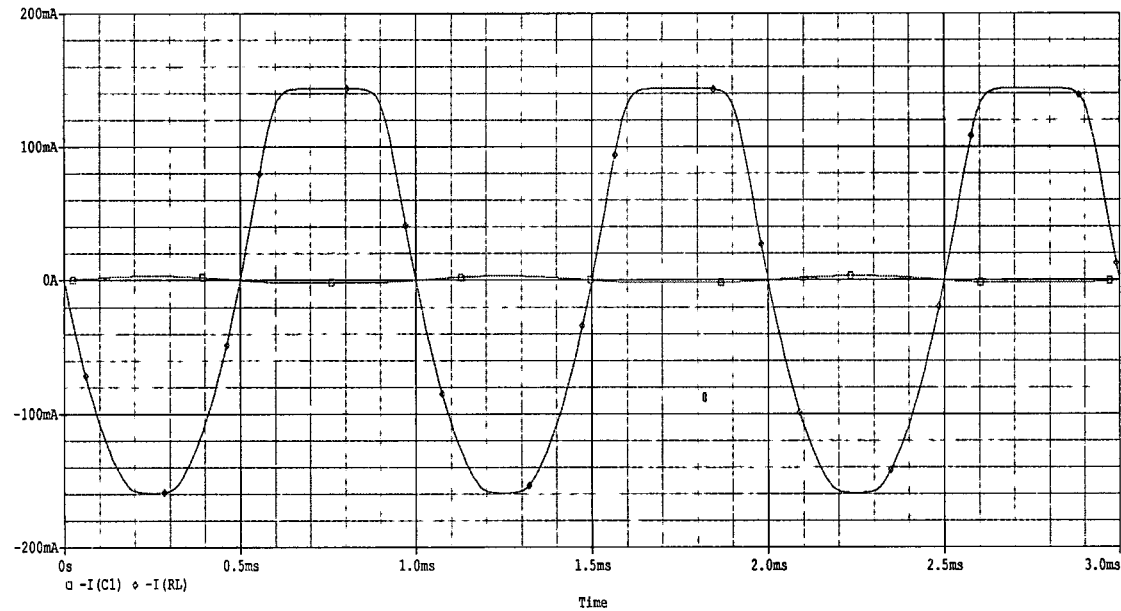
$$\beta = 200, R_{out} = \frac{0.9997mV}{15.097\mu A} = 66.22\Omega$$



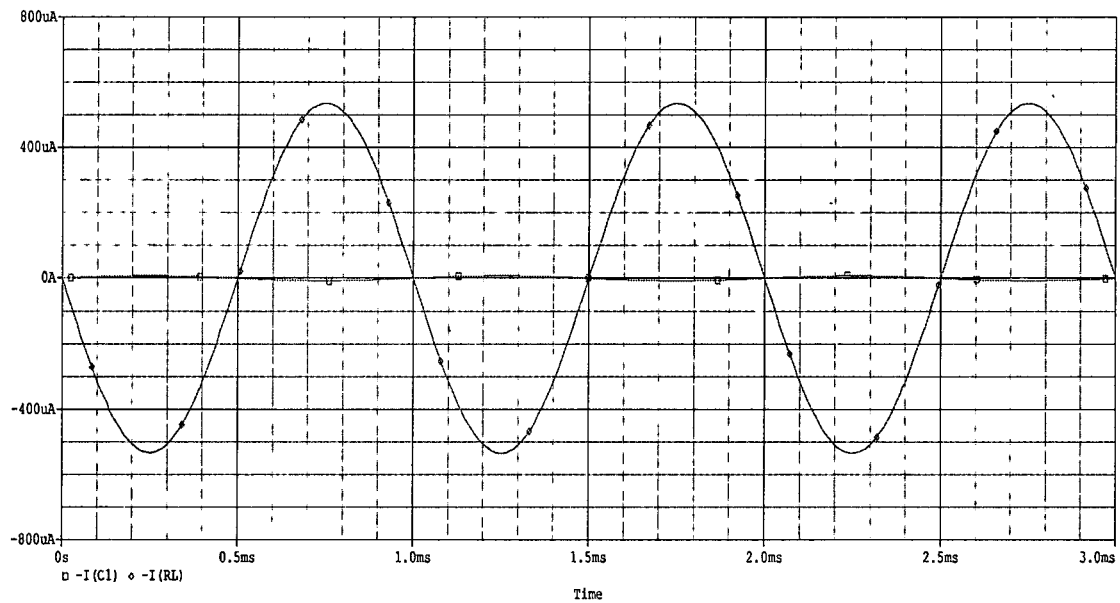
$\beta = 100$	$\beta = 200$	$\beta = 300$
71.02Ω	66.22Ω	2.93Ω

J) SIMULATION USING STANDARD RESISTOR VALUES

The plot of  $i_L$  with clipping at both the positive and negative peaks using a  $\beta = 200$ .

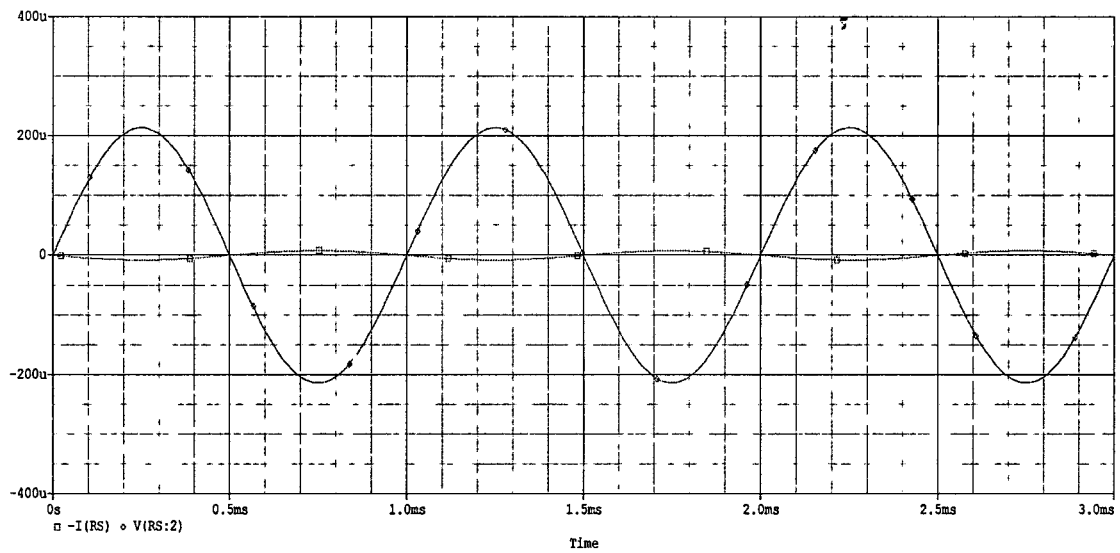


The plots of  $i_s$  and  $i_L$  under small signal conditions



$$\beta = 200, A_i = \frac{535.492 \mu A}{7.8581 \mu A} = 68.15$$

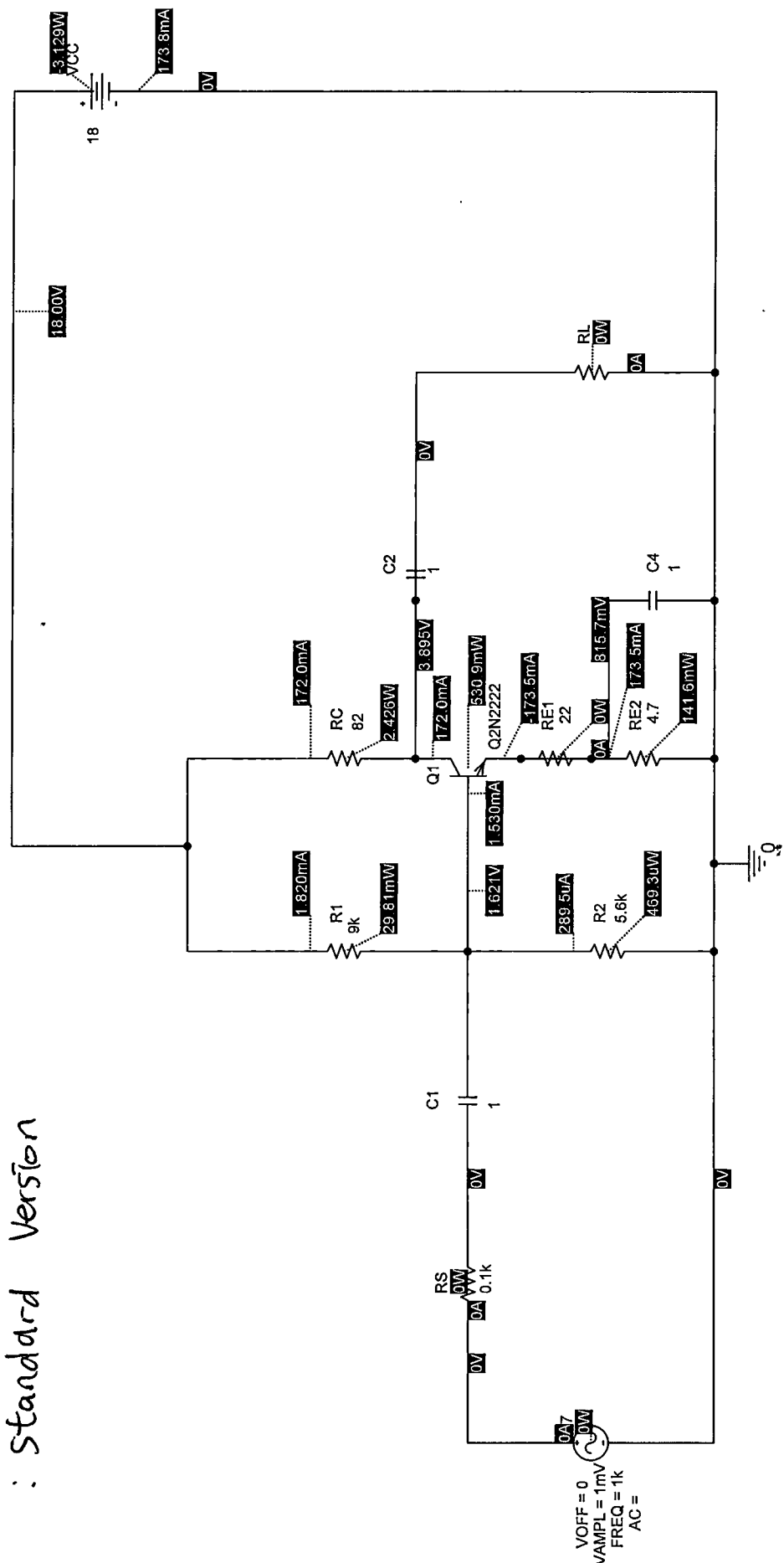
The plots of  $i_s$  and  $v_s$  for calculate the  $R_{in}$



$$\beta = 200, R_{in} = \frac{213.982 \mu V}{7.8529 \mu A} = 27.25 \Omega$$

Original design ( $R_{in}$ )	Standard design ( $R_{in}$ )
25.05 $\Omega$	27.25 $\Omega$

# J) Pspice Schematic : Standard Version



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