ECE345 Final Project Report

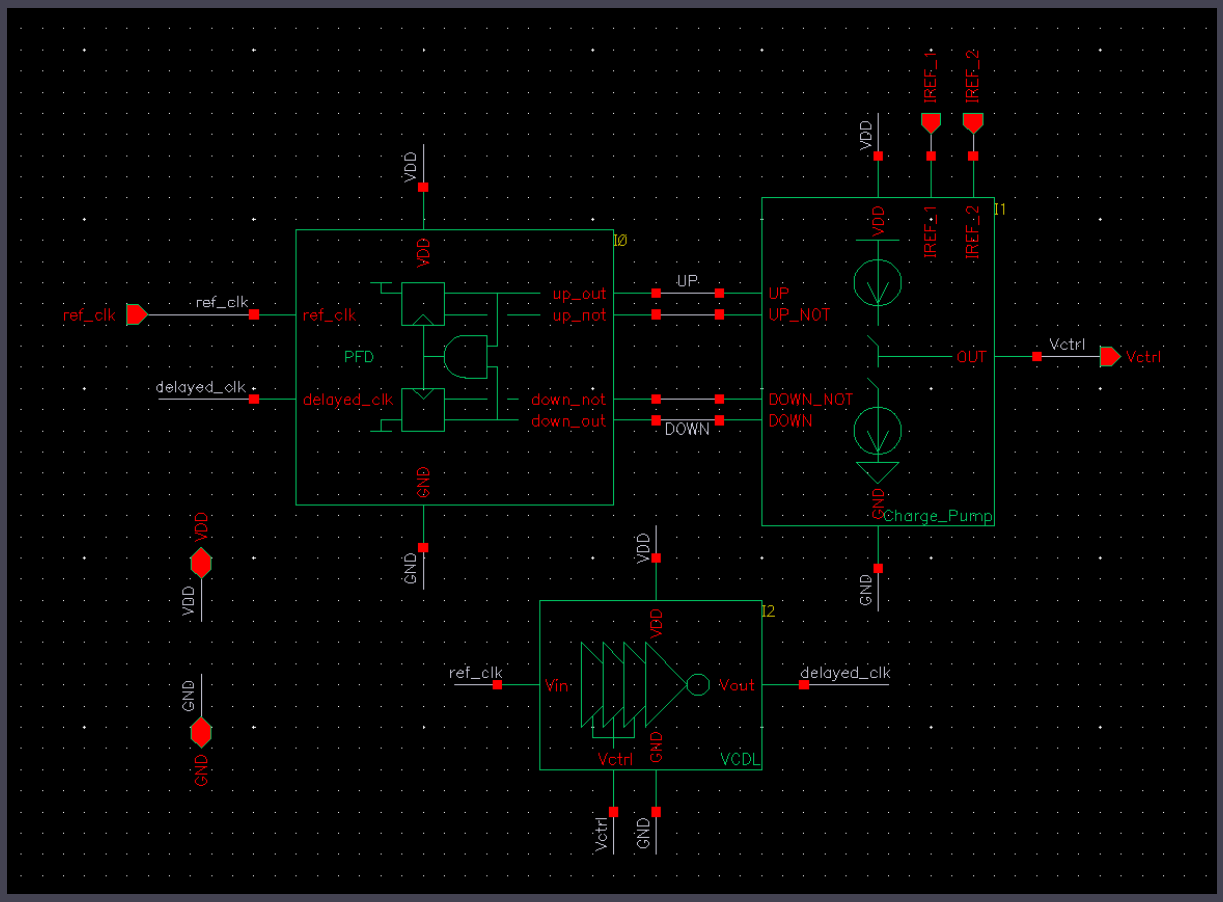

Figure 1: Overall architecture of the DLL

VerilogA Code

```
// VerilogA for DLL, Charge_Pump, veriloga

`include "constants.vams"
`include "disciplines.vams"

module Charge_Pump(OUT, UP, DOWN, UP_NOT, DOWN_NOT, VDD, GND, IREF_1, IREF_2);

output OUT;
input UP, DOWN;
input UP_NOT, DOWN_NOT;
input VDD, GND;
input IREF_1, IREF_2;

parameter real iamp = 50e-6;
parameter real tdel = 0;
parameter real trise = 10e-12;
parameter real tfall = 10e-12;

electrical OUT, UP, DOWN;
real iout;

analog begin
  if ((V(UP)==1)&&(V(DOWN)==0))
    iout = -iamp;
  if ((V(UP)==0)&&(V(DOWN)==1))
    iout = iamp;
  if ((V(UP)==0)&&(V(DOWN)==0))
    iout = 0;
  if ((V(UP)==1)&&(V(DOWN)==1))
    iout = 0;

  I(OUT) <+ transition(iout, tdel, tfall, trise);
end

endmodule
```

```
// VerilogA for DLL, PFD, veriloga

`include "constants.vams"
`include "disciplines.vams"

module PFD(up_out, down_out, up_not, down_not, ref_clk, delayed_clk, VDD, GND);

input ref_clk, delayed_clk;
input VDD, GND;
output up_out, down_out;
output up_not, down_not;
electrical up_out, down_out, ref_clk, delayed_clk;
electrical rst;

parameter real vh = 1.0, vl = 0.0, vth = 0.5;//VDD = 1.0V, GND = 0, Vth = VDD/2 =
0.5V;
parameter real ttol = 5p from [0:inf);//tolerance
parameter real td = 0 from [0:inf); //delay of PFD output
parameter real tt = 10p from [0:inf);//rise and fall time
integer state_up;
integer state_dn;
integer init;

analog begin
   @(initial_step) begin
    state_up = 0;
    state_dn = 0;
    init = 0;
  end
   @(cross((V(ref_clk)-vth), +1, ttol)) begin
    if (init == 0) begin
    init = 1;
    state_up = 0;
    end
    else
        state_up = 1;
   end

   @(cross((V(delayed_clk)-vth), +1, ttol)) begin
      state_dn = 1;
   end

  @(cross((V(rst)-vh), +1, ttol)) begin
    state_up = 0;
    state_dn = 0;
  end
   V(down_out) <+ transition((state_dn == 1) ? vh:vl, td, tt);
   V(up_out) <+ transition((state_up == 1) ? vh:vl, td, tt);
   V(rst) <+ transition((V(up_out)&&V(down_out)) ? vh:vl, {10e-12}, tt);
end

endmodule
```

```
// VerilogA for DLL, VCDL, veriloga

`include "constants.vams"
`include "disciplines.vams"

module VCDL(Vin, Vctrl, Vout, VDD, GND);

input Vin;
input Vctrl;
input VDD, GND;
output Vout;

electrical Vin, Vctrl, Vout;
electrical VDD, GND;

parameter real max_delay = 1e-9;
parameter real ttol = 5p from [0:inf);
real total_delay;
real vout;

analog begin
  @(cross(V(Vin)-0.5, +1, ttol)) begin
    total_delay = 700*(1e-12)-(500*1e-12)*V(Vctrl);
    vout = 1.0;
  end
  @(cross(V(Vin)-0.5, -1, ttol)) begin
    total_delay = 700*(1e-12)-(500*1e-12)*V(Vctrl);
    vout = 0.0;
  end
  V(Vout) <+ transition(vout, total_delay, {10e-12});
end

endmodule
```

DLL Testbench using Verilog

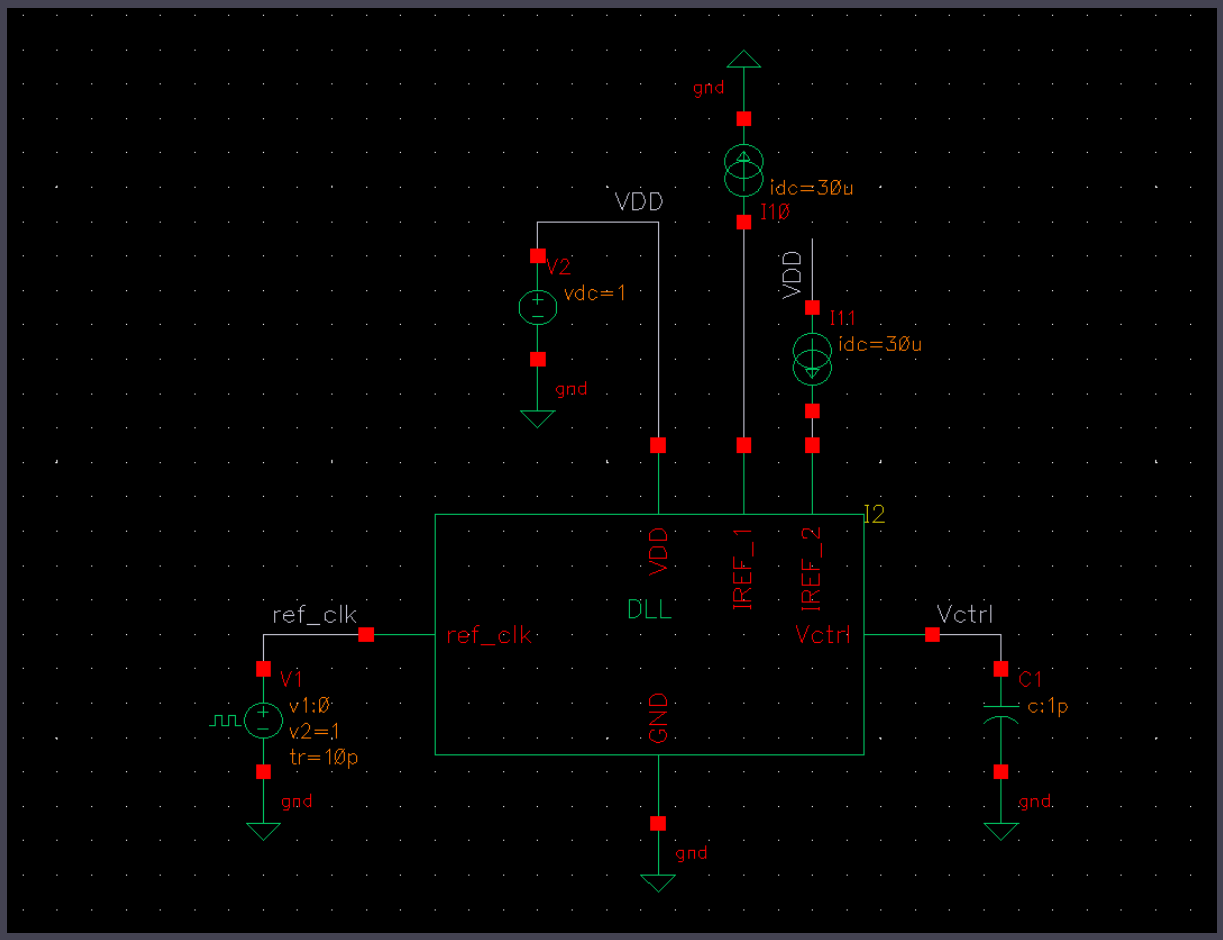

Figure 2: Testbench Schematic for the DLL

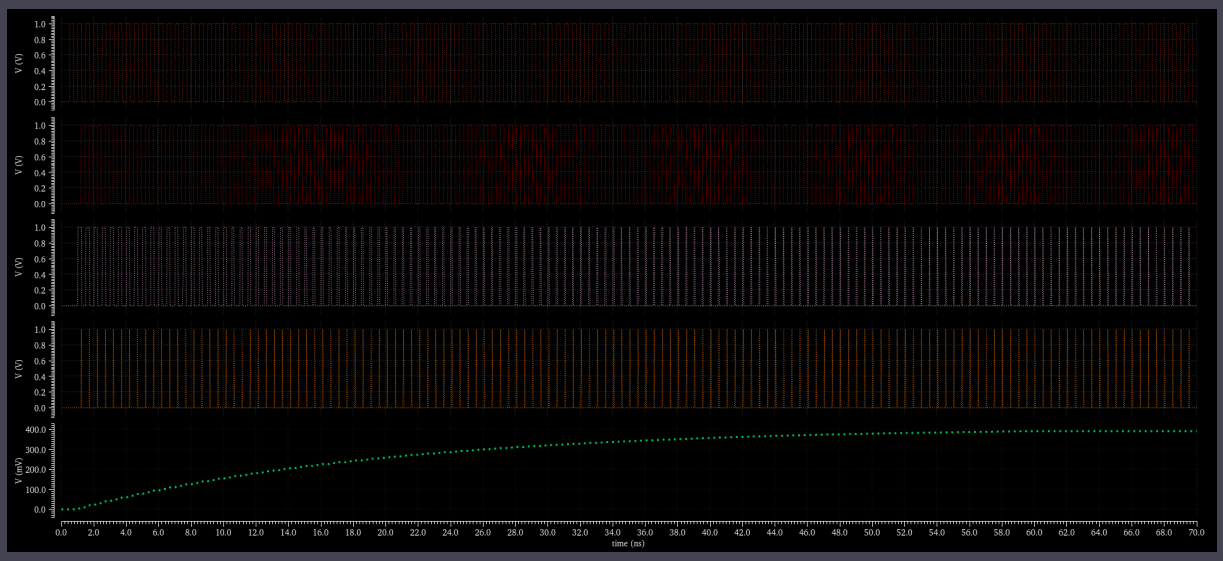

Figure 3: Verilog testbench result: DLL full operation (Inital Value of Vctrl = 0V)

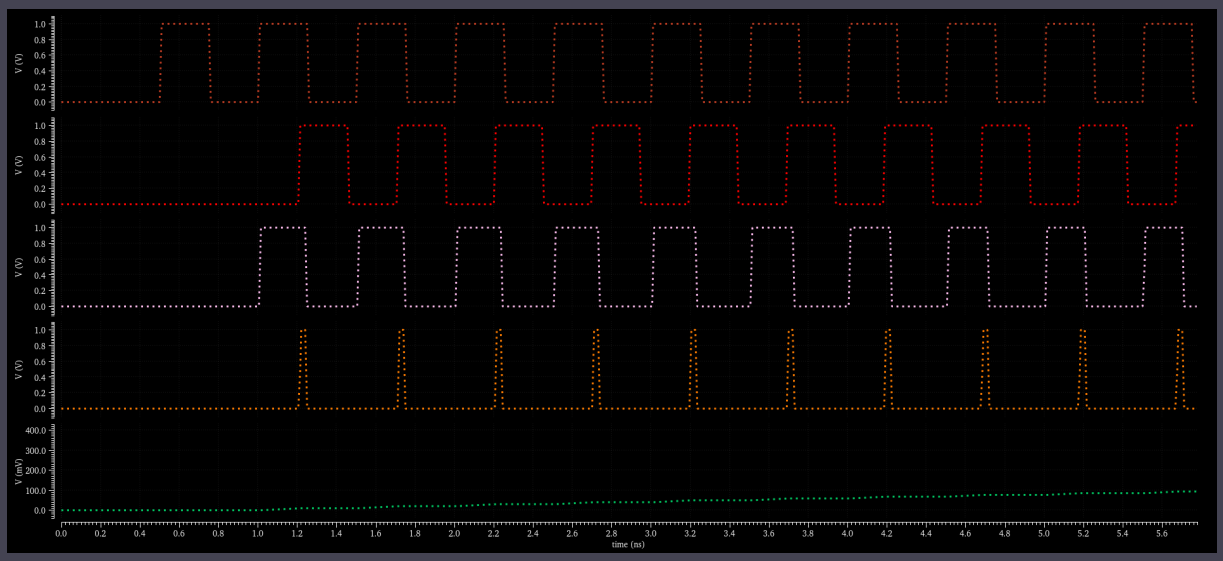

Figure 4: Verilog testbench result: DLL at start state (Inital Value of Vctrl = 0V)

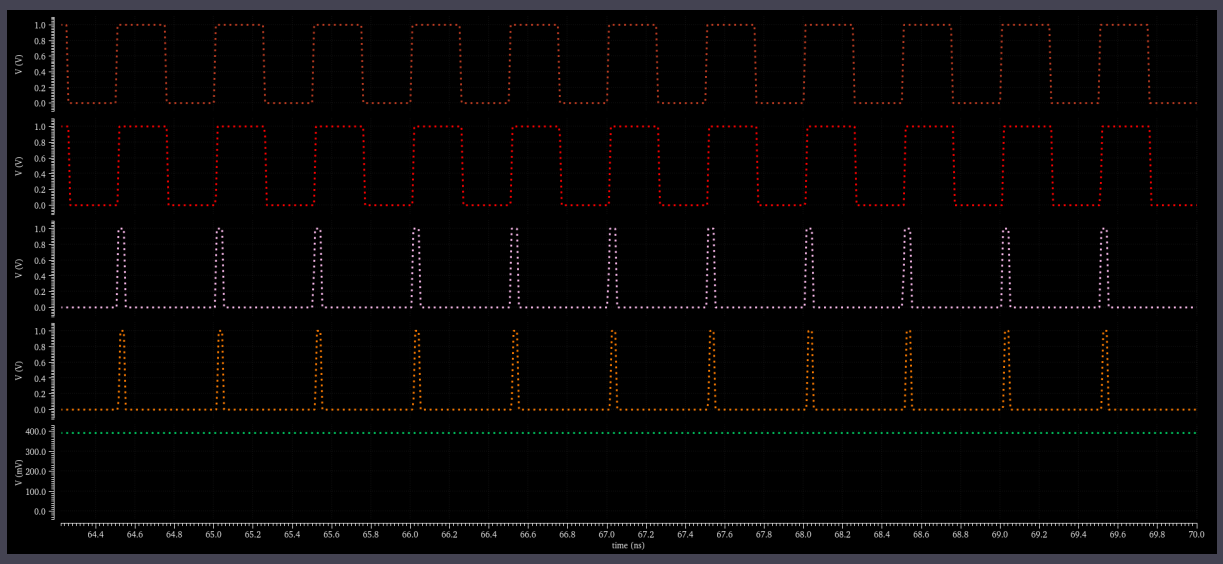

Figure 5: Verilog testbench result: DLL at end state (Inital Value of Vctrl = 0V)

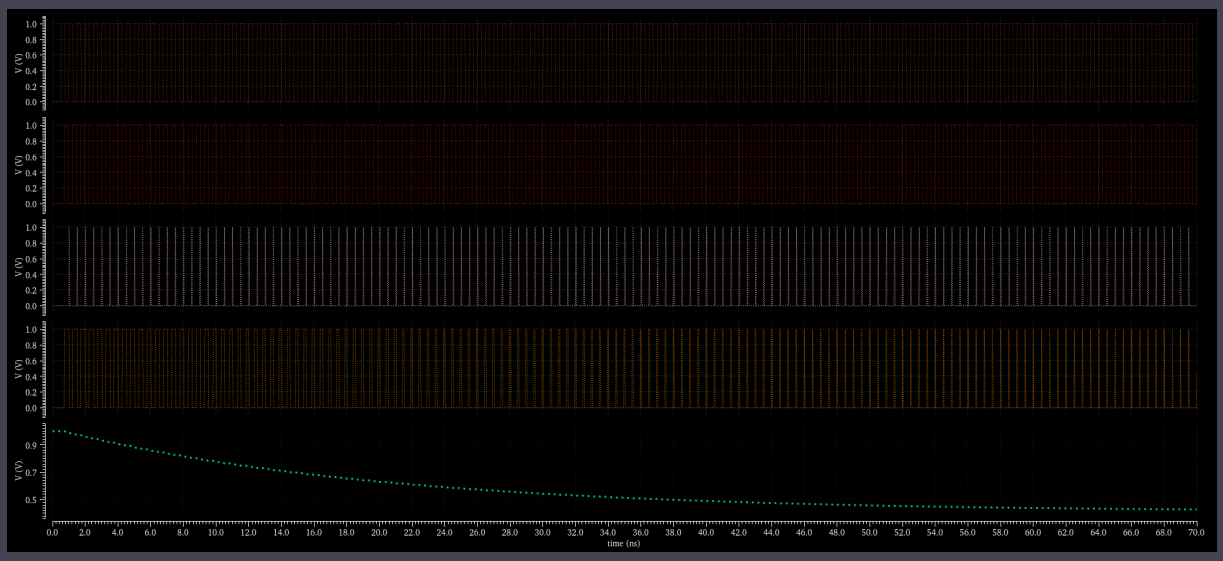

Figure 6: Verilog testbench result: DLL full operation (Inital Value of Vctrl = 1V)

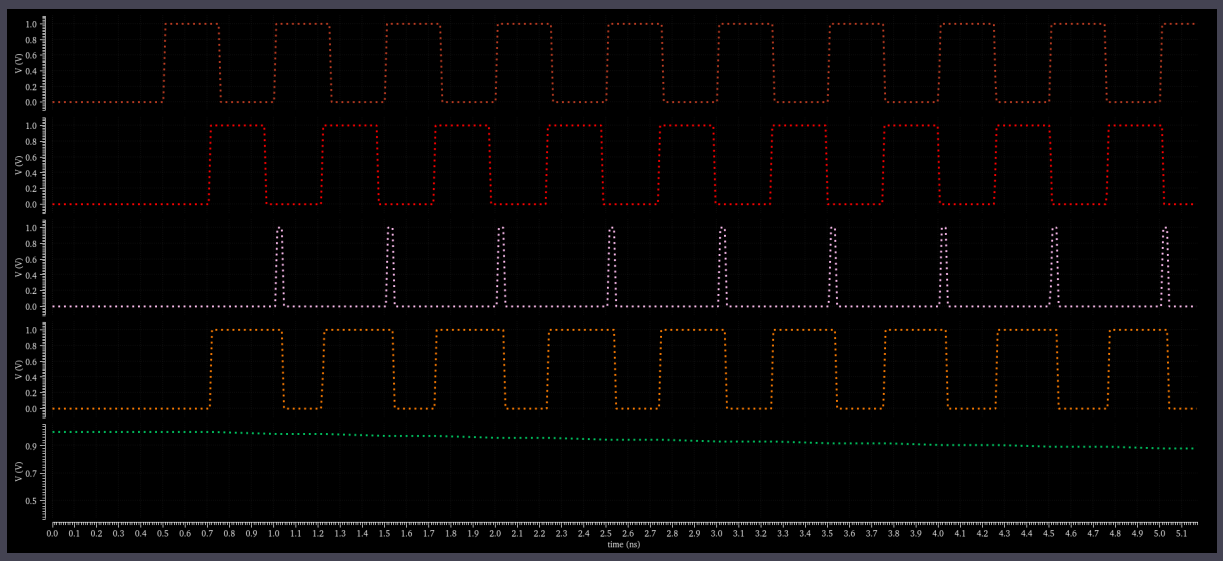

Figure 7: Verilog testbench result: DLL at start state (Inital Value of Vctrl = 1V)

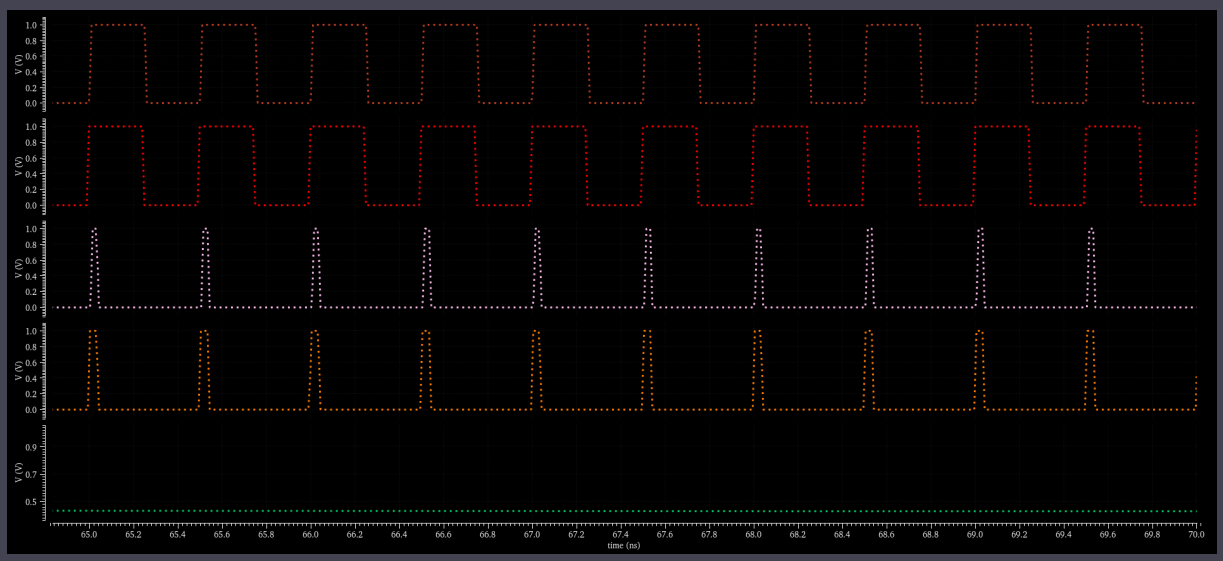

Figure 8: Verilog testbench result: DLL at end state (Inital Value of Vctrl = 1V)

Main Cells

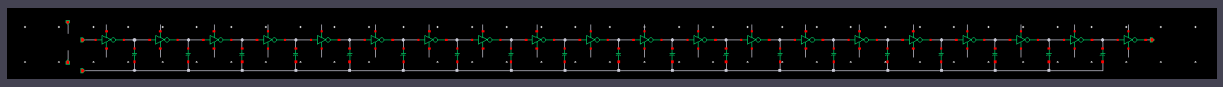

Figure 9: Complete schematic of the VCDL

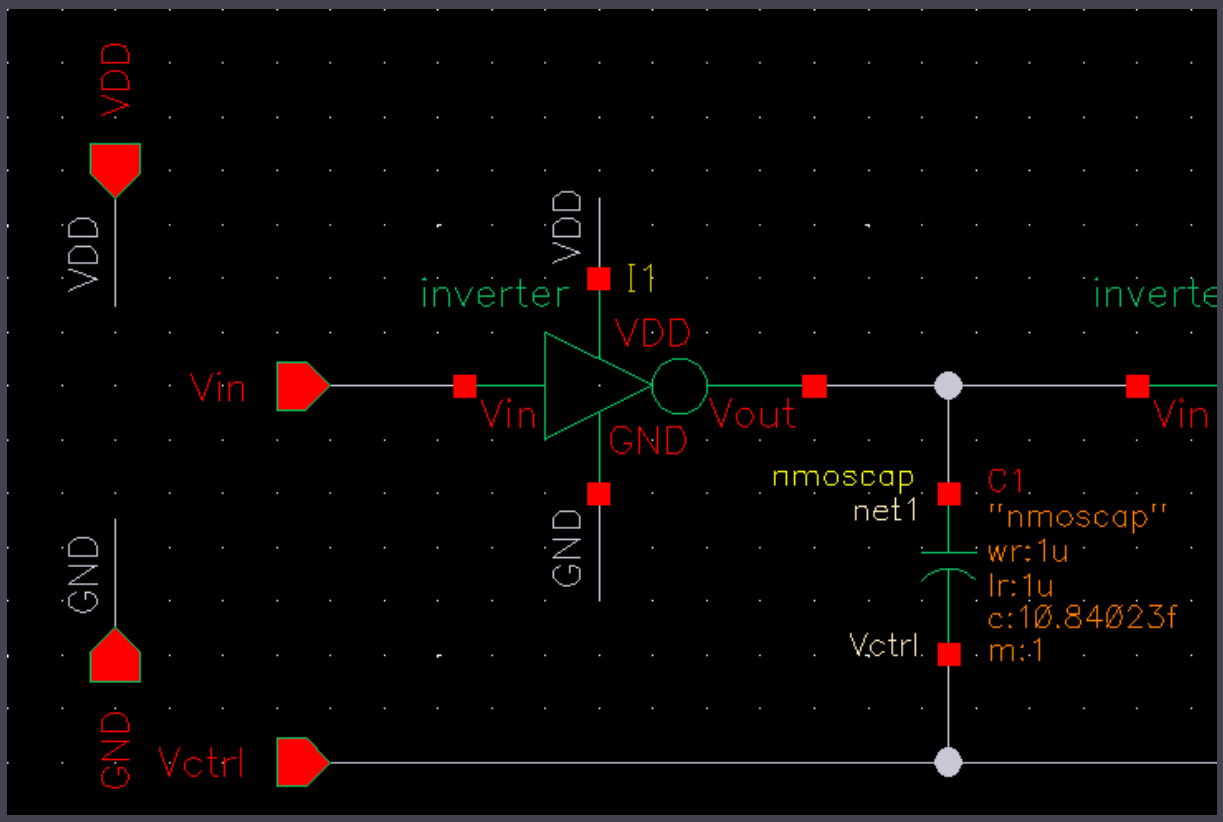

Figure 10: Single stage of the VCDL

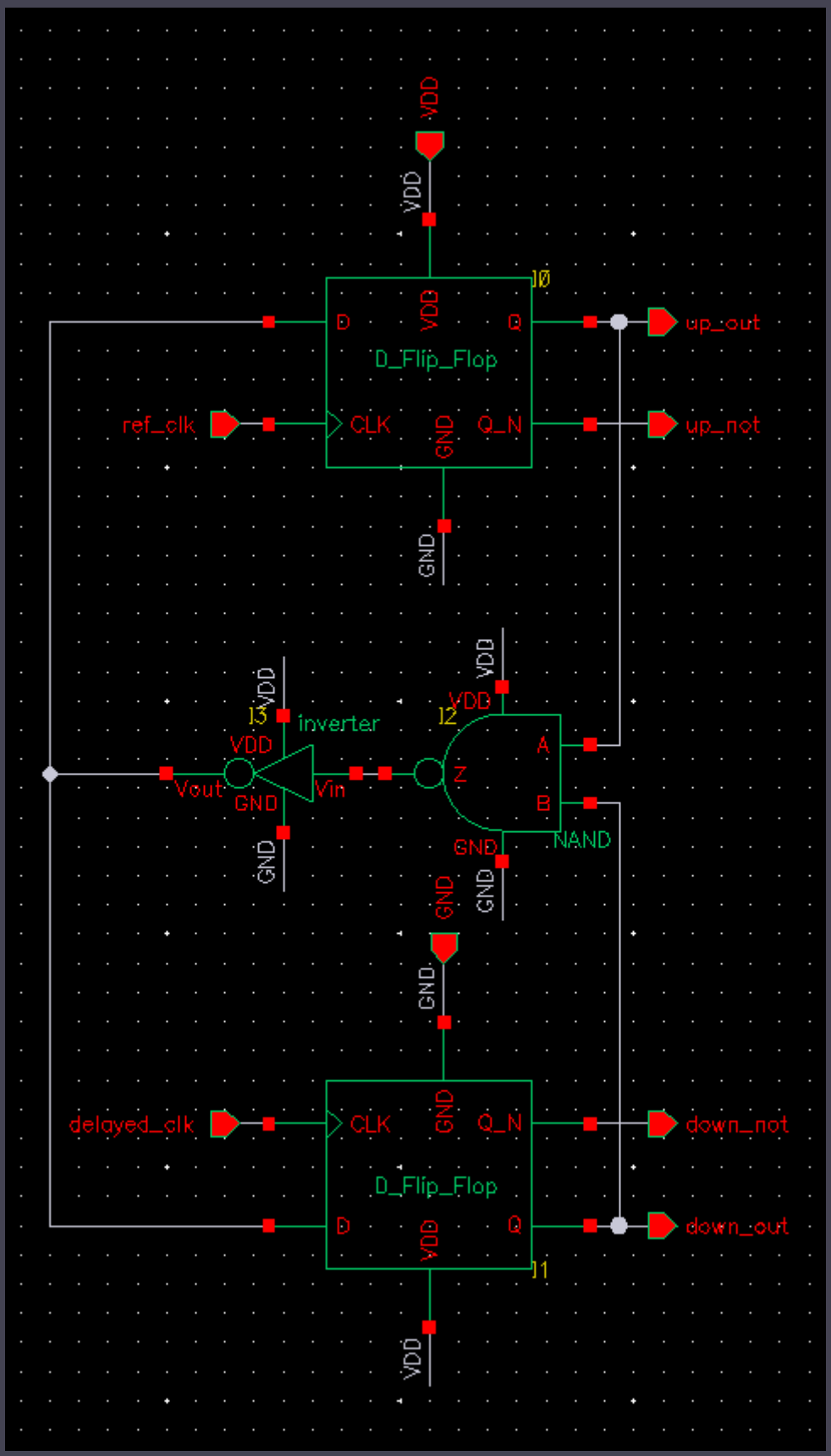

Figure 11: Schematic of the PFD

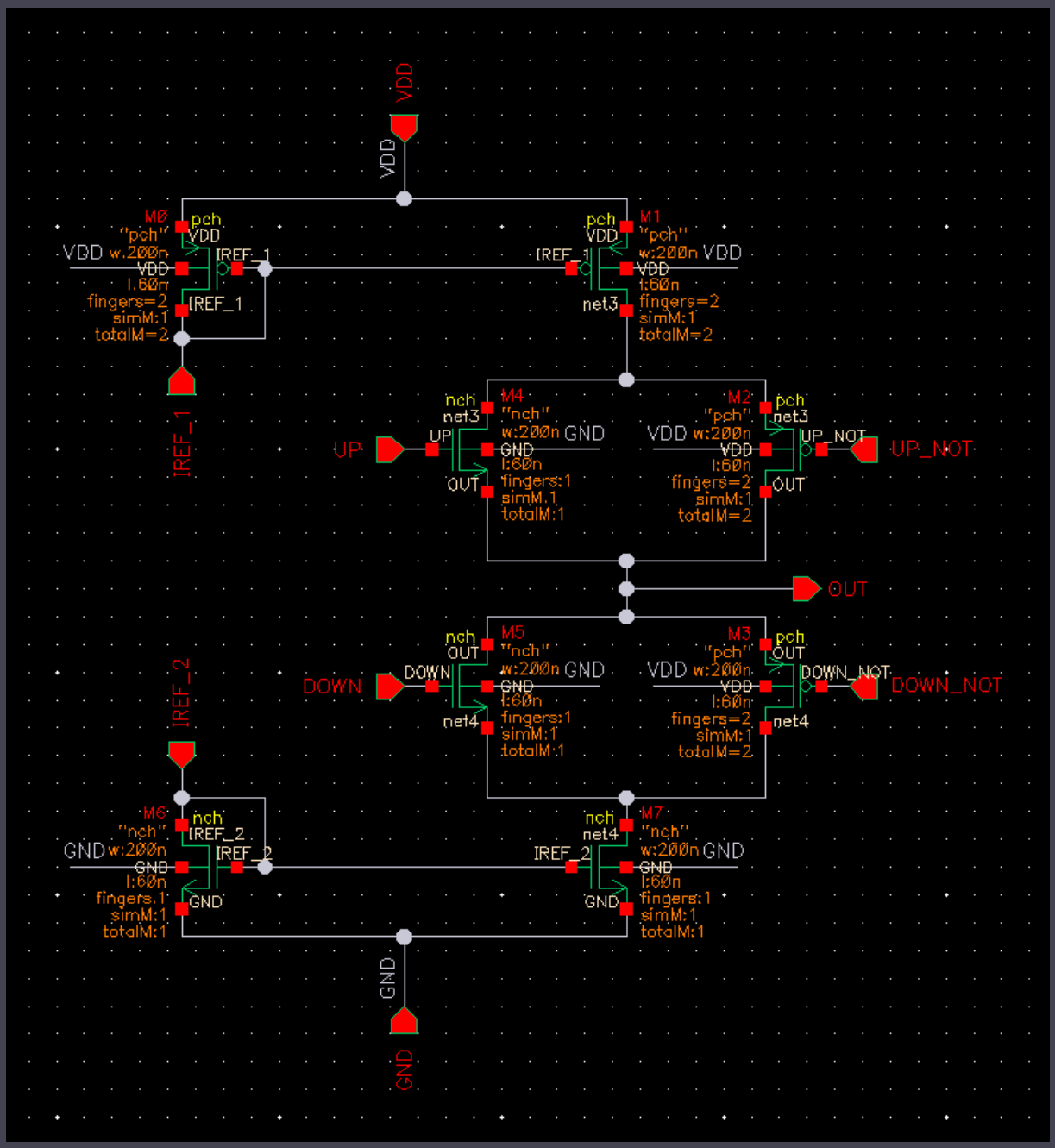

Figure 12: Schematic of the charge pump

Supplementary Cells

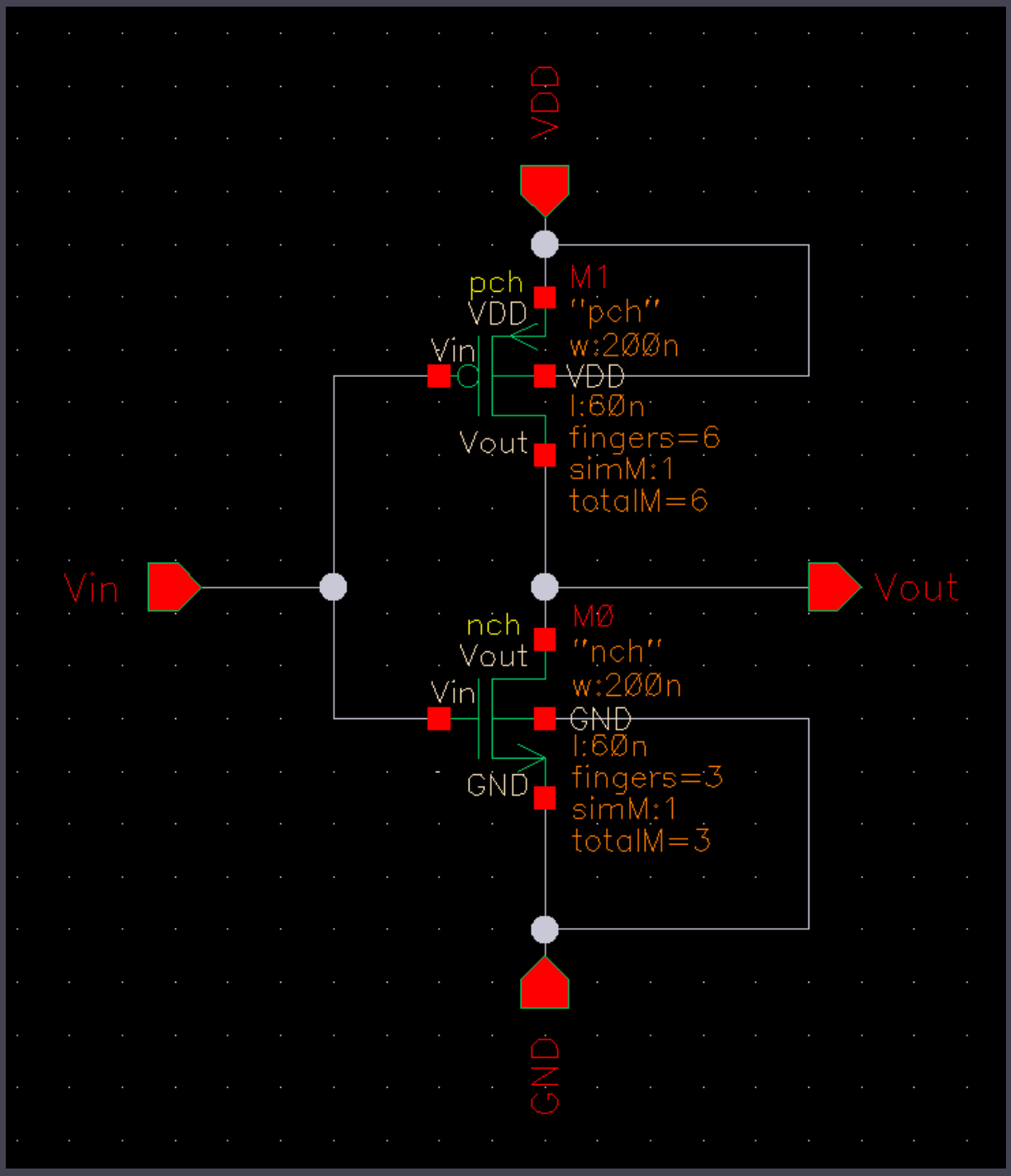

Figure 13: Schematic of the inverter

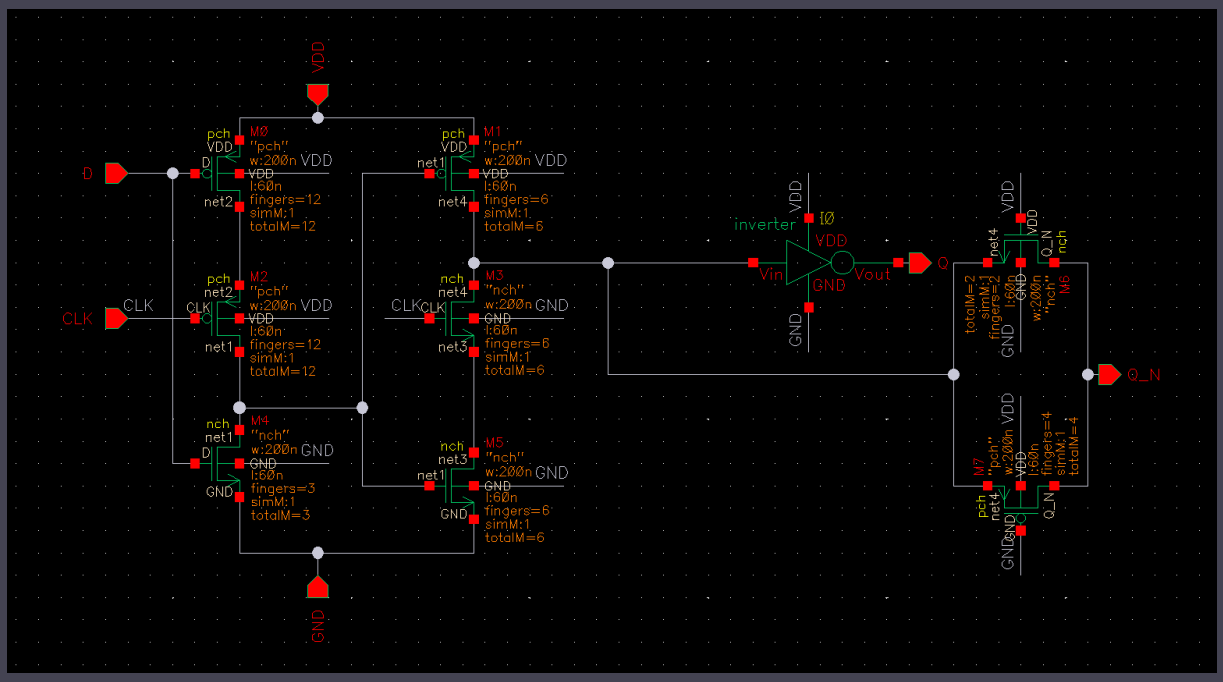

Figure 14: Schematic of the D Flip-Flop

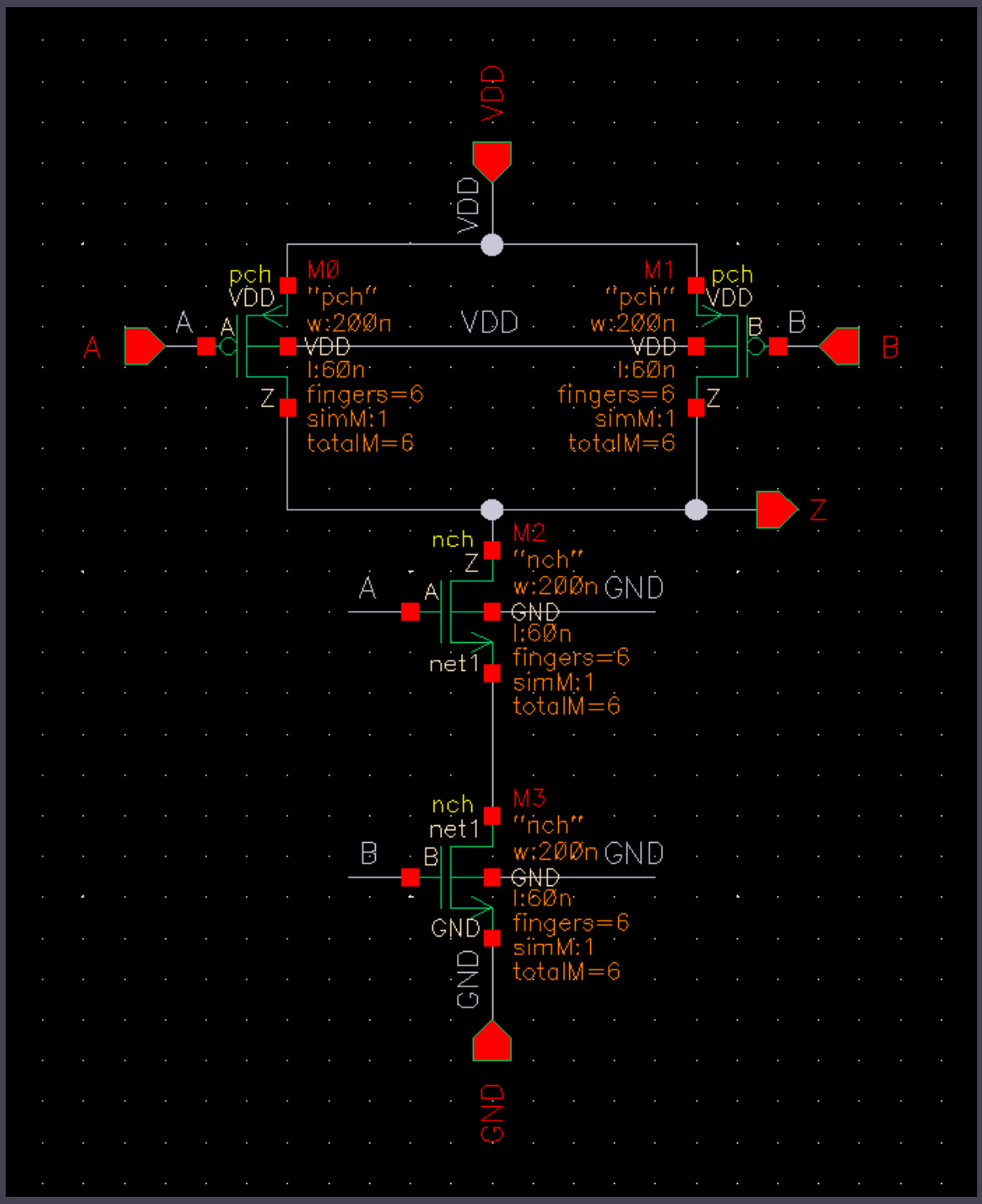

Figure 15: Schematic of the NAND gate

DLL Testbench using Schematics

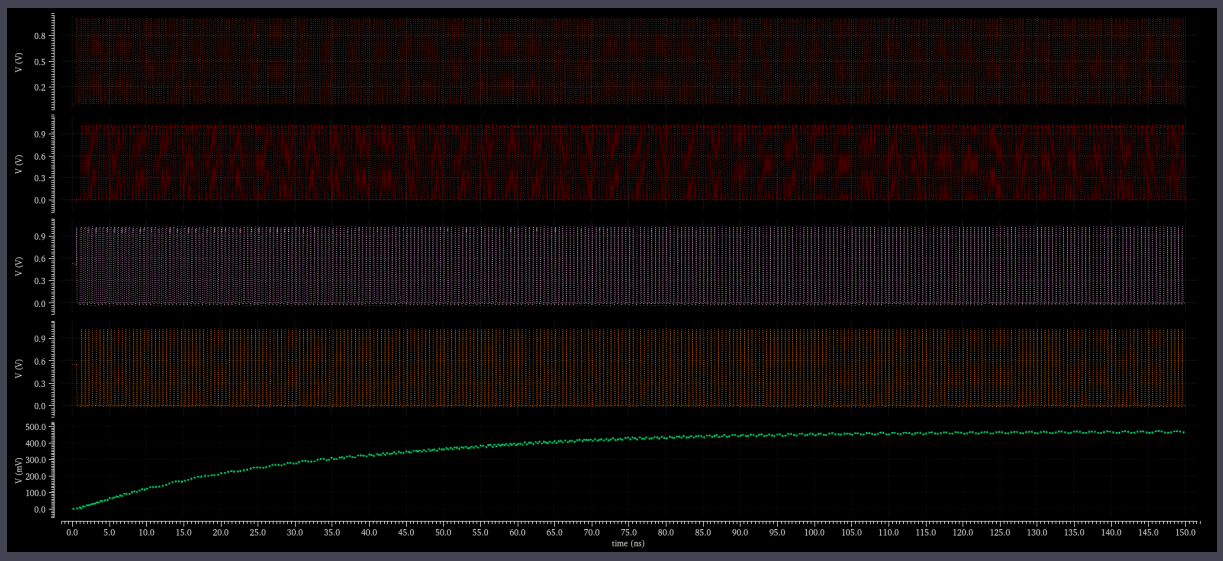

Figure 16: Simulation trace of DLL full operation (Inital Value of Vctrl = 0V)

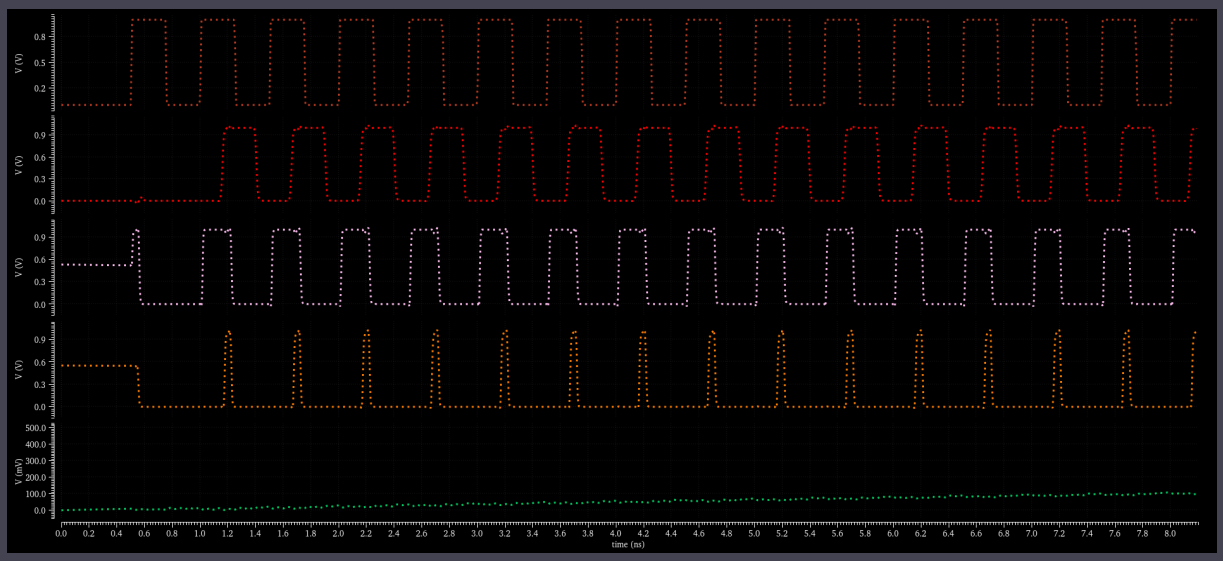

Figure 17: Simulation trace of DLL at start (Inital Value of Vctrl = 0V)

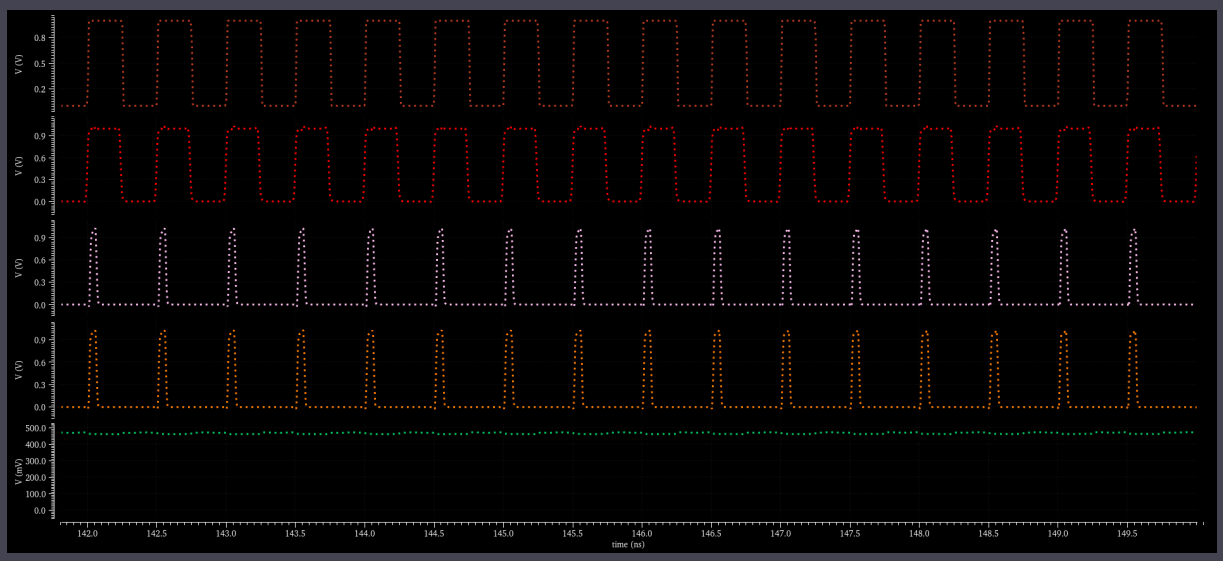

Figure 18: Simulation trace of DLL at end (Inital Value of Vctrl = 0V)

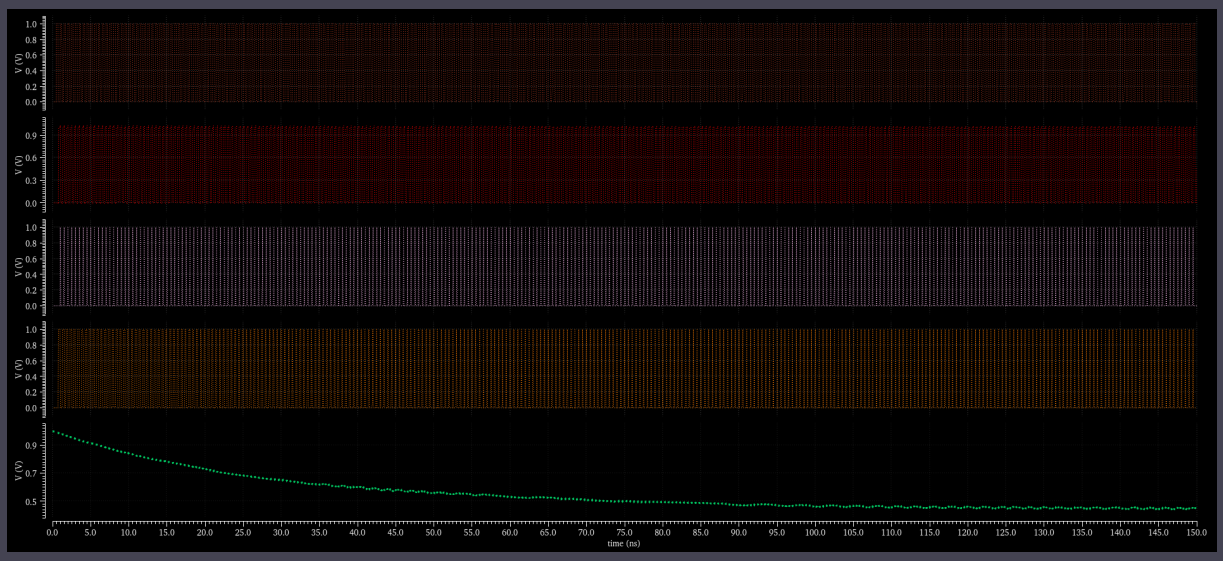

Figure 19: Simulation trace of DLL full operation (Inital Value of Vctrl = 1V)

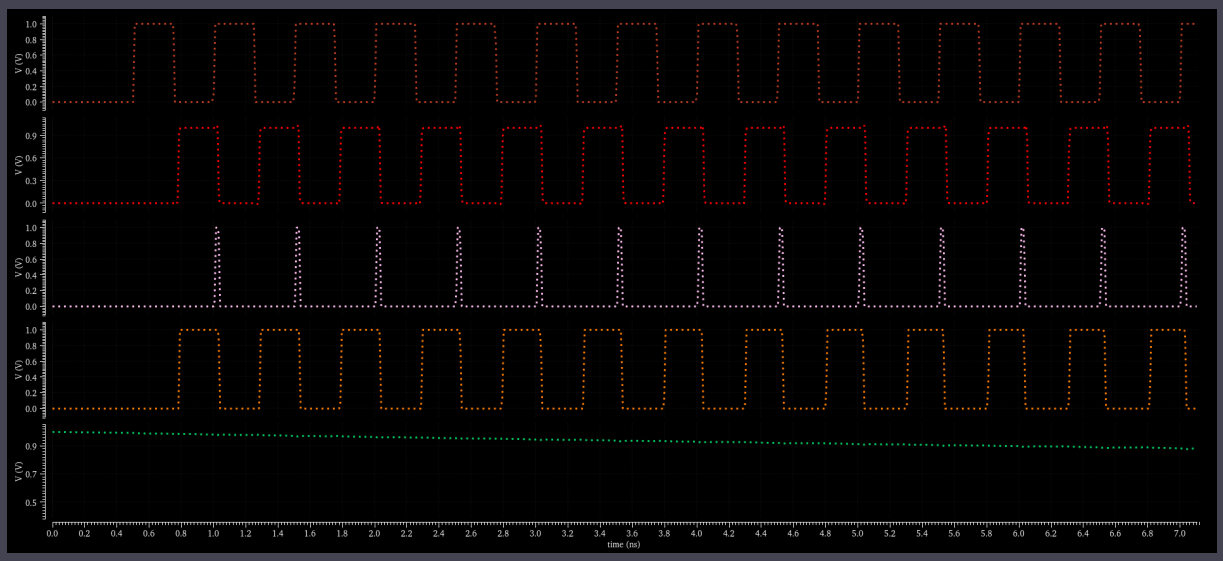

Figure 20: Simulation trace of DLL at start state (Inital Value of Vctrl = 1V)

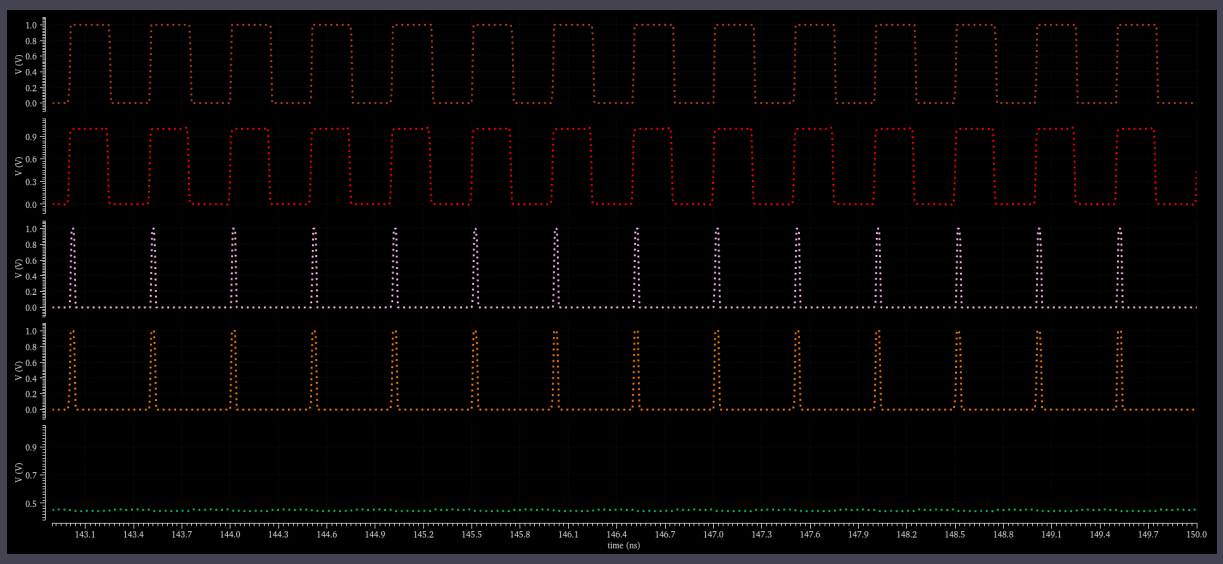

Figure 21: Simulation trace of DLL at end state (Inital Value of Vctrl = 1V)

Main Cell Testbenches

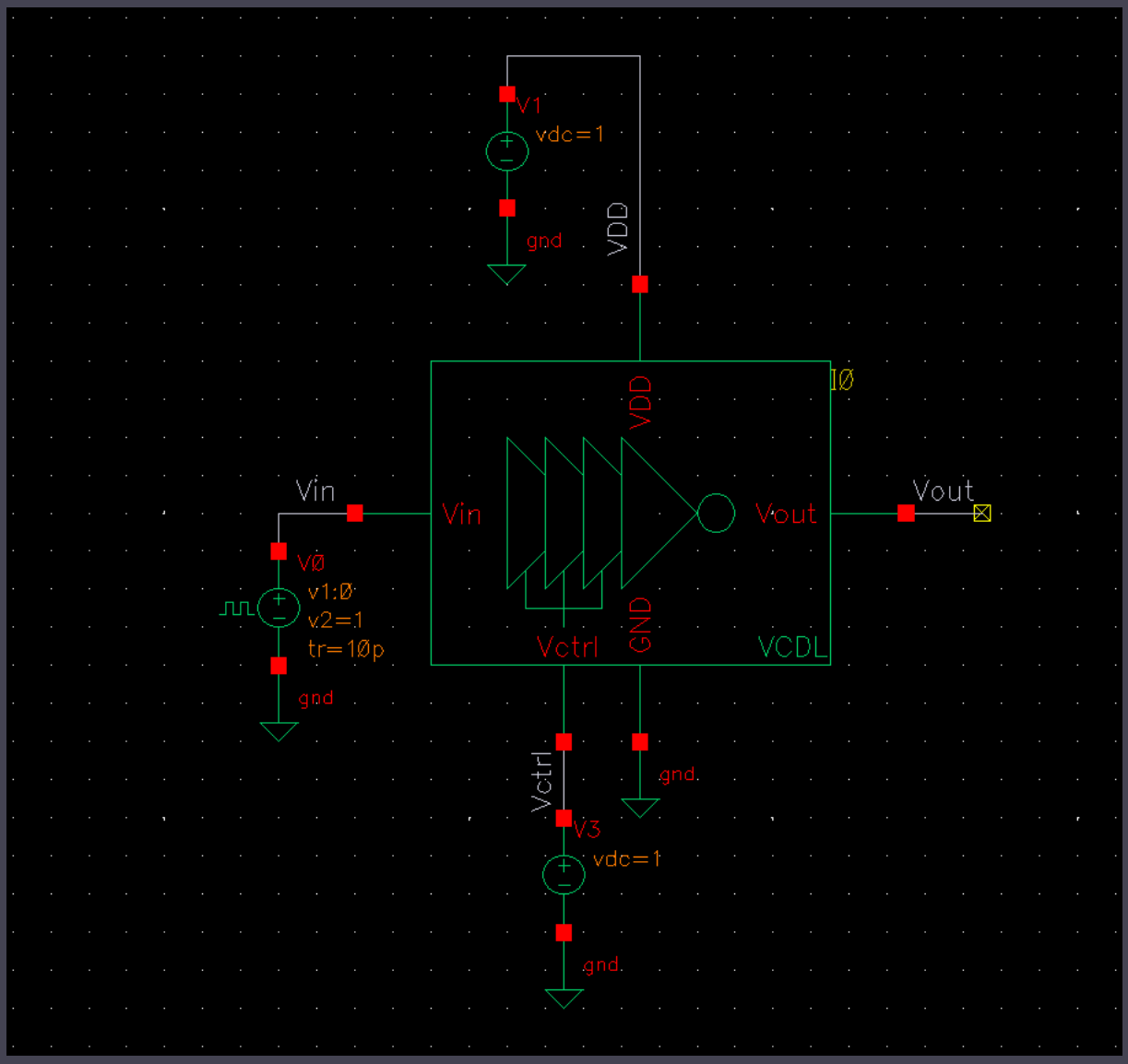

Figure 22: Testbench Schematic for the VCDL

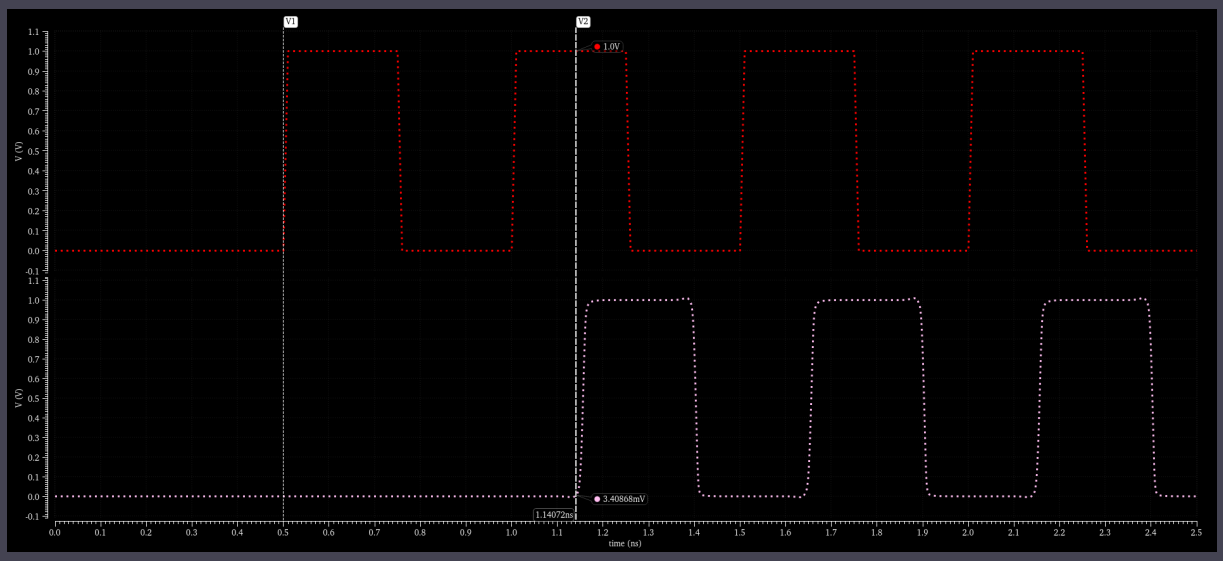

Figure 23: Simulation trace of the VCDL testbench (Vctrl = 0V)

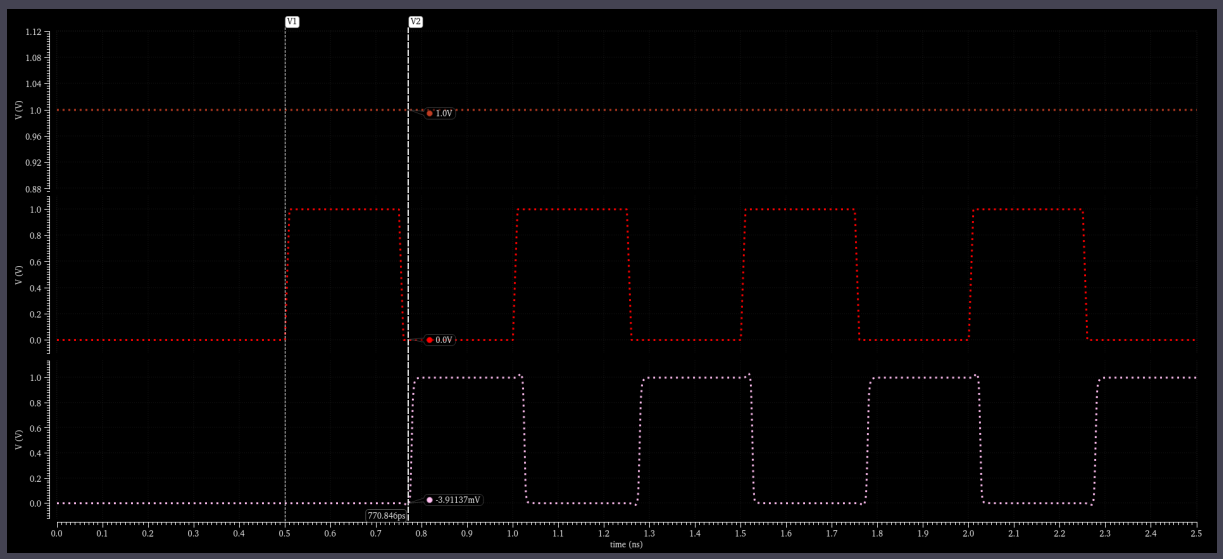

Figure 24: Simulation trace of the VCDL testbench (Vctrl = 1V)

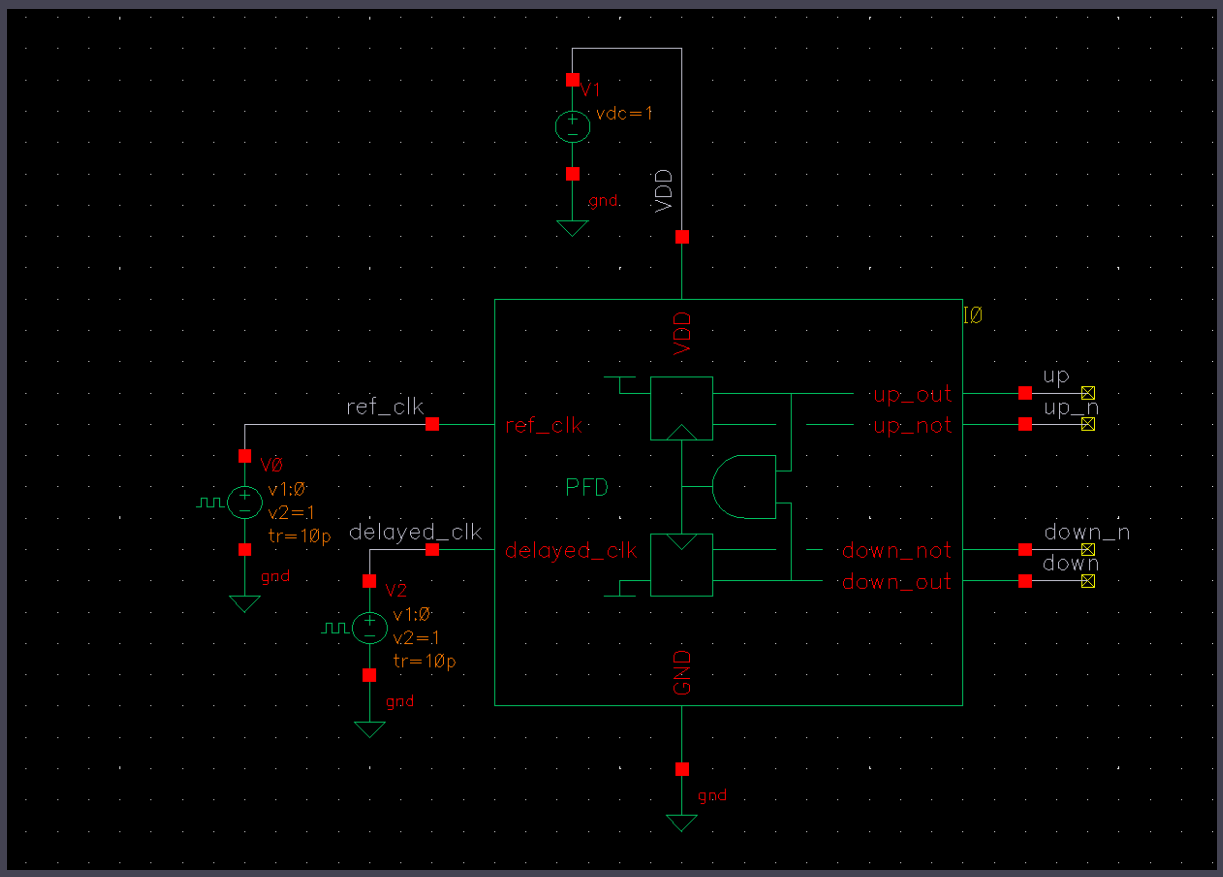

Figure 25: Testbench schematic for the PFD

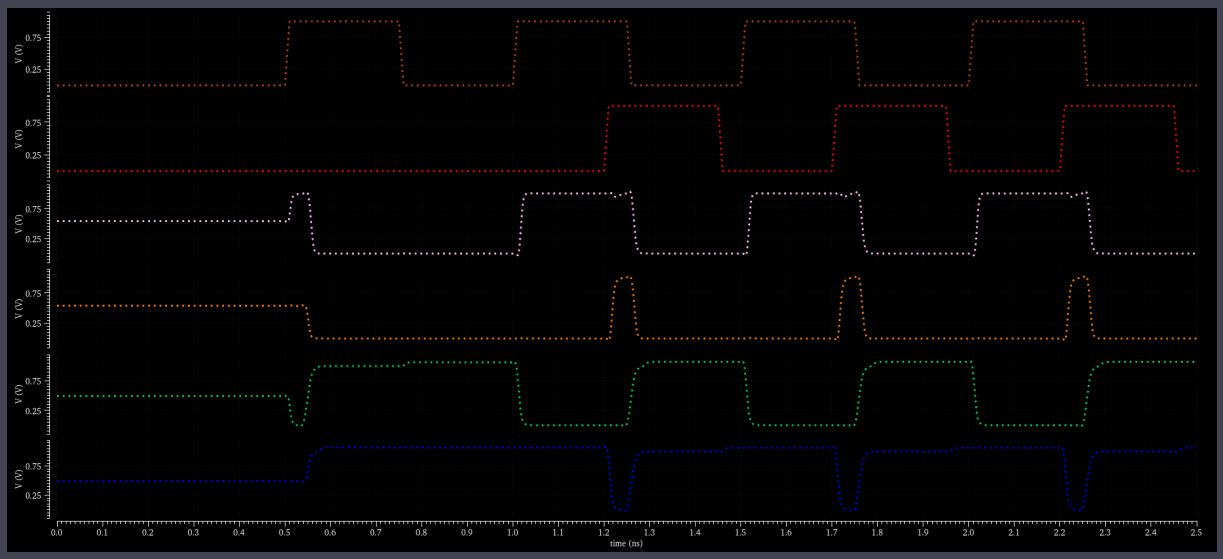

Figure 26: Simulation trace of the PFD testbench