ECE345 Midterm Project Report

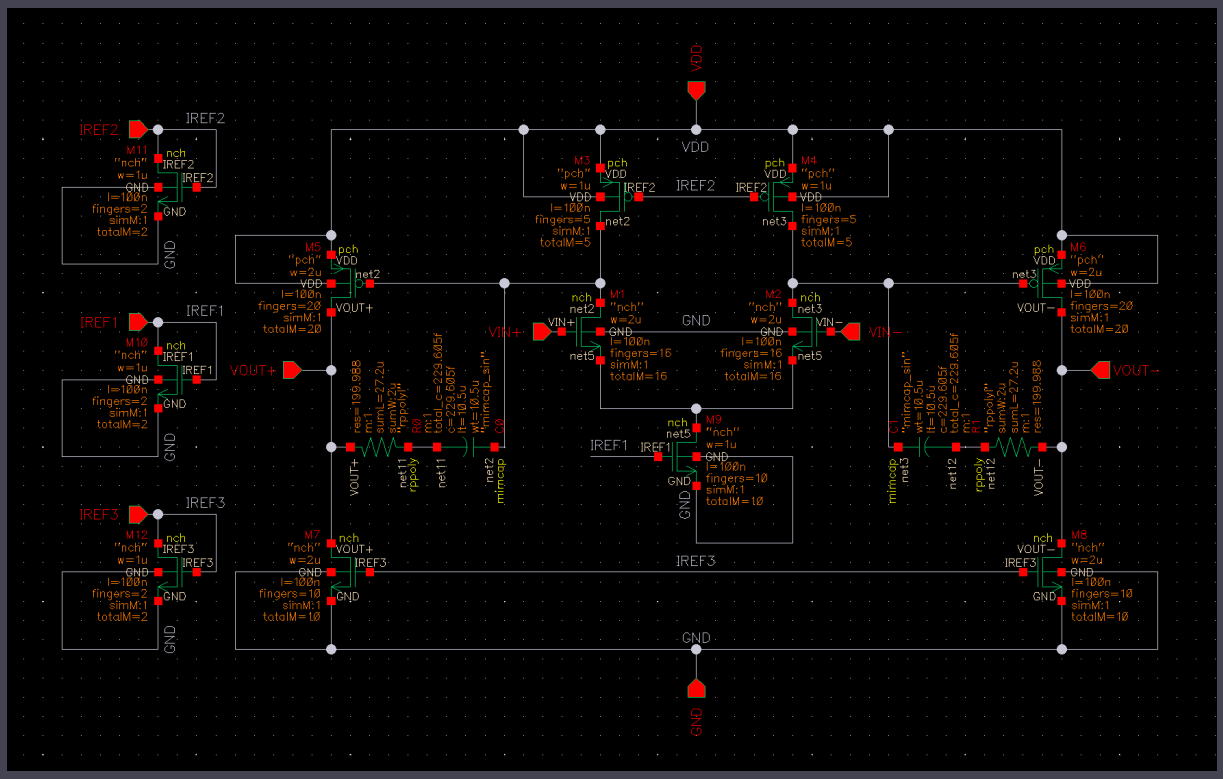

Figure 1: Schematic

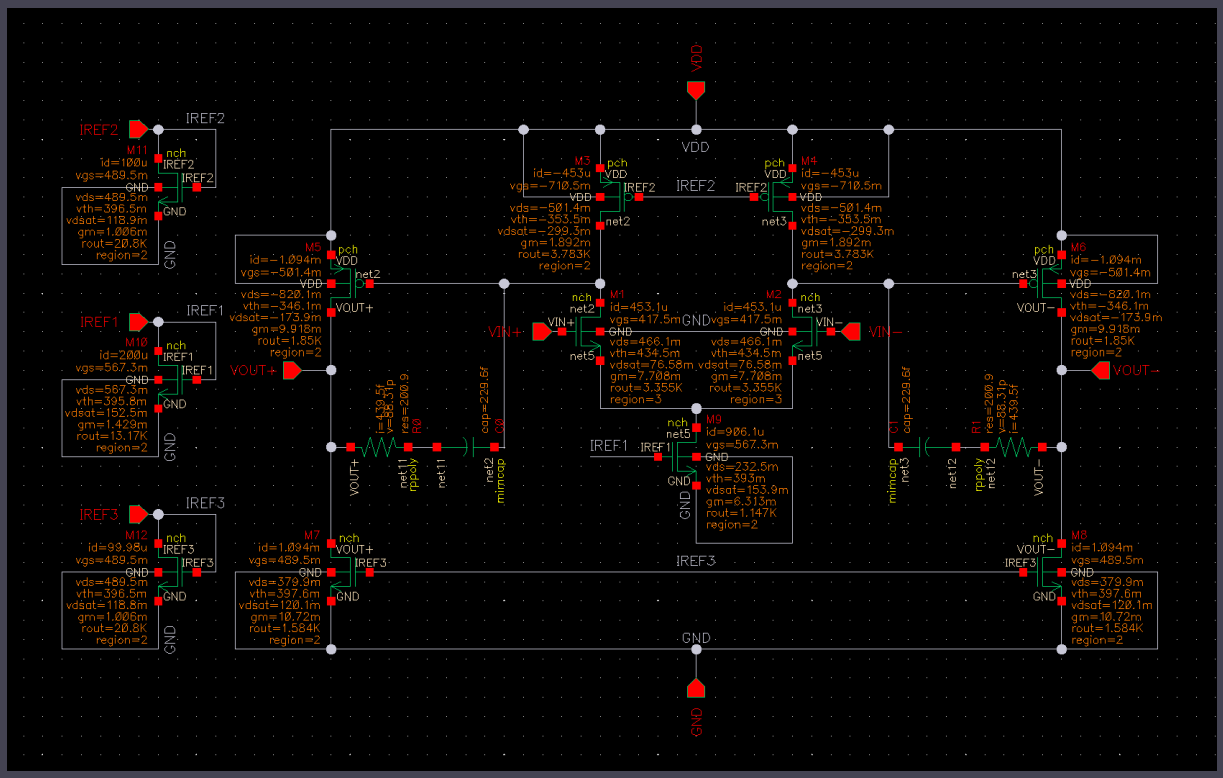

Figure 2: Schematic with DC Operating Points

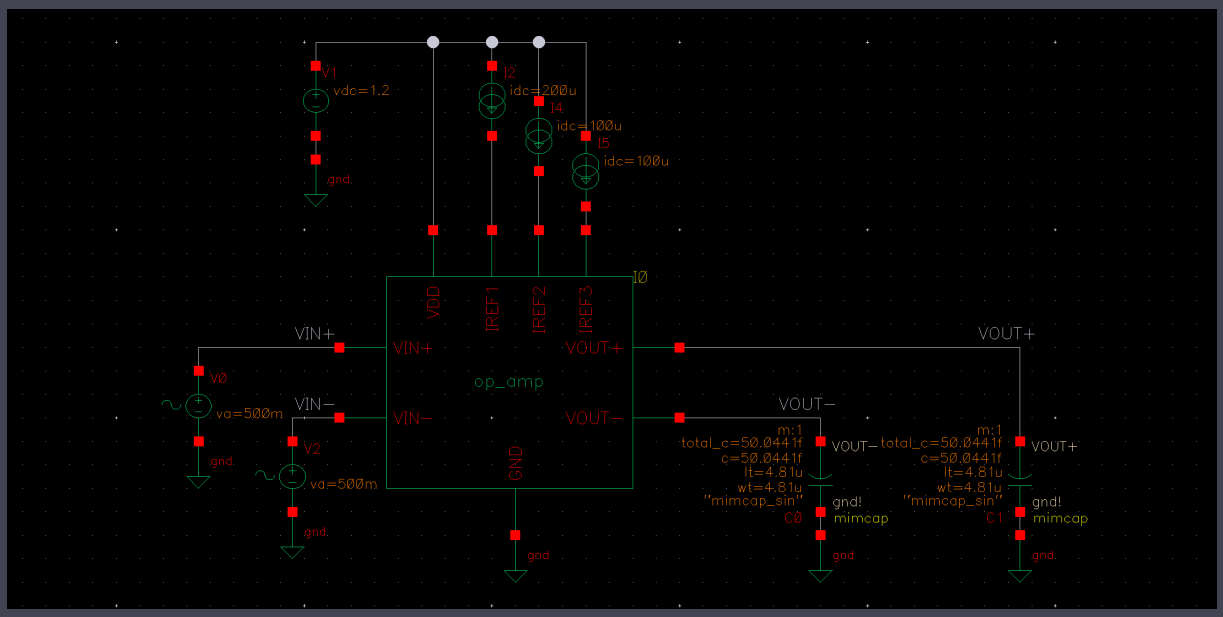

Figure 3: Testbench Schematic

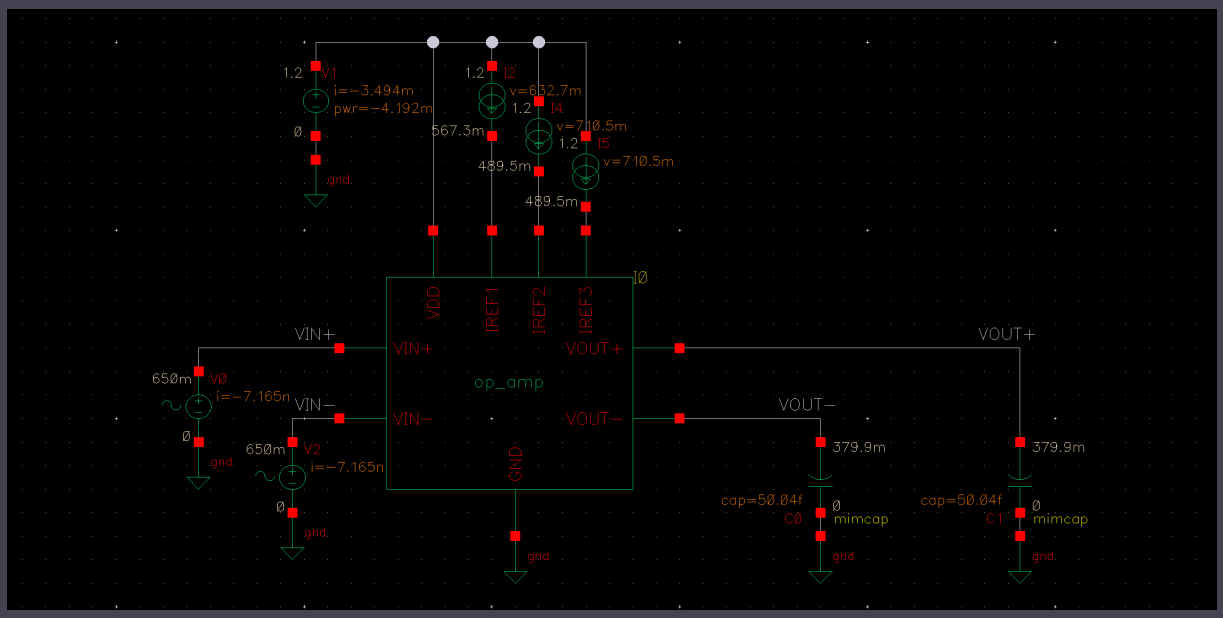

Figure 4: Testbench Schematic with DC Operating Points

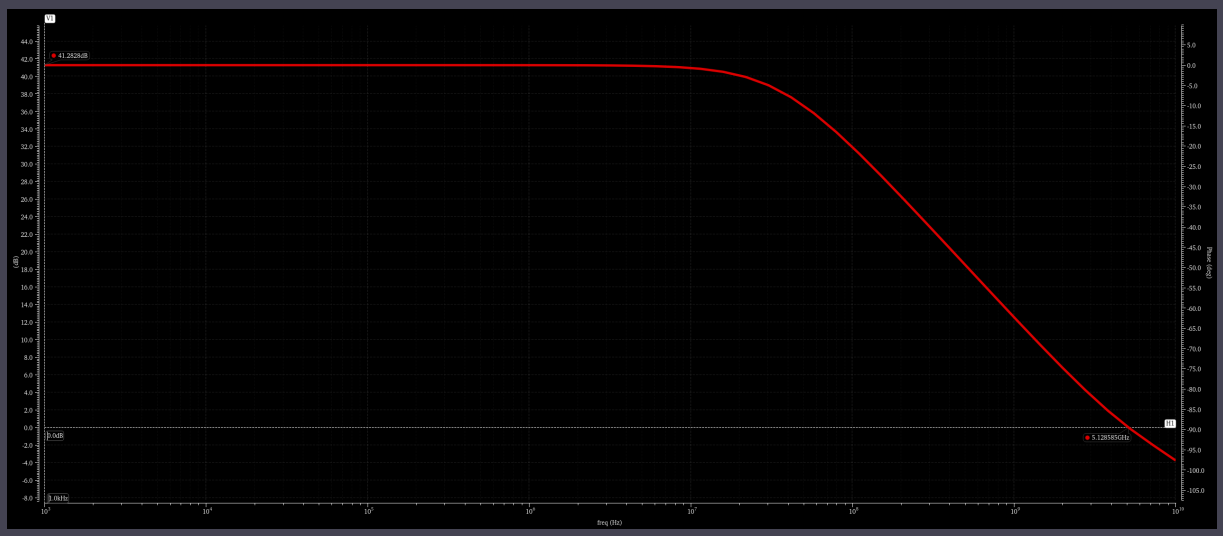

Figure 5: Gain Frequency Response

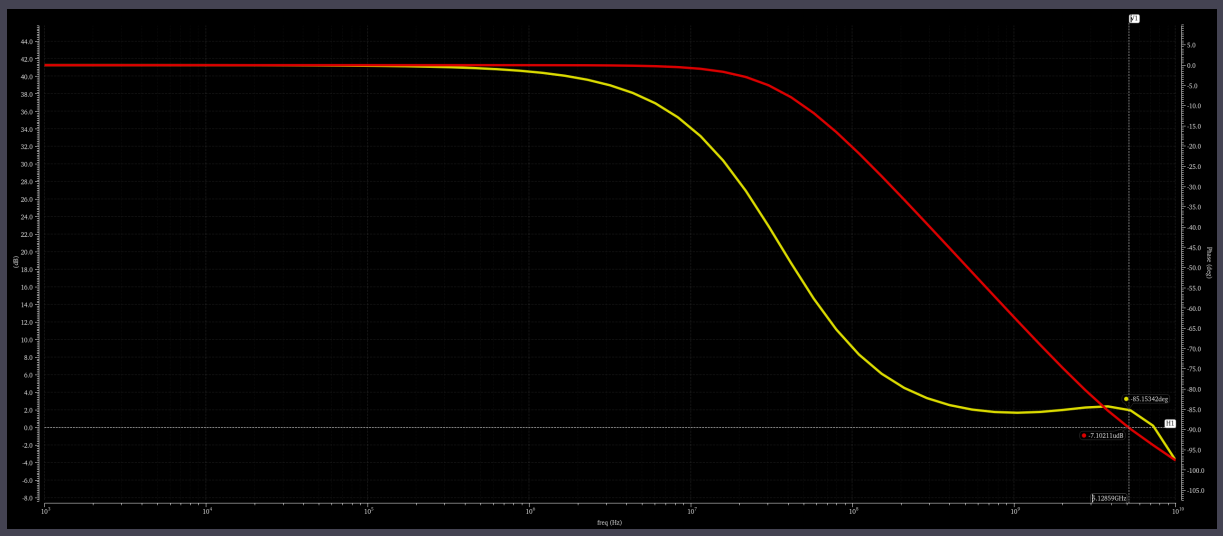

Figure 6: Gain & Phase Frequency Response

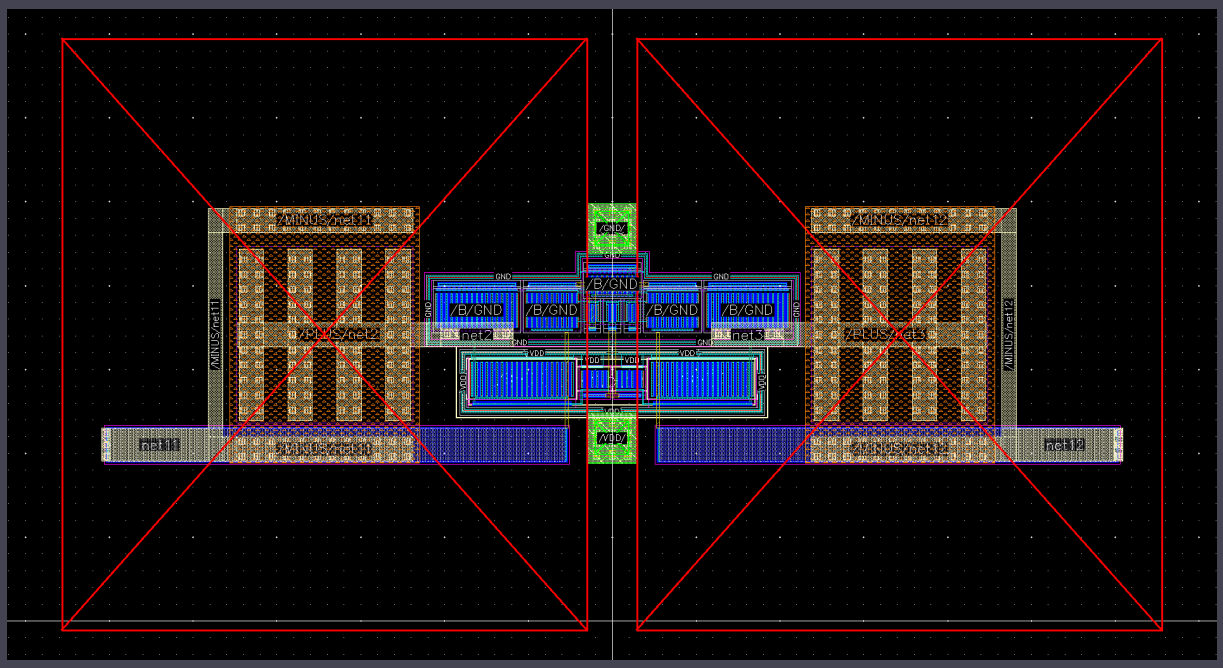

Figure 7: Full Layout

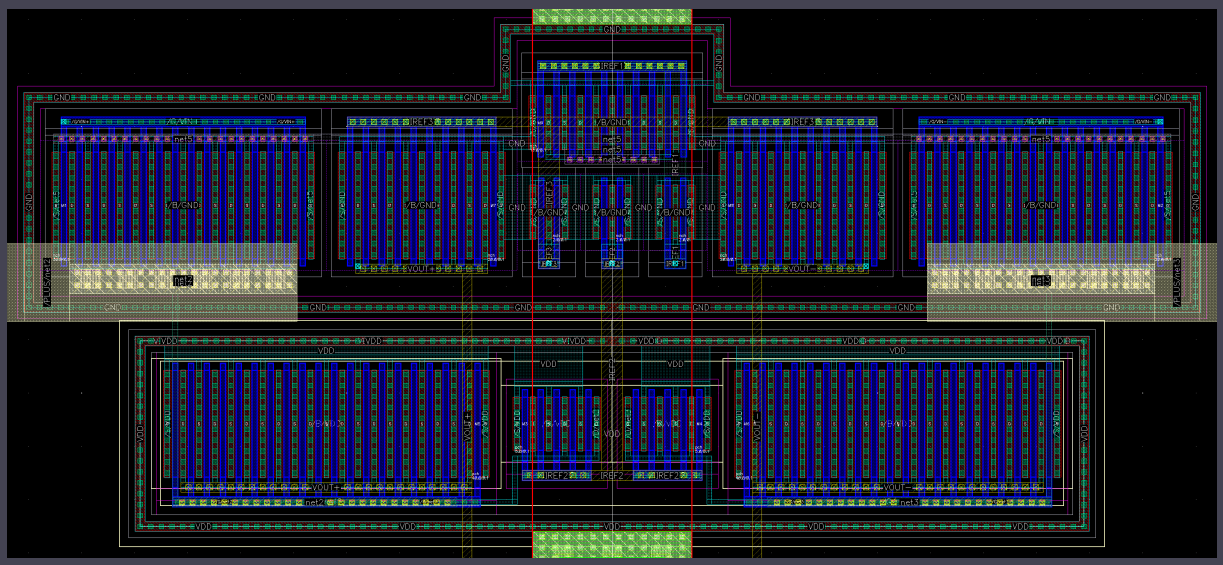

Figure 8: Focused Layout

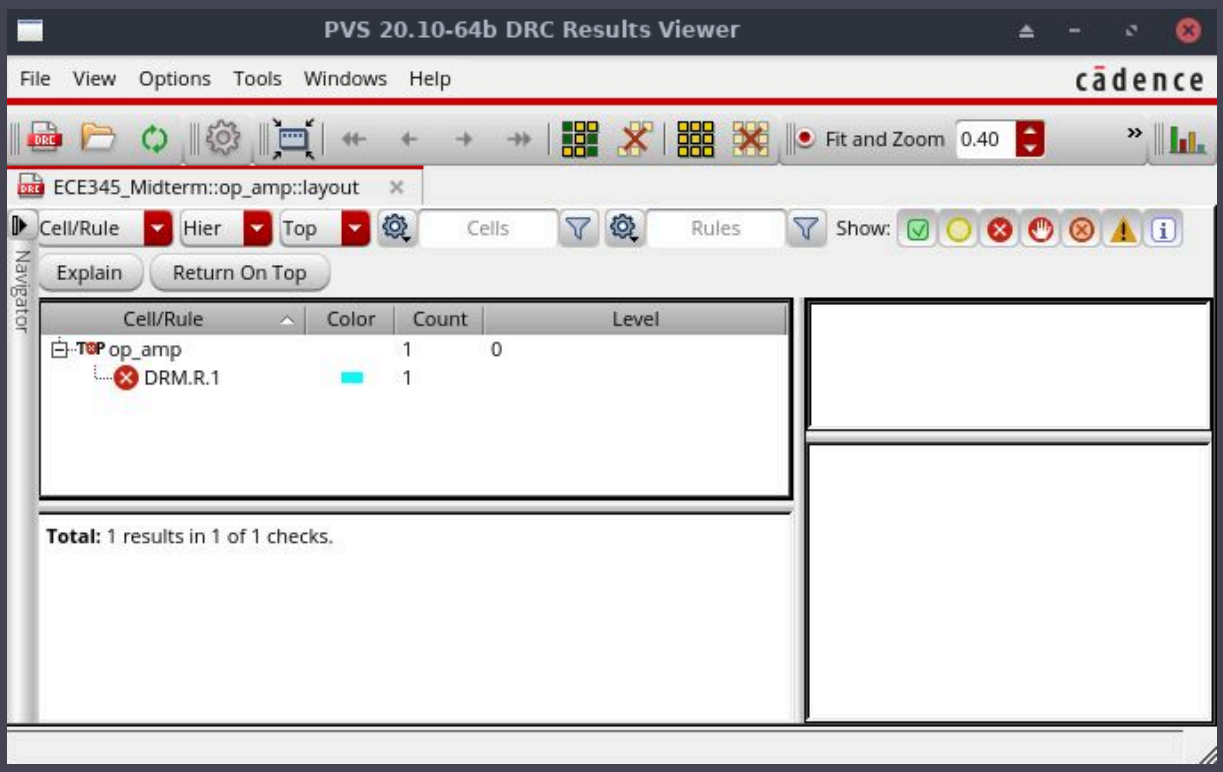

Figure 9: PVS DRC Results

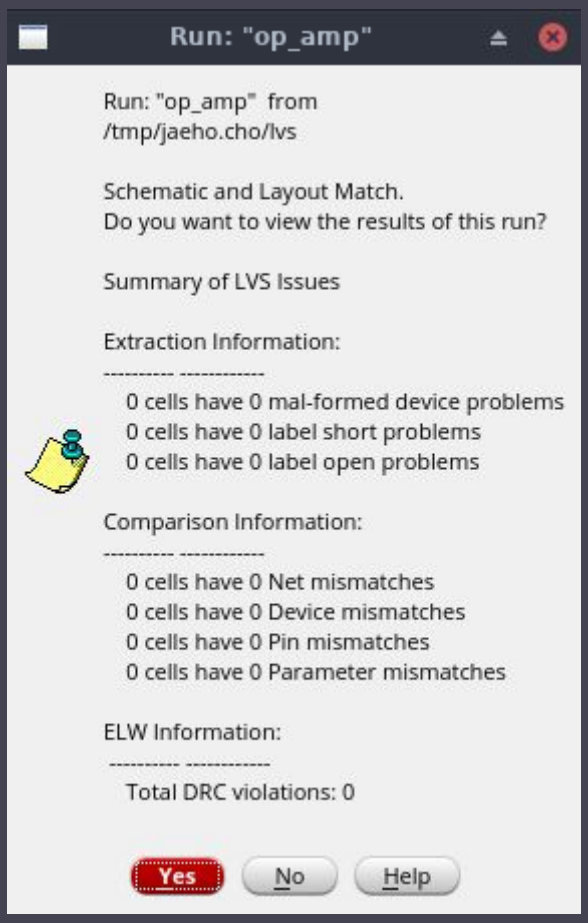

Figure 10: Assura LVS Results

Specification	Target	Achieved
Gain @ Low Frequencies	>40 dB	41.28 dB
Unity Gain Frequency	>5 GHz	5.13 GHz
Phase Margin	>60°	94.85°
Peak-to-Peak Amplitude	400 mV	906 mV

Table 1: Specifications