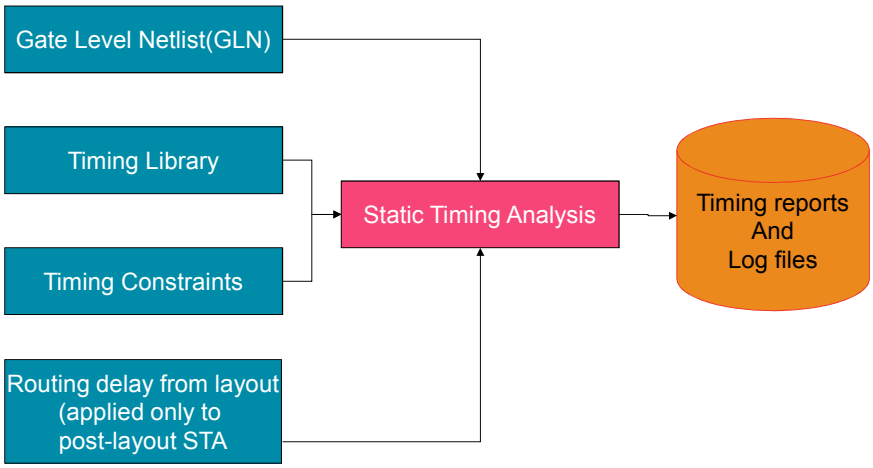
Static Timing Analysis



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Static-Timing Analysis?

- STA is a tool to determine the delay of integrated digital circuits.
- In order to have a properly operating circuit, not only the design needs to be well done, but also its operating points must be determined.
- its worst case delay determines the maximum speed (frequency) at which the circuit will operate as expected.
- Static-Timing Analysis - a key measurement for the circuit performace, as well be used for optimization purposes.
- Static-Timing Analysis is a determenistic way of computing the delay imposed by the circuits design and layout
- From Deterministic STA to Statistical STA

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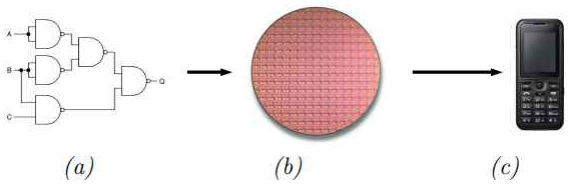

(a) (b) (c)

Model Uncertainty | Process Uncertainty | Environment Uncertainty

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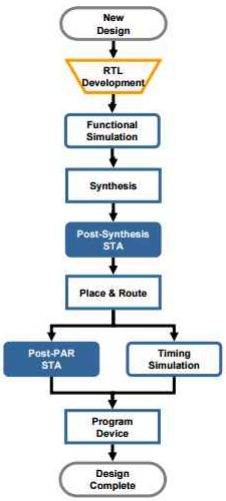
Design flow

Dynamic	Static
Difficult to cover all paths	✓ Checks every path for timing violations
Typically time and compute intensive	✓ Typical runtime is fast
Confirms function and timing	✓ Confirms timing only
Supports asynchronous designs	✓ Synchronous designs only
Simple timing checks	✓ Min/Max, clock skew, exceptions
Ex: Mentor Graphics ModelSim	✓Ex: Lattice Semiconductor *trace* program



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- There are several key abnormalilites in a real clock signal
  - **Skew** is the deterministic difference in the time when a clock arrives at a flip-flop
  - **Jitter** is the random difference in the time when a clock arrives at a flip-flop
  - **Latency** is the time taken by a clock signal to reach the pins of sequential cells from the source of the clock.
  - **Clock latency** is also known as the insertion delay.
  - **Clock uncertainty** refers to the deviation of the actual time event in a clock signal with respect to the time point where it would occur ideally

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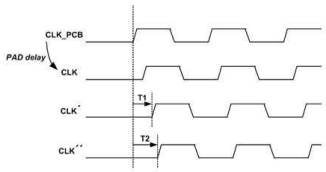
- Delay
  - RISE_Delay
  - FALL_Delay



- T1=2ns, T2=2.5ns, CIK's SKEW = 0.5ns
- SKEW는 클럭의 delay가 아니고, "가장 빨리 도달하는 클럭과 가장 늦게 도달하는 클럭의 차이"
- SLACK – 마진(여유)
  - Slack = -5ns, clock = 10ns, cell_delay = 15ns, → negative slack
- SLEW – PAD의 특성값, Slew Rate Control PAD

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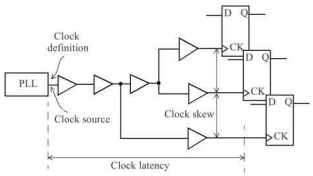
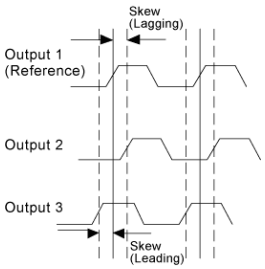
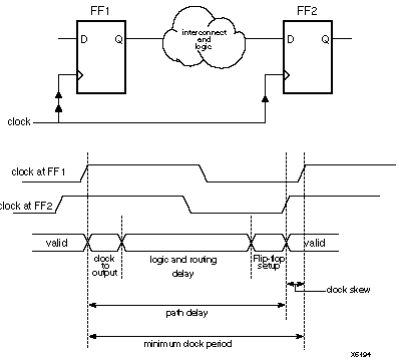


Figure 2-15 *Clock tree, clock latency and clock skew.*





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Data Required Time (setup)	=	capture edge time + destination clock path delay - clock uncertainty - setup time
Data Arrival Time (setup)	=	launch edge time + source clock path delay + datapath delay
Slack (setup)	=	Data Required Time - Data Arrival Time

Data Required Time (hold)	=	capture edge time + destination clock path delay - clock uncertainty + hold time
Data Arrival Time (hold)	=	launch edge time + source clock path delay + datapath delay
Slack (hold)	=	Data Arrival Time - Data Required Time

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- *launch edge*
- *capture edge*
- *source clock*
- *destination clock*
- *setup requirement*
- *setup relationship*
- *hold requirement*
- *hold relationship*

- Global Timing Constraints
- Path Specific Timing Constraints
- Multicycle Paths
- False Paths

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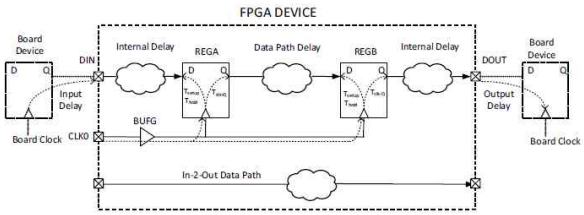

Figure 5-1: **Timing Paths Example**

- Source Clock Path
- Data Path
- Destination Clock Path

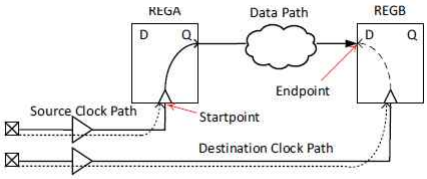

Figure 5-2: **Typical Timing Path**

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Introduction for Lab

- Xilinx Design Constraint (XDC) file to constrain the pin locations(Lab1)
- Xilinx Design Constraint (XDC) file to constrain the timing of the circuit(Lab2)
- Run static timing analysis(Lab3)
- Use IP Catalog to generate a clocking core(Lab4)
- a I/O Planning project(Lab5)
- Use hardware debugger to debug a design(Lab6)

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Achieving Timing Closure

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Objectives

After completing this module, you will be able to:

- Describe a flow for obtaining timing closure
- Interpret a timing report and determine the cause of timing errors
- Apply Timing Analyzer report options to create customized timing reports

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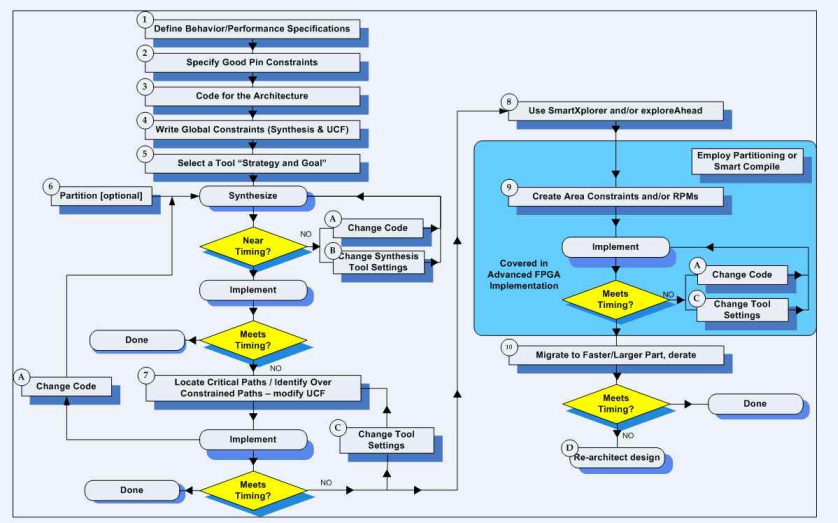
Timing Closure



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Timing Reports

- Timing reports help you determine why your design fails to meet its constraints
  - Reports contain detailed descriptions of paths that fail their constraints
- The implementation tools can create timing reports at two points in the design flow
  - Post-Map Static Timing Report
    - Use for an early indication as to whether your design might meet timing
  - Post-Place & Route Static Timing Report
    - Use as a final analysis of whether your design has met timing
- The Timing Analyzer is a utility for creating and reading timing reports

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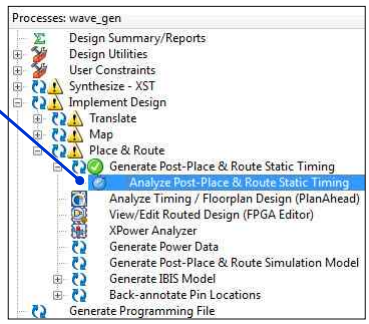
Using the Timing Analyzer

- Double-click **Analyze Post-Place & Route Static Timing**
  - Opens the Post-Place & Route Static Timing Report
  - Allows you to create custom reports
- Open a plain text version by clicking **Static Timing Report** in the Design Summary screen



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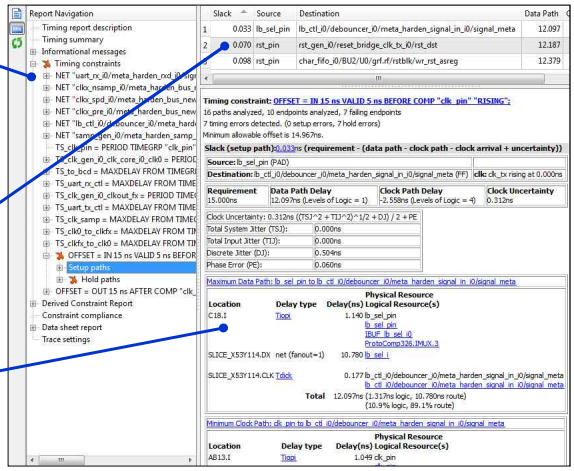
Timing Analyzer GUI

- Hierarchical browser
  - Quickly navigate to specific report sections
  - Failing constraints indicated with a red “X”
- Timing objects window
  - Summarizes the path displayed in the path detail window
- Report text
  - Logic highlighted in blue can be cross-probed



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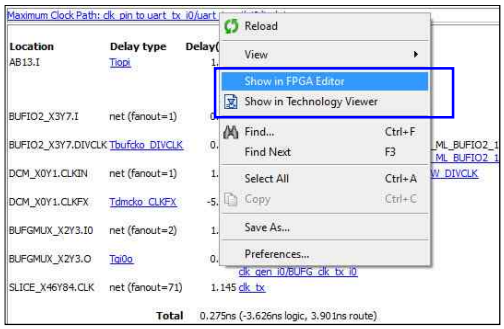
Cross-Probing

- Shows the placement of logic in a delay path
  - Right-click on the delay path to see this option
  - The FPGA Editor view is used for seeing the actual placement and routing used
  - The Technology view shows logical path through components



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Timing Report Structure

- Timing constraints
  - Number of paths covered and number of paths that failed for each constraint
  - Detailed descriptions of the longest paths
- Data sheet report
  - Setup, hold, and clock-to-out times for each I/O pin
- Timing summary
  - Timing errors (number of failing paths)
  - Timing score (total number of ps of all constraints that were missed)
- Timing report description
  - Allows you to easily duplicate the report

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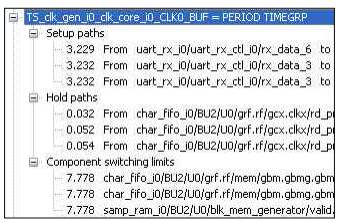
Paths Reported

- Setup paths
  - Slowest delay paths for each constraint
  - Defaults to the three longest paths
- Hold paths
  - Fastest delay paths for each constraint
- Component switching limits
  - Checks that the toggle rate and duty cycle are in limits with specification



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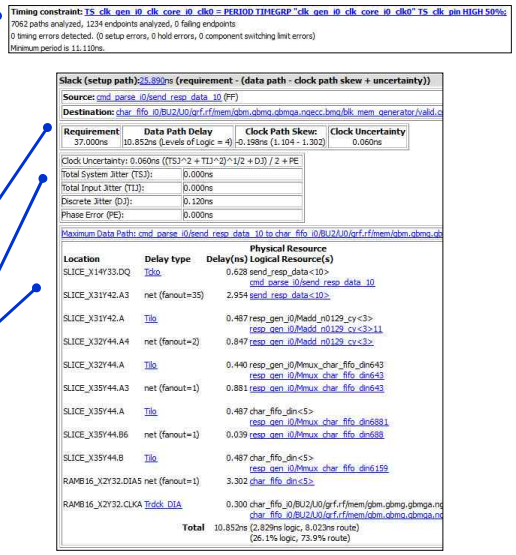
Report Example

- Constraint summary
  - Number of paths analyzed
  - Number of timing errors
  - Length of critical path
- Total delay
  - Clock and data breakdown
- Clock jitter analysis
- Detailed path description
  - Delay types are described in the data sheet
  - Worst-case conditions are assumed, unless pro-rated



Timing constraint: TS_clk_gen_i0_clk_core_i0_clk0 = PERIOD TIMEGRP "clk_gen_i0_clk_core_i0_clk0" TS_clk_pin HIGH 50%;
7062 paths analyzed, 1234 endpoints analyzed, 0 failing endpoints
0 timing errors detected. (0 setup errors, 0 hold errors, 0 component switching limit errors)
Minimum period is 11.110ns.

Slack (setup path): 25.890ns (requirement - (data path - clock path skew + uncertainty))
Source: cmd_parse_i0/send_resp_data_10 (FF)
Destination: char_fifo_i0/BU2/U0/grf.rf/mem/gbm.gbmg.gbmga.ngecc.bmg/blk_mem_generator/valid.c

Requirement	Data Path Delay	Clock Path Skew:	Clock Uncertainty
37.000ns	10.852ns (Levels of Logic = 4)	-0.198ns (1.104 - 1.302)	0.060ns

Clock Uncertainty: 0.060ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ):	0.000ns
Total Input Jitter (TIJ):	0.000ns
Discrete Jitter (DJ):	0.120ns
Phase Error (PE):	0.000ns

Maximum Data Path: cmd_parse_i0/send_resp_data_10 to char_fifo_i0/BU2/U0/grf.rf/mem/gbm.gbmg.gb

Location	Delay type	Delay(ns)	Physical Resource / Logical Resource(s)
SLICE_X14Y33.DQ	Tcko	0.628	send_resp_data<10>
			cmd_parse_i0/send_resp_data_10
SLICE_X31Y42.A3	net (fanout=35)	2.954	send_resp_data<10>
SLICE_X31Y42.A	Tilo	0.487	resp_gen_i0/Madd_n0129_cy<3>
			resp_gen_i0/Madd_n0129_cy<3>11
SLICE_X32Y44.A4	net (fanout=2)	0.847	resp_gen_i0/Madd_n0129_cy<3>
SLICE_X32Y44.A	Tilo	0.440	resp_gen_i0/Mmux_char_fifo_din643
			resp_gen_i0/Mmux_char_fifo_din643
SLICE_X35Y44.A3	net (fanout=1)	0.881	resp_gen_i0/Mmux_char_fifo_din643
SLICE_X35Y44.A	Tilo	0.487	char_fifo_din<5>
			resp_gen_i0/Mmux_char_fifo_din6881
SLICE_X35Y44.B6	net (fanout=1)	0.039	resp_gen_i0/Mmux_char_fifo_din688
SLICE_X35Y44.B	Tilo	0.487	char_fifo_din<5>
			resp_gen_i0/Mmux_char_fifo_din6159
RAMB16_X2Y32.DIA5	net (fanout=1)	3.302	char_fifo_din<5>
RAMB16_X2Y32.CLKA	Trdck_DIA	0.300	char_fifo_i0/BU2/U0/grf.rf/mem/gbm.gbmg.gbmga.ng
			char_fifo_i0/BU2/U0/grf.rf/mem/gbm.gbmg.gbmga.nc
	Total	10.852ns	(2.829ns logic, 8.023ns route)
			(26.1% logic, 73.9% route)

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Estimating Design Performance

- Performance estimates are available before implementation is complete
- Synthesis Report
  - Logic delays are accurate
  - Routing delays are estimated based on fanout
  - Reported performance is generally accurate to within 30 percent
- Post-Map Static Timing Report
  - Logic delays are accurate
  - Routing delays are estimated based on placement and fanout

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Analyzing Post-Place & Route Timing

- There are many factors that contribute to timing errors, including
  - Poor micro-architecture
  - Neglecting synchronous design rules or using incorrect HDL coding style
  - Poor synthesis results (too many logic levels in the path)
  - Inaccurate or incomplete timing constraints
  - Poor logic mapping or placement
- Each root cause has a different solution
  - Rewrite HDL code
  - Ensure that synthesis constraints are correct and use proper synthesis options
  - Add path-specific timing constraints
  - Resynthesize or reimplement with different software options
- Correct interpretation of timing reports can reveal the most likely cause
  - Therefore, the most likely solution

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Case 1

```
Data Path: source to dest
    Delay type         Delay(ns)  Logical Resource(s)
    -------------------------  -------------------
    Tcko                  0.290   source
    net (fanout=7)        0.325   net_1
    Tilo                  0.060   lut_1
    net (fanout=1)        1.500   net_2
    Tilo                  0.060   lut_2
    net (fanout=1)        0.245   net_3
    Tilo                  0.060   lut_3
    net (fanout=1)        0.204   net_4
    Tdick                 0.300   dest
    -------------------------  -----------------------------
    Total                 3.044ns (0.770ns logic, 2.274ns route)
                                  (25.3% logic, 74.7% route)
```

- This path is constrained to 3 ns
- What is the primary cause of the timing failure?

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Case 1 Answer

```
Data Path: source to dest
    Delay type          Delay(ns)  Logical Resource(s)
    ----------------------------  -------------------
    Tcko                  0.290   source
    net (fanout=7)        0.325   net_1
    Tilo                  0.060   lut_1
    net (fanout=1)        1.500   net_2
    Tilo                  0.060   lut_2
    net (fanout=1)        0.245   net_3
    Tilo                  0.060   lut_3
    net (fanout=1)        0.204   net_4
    Tdick                 0.300   dest
    ----------------------------  ------------------------------
    Total                 3.044ns (0.770ns logic, 2.274ns route)
                                  (25.3% logic, 74.7% route)
```

- What is the primary cause of the timing failure?
  - The net_2 signal has a long delay and low fanout
  - Most likely cause is poor placement

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Poor Placement: Solutions

- Increase placement effort level (or overall effort level)
- PAR extra effort or SmartXplorer
  - Covered in the “Advanced Implementation Options” module
- Area constraints with the PlanAhead™ tool
  - Covered in the *Designing with the PlanAhead Analysis and Design Tool* course

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Case 2

```
Data Path: source to dest
    Delay type          Delay(ns)  Logical Resource(s)
    --------------------------  -------------------
    Tcko                  0.290   source
    net (fanout=7)        0.125   net_1
    Tilo                  0.060   lut_1
    net (fanout=187)      2.500   net_2
    Tilo                  0.060   lut_2
    net (fanout=1)        0.174   net_3
    Tilo                  0.060   lut_3
    net (fanout=1)        0.204   net_4
    Tdick                 0.300   dest
    --------------------------  ------------------------------
    Total                 3.773ns (0.770ns logic, 3.003ns route)
                                  (20.0% logic, 80.0% route)
```

- This path is also constrained to 3 ns
- What is the primary cause of the timing failure?

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Case 2 Answer

```
Data Path: source to dest
    Delay type          Delay(ns)  Logical Resource(s)
    --------------------------  -------------------
    Tcko                  0.290   source
    net (fanout=7)        0.125   net_1
    Tilo                  0.060   lut_1
    net (fanout=187)      2.500   net_2
    Tilo                  0.060   lut_2
    net (fanout=1)        0.174   net_3
    Tilo                  0.060   lut_3
    net (fanout=1)        0.204   net_4
    Tdick                 0.300   dest
    --------------------------  ------------------------------
    Total                 3.773ns (0.770ns logic, 3.003ns route)
                                  (20.0% logic, 80.0% route)
```

- What is the primary cause of the timing failure?
  - The signal net_2 has a long delay, but the fanout is not low
  - Most likely cause is high fanout

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High Fanout: Solutions

- Most likely solution is to duplicate the source of the high-fanout net
  - If the net is the output of a flip-flop, the solution is to duplicate the flip-flop
    - Use manual duplication (recommended) or synthesis options
  - If the net is driven by combinatorial logic, locating the source of the net in the HDL code can be more difficult
    - Use synthesis options to duplicate the source
    - Duplicate one or more flip-flops upstream from the net

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Case 3

```
Data Path: source to dest
    Delay type          Delay(ns)  Logical Resource(s)
    --------------------------  -------------------
    Tcko                  0.290   source
    net (fanout=7)        0.521   net_1
    Tilo                  0.060   lut_1
    net (fanout=1)        0.280   net_2
    Tilo                  0.060   lut_2
    net (fanout=1)        0.223   net_3
    Tilo                  0.060   lut_3
    net (fanout=1)        0.223   net_4
    Tilo                  0.060   lut_4
    net (fanout=1)        0.310   net_5
    Tilo                  0.060   lut_5
    net (fanout=1)        0.233   net_6
    Tilo                  0.060   lut_6
    net (fanout=1)        0.308   net_7
    Tdick                 0.300   dest
    --------------------------  ---------------------------------------
    Total                 3.048ns (0.950ns logic, 2.098ns route)
                                  (31.2% logic, 68.8% route)
```

- This path is also constrained to 3 ns
- What is the primary cause of the timing failure?

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Case 3 Answer

```
Data Path: source to dest
    Delay type          Delay(ns)  Logical Resource(s)
    ----------------------------  --------------------
    Tcko                  0.290   source
    net (fanout=7)        0.521   net_1
    Tilo                  0.060   lut_1
    net (fanout=1)        0.180   net_2
    Tilo                  0.060   lut_2
    net (fanout=1)        0.223   net_3
    Tilo                  0.060   lut_3
    net (fanout=1)        0.123   net_4
    Tilo                  0.060   lut_4
    net (fanout=1)        0.310   net_5
    Tilo                  0.060   lut_5
    net (fanout=1)        0.233   net_6
    Tilo                  0.060   lut_6
    net (fanout=1)        0.308   net_7
    Tdick                 0.300   dest
    ----------------------------  ----------------------------------------
    Total                 3.048ns (0.950ns logic, 2.098ns route)
                                  (31.2% logic, 68.8% route)
```

- What is the primary cause of the timing failure?
  - There are no really long delays, but there are a lot of logic levels

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Too Many Logic Levels: Solutions

- The implementation tools cannot do much to improve performance
- The netlist must be altered to reduce the amount of logic between flip-flops
- Possible solutions
  - Check whether the path is a multicycle path
    - If yes, add a multicycle path constraint
  - Ensure that proper constraints were used during synthesis
  - Use the retiming option during synthesis to distribute logic more evenly among flip-flops
  - Confirm that good coding techniques were used to build this logic (no nested if or case statements)
  - Change the micro-architecture of this path
    - Add a pipeline stage, manually re-pipeline...

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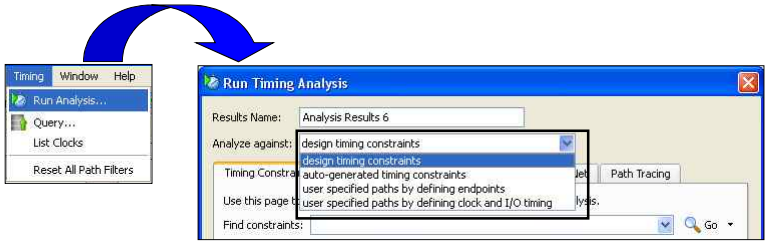
Selecting a Timing Report

- Select **Timing** > **Run Analysis** to create a report using the currently defined options
- From there you can select from four different types of timing reports



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Types of Timing Reports

- Analyze Against Design Timing Constraints
  - Compares design performance with timing constraints
  - Most commonly used report format
    - Used for Post-Map and Post-Place & Route Static Timing Reports if the design contains constraints
- Analyze Against Auto-Generated Design Constraints
  - Determines the longest paths in each clock domain
  - Use with designs that have no constraints defined
    - Used for Post-Map and Post-Place & Route Static Timing Reports if the design contains no constraints

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Types of Timing Reports

- Analyze Against User Specified Paths by Defining Endpoints
  - Custom report for selecting sources and destinations
- Analyze Against User Specified Paths by Defining Clock and I/O Timing
  - Allows you to define PERIOD and OFFSET constraints on-the-fly
  - Use with designs that have no constraints defined

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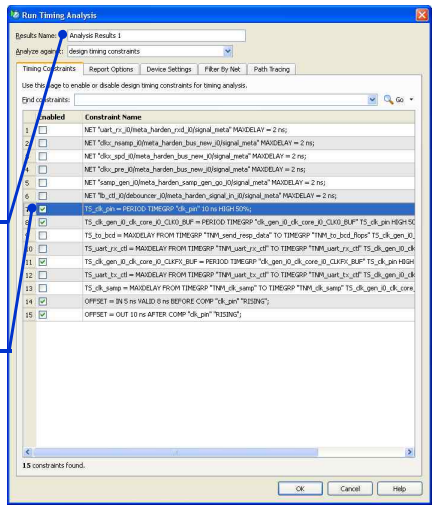
Timing Constraints Tab

- After selecting a type of report, you can select from various report options
- Select a name for the timing report
- You can select which constraints you want reported



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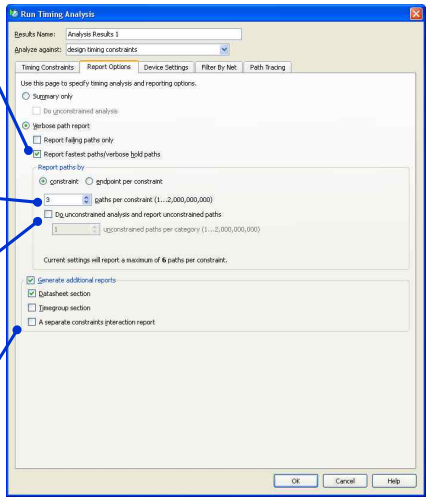
Report Options Tab

- Report failing paths only: Lists only the paths that fail to meet your specified timing constraints
- Constraint details
  - Specify the number of detailed paths reported per constraint
- Do unconstrained analysis: Allows you to list some or all of the unconstrained paths in your design
- You can also generate additional report sections



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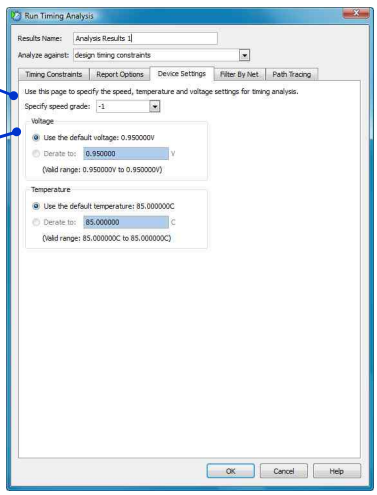
Device Settings

- Speed grade
  - Do the analysis using the timing of a different speed grade part
- Prorating
  - Specify your own worst-case environment



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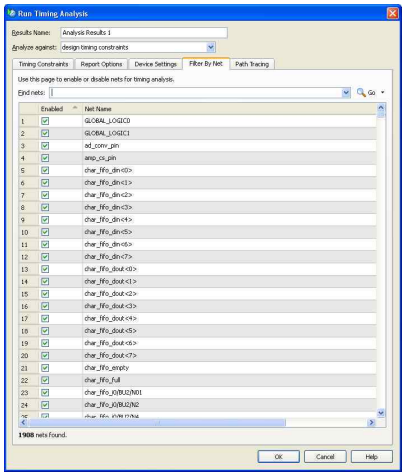
Filter by Net Tab

- Restrict which paths are reported by selecting specific nets
- Each net is set to default
  - Disabling any net *excludes* paths containing that net from being analyzed and included with the timing report
  - If all nets are left as Default, all nets are included



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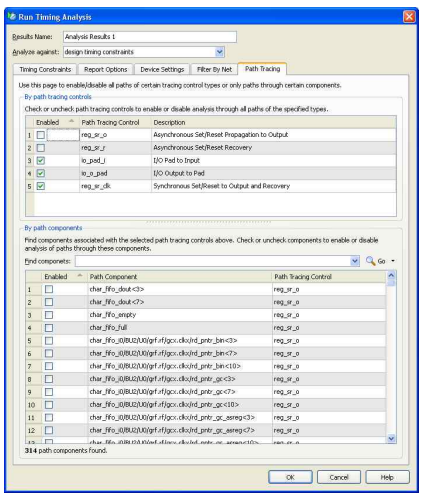
Path Tracing Tab

- Enables or disables certain propagation paths
  - reg_sr_o: If enabled, the path from the async preset/clear port of a flip-flop to the output is considered a combinatorial path
    - Describes the asserting edge of the preset/clear
    - Should be used when the preset/clear is not driven by a global reset, which is not recommended
  - reg_sr_r: If enabled, the recovery arc of the flip-flop is checked
    - Ensures that the preset/clear condition was deasserted sufficiently before the clock to ensure that the flip-flip assumes its non-reset behavior
    - Required to ensure that all flip-flops come out of reset at the same time
    - Should be enabled in the constraints: ENABLE = reg_sr_r;



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Summary

- Timing reports enable you to determine how and why constraints were not met
- Use the Synthesis Report and Post-Map Static Timing Report to estimate performance before running Place & Route
- The detailed path description offers clues to the cause of timing failures
- Cross-probe to see the placement and a technology view of a timing path
- The Timing Analyzer can generate various types of reports for specific circumstances

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